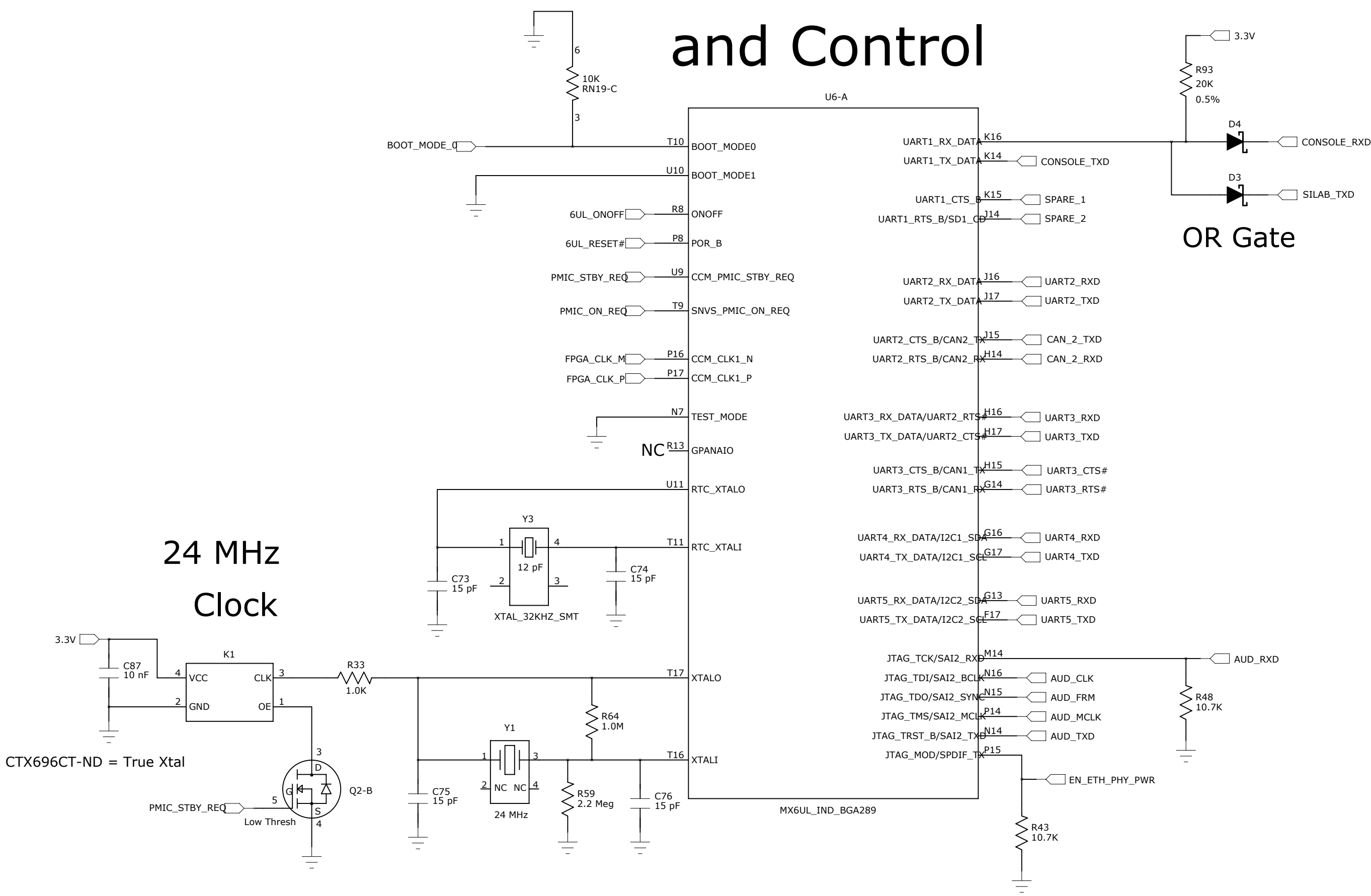
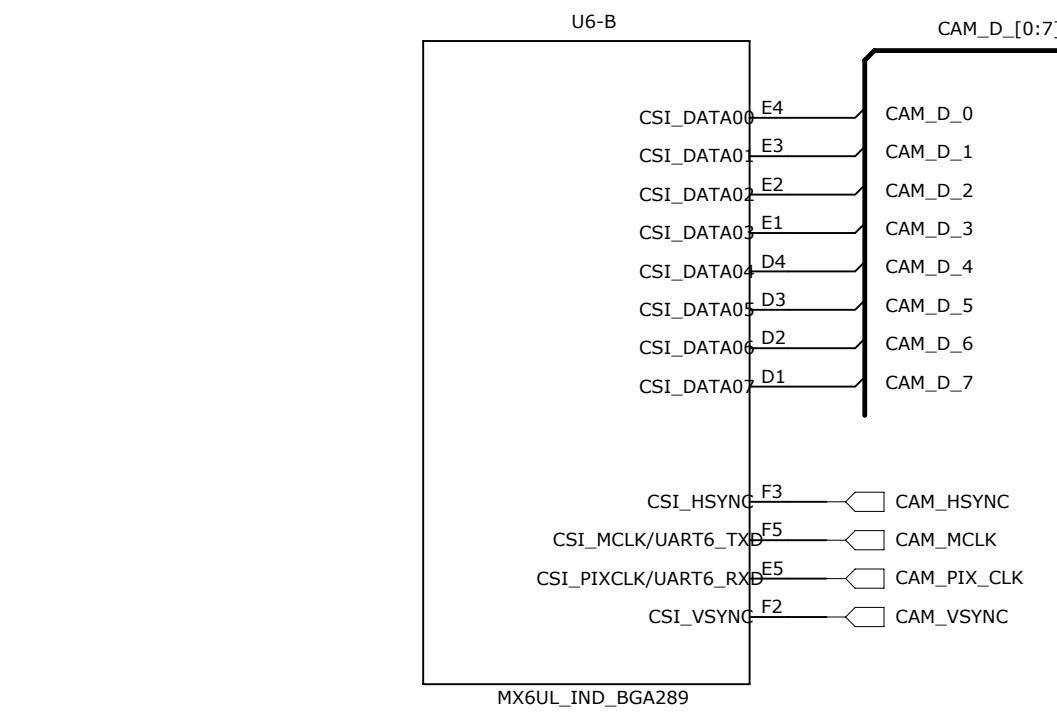


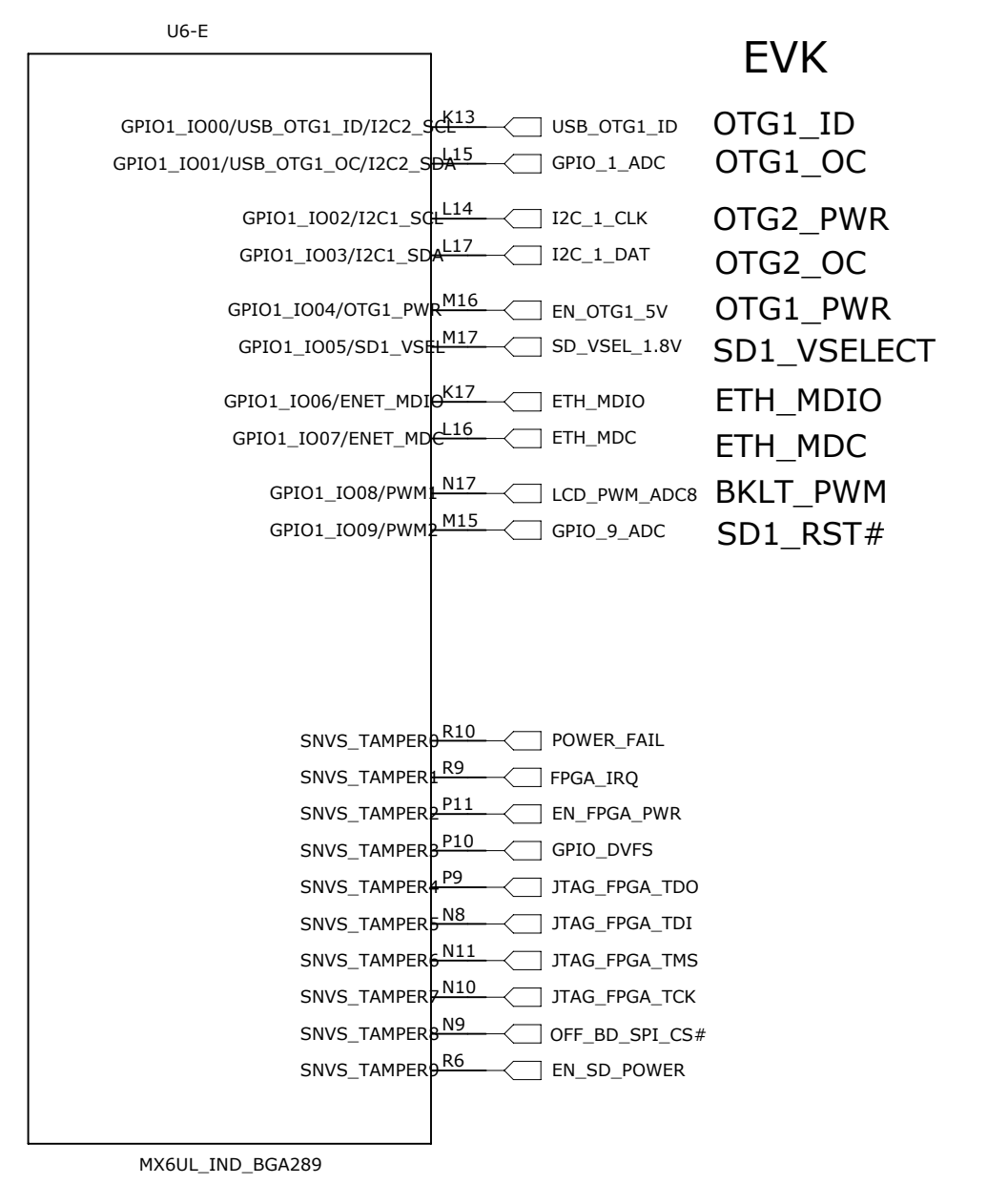
6UL UART and Control



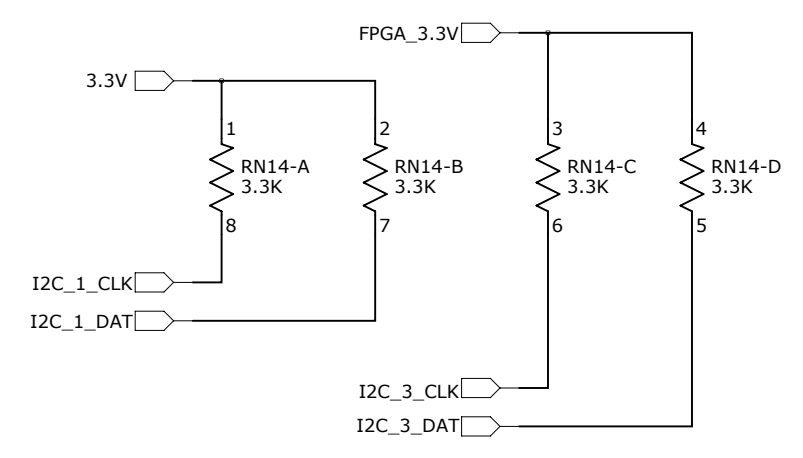
6UL Camera



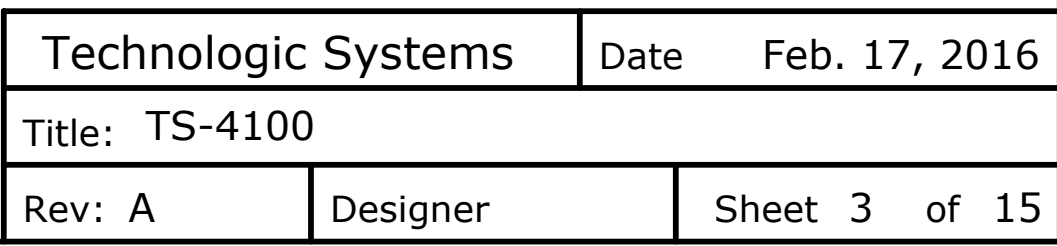
6UL DIO



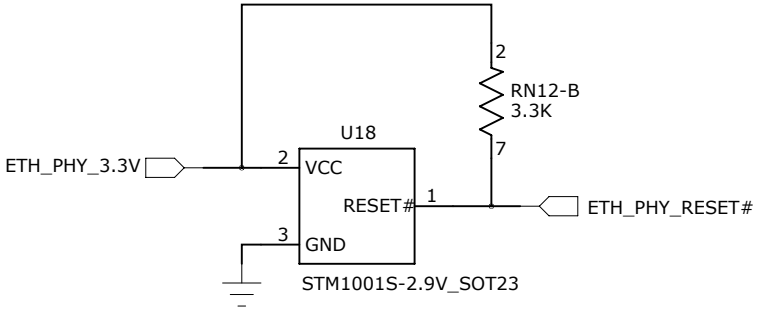
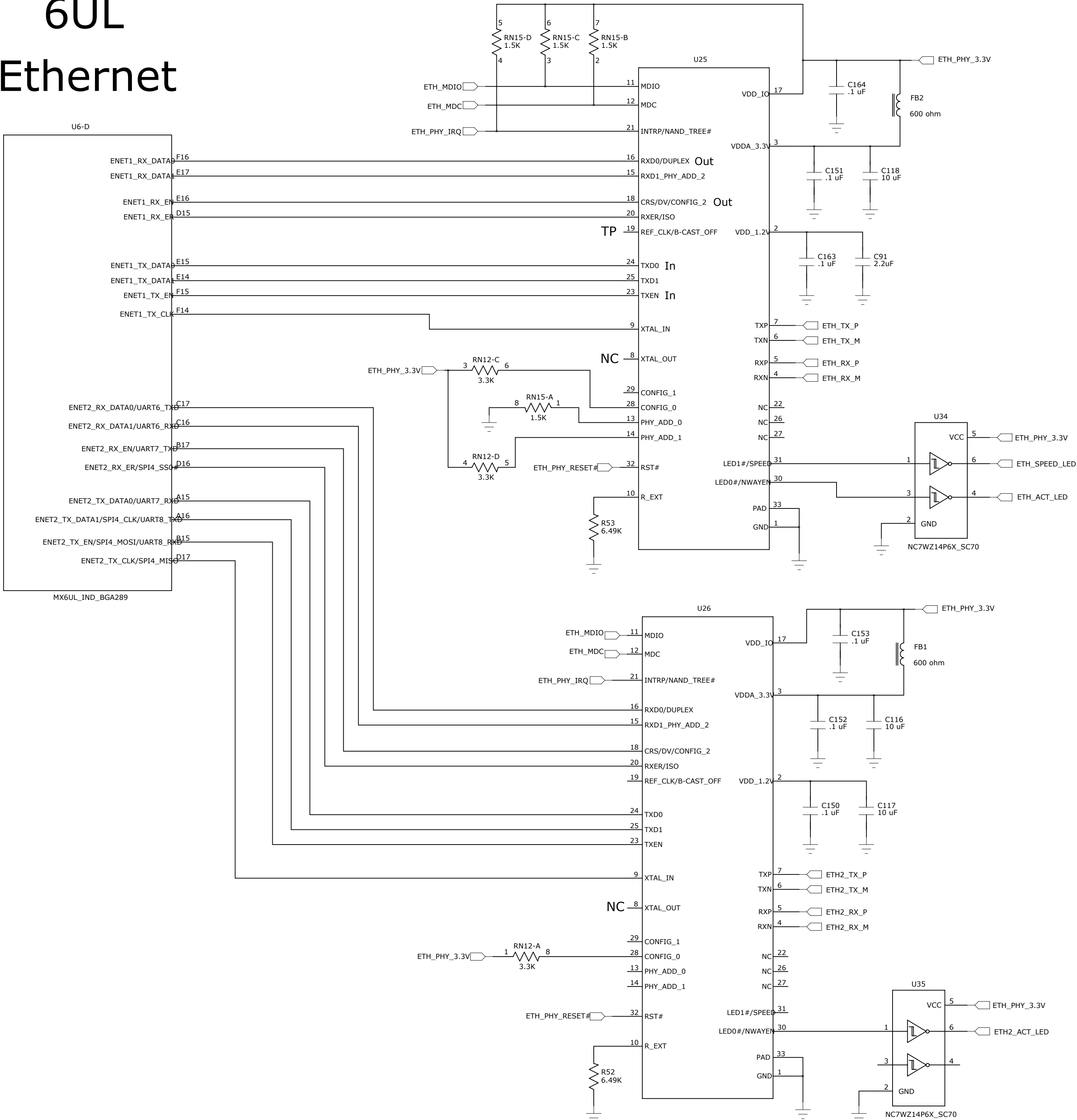
I2C PU Res.



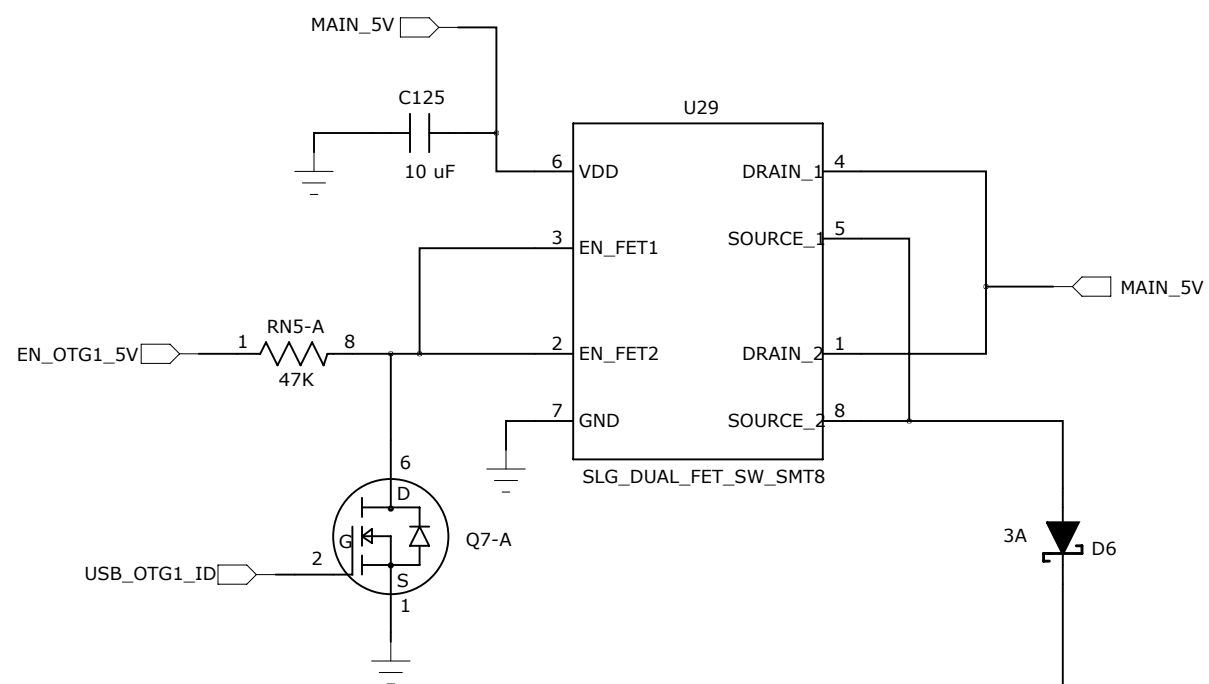
EVK has 512MB



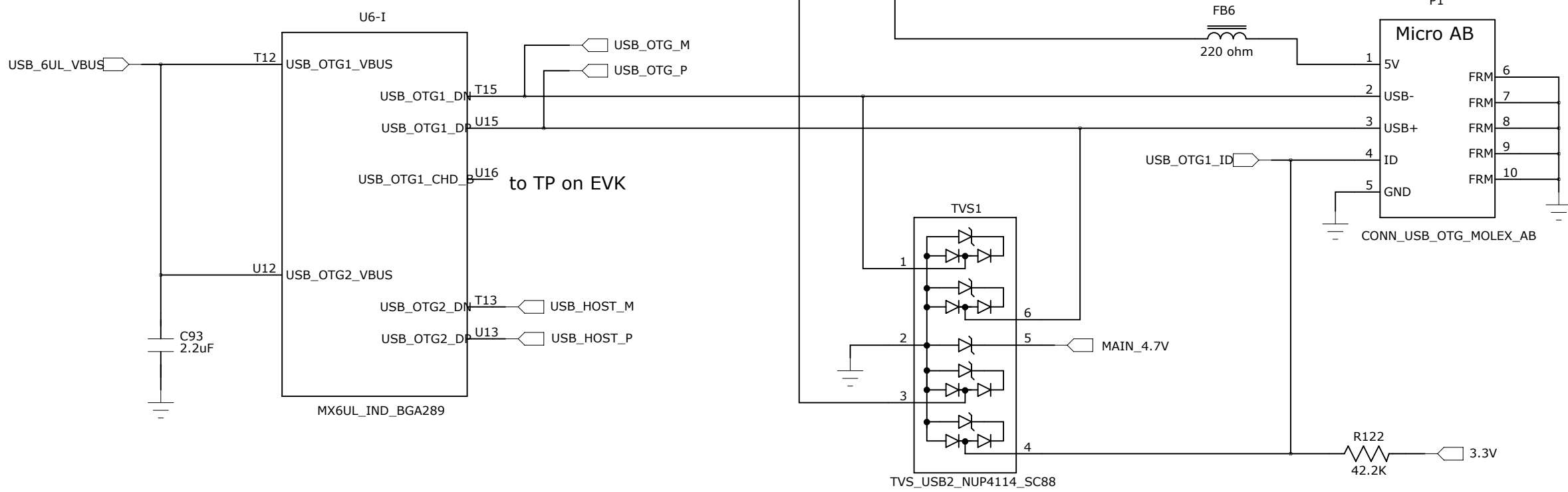
6UL
Ethernet



USB 5V Switch



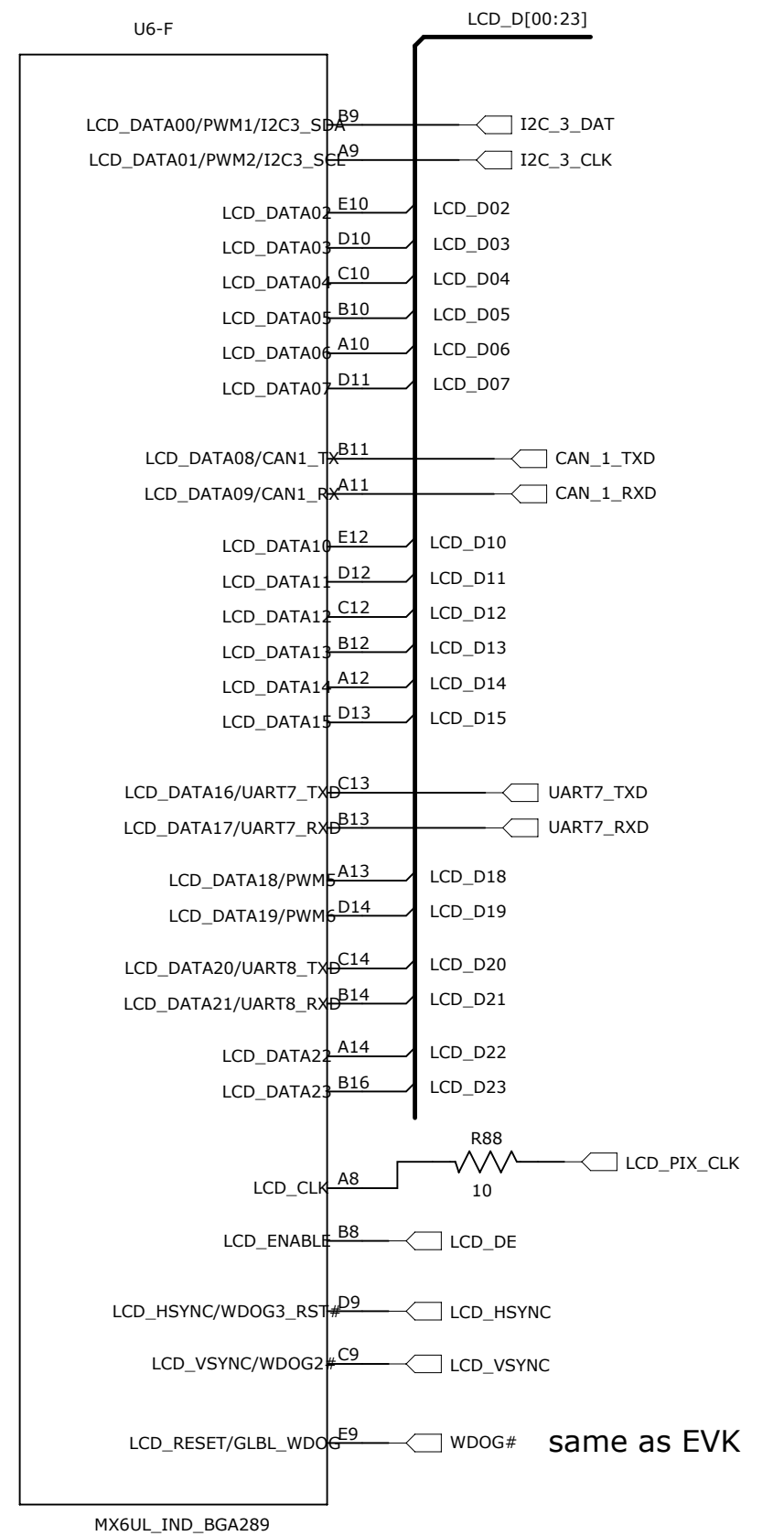
6UL USB Ports



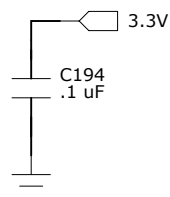
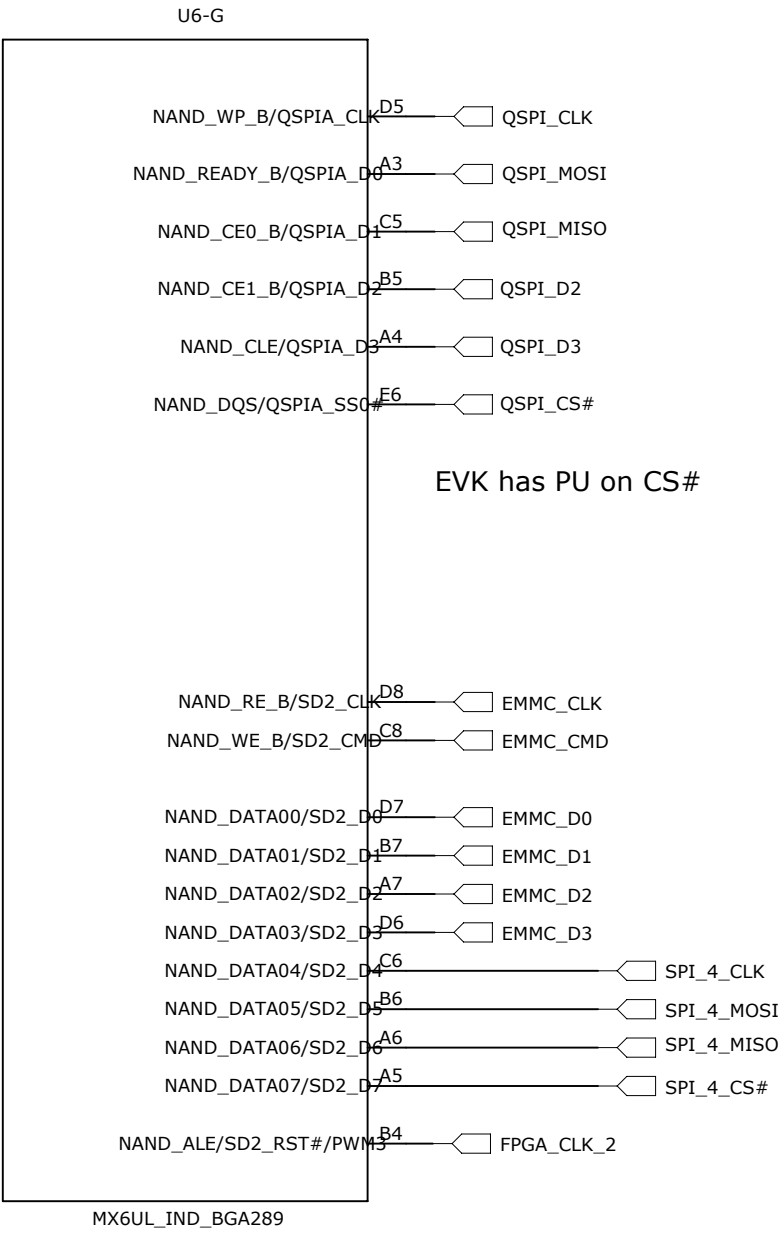
USB OTG

Micro AB

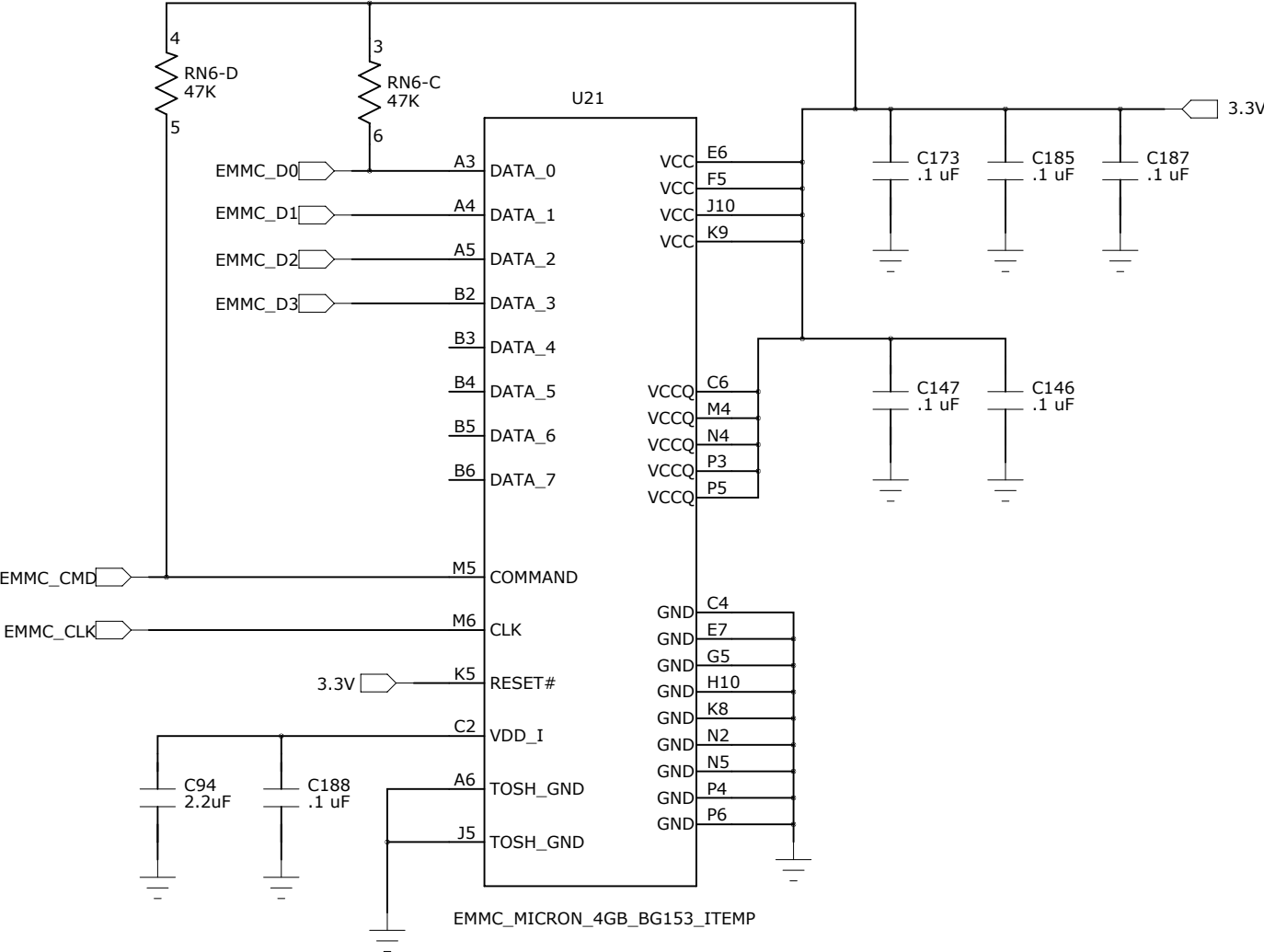
6UL LCD



6UL Flash

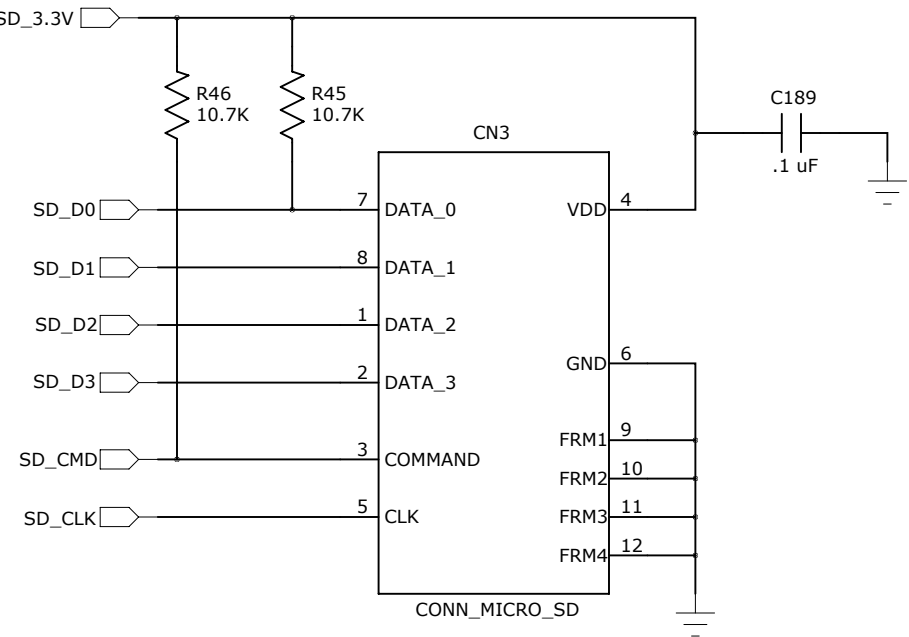
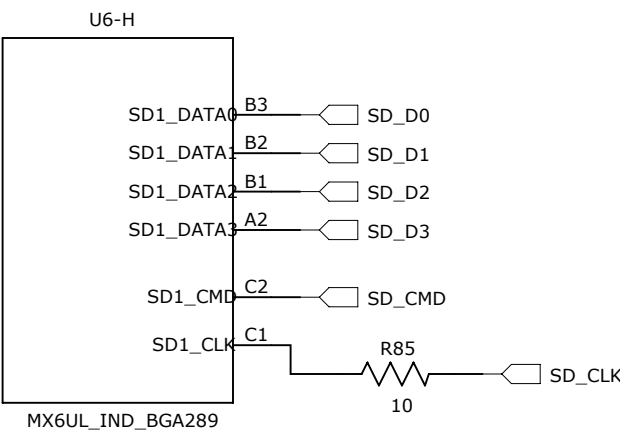


eMMC 4GB - 64GB

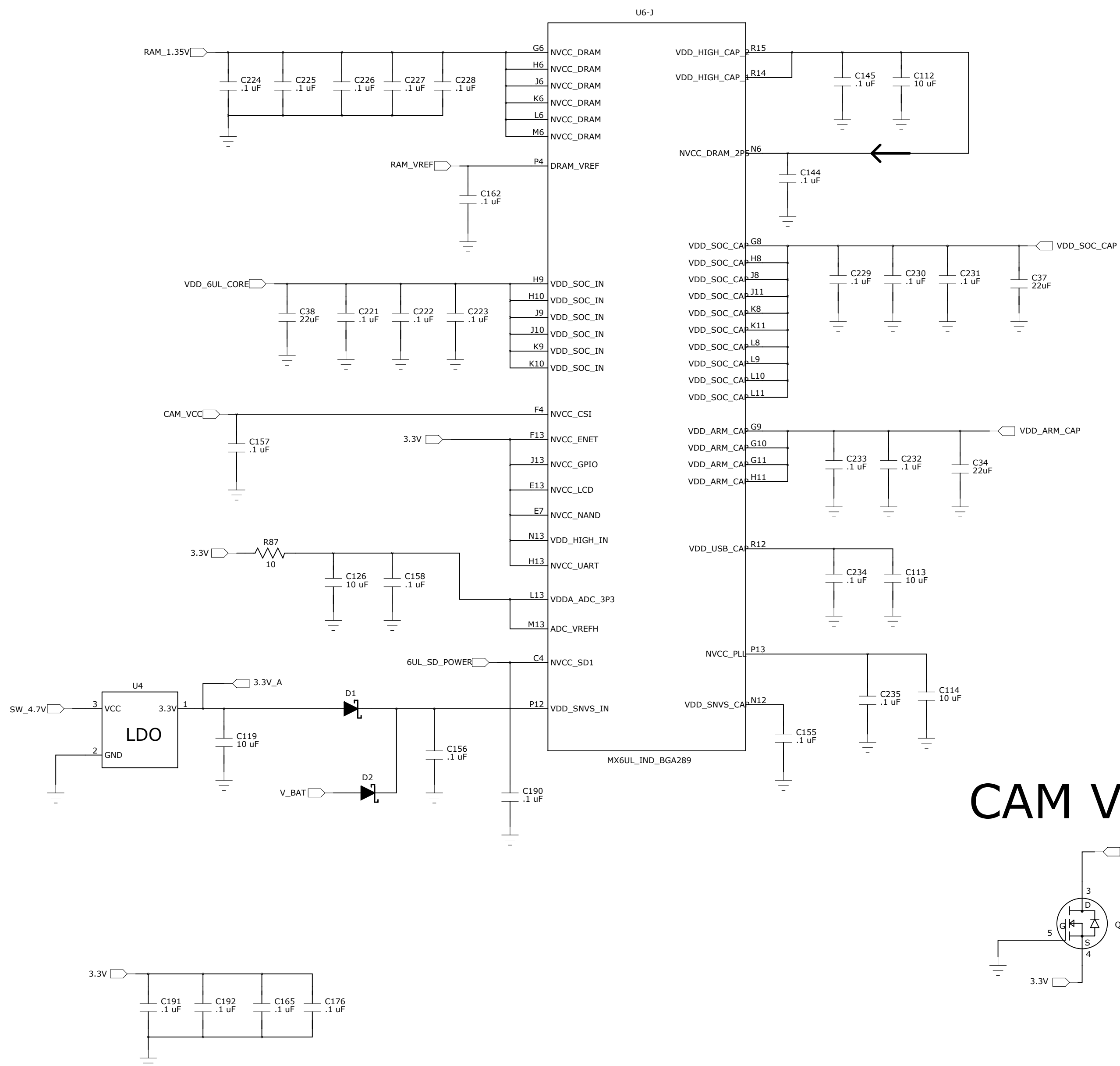


Micro SD Card Socket

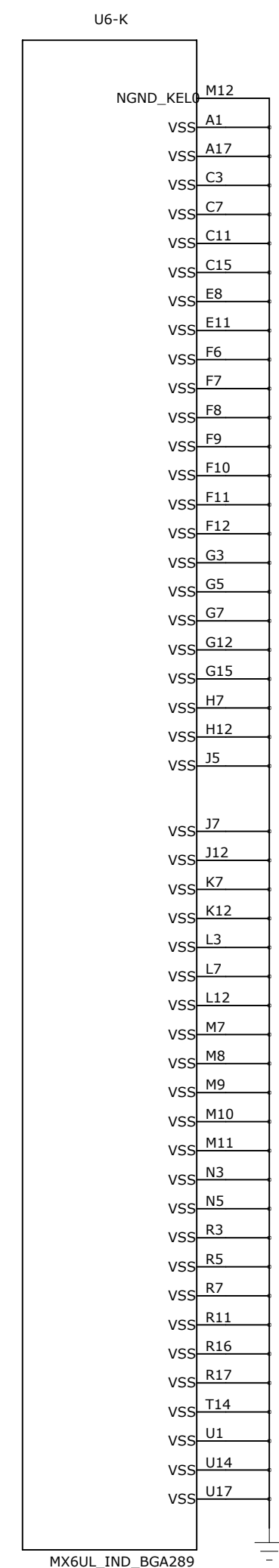
6UL SDIO



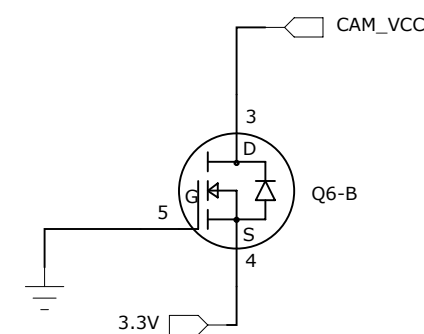
6UL Power



6UL GND



CAM VCC



SD Card 1A Reg
1.8V or 3.2V

3.3V --> 6UL_SD_POWER

3.3V 2A Reg

SW_4.7V --> 3.3V

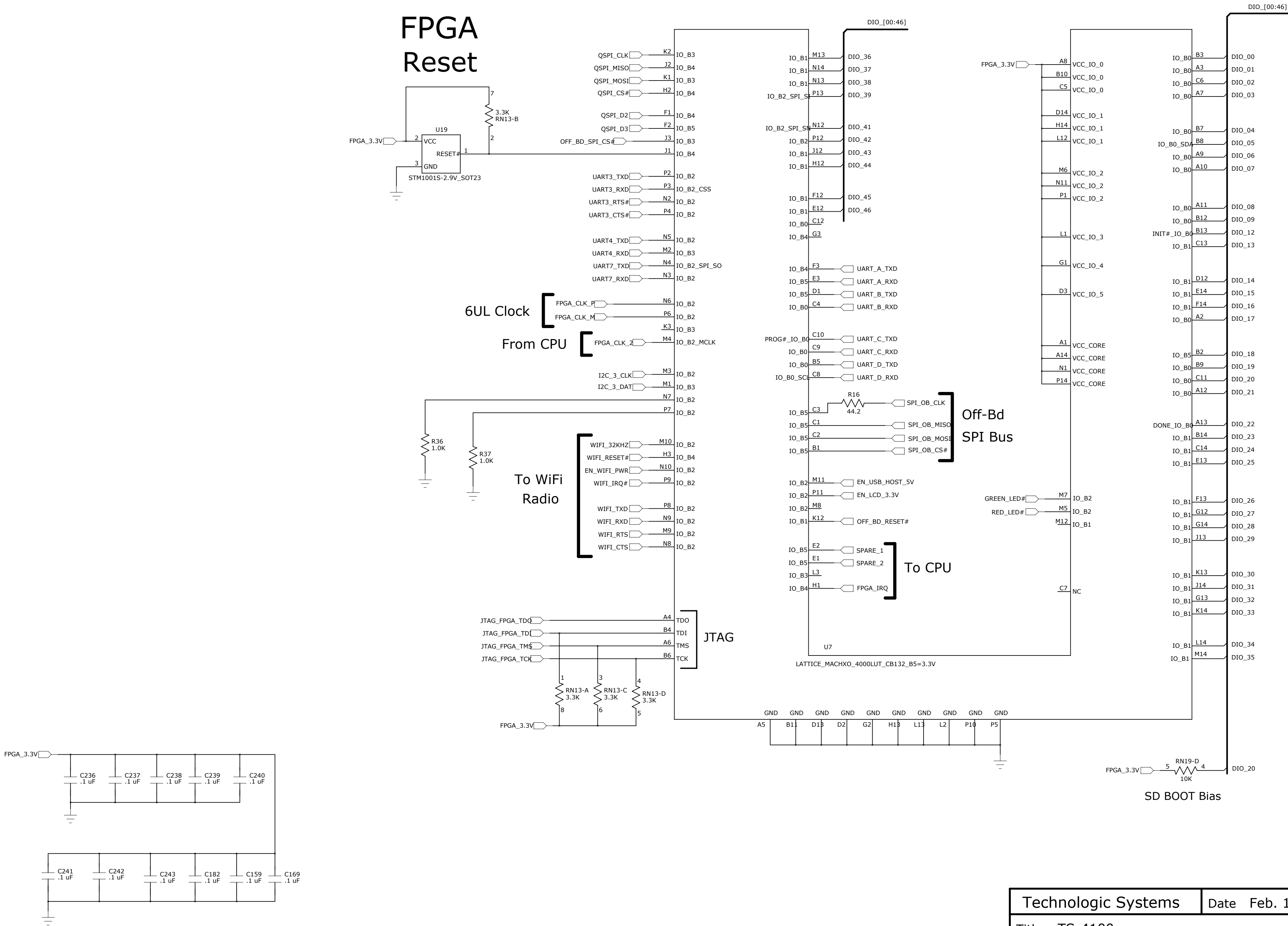
CPU Core 1A Reg

SW_4.7V --> VDD_6UL_CORE

RAM 1.35V 1A Reg

SW_4.7V --> RAM_1.35V

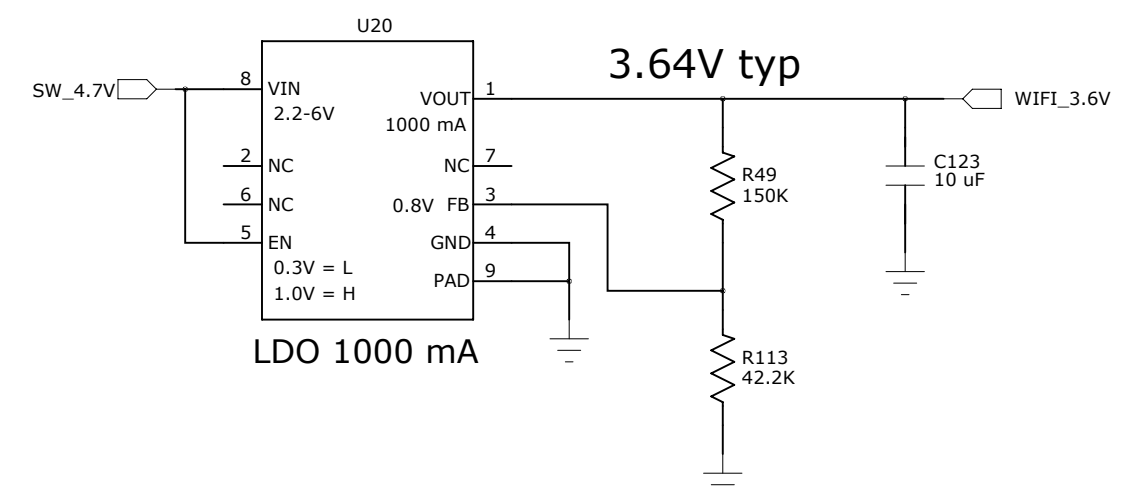
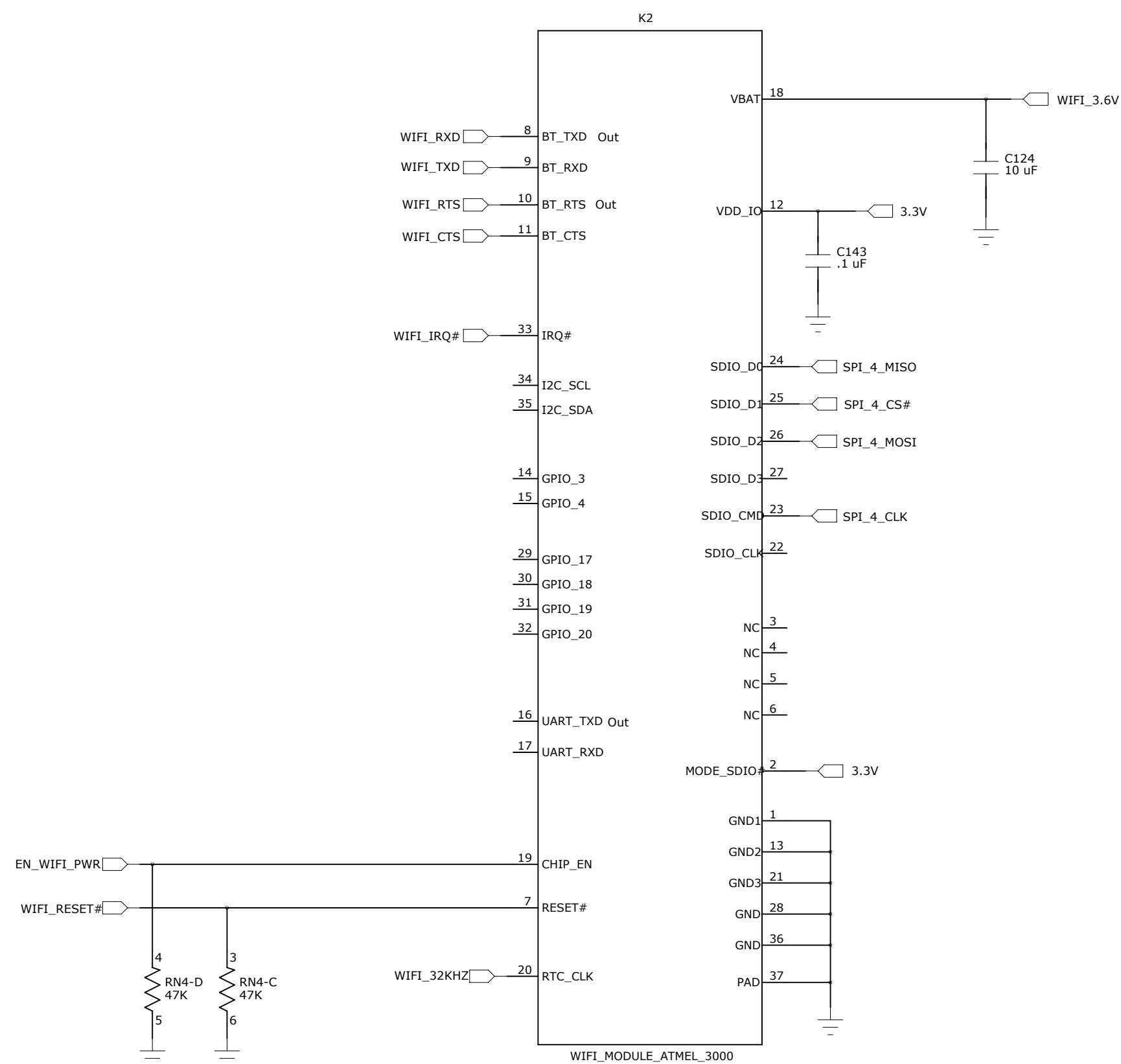
MACH XO2 FPGA



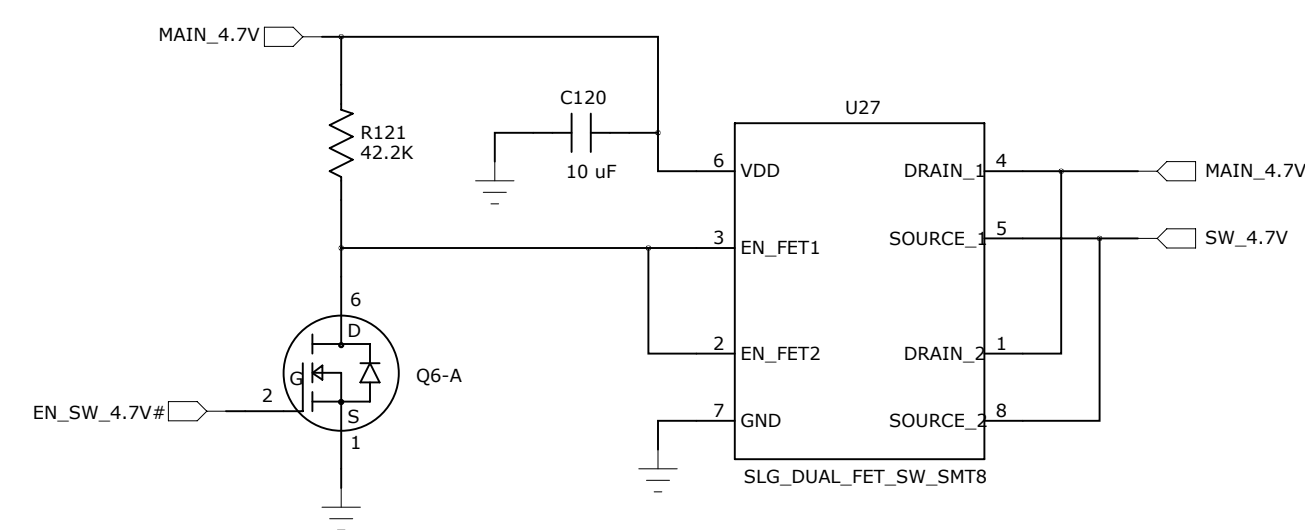
WiFi

WiFi / Bluetooth Radio Module

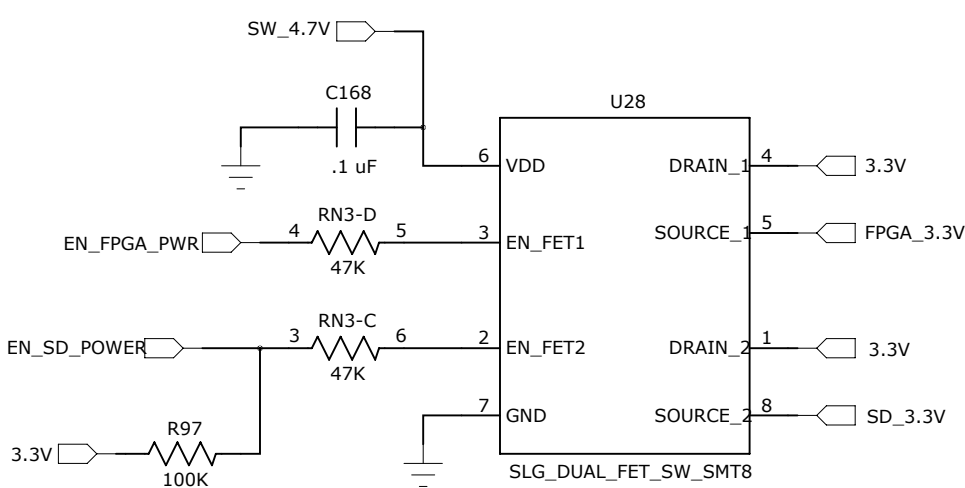
WiFi 3.6V Regulator



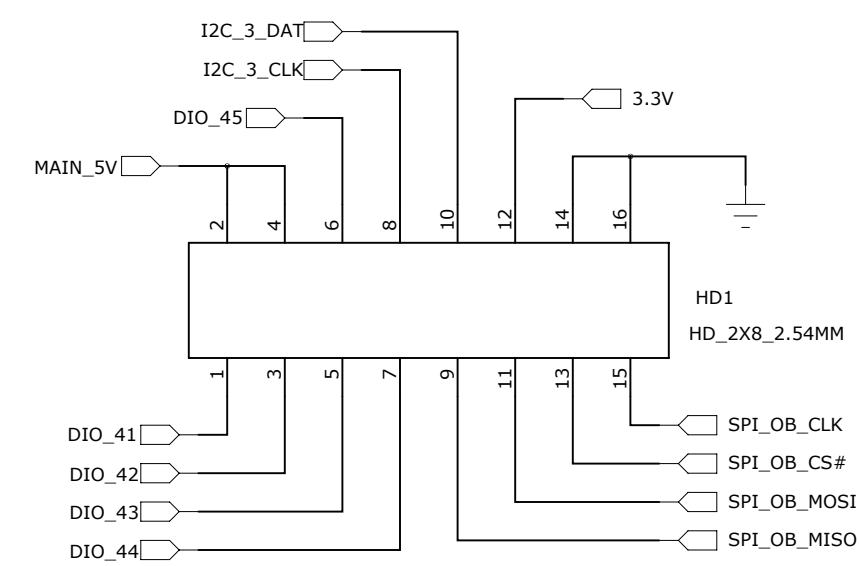
Main 4.7V Power Sw.



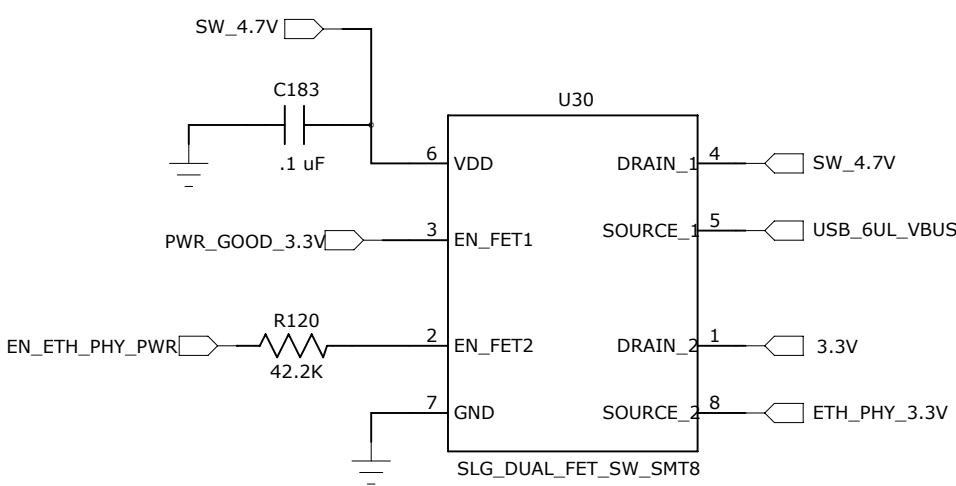
FPGA and SD Card Power Sw.



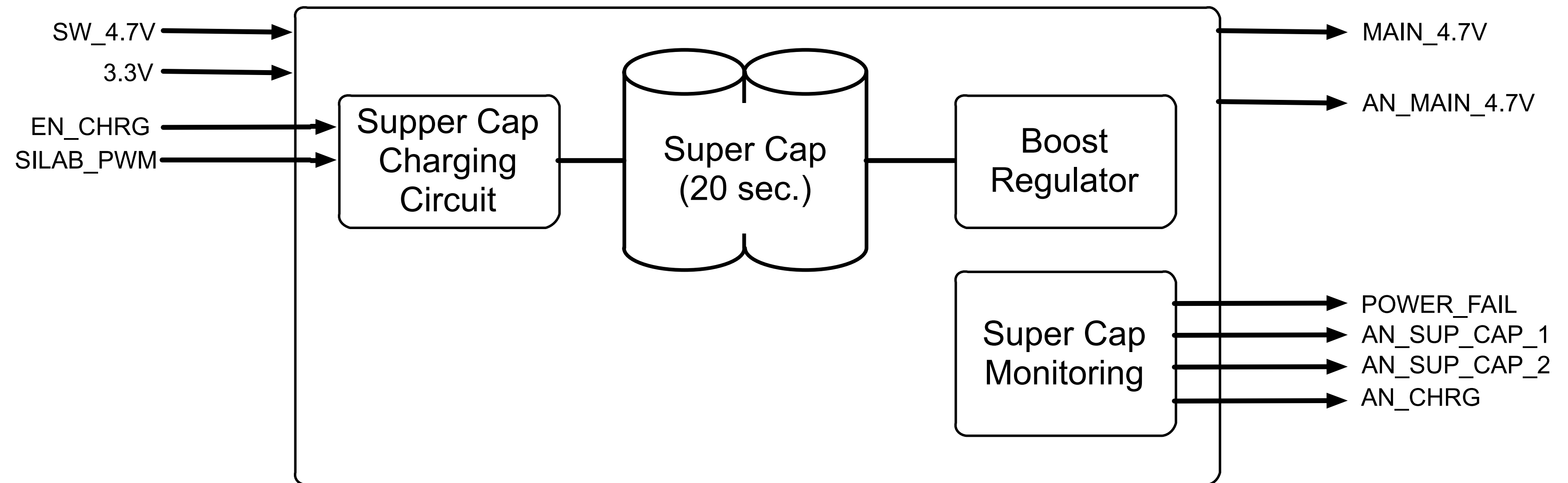
16-pin Header



USB VBus and Eth Power Sw.

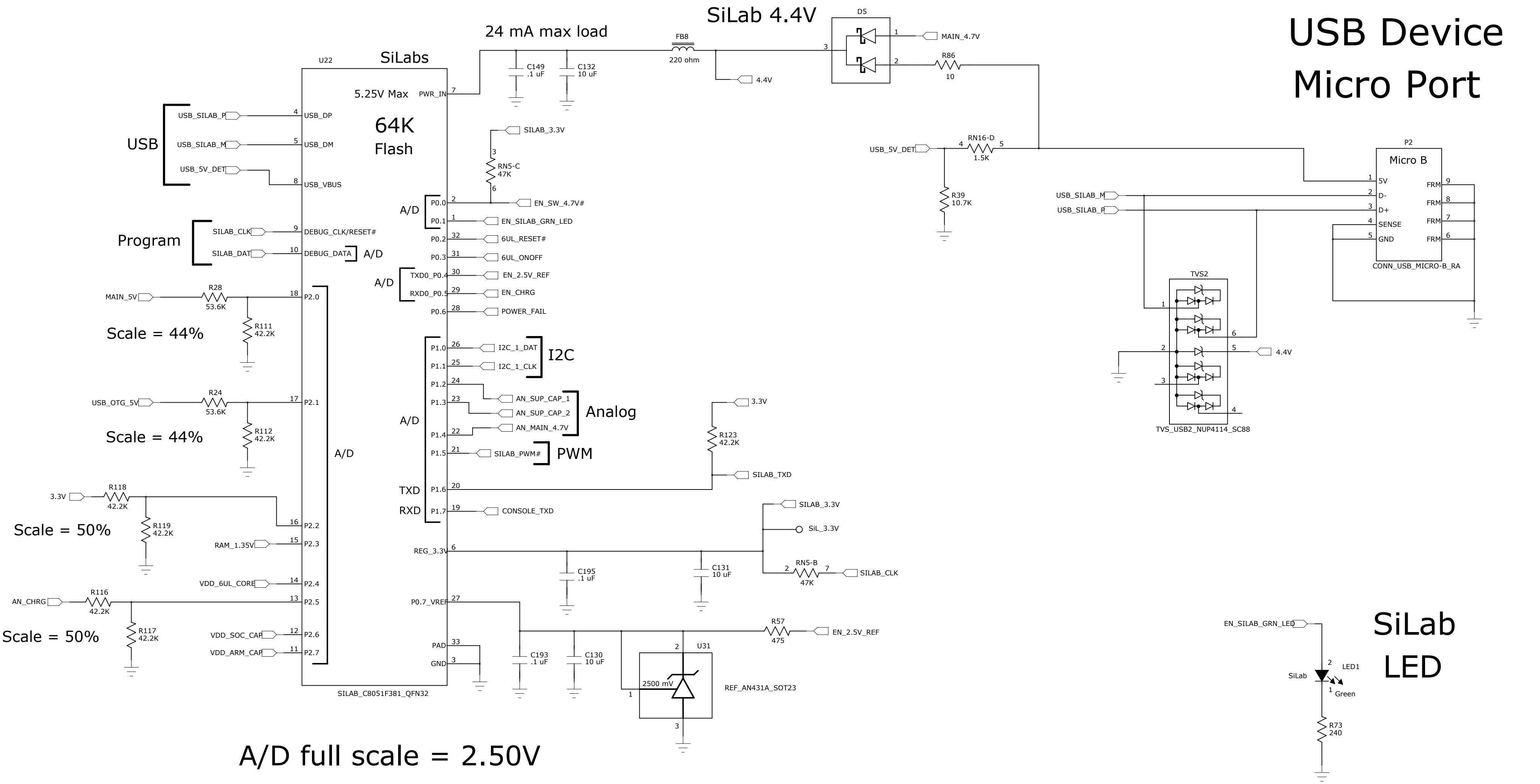


SuperCap 10 Second Power Hold



10 seconds assumes 2 watt load
10F SuperCaps charged to 4.7V
Functions down to SuperCap = 3.5V

USB Device Port and SiLab uC



Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 4.7V to 5.3V to these pins

Current drain is approximately 300 mA

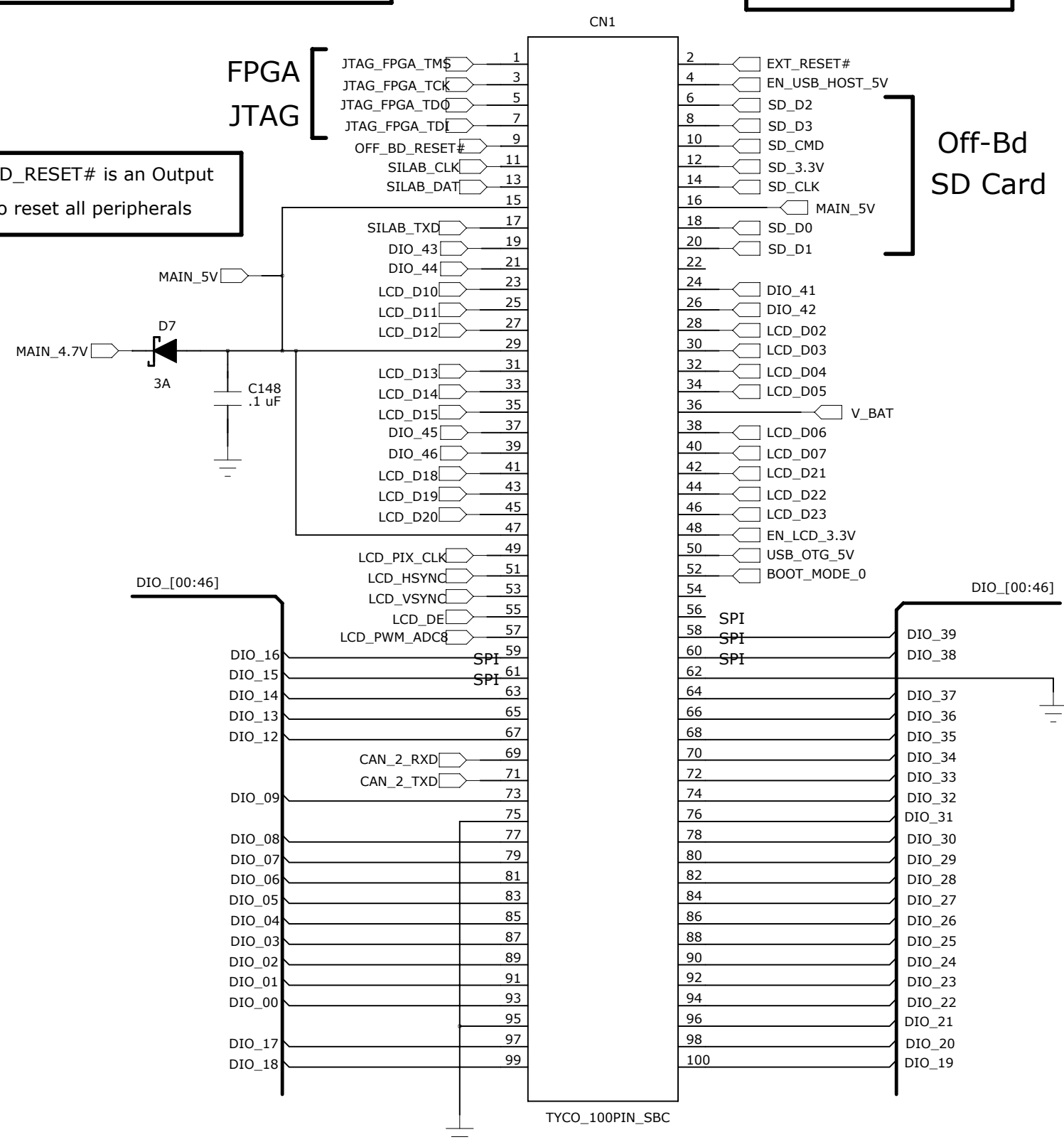
EXT_RESET# is an Input
used to reboot the CPU

Do not drive active high
(use open drain)

⚠ All signals driving DIO on CN1 & CN2 must be powered by the 3.3V on CN2, or remain at 0V until the CN2 3.3V rail is > 3.0V

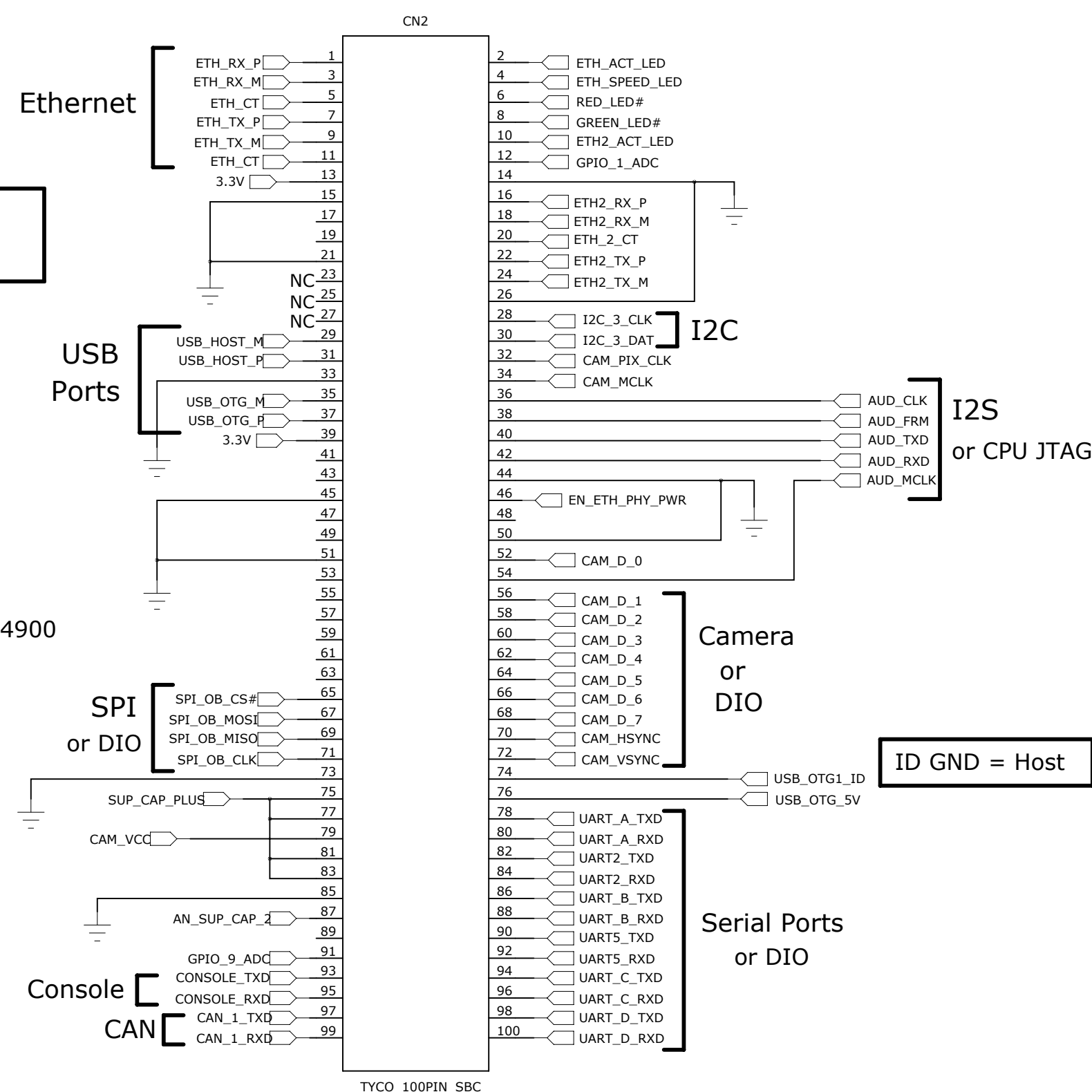
Left

Right



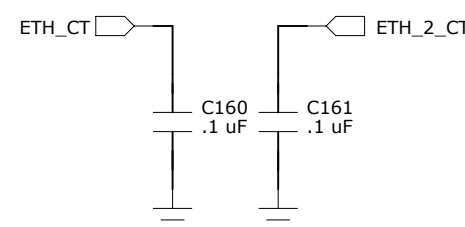
3.3V rail can supply up to 500 mA to base board

pin 63 = rail on 4900



Boot Strap

DIO_20 BIAS	TS-4100 Boots from
1	eMMC Flash
0	SD Card



Base board should connect CN2 pins 39 and 79 together if the CAM DIO should use 3.3V levels
If not connected, they will have 2.6V levels