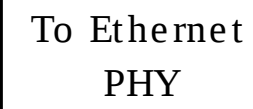


U3-C



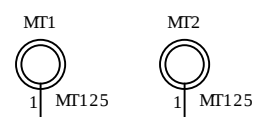
CPU_RESET#
is bi-directional and
can be programmed
to cause interrupt
instead of reset

Suggest PA6 = En_Power to RS-232 Transceivers

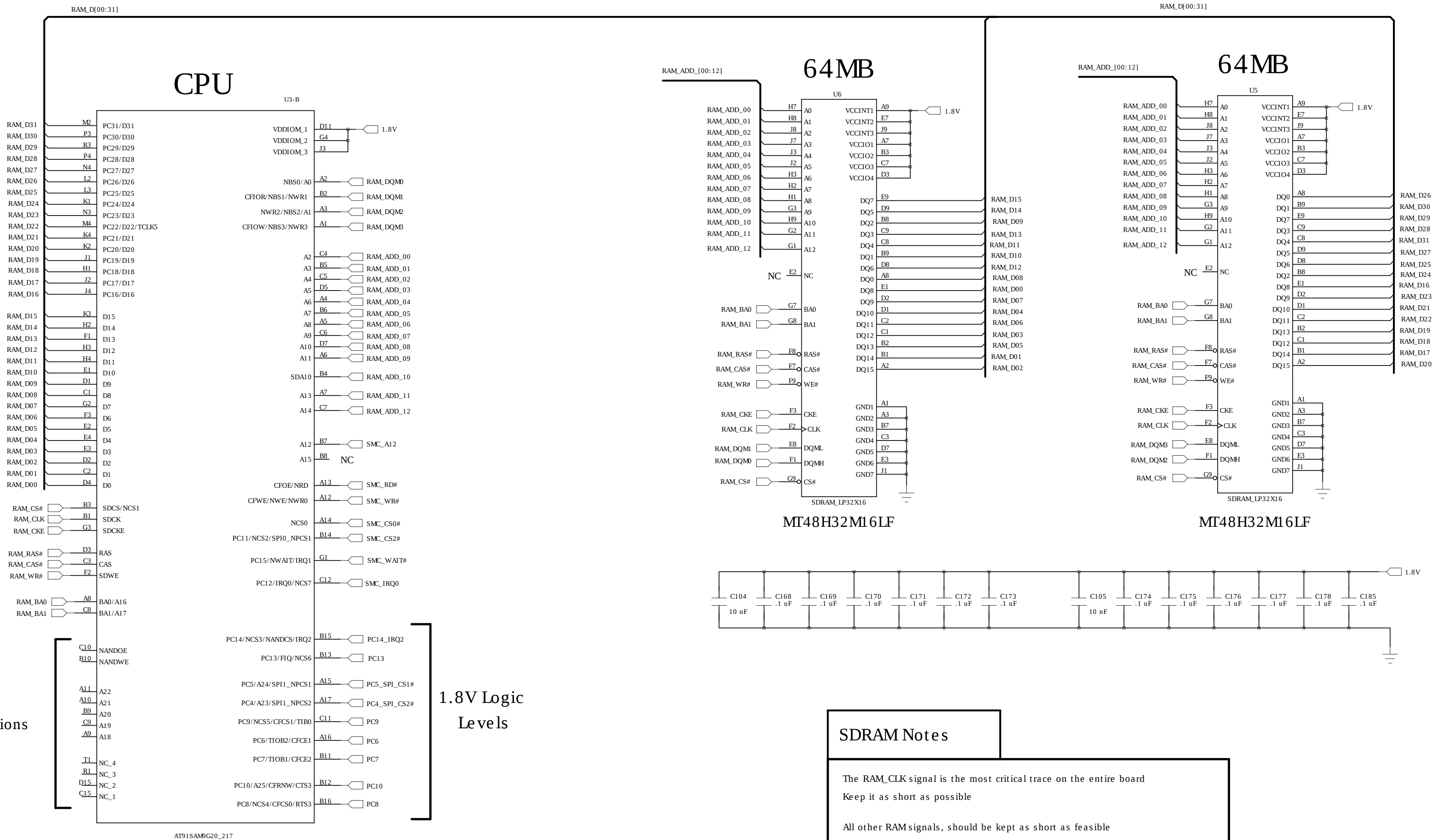
```
BMS = "1" --> Boot from Internal ROM
TST = "1" --> Factory Test Mode
OSC_SEL = "0" --> Use internal RC Oscillator
```

JTAG_SEL
= Boundary Scan
= CPU ICE mode

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Title: TS-4200 CPU			
Rev: D	Designer	Sheet	1 of 7



128 MB RAM



No Connections

1.8V Logic Levels

SDRAM Notes

The RAM_CLK signal is the most critical trace on the entire board
Keep it as short as possible

All other RAM signals, should be kept as short as feasible
Some RAM signals go to the FPGA also - this is a complication

RAM data signals can be swapped bit-wise or byte-wise
For example, D16-D23 can be swapped with D24-D31
This would require the respective DQMx lines to be swapped as well

Bit-wise swaps are allowed within a byte
For example, D2 and D5 can be swapped

A3P125 has:

- 3000 Tiles (about 1200 LUTs)
- 4 Kbytes total of Block RAM
- 97 I/O with 144 pin package
- "true instant ON"
- Input PLL clock = 1.5 MHz min

Warning: MUX_AD00 thru AD07 is used by NAND Flash

Devices connected to this bus must never drive it when BUS_RD# is deasserted (must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low if they need more than 150 nS strobe

FPGA_CLK = CPU Timer Out

DIO_09 = Push_switch

All NVRAM interface signals must be kept in low state when not accessing NVRAM

RED_LED# and GREEN_LED# must be Open Drain

When SYSTEM_RESET# asserted, then set these as follows:

Asserted:

- OFF_BD_RST#
- EN_SDCARD_PWR#
- RED_LED#
- GREEN_LED#

Deasserted:

- EN_ETH_PWR#
- REBOOT
- NVRAM_CS
- NAND_CS#

When SYSTEM_RESET# deasserted, Latch BUS_ALE# and BUS_RD# into a register

Early Boot code should deassert OFF_BD_RST# signal. (after SPI Flash loaded into RAM)

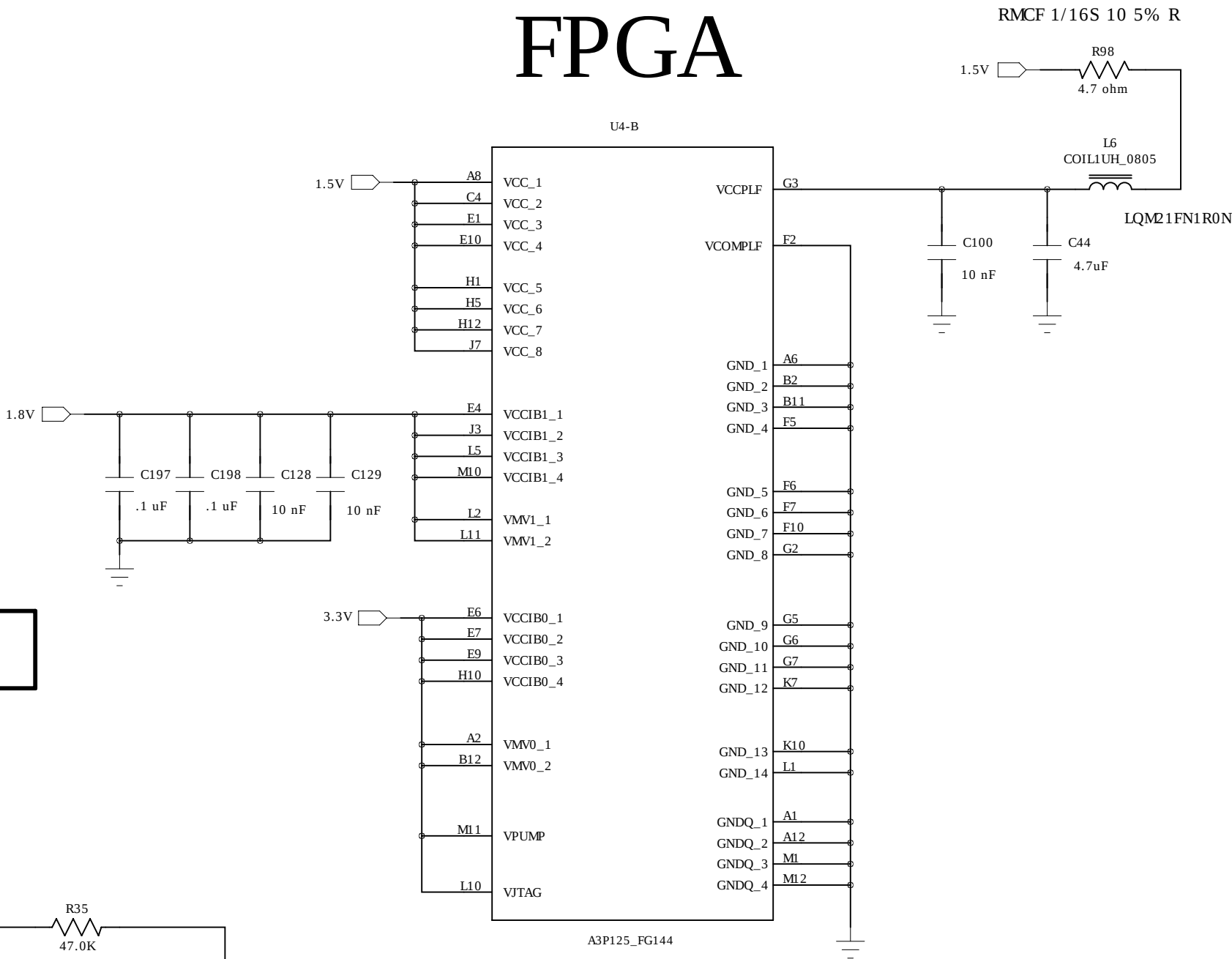
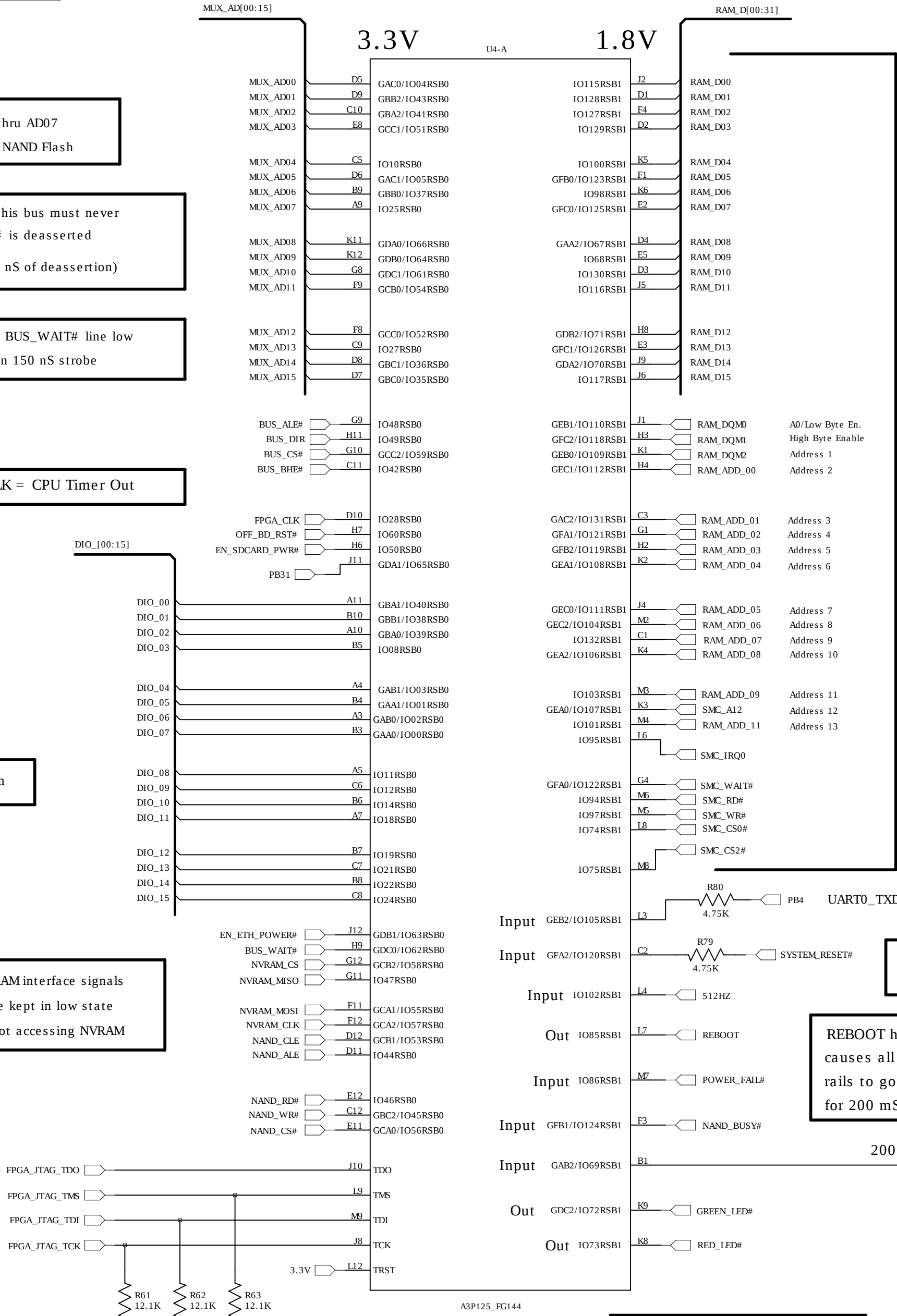
Boot Straps

Mode 2	Boots from
1	NAND Flash
0	SD Card

BUS_ALE# = MODE1
BUS_RD# = MODE2

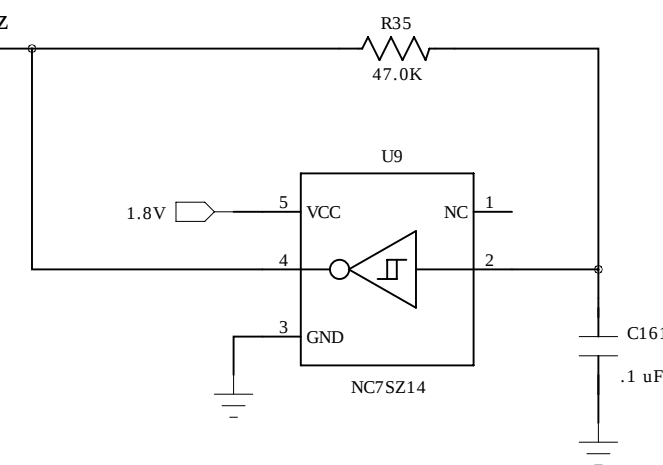
To CPU
Address/Data Bus

FPGA

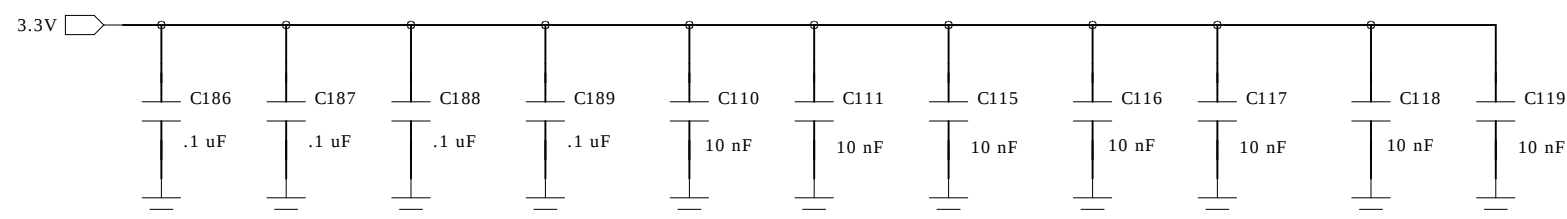
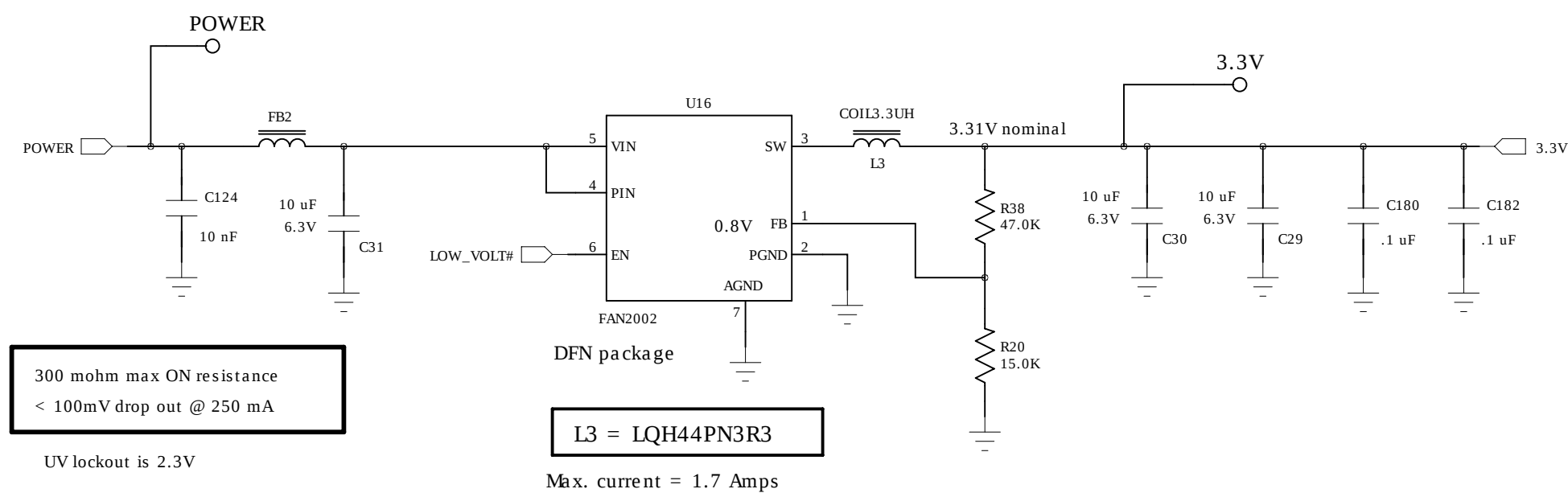


Inputs with 1.8V rail have diode clamp to 1.8V

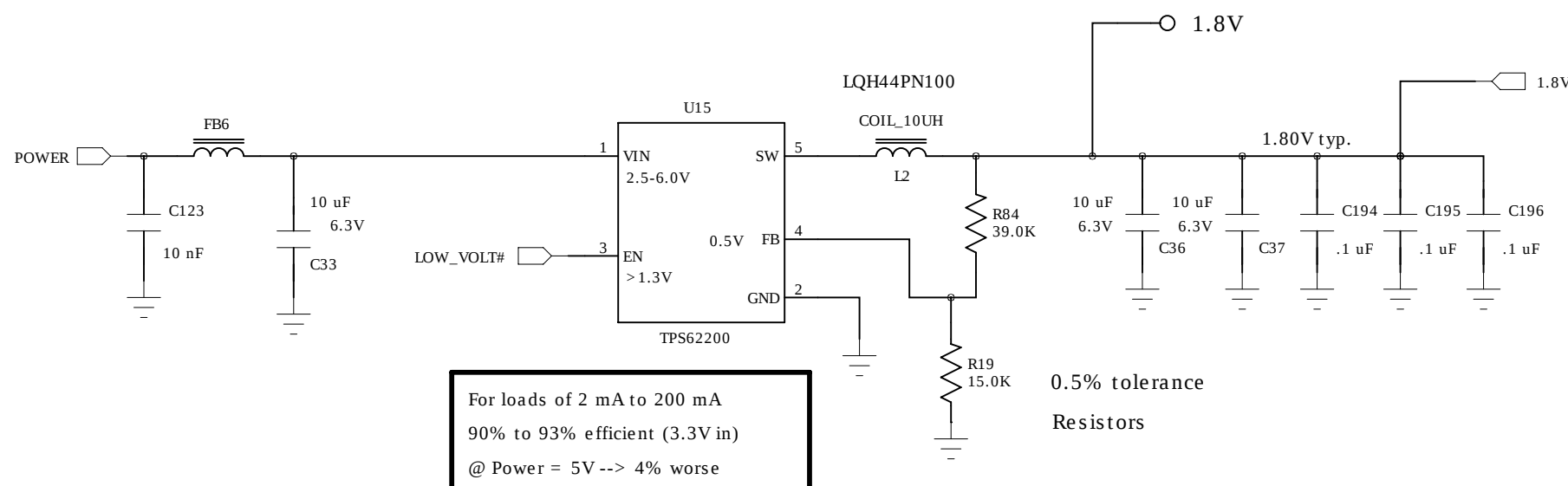
REBOOT high causes all power rails to go low for 200 mS



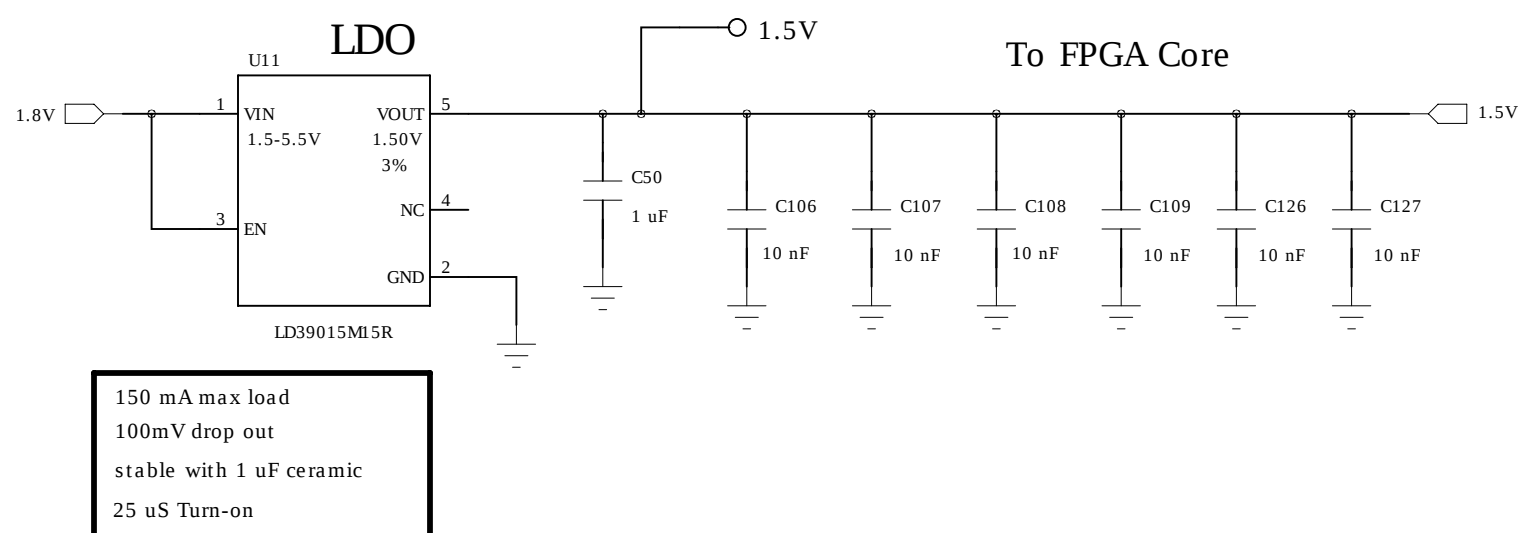
3.3V Supply



1.8V Supply



1.5V Supply



Power Sequence

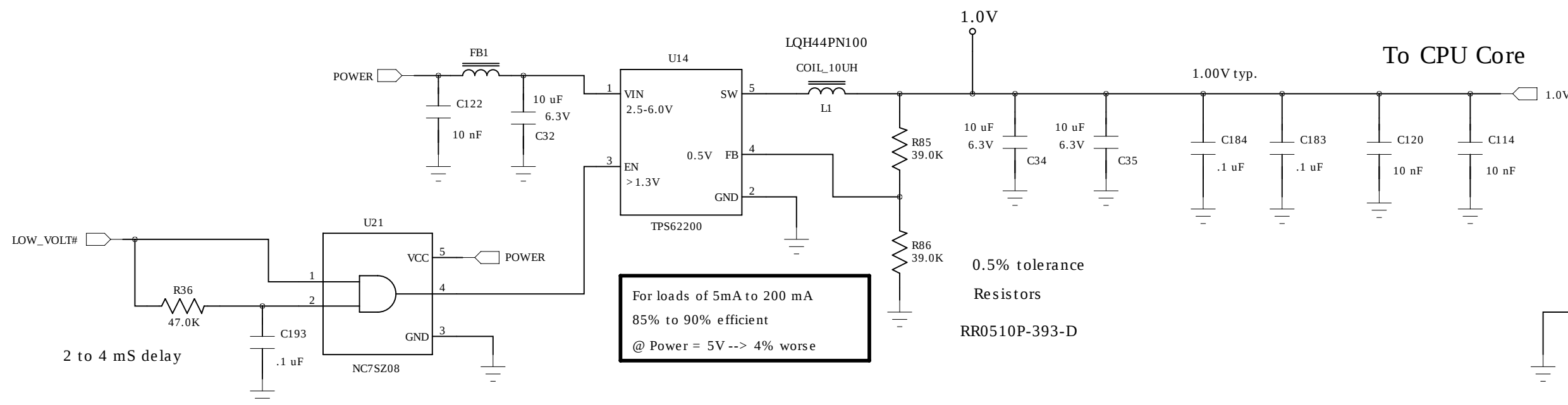
After power is first applied, or after a "Reboot"
All power rails are off for 200 mS then:

- the 3.3V and 1.8V are enabled
these will reach 95% in about 800 uS
(the 1.5V rail will ramp 25 uS delayed)

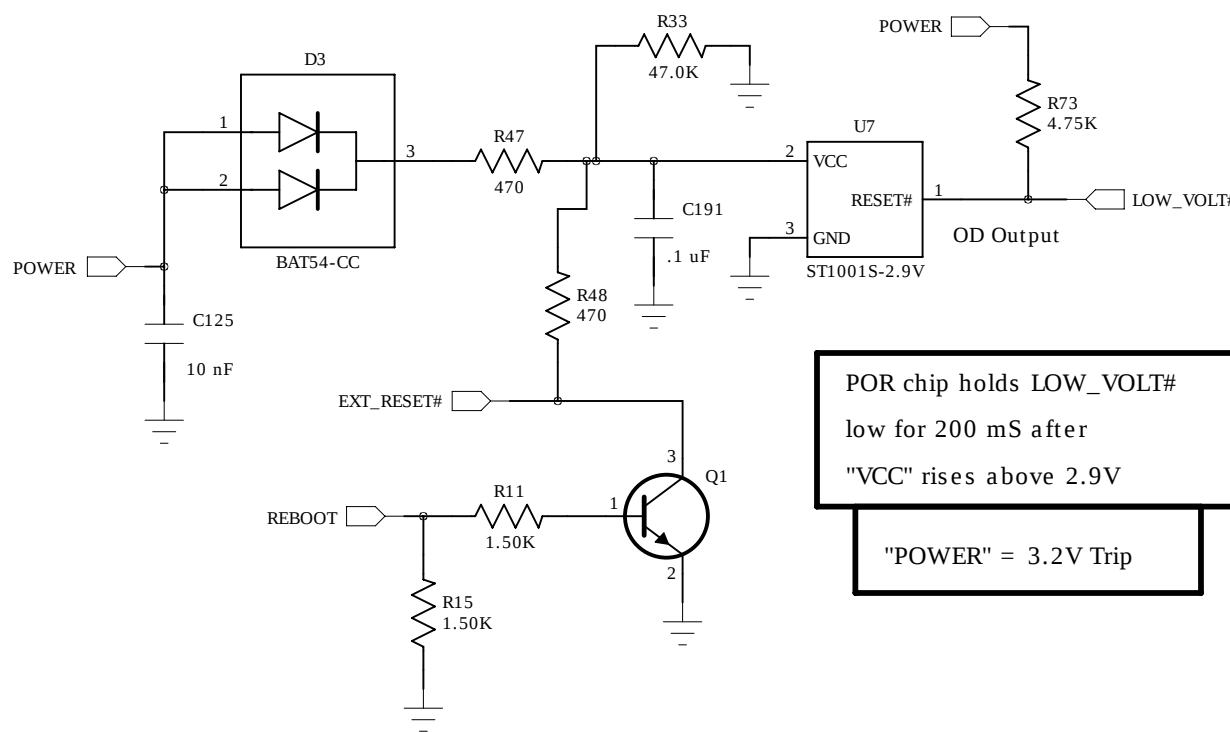
- Then 2-4 mS later, the 1.0V rail is enabled
It also requires about 800 uS to ramp

CPU Reset# is asserted before 1.0V rail is enabled

1.0V Supply



POR



Technologic Systems

Date Oct. 19, 2011

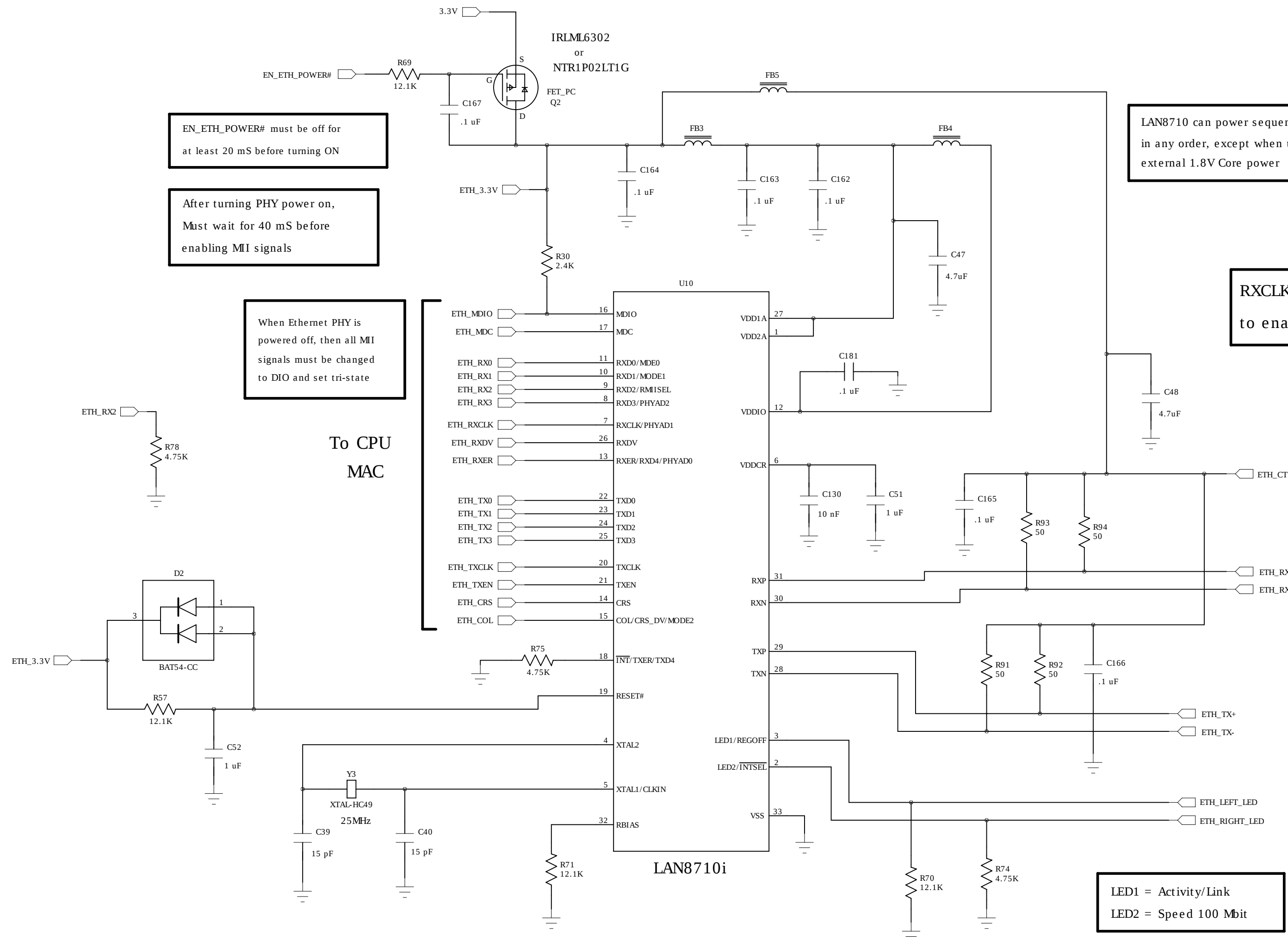
Title: TS-4200 Power Supplies and POR

Rev: D

Designer RLM

Sheet 4 of 7

10/100 Ethernet



Resistor PD on pin 18 is not required per data sheet
But Jesse could not get it to work until we added it

MDIO bus can not be used until 100 uS after Reset# is deasserted

MDCLK max is 2.5 MHz

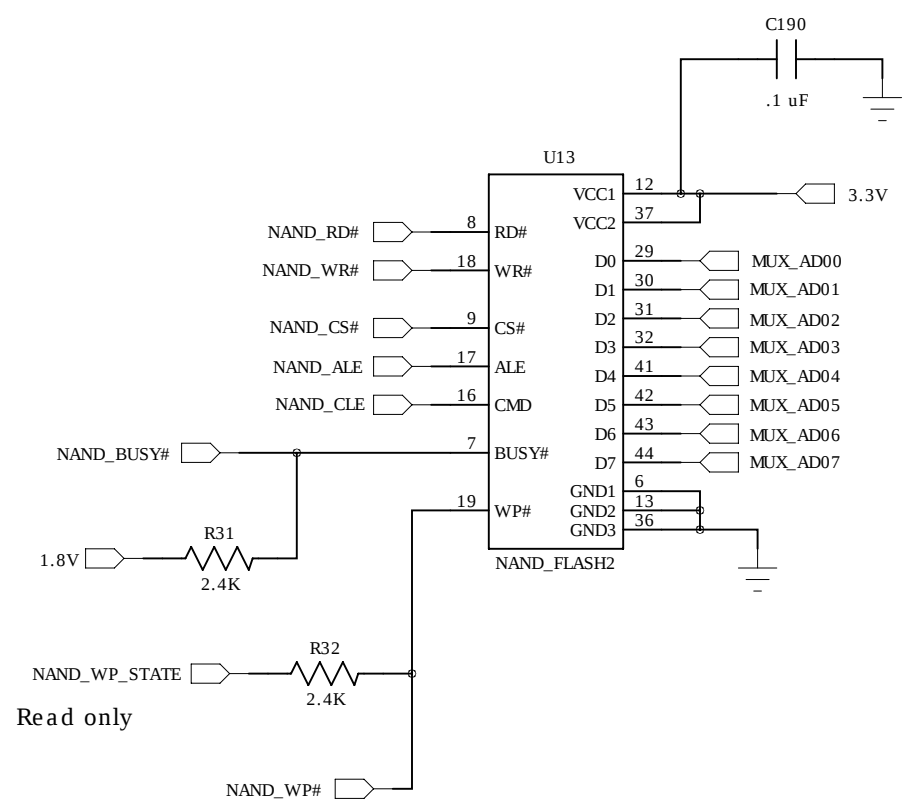
PHY PU and PD resistors are 67K ohm typical

CPU PU resistors are 70K typ. and 40K min.

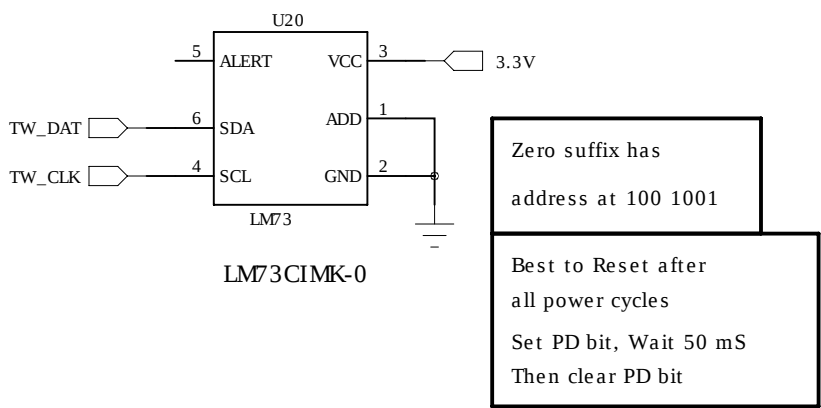
Beware

The PHY address is controlled by strapping pins. If CPU has PU; PHY has PD --> indeterminate

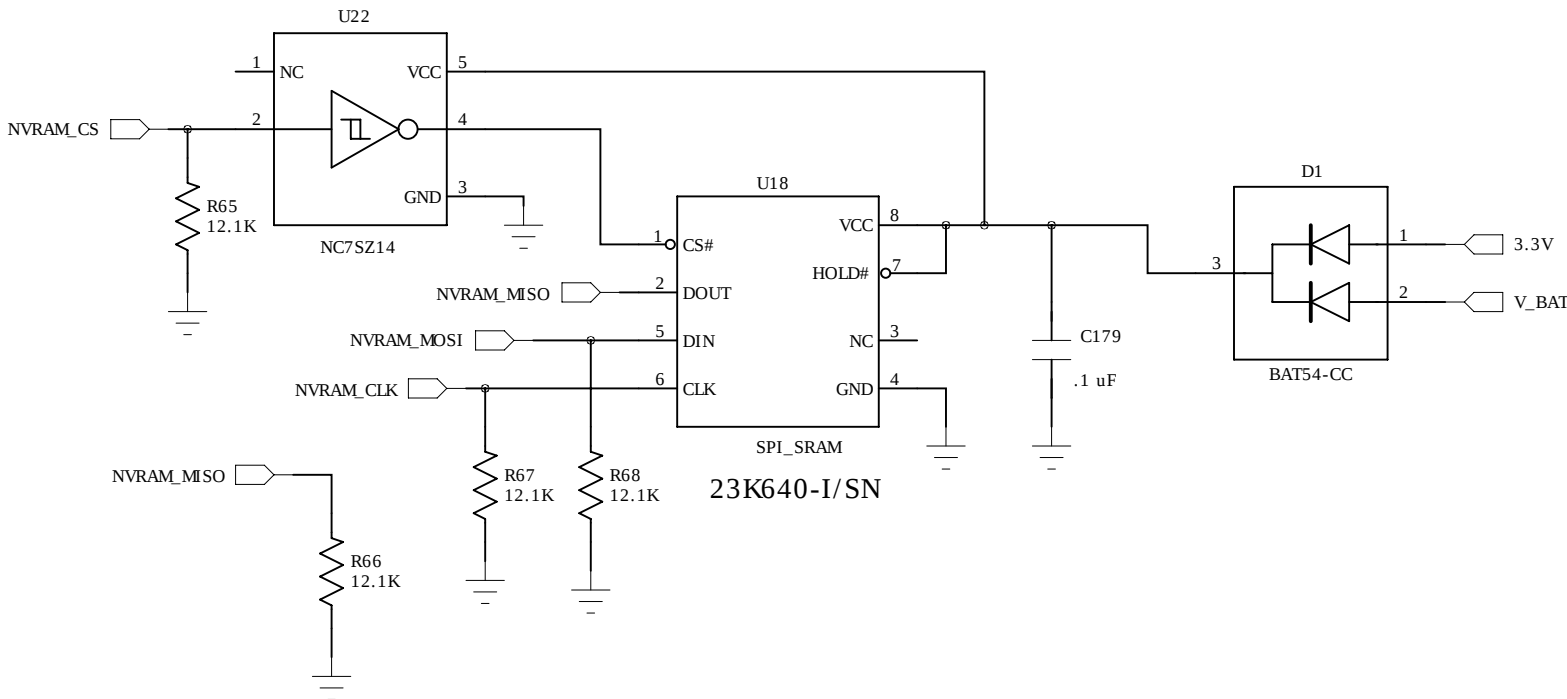
512 MB or 2 GB NAND Flash



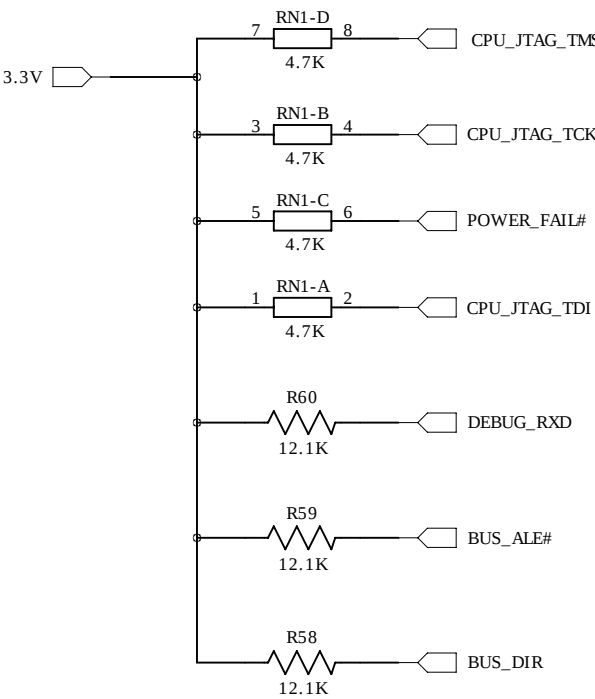
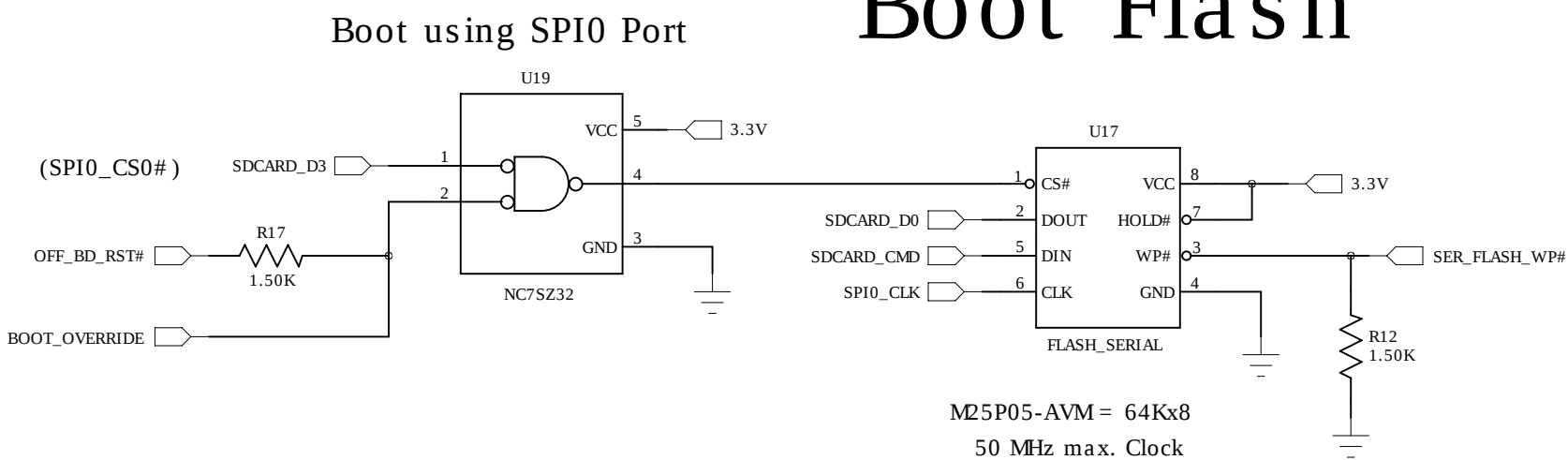
Temp Sensor



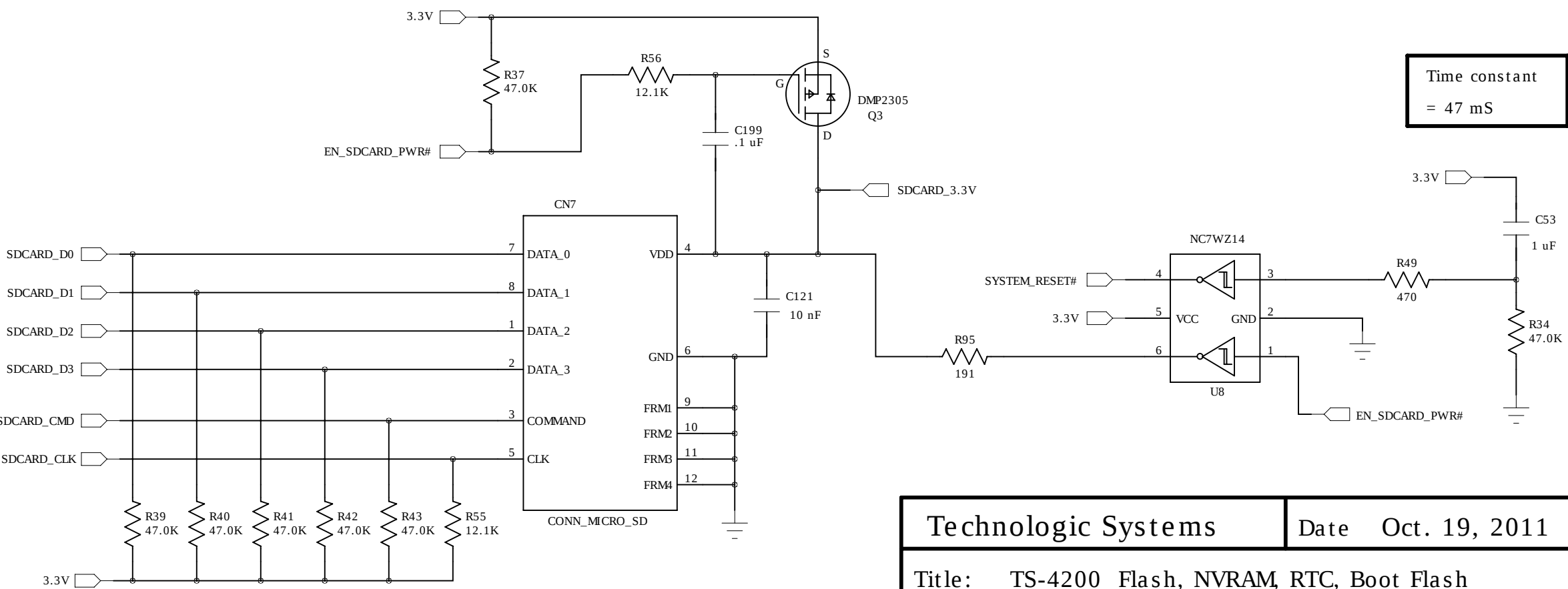
8K Byte NVRAM



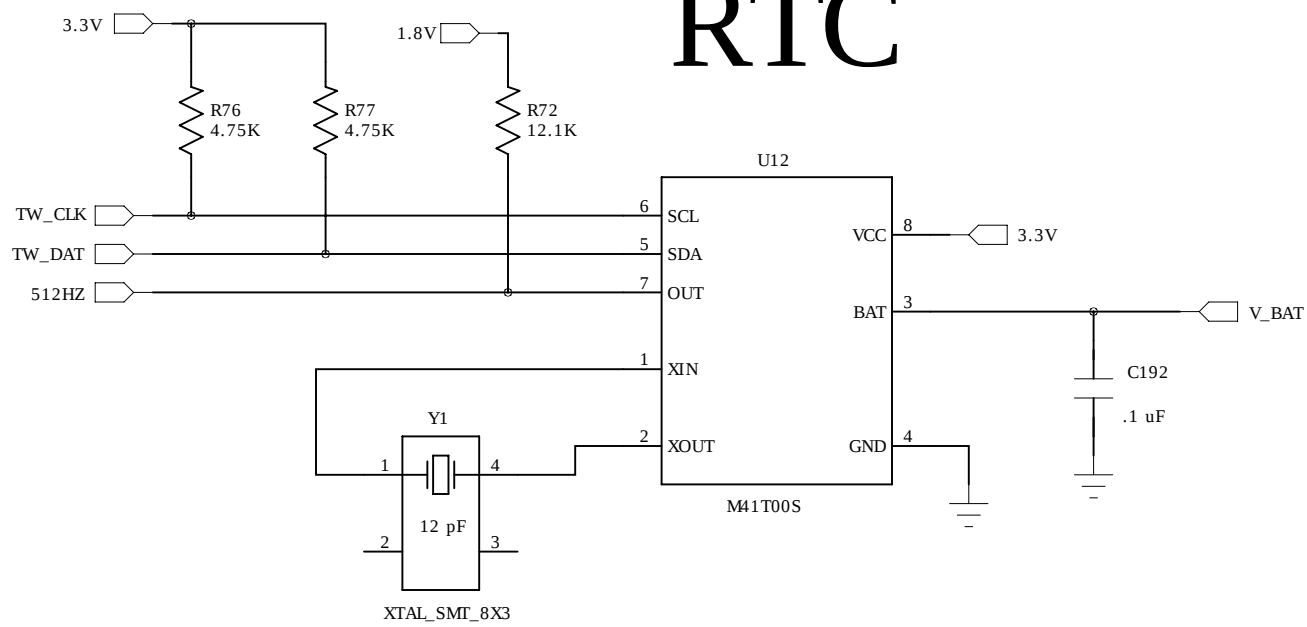
64KB Serial Boot Flash



Micro SD Card Socket



RTC



Technologic Systems	Date	Oct. 19, 2011
Title:	TS-4200 Flash, NVRAM, RTC, Boot Flash	
Rev: D	Designer	Sheet 6 of 7

Two 100-pin Off-board Connectors

"POWER" pins supply all power to the module
Apply 3.6V to 5.5V to these pins

Current drain is 50mA to 400 mA

Left

EXT_RESET# is an Input
used to reboot the CPU

CN2 pin 27 should be connected
to CN2 pin 33 on the base board

Right

FPGA
JTAG

FPGA_JTAG_TMS 1
FPGA_JTAG_TCK 3
FPGA_JTAG_TDO 5
FPGA_JTAG_TDI 7
OFF_BD_RST# 9
BOOT_OVERRIDE 11
SPI0_CLK 13
POWER 15
POWER_FAIL# 17

OFF_BD_RESET# is an Output
used to reset all peripherals

POWER_FAIL# must
not be driven high

SD Card

SD card signals on connector
are wired in parallel with
SD card socket. Only one
can be populated with SD card

Ethernet

ETH_RX+ 1
ETH_RX- 3
ETH_CT 5
ETH_TX+ 7
ETH_TX- 9
ETH_CT 11
3.3V 13

USB
Ports

DEV_USB_M 23
DEV_USB_P 25
1.0V_BU 27
HOSTA_USB_M 31
HOSTA_USB_P 33
Loop 1.0V 35
HOSTB_USB_M 37
HOSTB_USB_P 39
3.3V 41

3.3V max load is 300 mA

Maximum off-board load
on 1.8V, 1.5V and
1.0V pins is 10 mA each

SPI

SPI_CS0# 65
SPI_MOSI 67
SPI_MISO 69
SPI_CLK 71

Console

PC4_SPI_CS2# 75
PC5_SPI_CS1# 77
3.3V 79
PB23 81
PB24 83
PC9 85
PC10 87
PC13 89
PC14_IRQ2 91
DEBUG_TXD 93
DEBUG_RXD 95
DIO_15 97
PC7 99

Max. load on JTAG_Vcc
(CN2-79) is 20 mA

ETH_LEFT_LED 2
ETH_RIGHT_LED 4
RED_LED# 6
GREEN_LED# 8
SHUT_DOWN 10
WAKE_UP 12
PC6 14
PC0 16
PC1 18
PC2 20
PC3_SPI_CS3# 22
AN_VREF 24
PA22 26
TW_CLK 28
TW_DAT 30
PA6 32
NAND_WP# 34
PB16 36
PB17 38
PB18 40
PB19 42
CPU_JTAG_TMS 44
CPU_JTAG_TCK 46
CPU_JTAG_TDI 48
CPU_JTAG_TDO 50

A/D

I2C

I2S

CPU
JTAG

UART0

UART1

UART2

UART3

UART4

UART5

These DIO have 1.8V levels

PC4, PC5, PC6

PC7, PC8, PC9

PC10, PC13, PC14

All other DIO uses 3.3V levels

Boot Strap

Mode 2	Boots from
1	NAND Flash
0	SD Card

BUS_DIR = MODE2

MODE1 and MODE2 states
are latched prior to
OFF_BD_RESET# deasserted

MODE1 and MODE2
have PU resistors

Use 1.5K ohm resistor
to "OFF_BD_RESET#"
to set Mode pins "low"

Devices connected to this bus must never
drive it when BUS_CS# is deasserted
(must be off within 30 nS of deassertion)

Devices must pull the BUS_WAIT# line low
if they need more than 150 nS strobe

The data bus can not have more than
30 pF of off-board capacitive loading
May need data buffer chip for heavy loads

If Bus is not needed, the following
can be changed to DIO:

- Bus Control signals
- MUX_AD08 thru 15

Bus cycles use 11 address lines
AD0 thru AD10

This provides 1K address space
for 8-bit bus cycles (000-3FF)
and 1K for 16-bit cycles (400-7FF)

BUS_ALE# = Address Latch Enable

BUS_BHE# = Byte High Enable (for 16-bit cycles)

Technologic Systems

Date Oct. 19, 2011

Title: TS-4200 Off-board Connectors

Rev: D

Designer

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