TS-8550

Rev.A to Rev.B Changes

Relayout of 5V Regulator

Added res for SD Boot

Power Sw also switches 5V Input Power

Added PU resistor to CN1 pin 54

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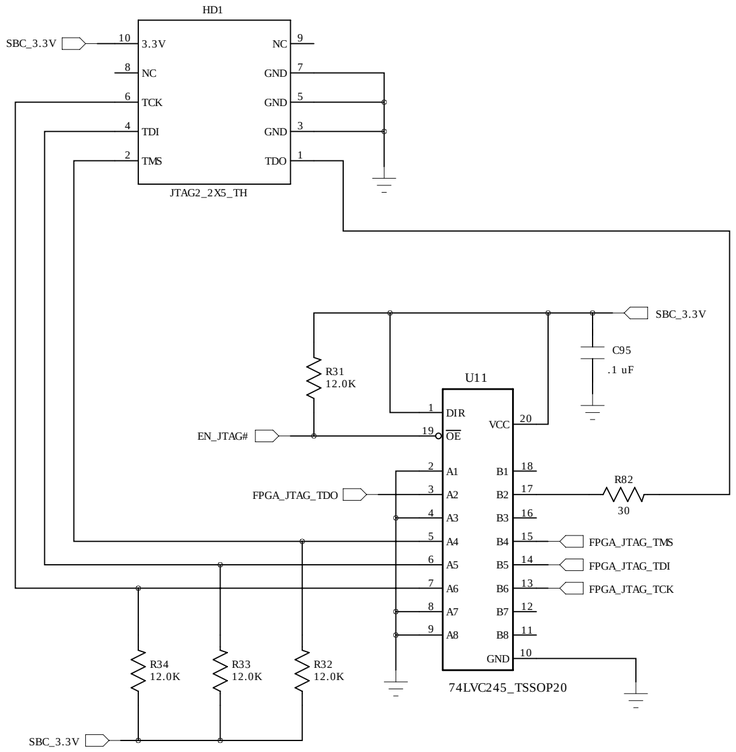
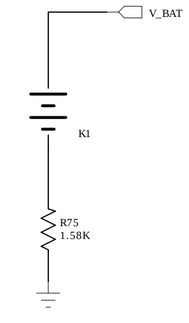
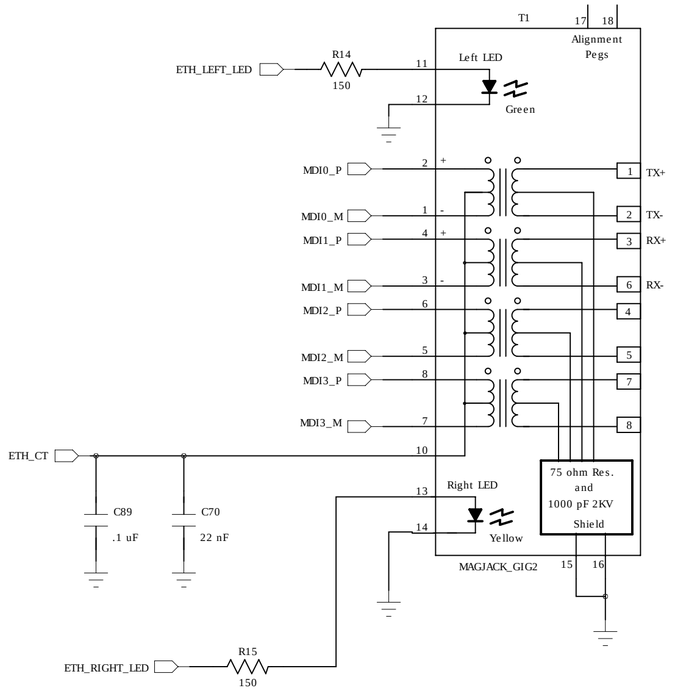
FPGA JTAG Header



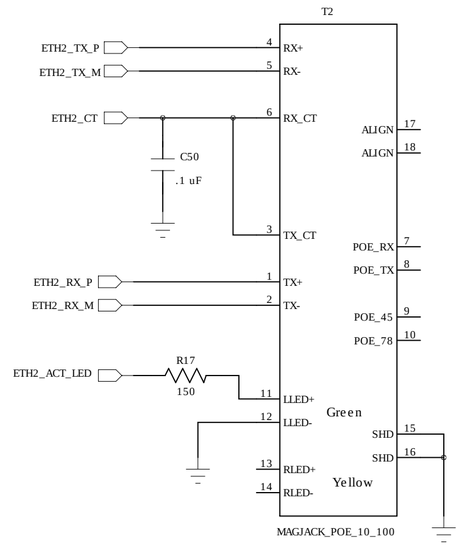
RTC Battery



Gig MagJack



10/100 MagJack



Swapped RX and TX Pairs

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Title: TS-8550 MagJacks, JTAG, Battery		
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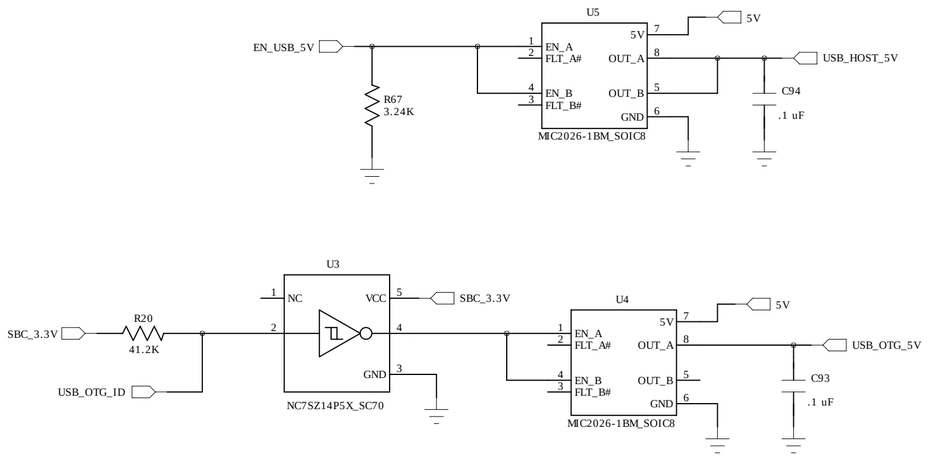
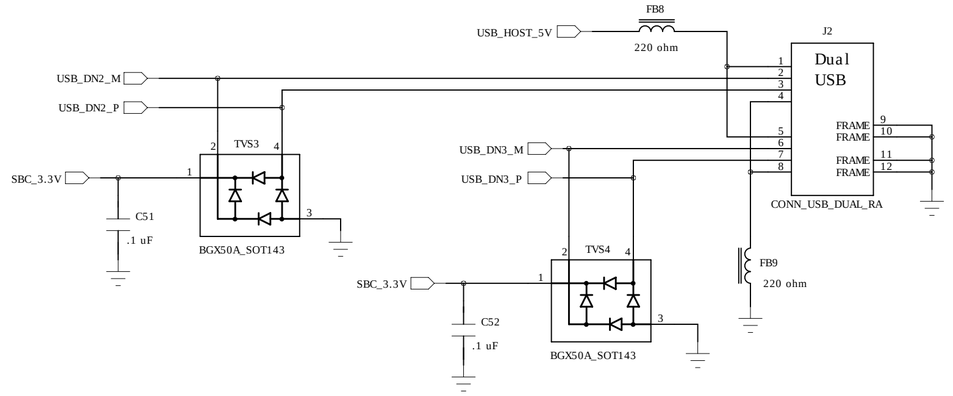
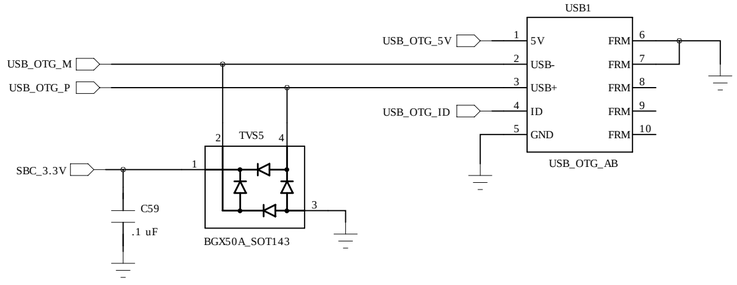
USB Power Switches



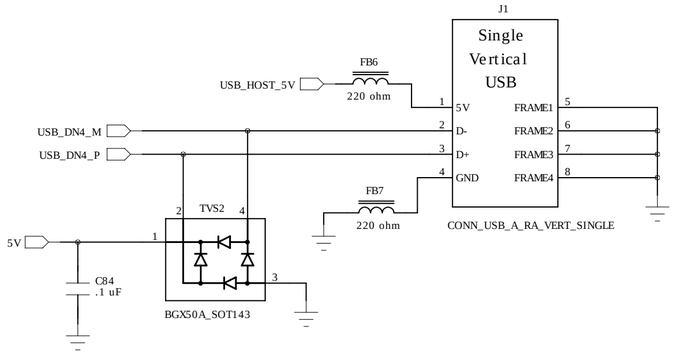
Dual Host USB



USB Micro A/B OTG Port



Host USB



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Title: TS-8550 USB Ports, USB Power		
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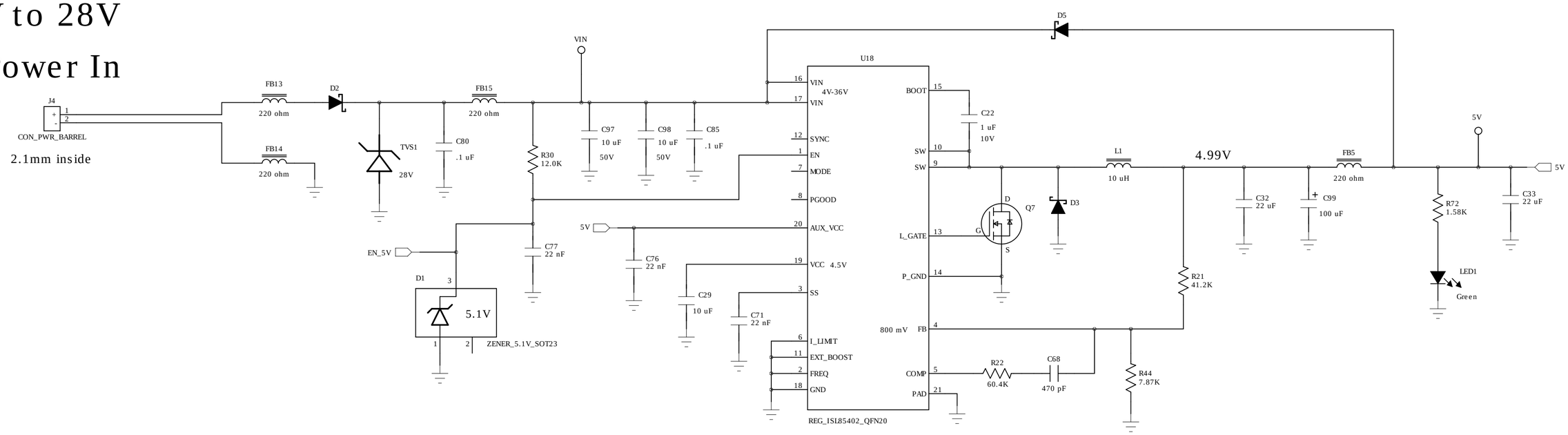
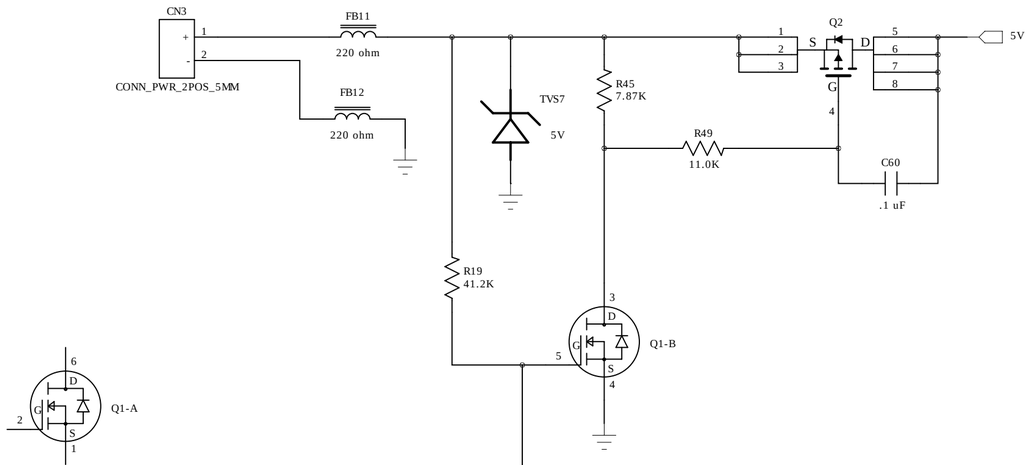
5V Power Supply (2000 mA)

8V to 28V Power In



5V Power In



5011K-ND = Black

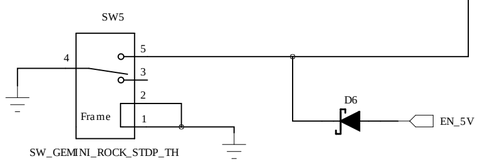
.063 hole

GND

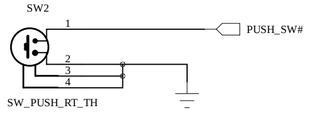
3.3V

SBC_3.3V

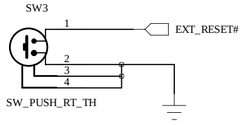
Power Switch

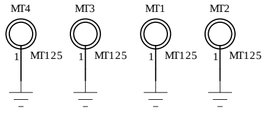


Push Switch



Reset Switch





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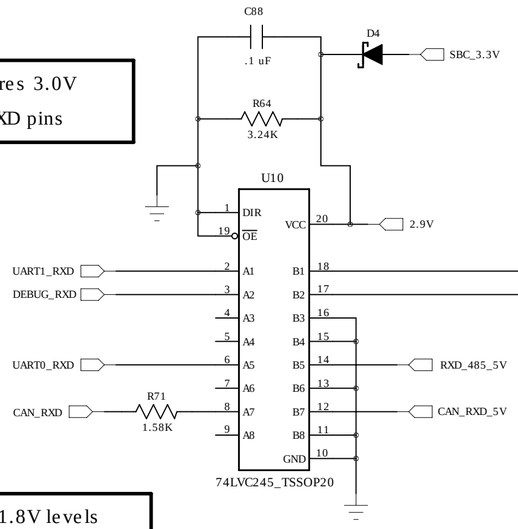
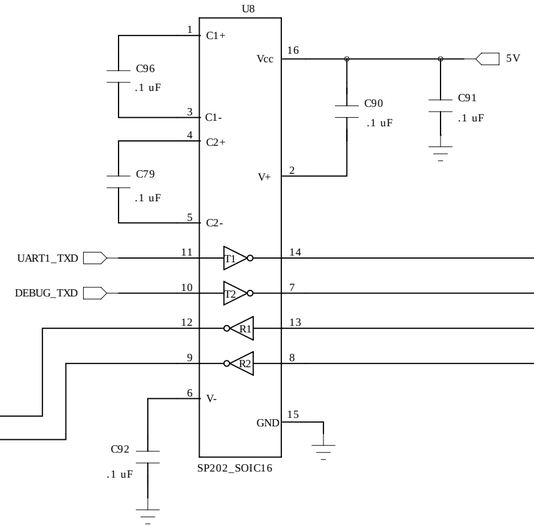
2.9V <-- 5V Level shifter

TS-4800 requires 3.0V max on the RXD pins

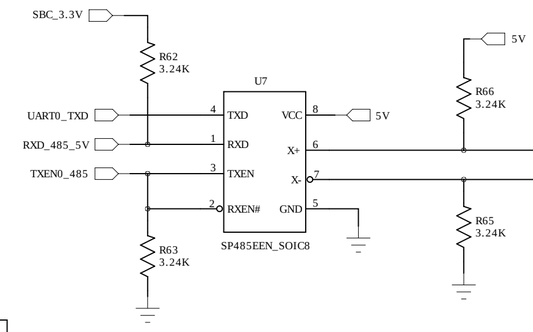


TS-4200 has 1.8V levels on the CAN RXD

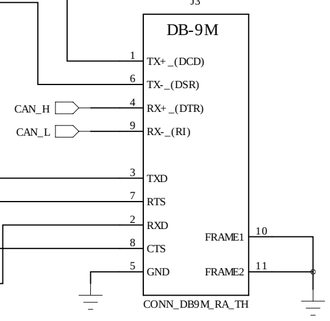
RS-232 Transceiver



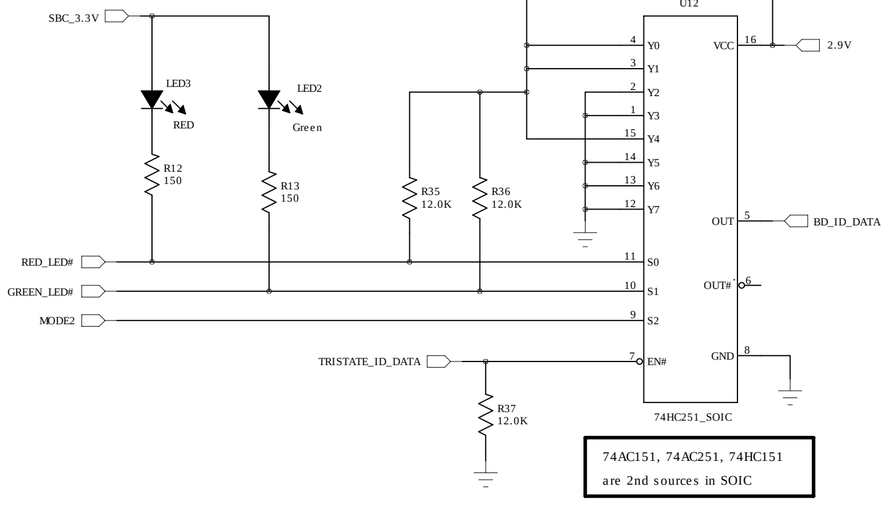
RS-485 Driver



COM DB9M



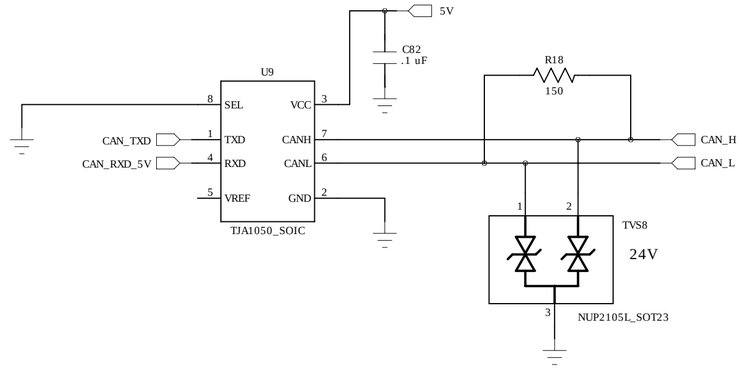
LEDs



Board ID = 19

74AC151, 74AC251, 74HC151 are 2nd sources in SOIC

CAN Tranceiver



Technologic Systems		Date Dec. 12, 2014
Title: TS-8550 COM Port, CAN, RS-485, ID		
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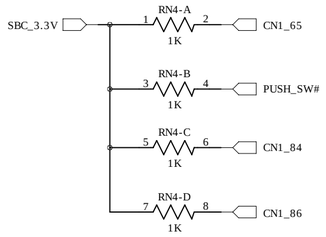
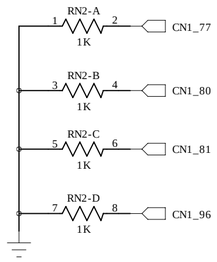
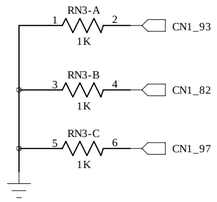
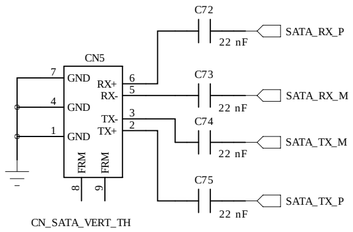
Bias Res.







SATA Port

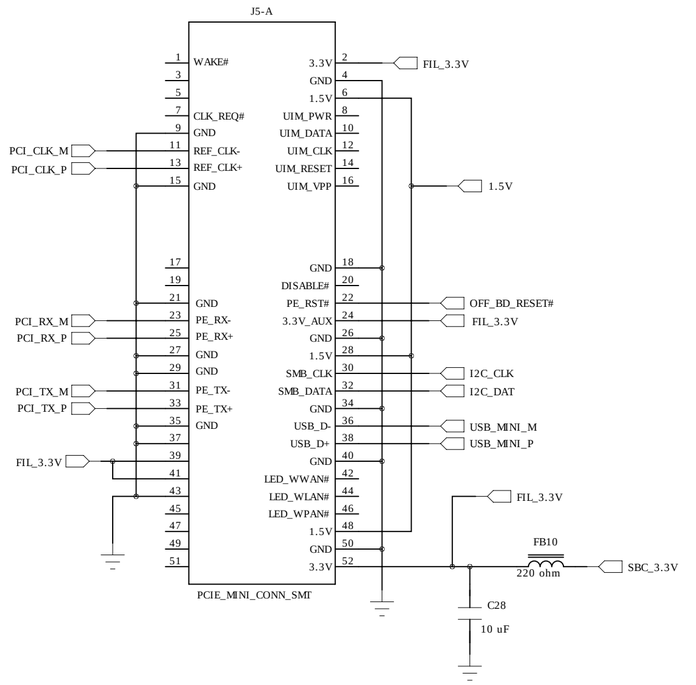


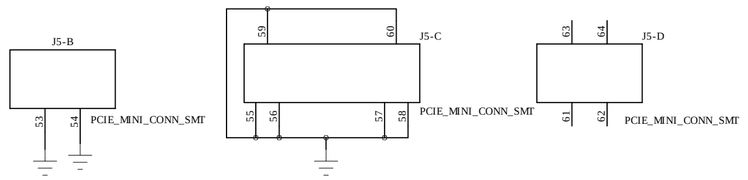
PCIe Diff Pairs can be Polarity swapped

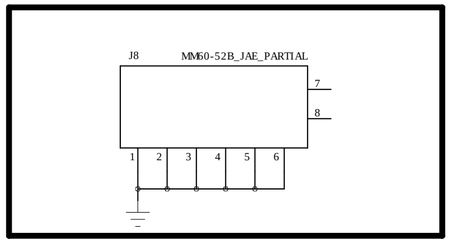
SATA can NOT have polarity swapped

SATA and PCIe Diff pairs do NOT have to be length matched

Mini PCIe Socket

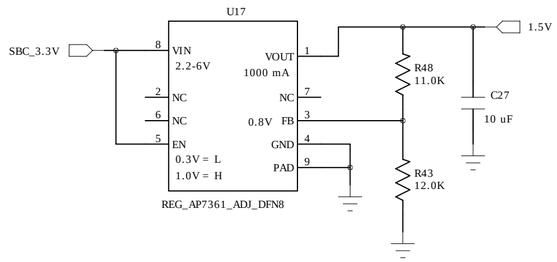




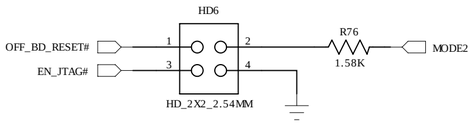


To Support Half-Size Mini-PCIe

Mini PCIe 1.5V Reg.



Jumpers



SD Boot and JTAG Enable

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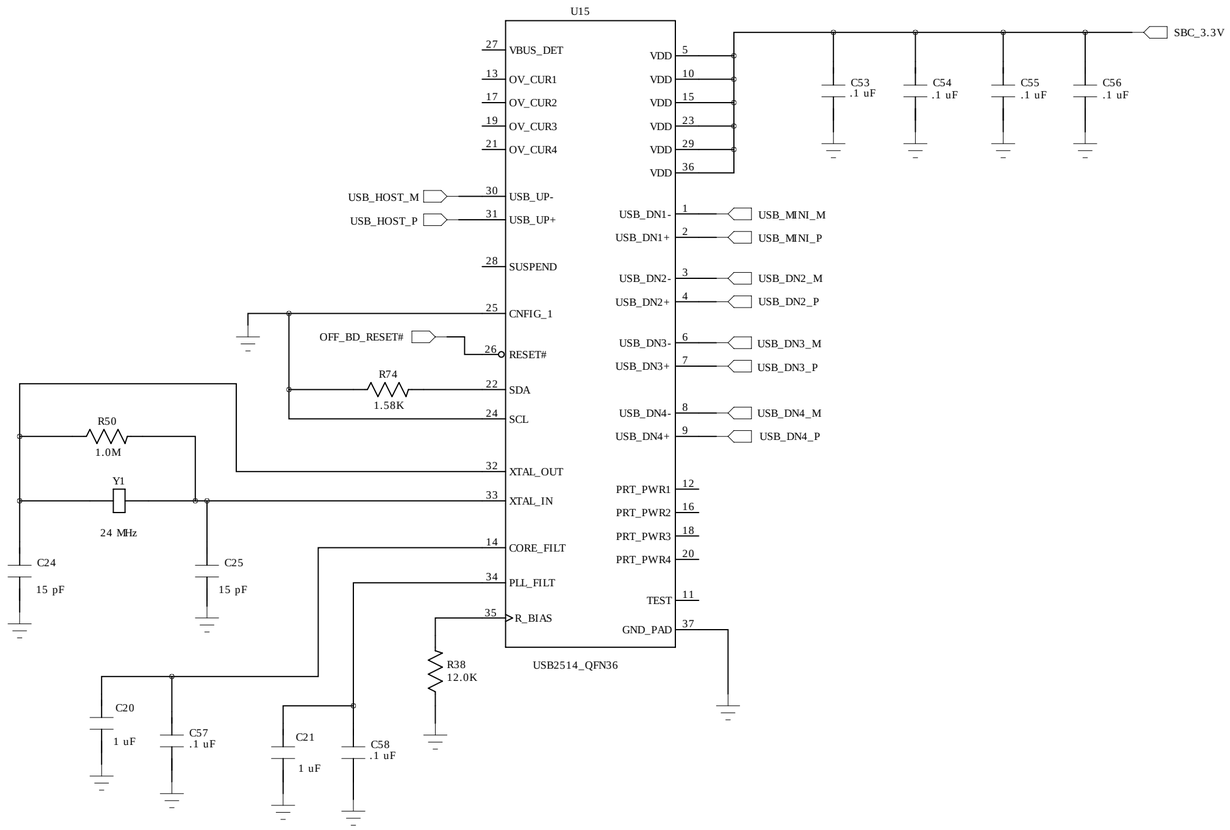
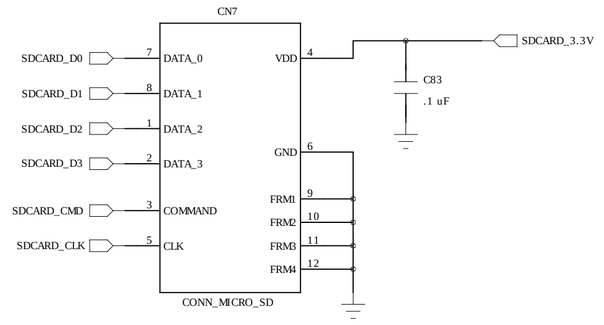
SMSC

USB Hub



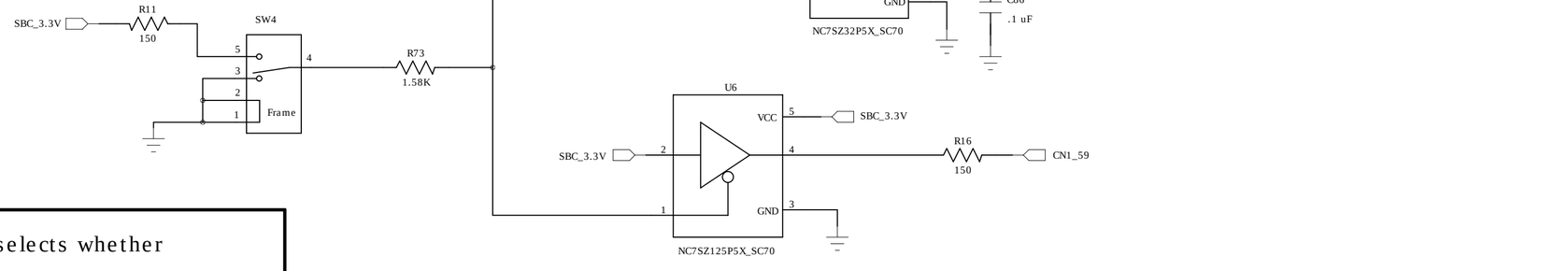
Micro SD Card Socket



TS-4900

SPI Boot Flash

Boot Select Switch



This switch selects whether the TS-4900 SPI Flash or the Base Bd. Flash is used to Boot

CN1_87 allows software to take control of which SPI Flash chip is accessed

Technologic Systems	Date Dec. 12, 2014	
Title: TS-8550 SPI Flash for 4900, USB Hub		
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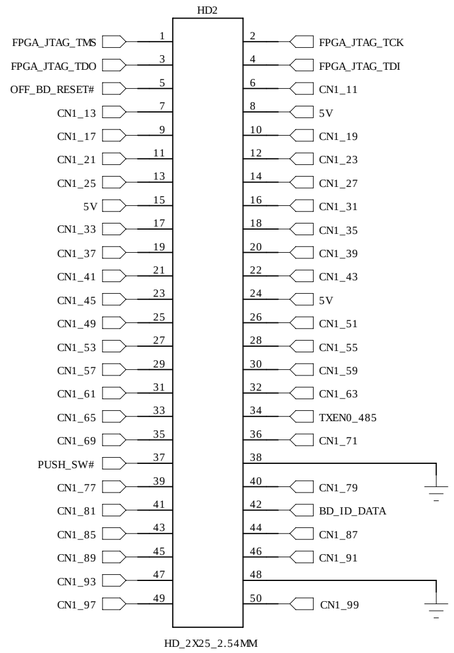
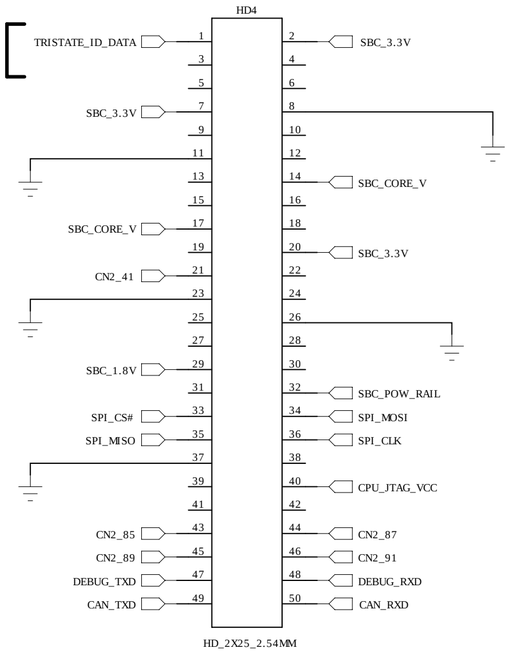
CN1 Odd Pins



CN2 Odd Pins

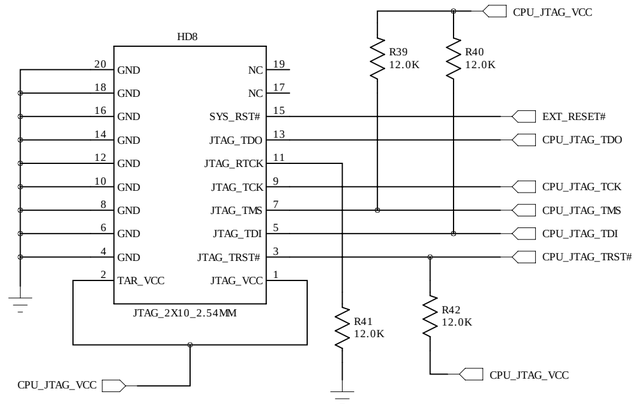
Special signals
Not on CN2



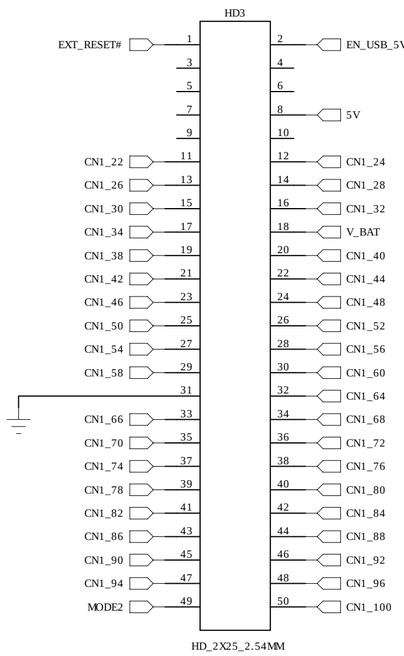
High-speed differential pairs
are not routed to these headers

USB, SATA, Ethernet, SD card,
PCIe and Ethernet pairs are not
connected because this would
mismatch the transmission lines.

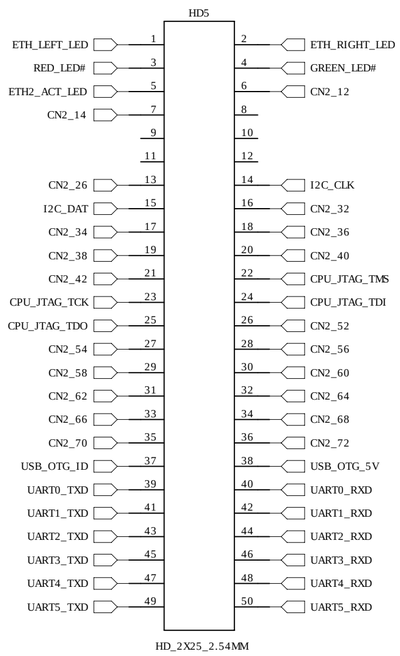
CPU JTAG



CN1 Even Pins



CN2 Even Pins



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Title: TS-8550 CPU JTAG, Headers for SBC		
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Two 100-pin Module Connectors

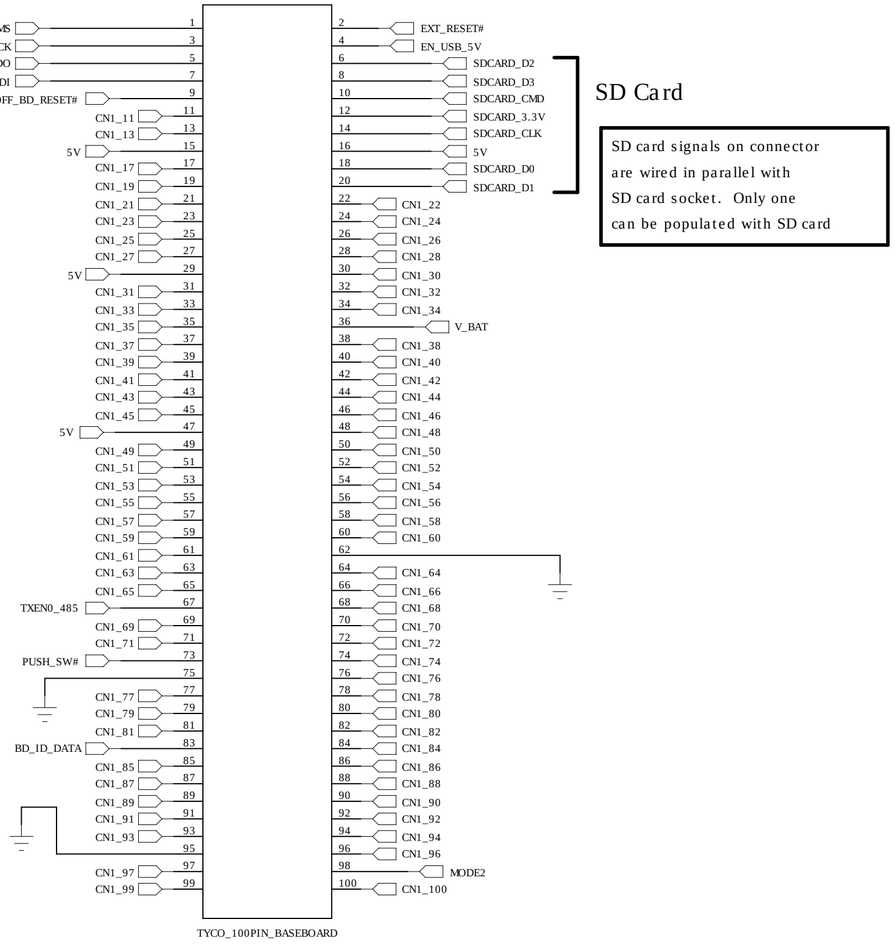
"5V" pins supply all power to the module
Apply 4.5V to 5.5V to these pins

Current drain is < 800 mA
(less than 4 Watts)

EXT_RESET# is an Input to the SBC used to reboot the CPU

Do not drive active high
(use open drain)

Left

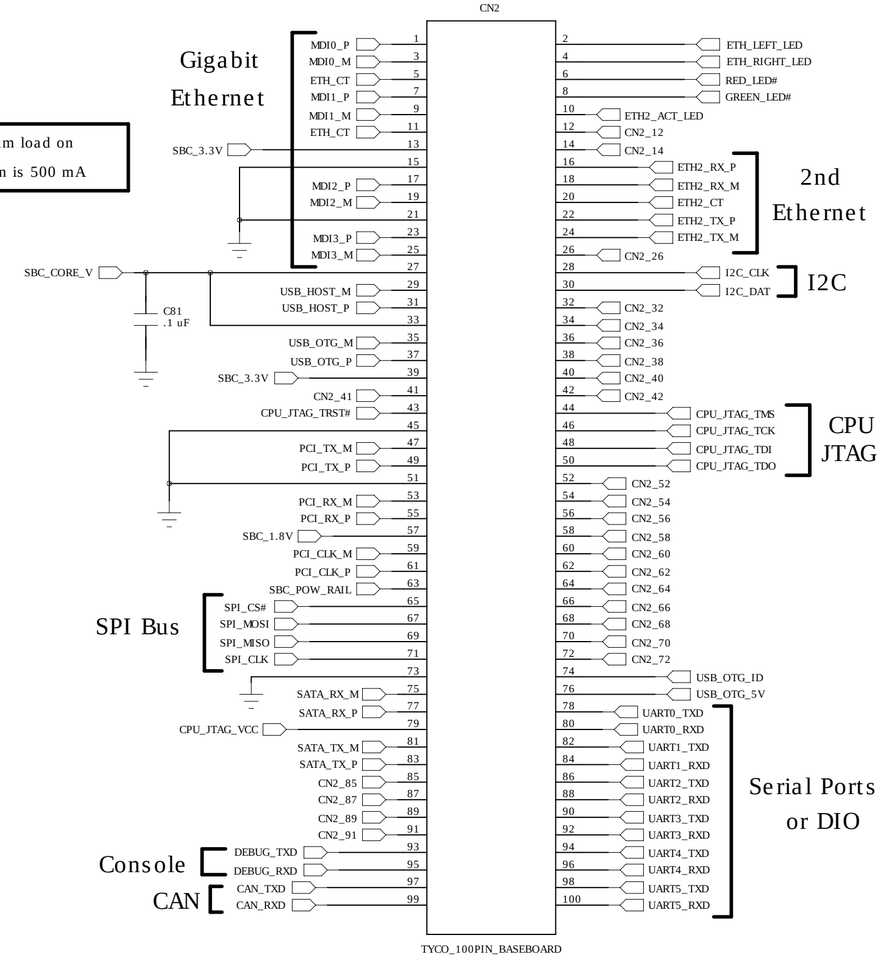


OFF_BD_RESET# is an output from the SBC

SD card signals on connector are wired in parallel with SD card socket. Only one can be populated with SD card

Right

Maximum load on 3.3V pin is 500 mA



Mode 2	Boots from
1	NAND Flash
0	SD Card

MODE2 state is latched prior to OFF_BD_RESET# deasserted

MODE2 has a 12K PU on the SBC module

Technologic Systems	Date Dec. 12, 2014	
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