Application Note AN-1123

Bootstrap Network Analysis: Focusing on the Integrated Bootstrap Functionality

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The intent of this document is to develop the bootstrap sizing theory and practice, while focusing in particular on topologies where the gate driver IC features integrated bootstrap functionality.

1. Introduction

One of the most widely used methods to supply power to the high-side drive circuitry of a gate driver IC is the bootstrap power supply. The bootstrap power supply consists of a bootstrap diode and a bootstrap capacitor; this circuit is illustrated in Figure 1.

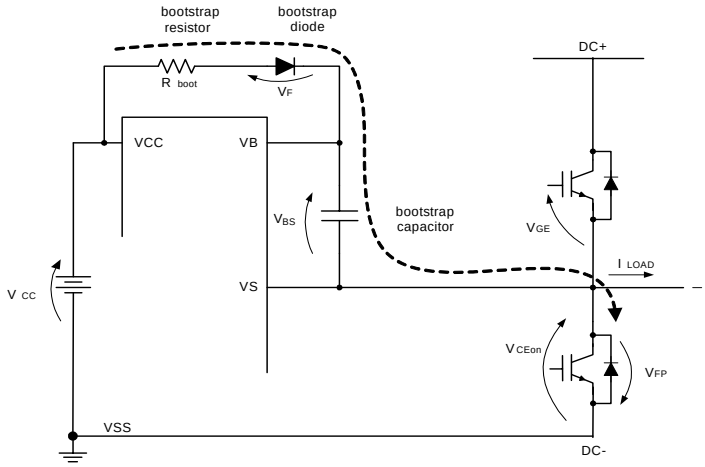

Figure 1: bootstrap power supply

This method has the advantage of being both simple and low-cost. However, the requirement to refresh the charge on the bootstrap capacitor may result in limitations on the power converter's duty-cycle and the power switch's on-time. Proper capacitor and bootstrap resistance selection can drastically reduce these limitations.

The maximum voltage that the bootstrap capacitor (V_{BS}) can reach is dependent on the elements of the bootstrap circuit shown in Fig. 1. The voltage drop across R_{BOOT}, V_F of the bootstrap diode, the drop across the low-side switch (V_{CEON} or V_{FP}, depending on the direction of current flow through the switch), and if present, the drop across a shunt resistor (not shown in Fig. 1) placed between the low-side switch's emitter and the DC- rail, all need to be considered.

The intent of this document is to develop the bootstrap sizing theory and practice, while focusing in particular on topologies where the gate driver IC features the integrated the bootstrap "diode"[1].

[1] The integrated bootstrap "diode" is described in this document in a simplified way by means of a resistor and an ideal switch in series. It may also be referenced as "bootstrap FET" as reflecting the real physical implementation in the silicon design.

2. Theoretical considerations about the bootstrap topology

Some preliminary considerations need to be understood before examining the details of sizing the bootstrap circuit that is used in the half-bridge topology. The following simplified schematic can aid to develop this understanding (see Figure 2).

This representation of the bootstrap circuit (as shown in Fig. 2) eases the computation of the V_{BS} behavior as a function of the S1 switch state, or, as a function of its duty cycle (D= *duty cycle*= $T_{ON}/T \equiv 1-D$*)[2], gate charge, leakage currents, and bootstrap resistor and capacitor.

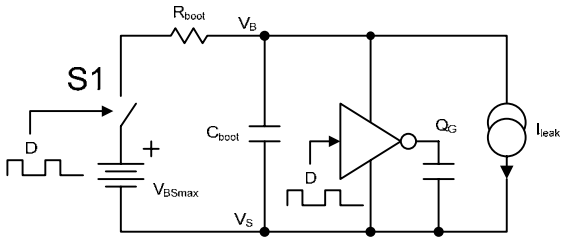

Figure 2: Simplified bootstrap schematic

V_{BSMAX}, in general, represents the supply voltage (V_{CC} in Figure 1) plus or minus the bootstrap circuit's static drops.

It is important to understand that in the discussion that follows, the duty cycle of switch S1 is assumed to have reached steady state and will remain constant. This implies that the formulas reflect results that are valid considering the duty cycle is constant in time.

Later, some important considerations will then be derived while dealing with the "AC" response of the system (i.e., as duty cycle varies in time).

"Static" equations: V_{BS} behavior in one PWM cycle:

The voltage (V_{BS}) that develops across the bootstrap capacitor (C_{BOOT}) is, in general, characterized by two contributions (according to Fig. 2). The first is represented by the voltage drop caused across the bootstrap resistor during the period in which the ideal switch (S1) is on (T_{ON}). The second is a superimposed ripple, characteristic of the switching nature of the system; the magnitude of the AC ripple is primarily determined by the sizing of the bootstrap capacitor and can be calculated when S1 is off (T_{OFF}). For the remainder of this discussion, V_{BSMAX} is defined as the maximum obtainable value for V_{BS}; this is represented by the V_{BSMAX} generator in Figure 2.

[2] T_{ON} is the on time of the switch, which represents the time while the gating signal of the low-side IGBT is active.

2.1 Bootstrap resistor contribution

The total charge that has to be supplied to the circuit by the supply (V_{BSMAX}) during the switching period (T_S) is shown in Eq.1.

$$Q_{TOT}^{*} = Q_G^{*} + I_{leak} \cdot T_S \quad \textbf{(EQ.1)}$$

The variable Q_G is defined as the total amount of charge needed by the gate of the power device and the gate driver level shifter, and I_{LEAK} takes into account the DC current that has to be supplied to the gate driver high side circuitry.

Considering that S1 is driven by a PWM waveform, and that charge is provided through the bootstrap resistor only during the T_{ON} time, then the average current flowing through the bootstrap resistor is as calculated in Eq.2.

$$\bar{I} = \frac{Q_G^{*} + I_{leak} \cdot T_S}{T_{on}} = \frac{Q_G^{*} \cdot f + I_{leak}}{D} \quad \textbf{(Eq. 2)}$$

$$\left(f = \frac{1}{T_S}; D = \frac{T_{ON}}{T_S} \right)$$

The average voltage drop across R_{BOOT} is then defined by the Eq. 3.

$$V_{Rboot} = \frac{Q_G^{*} \cdot f + I_{leak}}{D} \cdot R_{boot} \quad \textbf{(Eq. 3)}$$

2.2 Bootstrap capacitor contribution

The total charge supplied by the bootstrap capacitor to the high-side circuitry can be calculated by Eq. 4.

$$Q_{TOT} = Q_G^{*} + I_{leak} \cdot T_{off} = Q_G^{*} + I_{leak} \cdot (1 - D) \cdot T_S \quad \textbf{(Eq. 4)}$$

The ripple amplitude for V_{BS} can be determined by considering Eq. 5.

$$\Delta V_{BS} = \frac{Q_{TOT}}{C_{boot}} \quad \textbf{(Eq. 5)}$$

The shape of V_{BS} as a function of time is represented in Figure 3, where the various contributions have been distinguished. The calculation for V_{drop} (as shown in Fig. 3) given by Eq. 6.

$$V_{drop} = V_{Rboot} + \Delta V_{BS} / 2 \text{ [3]} \quad \textbf{(Eq. 6)}$$

The above mentioned formula is valid only when the duty cycle is low enough such that V_{Rboot} becomes greater than $\Delta V_{BS}/2$. This happens approximately when the recharge time is enough to fully charge the bootstrap capacitor (for this calculation, we will assume the capacitor is fully charged after a Δt of 4 time constants). Equation 7 shows the duty cycle's boundary condition.

$$D < \frac{4 \cdot R_{boot} \cdot C_{boot}}{T_S} . \quad \textbf{(Eq. 7)}$$

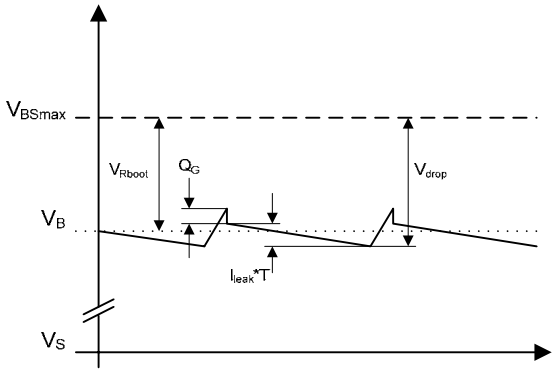

Figure 3: V_{BS} waveform

Whenever $D >> \frac{4 \cdot R_{boot} \cdot C_{boot}}{T_S}$, Eq. 6 is no longer valid and V_{drop} becomes equal to ΔV_{BS} as shown in Fig. 4.

$$V_{drop} = \Delta V_{BS} \quad \textbf{(Eq. 8)}$$

An important consideration that must be made is that while the V_{BS} ripple depends only on the bootstrap capacitor, the average voltage drop (V_{drop}) from the maximum reachable V_{BS} (V_{BSMAX}) depends only on the bootstrap resistor.

[3] V_{drop} represents the drop of V_{BS} from the maximum value that it can reach (V_{BSMAX}) considering all the elements of the bootstrap circuit, that are not mentioned in this simplified description. These elements will be described further ahead.

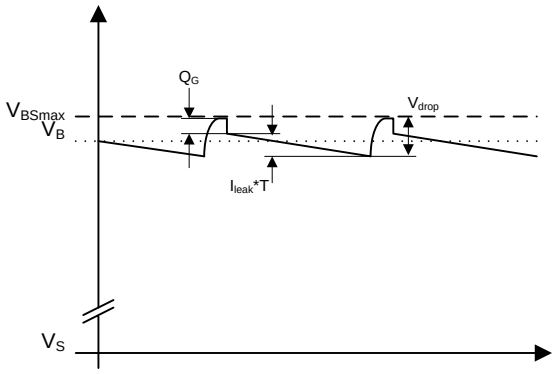

Figure 4: V_{drop} for $D >> \frac{4 \cdot R_{boot} \cdot C_{boot}}{T_S}$

It should be noted that even with a reasonably large bootstrap capacitor (to make ΔV_{BS} negligible) V_{Rboot} drop may be large. This contribution to the V_{BS} drop fixes a limit to the minimum acceptable duty cycle for a given bootstrap resistor. Equation 9 shows D_{MIN} while neglecting the ΔV_{BS} contribution and that V_{drop} is the maximum acceptable drop from the supply.

$$D_{MIN} = \frac{Q_G^* \cdot f + I_{leak}}{V_{drop}} \cdot R_{boot} \quad \textbf{(Eq. 9)}$$

Example:
Q_G^* = 40 nC, f = 20 kHz, I_{leak} = 200 µA, R_{boot} = 220 Ω, V_{drop} = 2 V ($V_{BS} = V_{CC} - V_{drop}$ = 13 V) . The minimum acceptable duty cycle will be 11%.

A simulation has been performed using the following parameters and the results are shown in Figs. 5 and 6. For this simulation, R_{boot} = 220 Ω, Q_G = 40 nC, I_{leak} = 200 µA, $f = 1/T_S$ = 20 kHz, the D_{MIN} duty cycles are either D=10% or D=30%, and C_{boot} = 47 nF or 1µF (pre-charged to V_{BSmax} = 15 V).

Below is an example of the calculation for the case where C_{boot} equals 47 nF and the duty cycle is 10%.

$$D = 10\% << \frac{4 \cdot R_{boot} \cdot C_{boot}}{T_S} = \frac{4 \cdot 220\ \Omega \cdot 1\ \mu F}{50\ \mu s} = 82.7\%$$

then

$$V_{drop} = V_{Rboot} + \Delta V_{BS} / 2$$

The expected V_{Rboot} for the worst case (D=10%) is:

$$V_{Rboot} = \frac{40\ nC \cdot 20\ kHz + 200\ \mu A}{10\%} \cdot 220\ \Omega = 2.2\ V$$

The expected ripple (C_{boot} = 47 nF) is:

$$\Delta V_{BS} = \frac{40\ nC + 200\ \mu A \cdot (1-10\%) \cdot 50\ \mu s}{47\ nF} = 1\ V$$

$$V_{drop} = V_{Rboot} + \Delta V_{BS}/2 = 2.7\ V \Rightarrow V_{BS} = 12.3\ V$$

Dynamic response:
The simulations plotted in Figure 5 and 6 are shown with C_{boot} equal to 47 nF or 1 µF and the duty cycle equal to 10% or 30%. The green and yellow curves represent V_{BS} with a 47 nF bootstrap capacitor. The purple and red curves represent V_{BS} with a 1 µF bootstrap capacitor.

Figure 6 shows the effect of the different bootstrap capacitors, which affects only the V_{BS} ripple (the average value is, in fact, kept constant).

Figure 5 shows the step response of the system starting with the bootstrap capacitor fully charged to 15 V (D=100%). In particular this picture shows that the average V_{BS} has a behavior that is similar to a single pole system with a time constant that is calculated in Eq. 10.

$$\tau = \frac{R_{boot} \cdot C_{boot}}{D} \quad \textbf{(Eq. 10)}$$

This relationship between the duty cycle and the step response of the system allows us to understand that for lower duty cycles, the time constant (τ) becomes larger (and thus the response is slower) and that for higher duty cycles, the response is faster.

This behavior works as an adaptive filter for changes in the duty cycle. This can be seen in a further simulation (see Fig. 7) in which a sinusoidal wave (40 Hz fundamental plus the 3rd harmonic) modulated duty cycle is fed to the circuit (T_S= 50 µs, electrical frequency = f_e).

In Figure 5 the parameters are R_{boot} = 220 Ω, C_{boot} = 1 µF and D = 10%.

$$\tau = \frac{220 \cdot 1\ \mu F}{0.1} = 2.2\ ms \rightarrow f_\tau = \frac{1}{2\pi\tau} = 72\ Hz$$

The combination of R_{boot} = 220 Ω, C_{boot} = 1 µF and D = 10% is also shown.

$$\tau = \frac{200 \cdot 1\ \mu F}{0.3} = 733\ \mu s \rightarrow f_\tau = \frac{1}{2\pi\tau} = 217\ Hz$$

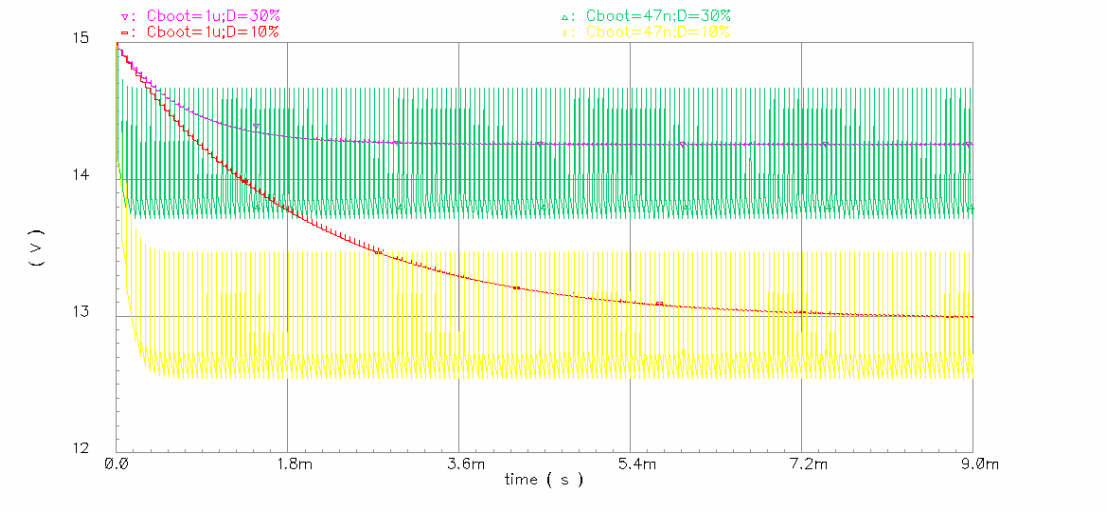

Figure 5: Bootstrap circuit parametric simulation: S1 duty cycle and bootstrap capacitor

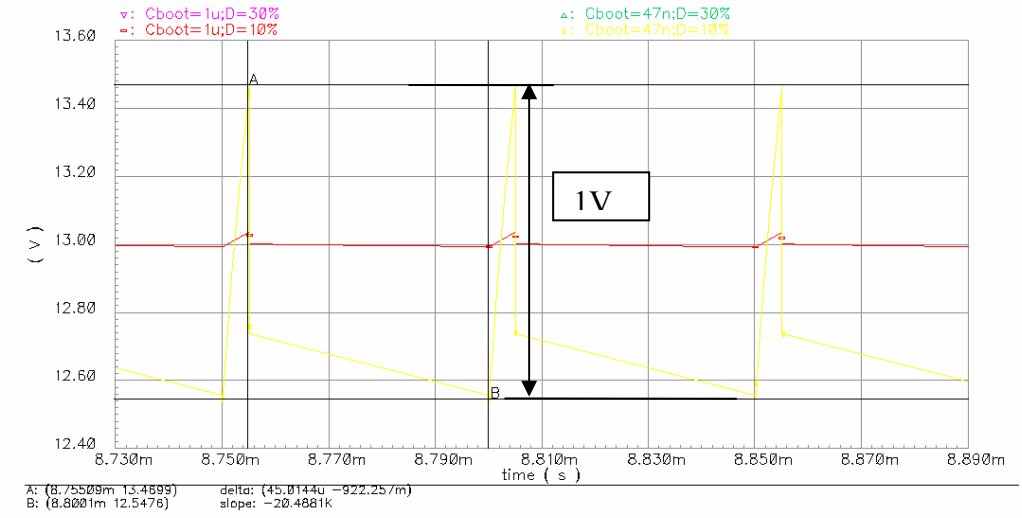

Figure 6: Ripple behavior for different C_{boot}

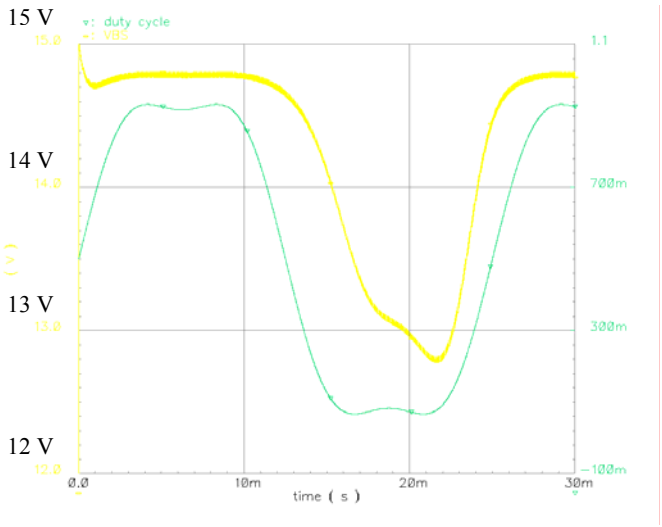

Figure 7: 40 Hz Sine plus 3rd harmonic modulation of S1 duty cycle[4]

As a drawback, $Q_{TOT} = Q_G^* + I_{leak} \cdot T_{off} = Q_G^* + I_{leak} \cdot (1-D) \cdot T_S$ increases for low duty cycles. In this case, a larger bootstrap capacitor will do the job of keeping the ripple under control and increasing the average time constant.

The dynamic response of the system is of particular interest. Fig. 8 shows the expected (calculated) V_{BS} for different electrical frequencies. The duty cycle is represented as a function (sine + 3rd harmonic) of an angle (which is equal to $2\pi f_e$, where f_e is the electrical frequency of the rotor) which swings from 0° to 360°.

In the same plot, V_{BS} voltages that are obtained with different f_e are shown. An additional note to mention regarding this figure is that the yellow curve, V_{BS} (DC), represents the curve obtained when using the static equations mentioned previously (Eqs. 3, 5, 6, & 8). The cyan curve is obtained with f_e = 40 Hz as in the simulation of Fig. 7.

3. Sizing the bootstrap circuit using the integrated bootFET

As shown in Figure 1 the bootstrap circuit includes some components that must be taken into account when sizing the bootstrap resistor and capacitor. In the case of using a gate driver with integrated bootstrap functionality (e.g., those with an integrated bootstrap FET), the external bootstrap diode is not used (for most applications) and the voltage drop across the bootstrap FET replaces the V_F typically considered during circuit

[4] Same data as per previous pages: R_{boot} = 220 Ω, Q_G = 40 nC, I_{leak} = 200 µA, $f = 1/T_S$ = 20 kHz

analysis. The other elements that must be considered include power switch (e.g., IGBT), the free wheeling diode in parallel with the switch, and any shunt resistors used on the DC- rail or in series with the low-side switch and the DC- rail.

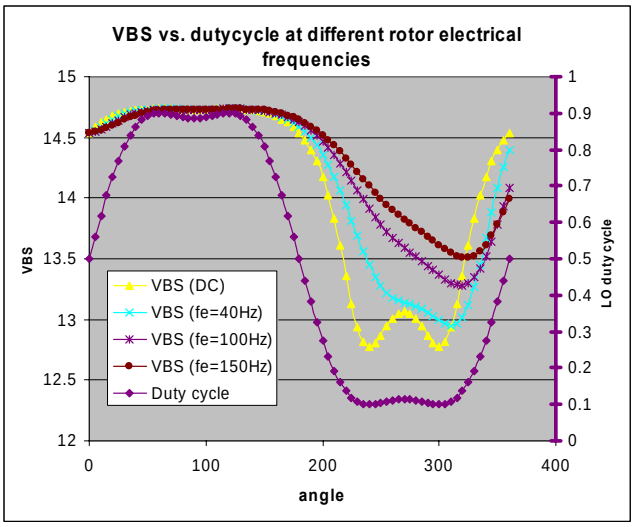

Figure 8: Expected V_{BS} drop at different rotor electrical frequencies

Following the nomenclature used in the above paragraphs, V_{BSmax} (see Figure 2 and 5) can be computed as follows:

$$V_{BS\max} = V_{CC} - V_{CE} \quad \textbf{(Eq. 11: bootstrap FET)}$$

or

$$V_{BS\max} = V_{CC} - V_F - V_{CE} \quad \textbf{(Eq. 12: bootstrap diode)}$$

Where V_{cc} is the low-side supply, V_F is the forward drop of the bootstrap diode, V_{CE} can be either the voltage drop on the IGBT (when current is flowing into the power device) or the forward biased voltage drop of the freewheeling diode (in this case, it is a negative contribution which increases V_{BSMAX}). In the worst case sizing, V_{CE} is represented by the V_{CEon} of the low-side IGBT.

The following design example will consider a system as shown in Figure 9, where the bootstrap FET is represented by an ideal switch and a resistor.

The first step in sizing the bootstrap circuit is to determine the minimum voltage drop (V_{drop}) when the high-side IGBT is on. Considering that a minimum gate voltage must be provided to the IGBT's gate (V_{GEmin}), V_{drop} is the maximum possible voltage drop of the V_{BS} supply, and is defined by the following formula:

$$V_{drop} \le V_{CC} - V_{GE\min} - V_{CEon} \quad \textbf{(Eq. 13)}$$

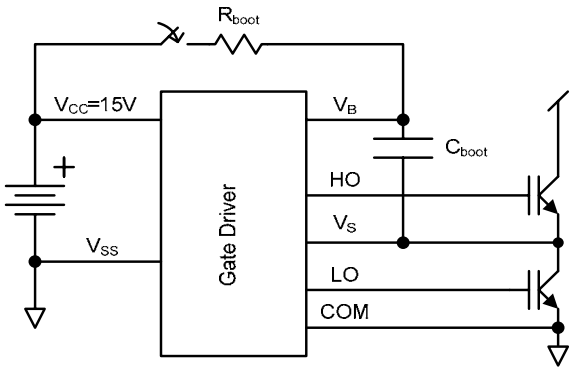

Figure 9: Bootstrap FET represented by ideal switch and R_{boot}

It should be noted that gate drivers from International Rectifier are equipped with under voltage lock-out (UVLO) protection on the high-side gate drive where the V_{BS} voltage is monitored to ensure a minimum threshold; should the V_{BS} decrease below this threshold, the UVLO protection would engage and disable the gate driver IC. Therefore, the minimum V_{GE} should be greater than the high-side supply undervoltage negative going threshold (V_{BSUV-}).

$$V_{GE\min} > V_{BSUV-}$$

The following factors that contribute to the discharge of the bootstrap capacitors voltage (V_{BS}) during the time that the low-side switch is off must also be considered.

– IGBT required gate charge during turn-on ($\boldsymbol{Q_G}$);
– IGBT gate-source leakage current ($\boldsymbol{I_{LK\_GE}}$);
– Floating section quiescent current ($\boldsymbol{I_{QBS}}$);
– Floating section leakage current ($\boldsymbol{I_{LK}}$)
– Bootstrap diode reverse bias leakage ($\boldsymbol{I_{LK\_DIODE}}$)
– Charge required by the internal level shifters ($\boldsymbol{Q_{LS}}$);
– Bootstrap capacitor leakage current ($\boldsymbol{I_{LK\_CAP}}$);
– High-side maximum on time ($\boldsymbol{(1-D_{MIN})*T_S}$ where D_{MIN} is the minimum duty cycle).

I_{LK_CAP} is only relevant when using an electrolytic capacitor and can be ignored if other types of capacitors are used. It is strongly recommend to use at least one low ESR ceramic capacitor (paralleling electrolytic and low ESR ceramic may result in an efficient solution).

The total amount of charge that is removed from the bootstrap capacitor during the time that the high-side device is referred to as Q_{TOT} (see Eq. 4) and can be calculated by Eq. 14.

$$Q_{TOT} = Q_G + Q_{LS} + (I_{LK\_GE} + I_{QBS} + I_{LK} + I_{LK\_CAP}) \cdot (1 - D_{MIN}) \cdot T_S$$
$$= Q_G^{*} + I_{leak} \cdot (1 - D_{MIN}) \cdot T_S \quad \textbf{(Eq. 14)}$$

The bootstrap capacitor can be chosen by using $C_{boot} > \frac{Q_{TOT}}{V_{drop}}$ and verifying that:

$$D_{MIN} > \frac{4 \cdot R_{boot} \cdot C_{boot}}{T_S}$$

so that $V_{drop} = \Delta V_{BS}$ (see Figure 4).

Let's suppose the above equation is not verifiable, V_{drop} may be calculated by $V_{drop} = V_{Rboot} + \Delta V_{BS}/2$. Using the formula mentioned in Eq. 3 and the known value of V_{drop}, V_{BS} can be determined by $V_{BS\,\min} = V_{CC} - V_{CEon} - V_{drop}$ while remembering the V_{GEmin} requirement.

4. Test bench measurements with no load current

To provide a better example of the integrated bootstrap circuitry's behavior/performance, a comparison of some lab examples are included. There are three comparisons shown and include:

- 10 Ω bootstrap resistor and external bootstrap diode circuit
- Integrated bootstrap circuitry
- Parallel of integrated bootstrap circuitry and external bootstrap components

Test conditions:

- PWM=20 kHz
- C_{boot}=1 µF
- Fundamental=25 Hz
- Minimum pulse = 560 ns (modulation index=97.7%)
- No load current
- Gate driver IC: IR2136 (external bootstrap topology) or IRS2136D (integrated bootstrap)

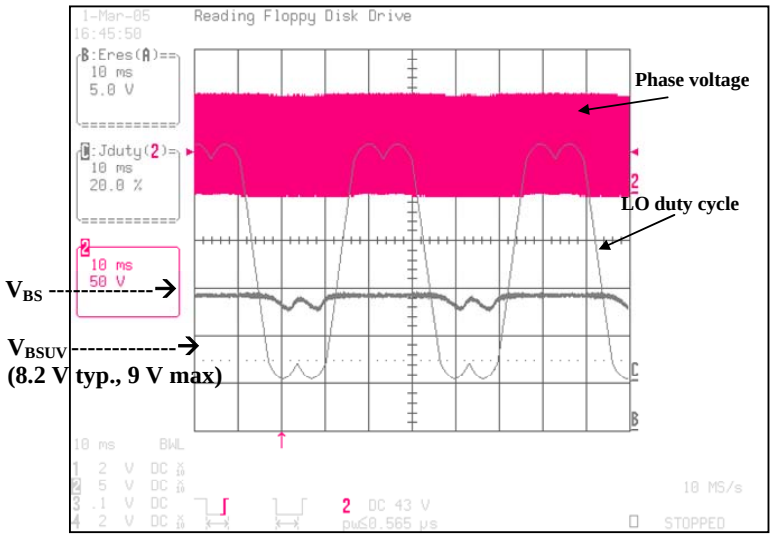

Figure 10: 10 Ω + diode external bootstrap circuit (560 ns min pulse)

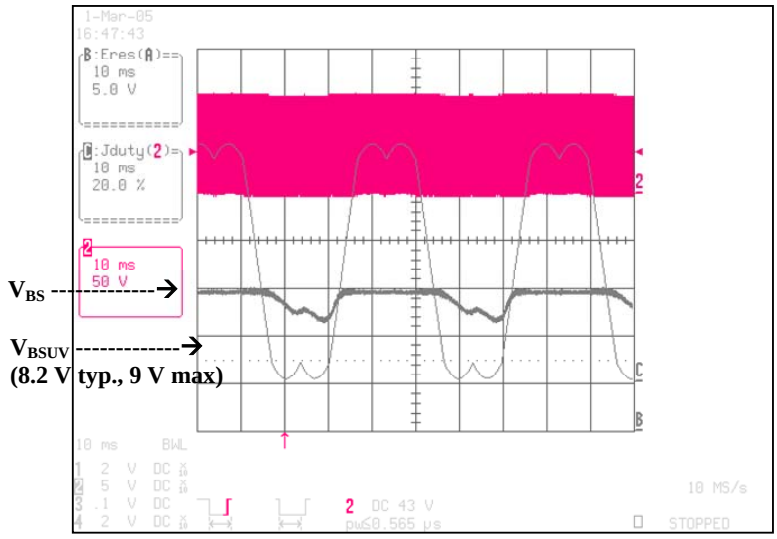

Figure 11: Integrated bootstrap circuitry (560 ns min pulse)

It is interesting to note (see Fig. 11) the integrated bootstrap network provides a filtering effect at the 25 Hz fundamental frequency. In the same picture V_{BS} can be seen to reach nearly 15 V without losing the forward drop of the bootstrap diode.

In this second example, the minimum pulse is increased to 5 µs and the modulation index decreased to 80%.

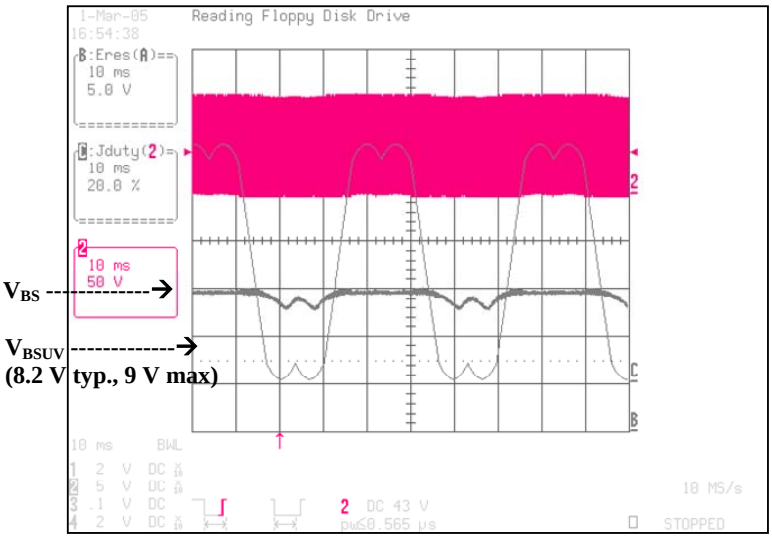

Figure 12: Integrated bootstrap circuitry in parallel with external bootstrap components (560 ns min pulse)

Test conditions:

- PWM=20 kHz
- C_{boot}=1 µF
- Fundamental=25 Hz
- Minimum pulse = 5 µs (modulation index=80%)
- No load current
- Gate driver IC: IR2136 (external bootstrap topology) or IRS2136D (integrated bootstrap)

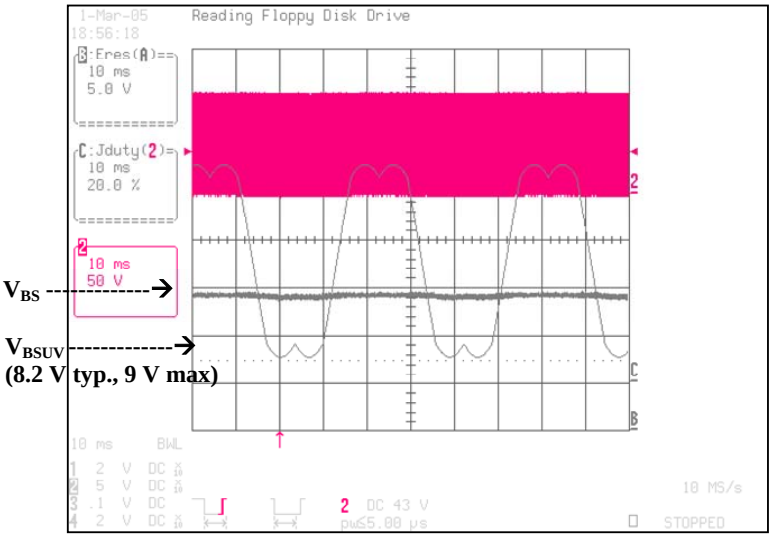

Figure 13: 10 Ω resistor + diode external bootstrap circuit (5 µs min pulse)

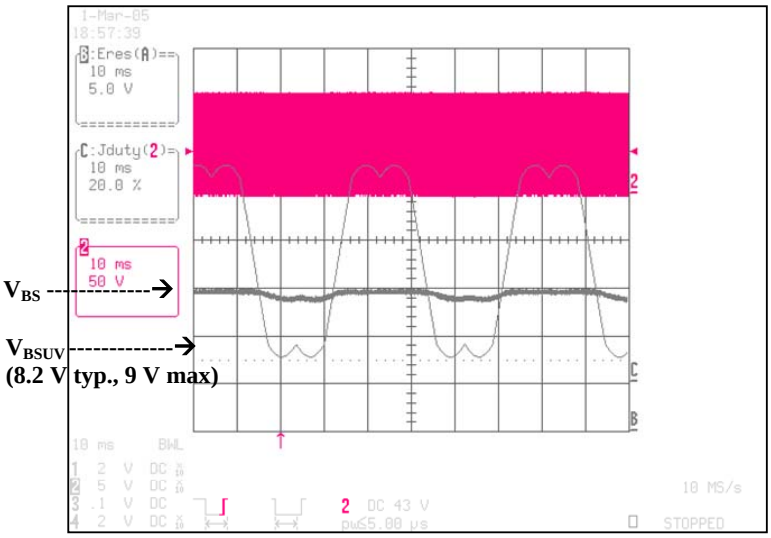

Figure 14: Integrated bootstrap circuitry (5 µs min pulse)

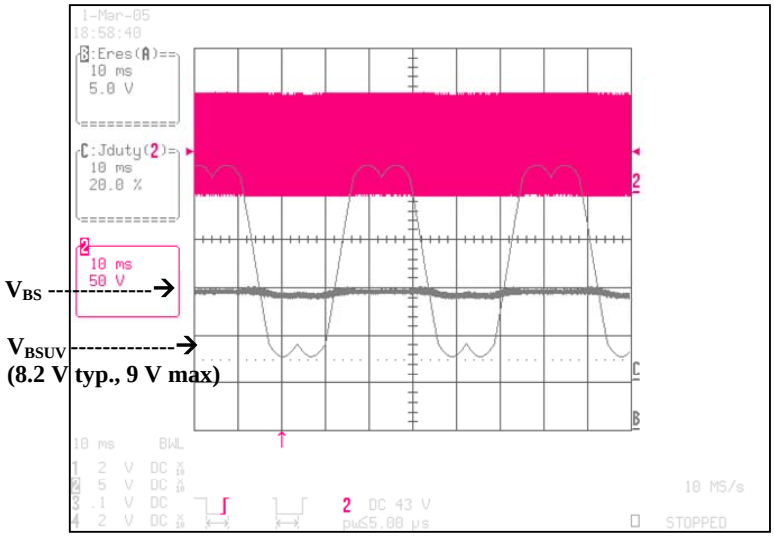

Figure 15: Integrated bootstrap circuitry in parallel with external Bootstrap components (5 µs min pulse)

With a low modulation index, the integrated bootstrap circuitry provides results as good as those obtained with the external bootstrap circuit at 25 °C.

5. Considering the bootstrap circuit for varying loads

In the examples shown above, the tests do not consider the effect of the current delivered (positive or negative) to the load. The effect of the load current influences the value of V_{BSMAX}. A description of this effect follows.

There are three different situations that can occur. The first is the case where I_{LOAD} is less than zero.

- $I_{LOAD} < 0$; the load current flows into the low-side IGBT and generates a given V_{CEon}

$$V_{BSMAX} = V_{CC}(-V_F) - V_{CEon} \quad \textbf{(Eq. 15)}$$

In this case, we find the lowest value for V_{BSMAX}. This represents the worst case for the sizing of the bootstrap capacitor. The low-side IGBT's V_{CEON} pulls up the V_S node and reduces the available voltage for charging the bootstrap supply. In the case of a circuit that uses a shunt resistor in series with the IGBT, its voltage drop may influence the result as well.

If we consider a small phase shift between the phase current and the phase voltage (a phenomenon that happens when the phase duty cycle is high and the bootstrap capacitor has more time to charge), depending on the magnitude of V_{CEON}, the induced voltage drop may be reduced.

In the second case, the load current is zero and the voltage drop across the switch can be neglected. This situation was discussed above in this document and happens during current zero crossings.

- $I_{LOAD} = 0$; the IGBT is not loaded while being on and V_{CE} can be neglected

$$V_{BSMAX} = V_{CC}(-V_F) \quad \textbf{(Eq. 16)}$$

In the third case, the load current is positive and the voltage drop across the switch is due to the drop that results from the freewheeling diode.

- $I_{LOAD} > 0$; the load current flows through the freewheeling diode

$$V_{BSMAX} = V_{CC}(-V_F) + V_{FP} \quad \textbf{(Eq. 17)}$$

In this case we have the highest value for V_{BSMAX}. I_{LOAD} flows into the free-wheeling diode, the voltage drop of which increases the available voltage for charging V_{BS}. The

same consideration can be made for $I_{LOAD} < 0$, but in this case the phenomenon happens when the duty cycle is at a minimum (which helps by increasing V_{BSMAX}).

Figure 16 shows the result of a simulation where the load current is phase shifted with the applied voltage. The plots show the duty cycle (green), simulated V_{BS} voltage (blue = 200 Ω bootstrap resistor, Cyan = 10 Ω bootstrap resistor + diode, Orange = maximum achievable V_{BS}) and the load current (red) positive entering the phase.

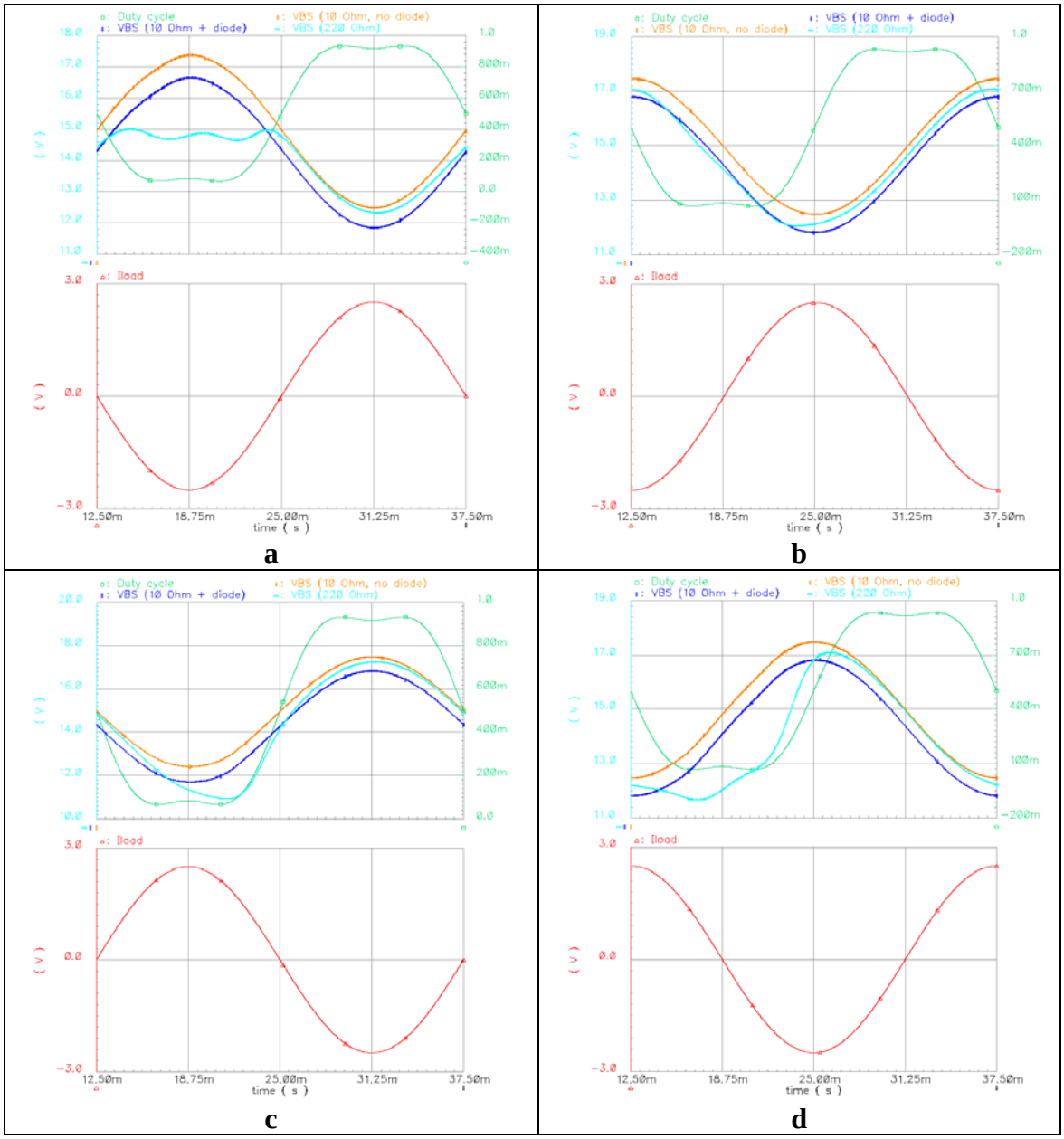

Figure 16: Simulation of V_{BS} with variable duty cycle and load current phase

The parameters for the simulation include:

I_{QBS} = 150 µA;
I_{LK} = 50 µA;
Q_{LS} = 1.2 nC;
Q_G = 40 nC;
T_S = 50 µs (*f=20 kHz*);
V_F=*1 V;*
R_{boot} =*220Ω;*
V_{CC} = 15 V;
V_{CEon} = 3 V;
V_{GEmin} = 10 V; and
D_{MIN}=10% (minimum duty cycle of the PWM carrier).

The schematic of the simulation is a modification of the circuit shown in Figure 2, to allow us to consider the effects of V_{CEON} and V_{FP} (that have been idealized as having a sinusoidal shape).

Now we'll examine a series of test measurements that help us understand the V_{BS} behavior as a function of both modulation and current phase lag with voltage. The test conditions are shown below (slightly different from previous test conditions).

- PWM=20 kHz
- C_{boot}=1 µF
- Fundamental= 11 Hz
- Minimum pulse = 367 ns (m=98.5%)
- Load current (positive toward the inverter stage)= 5 A peak-peak

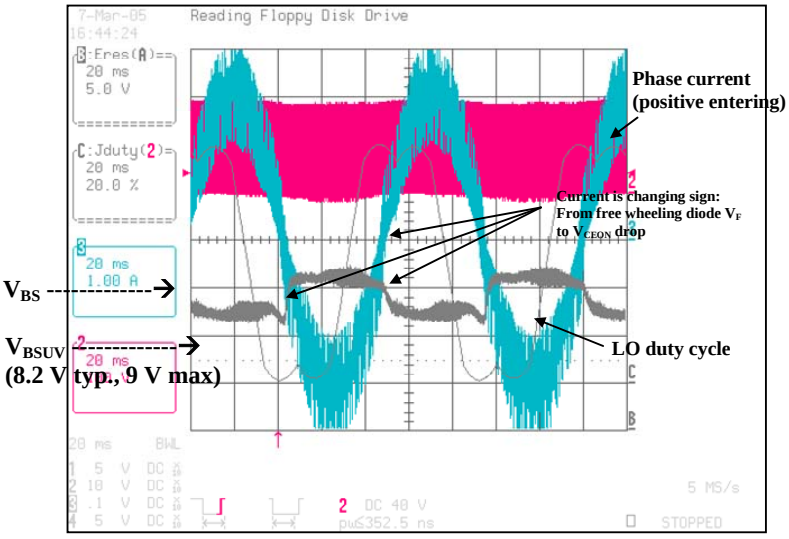

Figure 17: 10 Ω + external diode bootstrap circuit

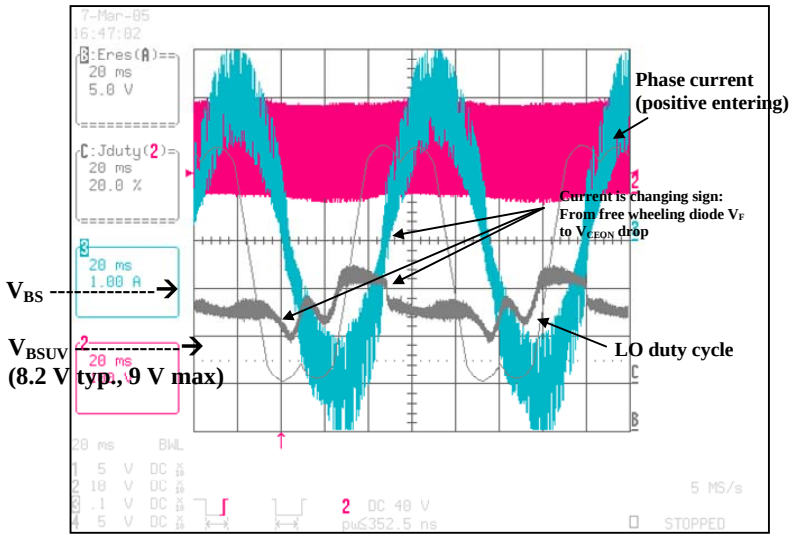

Figure 18: Integrated bootstrap circuitry

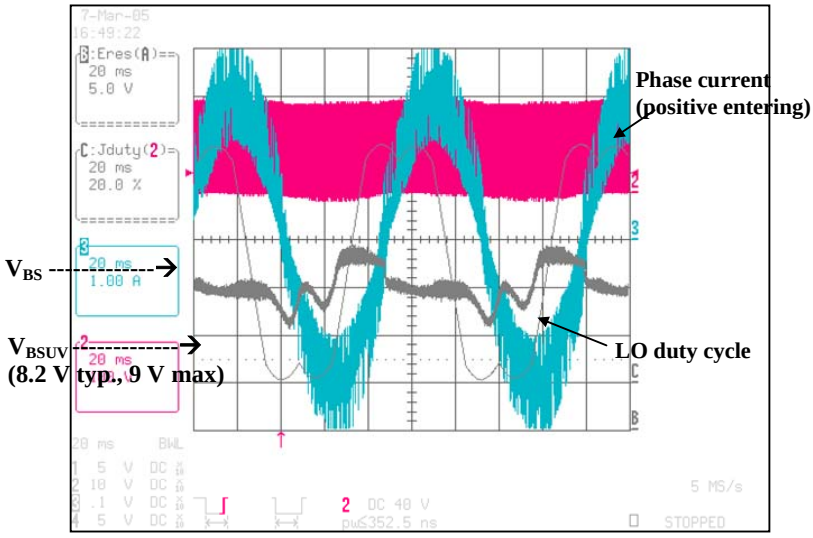

Figure 19: Integrate bootstrap circuitry with 17 V V_{CC} supply

6. Limitations of the integrated bootstrap

The integrated bootstrap FET considered above follows the assumption that the bootstrap FET is turned on only when LO is active (and the V_S pin is tied to V_{SS}). This working principle leads to a waste of the deadtime period, which can be used for recharging the bootstrap capacitor during low-side freewheeling recirculation. The topology which uses the external bootstrap diode does not suffer from this issue. In most cases, (motor drive applications usually have a max switching frequency of around 20 kHz, with deadtime periods less than 3 µs), the resulting loss of charge is negligible.

A second limitation, which is related to the integrated bootstrap is for non-complementary switching schemes.

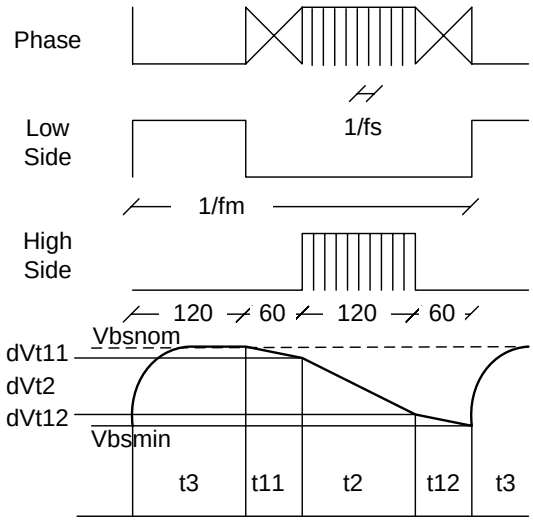

Figure 20: Behavior of V_{BS} voltage for 6-step non-complementary switching scheme

As an example, we considered the 6-step switching scheme with the high-side IGBT chopped while the low-side IGBT remains off (see Figure 20). V_{BS} charges only during the period in which low-side IGBT is on (t3) and the C_{boot} charge is never refreshed during high side switching period (t2).

A way to overcome this problem is, while chopping the high-side switch, to switch the low-side in a complementary way; this will allow a refresh of the bootstrap capacitor. In the case of complementary switching, the equations developed in section 2 apply.

International Rectifier provides also devices with a different integrated bootstrap turn-on strategy, which are suitable for non-complementary PWM schemes. This topic is not discussed in this application note.

7. Conclusions

We considered the effects of the bootstrap resistor and capacitor on the charge of the floating supply. The main issue introduced by the resistive bootstrap circuit is an average voltage drop that impacts the minimum duty cycle obtainable for the application. Examples have been shown that this effect is not preventing the use of integrated bootstrap topology for sinusoidal drive.

The equations that have been obtained are valid in general, and must be verified by the use to determine if the integrated bootstrap topology can match the design requirements.

This Application Note mainly describes applications which use the 3-phase space vector (or 3-phase sinusoidal + 3rd harmonic) modulation. Other kinds of modulations (e.g., 2-phase space vector, 6-step, etc.) have to be considered separately.

Low cost applications can benefit from the integration of the bootstrap functionality by reducing the number of external components (3 HV diodes + 1 resistor) and saving space on the board. This solution can be particularly appealing to modules that utilize a high degree of integration.