

The Designer's **HANDBOOK** for



DFM

SIERRA
CIRCUITS

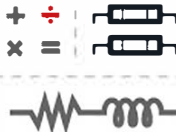
The Designer's Toolkit

Bandwidth, Rise Time
and Critical Length
Calculator



Impedance Calculator

$$\Delta W = W - W1$$



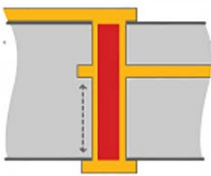
Trace Width, Current
and Temp Rise Calculator

$$W = (I_{MAX} \cdot \Delta T) \div T_h$$



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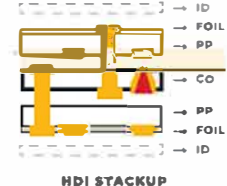
Maximum Via Stub
Length Calculator



PCB Material Selector



PCB Stackup Designer



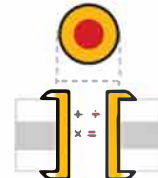
Signal Layer Estimator



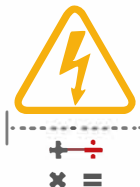
Transmission Line
Reflection Calculator



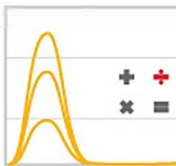
Via Current Capacity
and Temperature Rise
Calculator



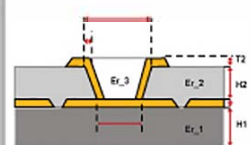
PCB Conductor Spacing
and Voltage Calculator



RLC Resonant
Frequency & Impedance
Calculator



Via Impedance
Calculator



BOM Checker



TRY TOOLS

Better DFM



THE DESIGNER'S HANDBOOK FOR DFM

Scope Of This Document

This DFM guide gives designers a better understanding of how the design (PCB fabrication data in the form of Gerber) data provided by them is transformed into physical circuits.

DFM predicts the design violation with respect to the manufacturing guidelines.

TABLE OF CONTENTS

1. OVERVIEW.....	4
1.1 What Is DFM?.....	4
1.2 Design For Manufacturability In PCBs.....	5
1.3 Why DFM?.....	6
1.4 DFM vs DRC.....	7
1.5 DFT (develop).....	9
2. THE MANDATORY FILES.....	10
2.1 DFMIPCNetlist.....	10
3. DFM CHECKS.....	13
3.1 Drill Checks.....	13
3.1.1 The Drill Technologies.....	14
3.2 Aspect Ratio.....	15
3.3 Drill-To-Copper.....	18
3.4 Nomenclature And Types Of Holes.....	20
3.5 Board complexity Vs price of the board.....	21
3.6 Drilling Disasters.....	23

4.	PCB VIA DESIGN.....	25
4.1	Types Of Vias.....	25
4.2	Microvias.....	26
4.3	Via-In-Pad.....	28
4.4	PCB Design Tips For Vias.....	31
5.	ANNULAR RING CHECKS.....	33
5.1	What Is An Annular Ring?.....	33
5.2	Construction Of An Annular Ring	35
5.3	The Cosy Annular Ring Width.....	35
5.4	Annular Ring: The Horror!.....	36
5.5	Annular Ring: The Safe Zone!.....	38
5.6	Inspection Guide.....	39
5.7	IPC Class2 Vs Class3.....	39
5.8	Design Rules For Annular Rings.....	40
5.9	PCB Through-Hole Plating Requirement.....	41
6.	SIGNAL CHECKS.....	42
6.1	Conductor Width.....	42
6.2	Spacing.....	46
6.3	Hole Registration.....	50
6.4	Missing Copper.....	51
6.5	Featured Connection.....	51
6.6	Unconnected Or Dangling Lines.....	51
7.	SOLDER MASK CHECKS.....	52
7.1	Solder Mask Clearance.....	52
7.2	Solder Mask Opening.....	55
7.3	Solder Mask Coverage or Expansion.....	57
7.4	Solder Mask Relief Or Solder Mask Web.....	59
7.5	Solder Mask Dam Or Spacing In Solder Mask.....	61
7.6	Solder Mask Slivers.....	62
7.7	Re flow Soldering.....	63

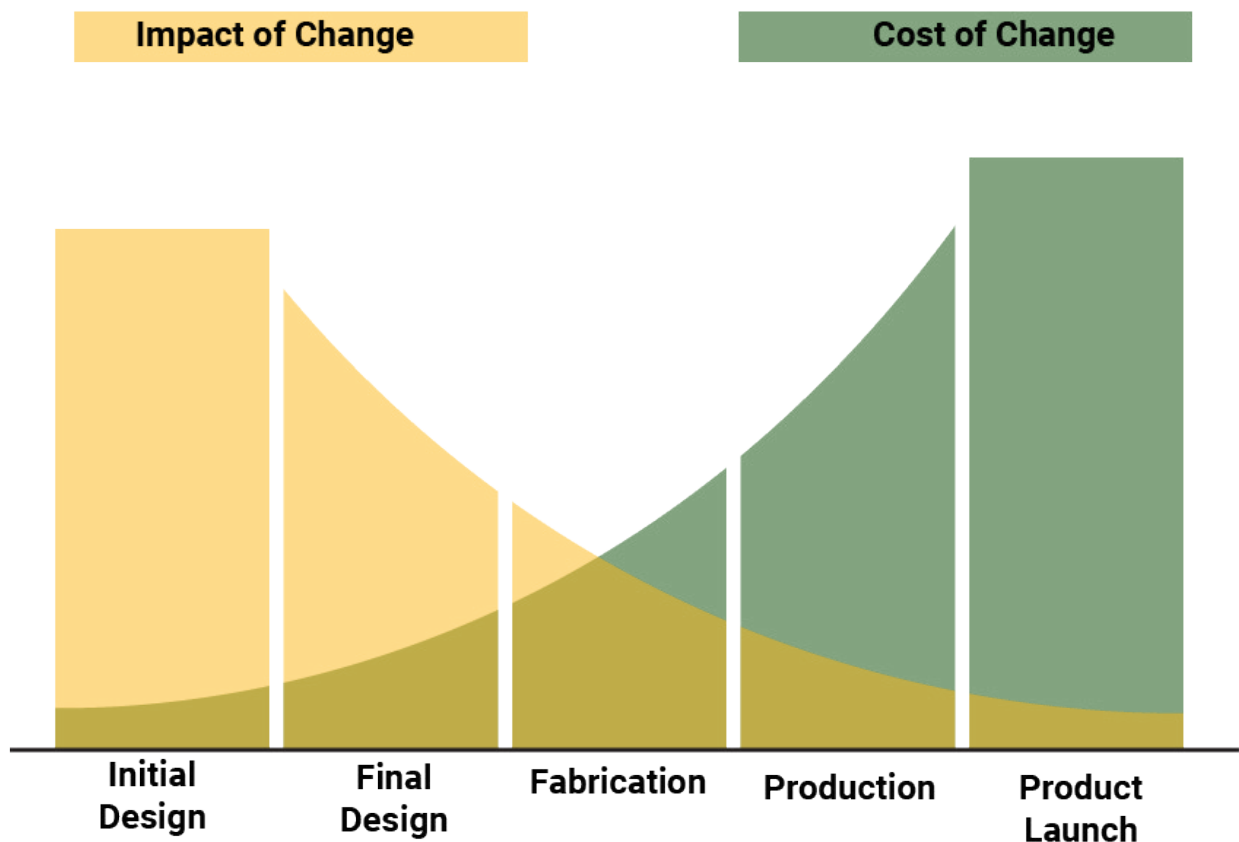
8.	SILKSCREENCHECKS.....	63
8.1	Silkscreen To Mask Spacing.....	65
8.2	Silkscreen To Copper Spacing.....	65
8.3	Silkscreen To Hole Spacing And Route Spacing.....	65
8.4	Line Width And Text Height.....	66
9.	PCB MANUFACTURING TOLERANCES.....	67
9.1	Board thickness tolerances.....	67
9.2	Copper thickness tolerances.....	68
9.2.1	Start copper thickness.....	69
9.2.2	End copper thickness.....	69
9.3	Copper trace width tolerances.....	70
9.4	Copper trace spacing tolerances.....	72
9.4.1	Trace to edge spacing.....	72
9.4.2	Trace-to-trace spacing.....	72
9.5	Drilling tolerances.....	74
9.6	Annular ring tolerance.....	75
9.7	Solder mask feature tolerances.....	76
9.8	Layer-to-layer registration tolerances.....	78
9.9	Controlled impedance tolerances.....	78
9.10	Bow and twist tolerances.....	79
10.	OUTPUTTING YOUR DATA/POLARITY.....	81
10.1	Designer Tips.....	81
11.	BETTER DFM.....	85
11.1	Operation And Design Characteristics.....	86

1 OVERVIEW

1.1 What Is DFM?

DFM is the manufacturer's opinion on the manufacturability of products. What are the loopholes and complexities of the design? How to simplify them? Is the design even manufacturable? Or can it be designed to get it done in an optimized cost? A properly-executed DFM looks like an amalgamation of all the stakeholders including designers, engineers, contract manufacturers, and material suppliers. DFM ensures that the design is optimized and does not have unnecessary cost embedded in it.

Therefore, DFM is knowing the best design to fit your electronics in terms of both cost and complexity. DFM is an abbreviation for design for manufacturability.



This image is a real time rendition of why we need DFM. The simultaneous impact and cost of a change in design as we go into the process actually defines the purpose of DFM in the PCB industry.

It is a critical manufacturing tooling design and process development step before making a new product.

Coming together of all stakeholders early in the design process is easier if you're developing a new product. But you must keep this in mind that even with an established product, challenging the original design is a necessary element of a thorough DFM. Too often, mistakes in the design are repeated by replicating a previous design. Question every aspect of your design.

If done well, DFM will assure quality, reliability and productivity through the life of the product.

1.2 Design For Manufacturability In PCBs

DFM for PCB is a set of design guidelines that attempt to ensure manufacturability. Imagine finding errors in the fabrication and assembly process in the final stage. That would be a nightmare!

But isn't that a manufacturer's thing. Why should the designer consider DFM?

You will be on your toes to submit your designs to a manufacturer and then wait at your door like waiting for that cheesy pizza that you had ordered. But it might turn out to be depressing when you find faults that could have been easily prevented. The big question: Was it your fault in the design or did the manufacturer spill some coffee during the process?

DFM is not only a manufacturer guide to a better fabrication and assembly but can also help designers. It's true that manufacturers do use DFM or sort of a checklist to look for issues and fix them. But where this tradition tends to lose its content is, very often manufacturers do not intimate designers about the changes they made. And sometimes even the changes made are not on the same page with the design and its performance or electrical requirements. What do you think will happen if the design team sends what they think is the spec for the boards off to a new production line? The results can be devastating with PCB failing in some, most or even worse all of the finished products.

PRO TIP!

DFM is more manufacturing dependent for more complex technology. It takes time but can save you in total cost.

Therefore, both designers and manufacturers use DFM. Or at least, they should. DFM analysis software can prevent many issues. This process basically compiles the PCB layout to ensure the design is suitable enough for PCB fabrication and assembly. Some manufacturers can hold tighter tolerances on drill true position and etched trace/space because of people, process and equipment.

1.3 Why DFM?

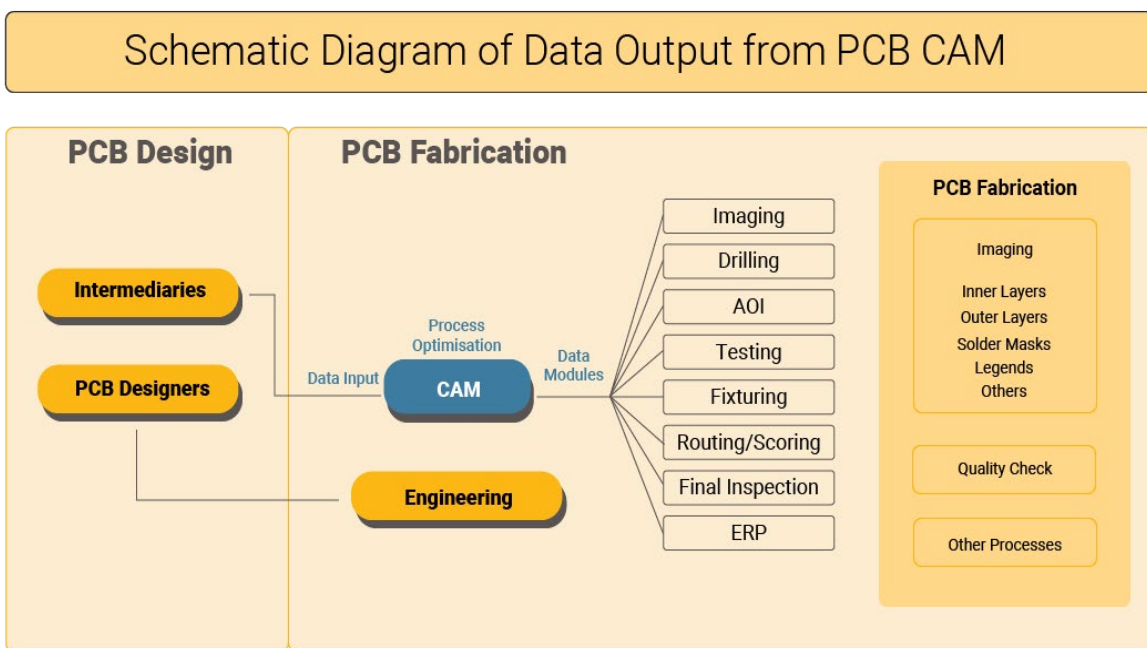
First and foremost, it will ensure that you are not daydreaming! It means that your PCB design is actually manufacturable in the real world. Because there is a difference between daydreaming about something and that thing really happening. Therefore, it tests the design in a production facility condition, instead of in an R&D lab or a computer simulation. In fabrication, it tends to be extremely challenging to accomplish designed highlights of a section or execution of a framework. In the worst outcome imaginable, PCB configuration may not be manufacturable and it needs to return to the planning phase once more.

With ensuring the manufacturability of the product, it can change the way you envisaged your circuit board. It can affect the look, feel, precision, and function of your product. DFM incorporates all designs for the bill of materials (BOM) and the final assembly, for example, form factors, tooling structure, and fabricating process structure. Just with effectively designed instruments, it is conceivable to accomplish the right look, feel, precision, and efficiency of your high-end PCB.

PRO TIP!

Save your time by building and not just simulating.

It can as well affect your timeline. Sometimes you just don't consider DFM because it's an extra thing to carry off during the product turn-out. It's true that DFM can go back and forth between the fabricator and you for a week, depending on the quality requirements and the complexity of a new product. And you feel that time is money, and rightly so in this PCB industry. Imagine going through the final stages in shipping your product to market when you come to find errors in the fabrication or assembly process. You then begin to think of everything that could have gone wrong. Was it the PCB layout? Was it the materials used? Was it in assembly or fabrication? Were the specifications given wrong? This will not only cost you money but ruin your reputation as well. Sometimes, you will risk losing your entire company! Even with all the latest technology, things may still go wrong. So, eventually, DFM will actually cut down your time, rise up your precision and make you famous!



1.4 DFM Vs. DRC

DFM stands for design for manufacturing, which is nothing but put the PCB layout topology in a way that avoids all the problems that could be encountered during the PCB fabrication and assembly processes.

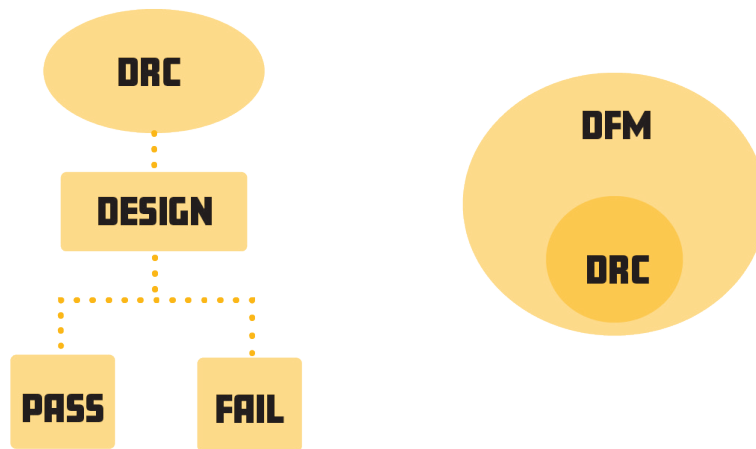
DFF stands for design for fabrication. Therefore, as the name suggests, this addresses the issues related to fabrication.

DFA stands for design for assembly. In most cases, DFF and DFA together make up DFM.

DRC (Design Rule Checking) in many cases is used for DFM, but is not sufficient. That's also acceptable to some extent because DRC issues detected in manufacturing can indeed have a direct impact on the manufacturability of a PCB. However, DRC is different from DFA. DRC checks whether a problem exists or not. Like a hard pass/fail detection of a problem in PCB. It ensures whether the PCB layout connectivity precisely matches with the schematic diagram's defined connectivity. DRCs don't include all the rules required to make a bare PCB or assembled PCB. But that is only one aspect of DRC. Most commonly, DRC includes rules that stand for defining the minimum spacing between PCB components for the entire circuit board or for individual layers. So, if we consider from the spacing aspect, DRC becomes a subset of DFM, but only if the rules checked by DRC reflects a manufacturer's requirements for spacing. If not, DRC is solely for electrical verification.

As in most cases, DFM's two primary components are DFF and DFA. They are more involved in the nuances as compared to DRC. DRC is all about detecting very specific deviations from the intended interconnect. On the other hand, DFM checks in PCB topology for potential manufacturing issues. Therefore, we can also say, a DRC defect, suppose a short, will get repeated in every copy of the PCB, irrespective of the quantity. Whereas it has been witnessed, if the same PCB quantity contains DFM issues, the manifestation of problems may be seen in some PCBs only.

For instance, a PCB layout that contains very thin pieces of copper can be correct if we go by the schematic. And it will pass DRC if there is no issue with the spacing. However, the same copper, being so thin, could form a sliver. Therefore, it could potentially detach from the PCB and form solder bridges with other components during assembly. Physically, this could happen in some PCBs and some PCBs may work as expected. So, this sort of situation can pass DRC, but in real-world manufacturing, it can cause havoc. DFM will detect such issues and save manufacturers and assemblers from scrap and rework.



1.5 DFT (develop)

DFT again is design for testability and we cannot afford to confuse it with DFM. Though both of them are an aid for designing depending upon the manufacturer's equipment and capabilities. When we substitute our operational design with elements and test points, that make functional testing of the board easier, that is what we call DFT. In an easy language, adding test points to the board such that the intended

Design > DFM>Fabrication>Assembly

2 THE MANDATORY FILES

List of files to be sent for fabrication of board:

1. Gerber files
 - TOP overlay silk layer
 - TOP solder mask
 - Top paste
 - Top signal
 - All inner layers
 - BOT overlay silk layer
 - BOT solder mask
 - Assembly top
 - Assembly bot
 - Fab drawing
 - Drill drawing
 - Board outline
2. NC drill file
3. IPC 356A netlist
4. Component placement file (pick and place)
5. PDF files
 - Assembly top
 - Assembly bot
 - Fab details
 - Schematic PDF
6. ODB file

Sierra's capabilities for PCBs:

- We accept RS-274X extended Gerber format, ODB++ format and IPC-2581 format.
- If your file is not in RS-274X, send an aperture file.
- Drill files should be in ASCII format.

2.1 IPC Netlist

A netlist is a list of nets which define the conductivity interconnection scheme of a bare circuit board.

ODB++ and IPC-2581 include a netlist. Gerber 274x does not.

What is IPC netlist 356A?

The netlist file (formatted as IPC-356) is nothing more than an ASCII text file that includes instructions for the PCB CAM software such as net names, pins, and XY locations of start and end points for each net or node.

The CAD netlist is the original netlist extracted from the basic schematic captured and supplied by the designer from the CAD software database. The CAD netlist can be received in various formats, for example:

- IPC-D-356
- ODB++
- Mentor Graphics neutral file

Why should you provide the netlist?

It is important to emphasize here that netlist integrity is a critical factor in PCB production. Unlike other errors which can result in lower yields or less reliability, netlist errors will almost always result in non-functional boards. Therefore, it is essential to catch netlist errors as early as possible in the design-manufacturing cycle and correct them.

Intentional anomalies, intentional shorts, must be addressed ahead of time so that the manufacturer doesn't put the work on hold considering it to be an error. **The notes should be provided on their drawing or in a separate information file labelled with the correct part number revision of the design.**

With the Gerber and the drill data, it is recommended to provide the IPC netlist since it acts as a fail-safe during the DFM process.

Sometimes, the Gerber files exported from your PCB CAD program may contain an error that went undiscovered since there was no way to verify that the files matched your design intent. This can be averted by supplying an IPC-356 format netlist file with your fabrication data package. IPC netlist helps in spotting the errors in the preproduction state rather than being detected at the test bench.

PRO TIP!

Always review your PCB Gerber data in a Gerber viewer. And the same applies to ODB++ and IPC-2581.

How does a fabricator use the netlist?

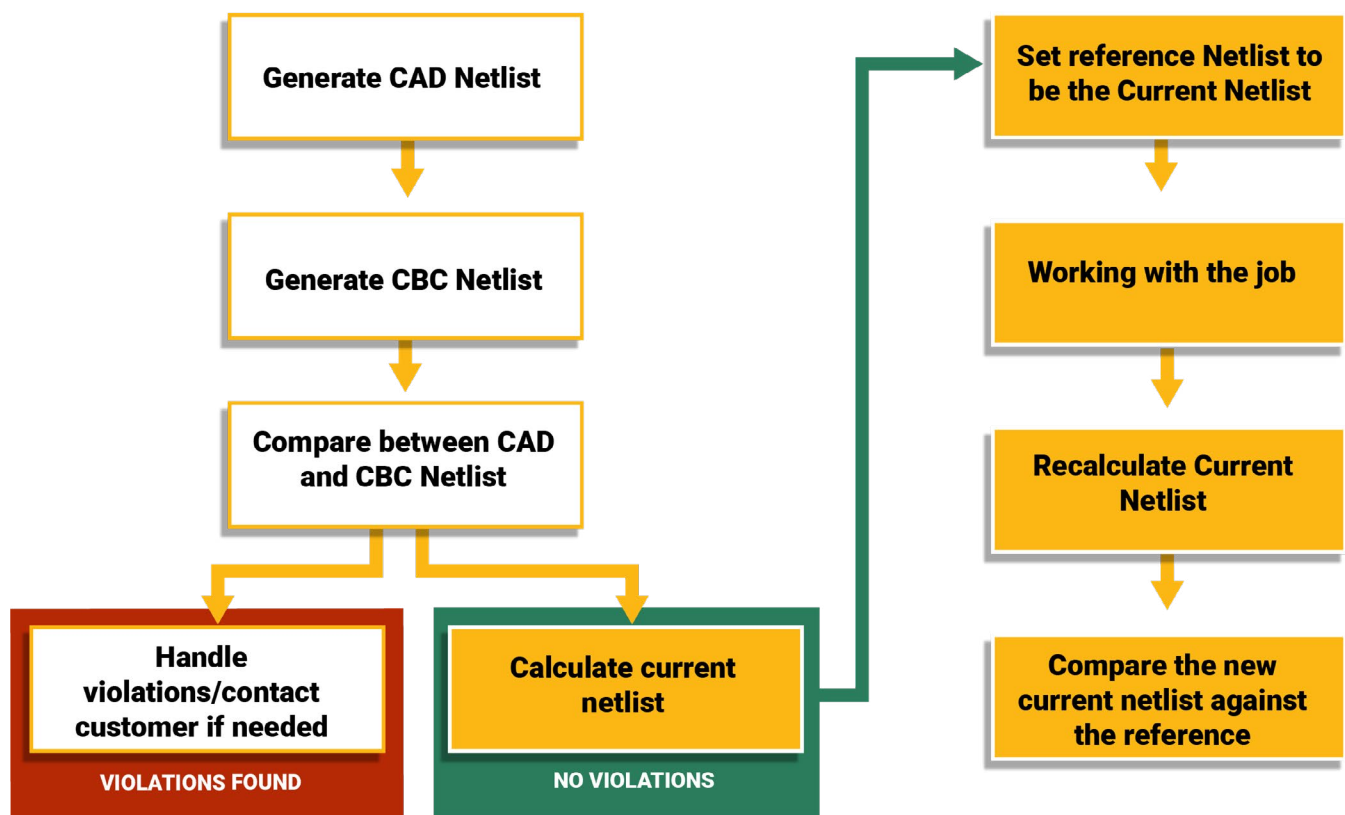
The customer-supplied CAD netlist will be compared with the netlist extracted from the customer supplied Gerber data and any violations during the comparison will be intimated to the customer.

There are two cases when the netlist should be checked:

1. When a job has a CAD netlist, we want to confirm that the netlist given by the designer is identical to the netlist according to the graphical data.

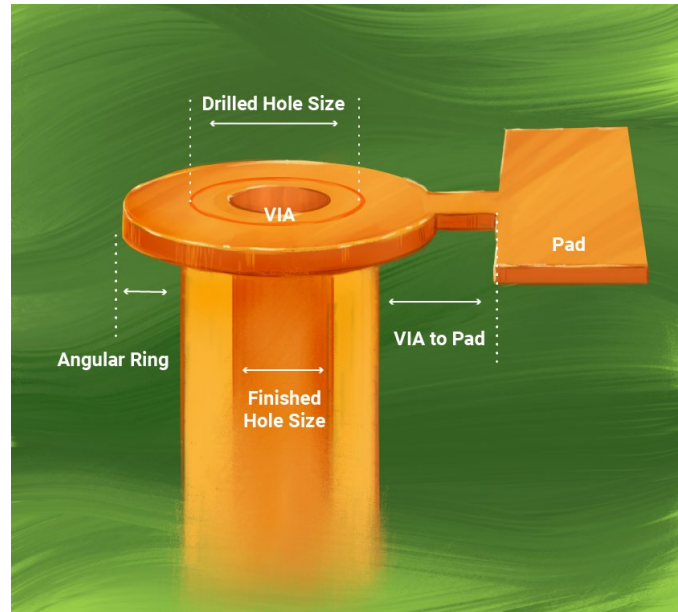
2. While editing the board and also when we finish editing, we want to make sure that our editing operations have not caused any netlist violations. This includes manual editing as well as DFM functions.

3. At the time of electrically testing the PCB, we use the customer-supplied netlist. If the manufacturer generates their own netlist for testing, there could be a designed short that cannot be caught.



Make sure the updated file is sent to the manufacturer.

3 DFM CHECKS FOR DRILLING HOLES

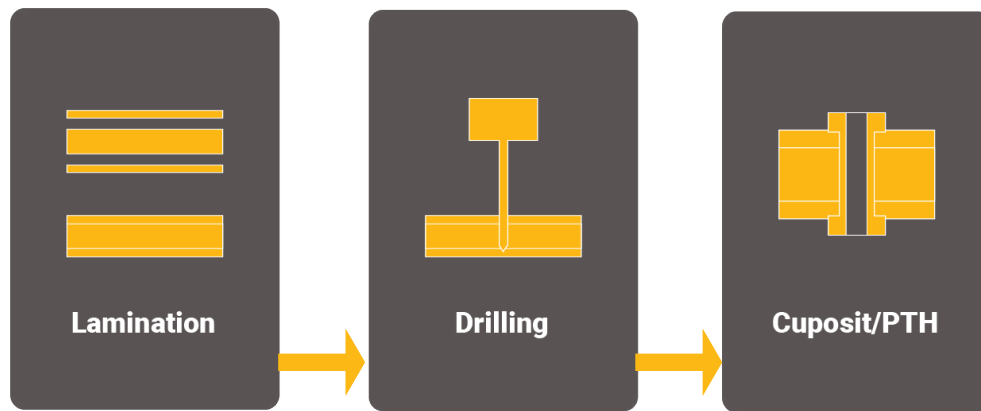


3.1 Drill Checks

The drilling process is the foundation for vias and the connectivity between different layers. If the designer understands the things that happen on the shop floor, they will have a better perception of how their design is brought to life. With this insight, the PCB designer ensures the designs are manufacturable. This, in turn, reduces the cost and the product can be delivered in a minimum turnkey time.

Drilling is the most expensive, irreversible, and time-consuming process in the PCB manufacturing process. It happens after lamination. The PCB drilling process must be carefully implemented since even a small error can lead to a great loss. The drilling process is considered the most critical to quality and is a bottleneck to the manufacturing process. Mechanical holes can only be drilled at 5,000 holes per hour. Therefore, more holes are more expensive. Closer the holes more chance drill to drill spacing is an issue.

Keep calm and drill.



PCB drilling flow chart

3.1.1 The Drill Technologies

Basically, there are two kinds of drilling technologies: mechanical and laser drilling.

The mechanical drills are used for through-holes and back drilling. This drilling technology implements drill bits. The smallest hole diameter that can be drilled by this operation is about 6 mils (0.006"). Mechanical drills need a larger annular ring because of drill wander.

The laser drills are more precise, can drill way smaller holes. Laser drilling is a non-contact process where the workpiece and the tool do not come in contact with each other. Laser drills are from one layer to the next. They are not used to drill through the whole board.

The laser technology is used to drill blind and buried vias with ease. Here, a minimum hole diameter of 4 mils (0.004") can be lasered with precision.

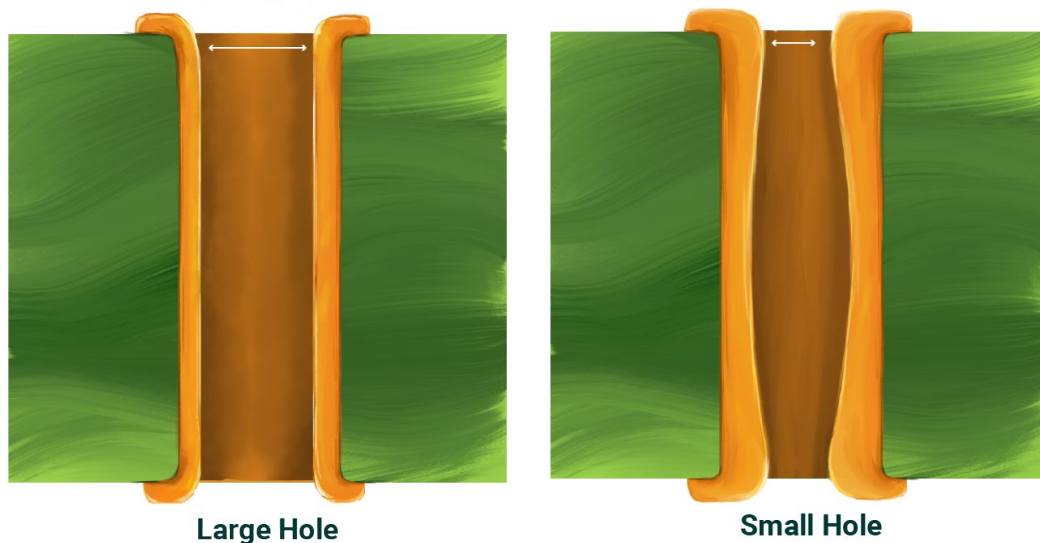
At Sierra circuits, the superior Hitachi drilling machines are implemented with a 1-mil hole placement tolerance. This is called drill true position. This is done with vision drill systems which allow designers to design with less than 3-mil annular rings for certain layer counts.

Unlike the etching and plating process, the drilling process doesn't have a fixed duration. The drill time varies on the shop floor depending on the number of holes to be drilled. This is what happens behind the curtains in a PCB manufacturing unit.

Two significant aspects to be considered in the drilling process:

- The aspect ratio
- The drill-to-copper clearance (drill to the nearest copper feature)

3.2 Aspect Ratio



Aspect ratio (AR) is the parameter that decides the reliability of a PCB.

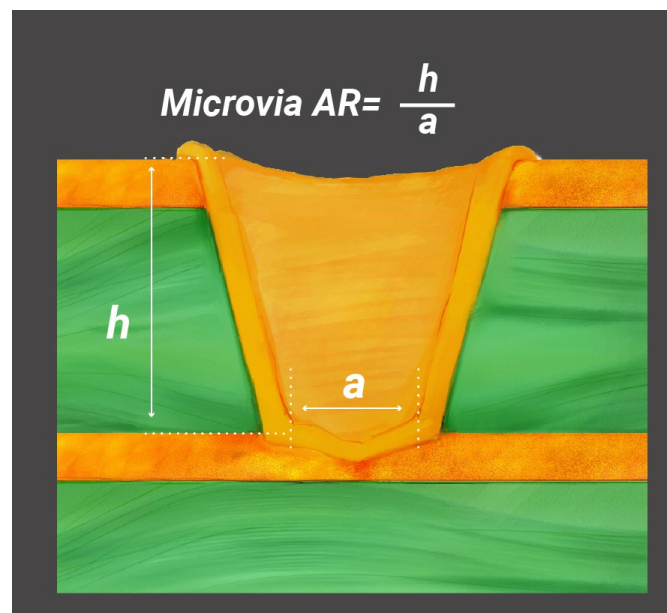
For a through-hole, aspect ratio is the ratio between the PCB thickness and the diameter of the drilled hole. While considering micro vias, it's the ratio between the depth of the hole to the diameter of the drilled hole.

Aspect ratio determines the ability to effectively deposit copper inside the holes(vias). The copper plating of the interior part of the holes becomes a tedious task when the diameter is decreased and the depth of the hole is increased. This requires a copper plating bath with a higher throwing power so that the liquid could gush into the tiny holes to deposit copper.

Aspect ratio (Through-Hole) = (Thickness of the PCB) / (Diameter of the drilled hole)

Since microvias don't protrude through the entire board, the aspect ratio will be:

Aspect ratio (Microvias) = (Drill Depth) / (Diameter of the drilled hole)



The ideal aspect ratio is 10:1 for through-holes and 0.75:1 for microvias.

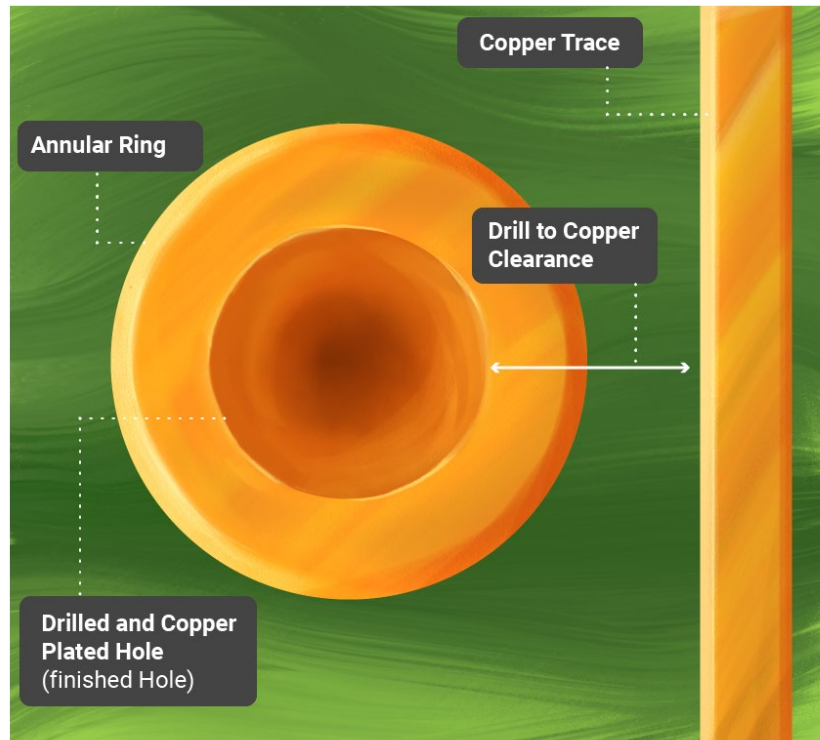
The drilled holes that are smaller compared to the board thickness can result in non-uniform or unsatisfactory copper plating.

The larger the aspect ratio, the more challenging it becomes to achieve a reliable copper plating inside the vias. Hence, smaller the aspect ratio, higher the PCB reliability.

At Sierra Circuits, we offer an aspect ratio of 0.75:1 for microvias. Aspect ratio reference table:

Microvia Hole Diameter (mils)	Maximum Dielectric Layer Thickness (mils for Aspect Ratios AR))			
	AR=0.5	AR=0.75	AR=0.9	AR=1
6.00	3.00	4.50	5.40	6.00
5.00	2.50	3.75	4.50	5.00
4.00	2.00	3.00	3.60	4.00
3.00	1.50	2.25	2.70	3.00
2.00	1.00	1.50	1.80	2.00

3.3 Drill-To-Copper



The drill-to-copper is the land clearance between the edge of a drilled hole to the nearest copper feature. The nearest copper feature can be a copper trace, copper pour or any other active copper region.

Drill-to-copper:

It varies from PCB factory to PCB factory but everybody should be able to achieve 8 mils. There are no DRCs in PCB layout tools for drill-to-copper. But if you use adequate spacing for other DRCs then you will maintain your 8-mil clearance.

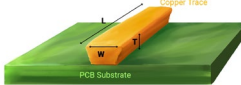
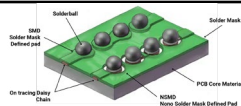
Why is drill-to-copper challenging?

It is challenging because it is impacted by separate process tolerances throughout the manufacturing process, including the glass weave and resin content in the PCB materials, PCB lamination thermal profile control, and accuracy of the drill machines drill true position.

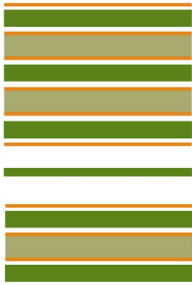
Achieving tight drill-to-coppers requires X-rays into the inner layers to get scaling information after lamination. Always check if your fabricator has that capability.

Drill-to-copper reference tables:

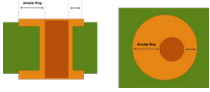
Single lamination:

Pattern	No. of Cores	12x18 panel size	18x24 panel size
	1 CORE	5.0	6.0
	2 CORE	5.5	6.5
	3 CORES	5.5	6.5
	4 CORES AND ABOVE	7.0	8.0

Sequential lamination:

For Final LAM (Blind or Burid Via) & Final Mechanical Drill Only			
Pattern		12x18 panel size	18x24 panel size
	Each core inside the individual subs shall be treated the same way as normal	1CORE = 6.0 2CORE = 6.5 3 CORE = 7.0 4 CORE & ABOVE = 8.0	8.0

Matching SUBs:

For Final LAM (Blind or Burid Via) & Final Mechanical Drill Only			
Pattern		12x18 panel size	18x24 panel size
	Each core inside the individual subs shall be treated the same way as normal	1CORE = 7.0 2CORE = 7.5 3 CORE = 8.0 4 CORE & ABOVE = 9.0	1CORE = 10.0 2CORE = 10.5 3 CORE = 11.0 4 CORE & ABOVE = 12.0

3.4 Nomenclature And Types Of Holes

The drilled holes are classified into plated holes (PTHs) and non-plated holes (NPTHs).

The plated holes (PTHs) are the signal carrying conductive vias that establish interconnection between the different layers in the PCB.

The non-plated holes (NPTHs) are non-conductive. These are used to hold the components in position during the PCB assembly process. The component mounting holes are NPTHs.

If you have NPTHs in your design, please leave a note for the manufacturer so that they understand the purpose of it and won't reach back to you thinking it was A rule is a rule even for a hole.

Also indicate via-in-pad holes in your drill chart.

Plated through-hole (PTH):

Finished hole size (minimum) = 4 mils

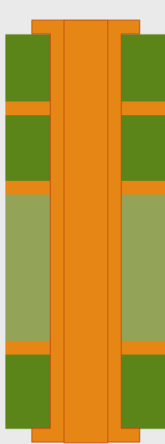
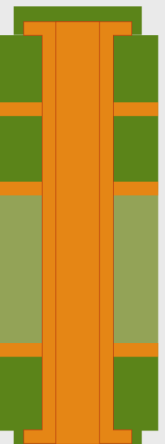
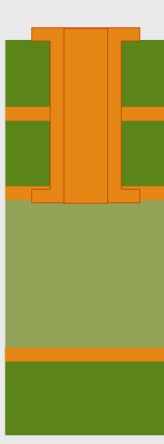
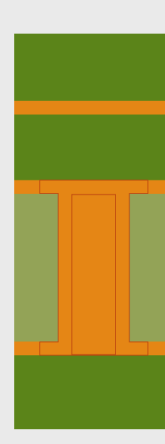
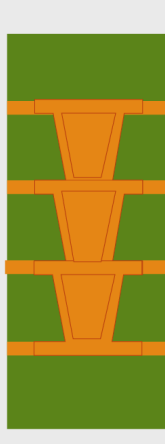
Annular ring size (minimum) = 3 mils

Drill diameter tolerances must be specified on the drill chart. Sierra Circuits prefers a drill diameter tolerance of $\pm 0.003"$ for PTH and NPTH drills.

The accuracy of the hole location is compromised when the drill rules are violated.

3.5 Board complexity Vs price of the board:

The number of different drill sizes does not impact the cost. It is the different via structures that start and stop on different layers. This results into multiple laminations and causes problems in registration which impacts time and yield. Work with your manufacturer to design the most efficient PCB stack-up for your technology requirements. Only a PCB manufacturer truly knows what it takes to build a circuit board.

	Through Via	Tented Via	Blind Via	Buried Via	Stacked Via	Epoxy Fill
						
Price	Standard	Standard	+\$	++\$	++\$\$	\$\$\$
Duration	Standard	Standard	+⌚	+⌚	+⌚	+⌚

FOR YOUR EYES ONLY!

The CNC drill machine:



The drilling machine is a preprogrammed computer numerically controlled (CNC) machine. The drill takes place based on the XY coordinates fed into the CNC system. The spindles rotate at a high RPM and ensure an accurate drill hole in the PCB. When the spindle rotates with a rapid speed, heat is generated due to the friction between the hole wall and the spindle. This melts the resin content on the hole walls and results in a smear of resin. Once the required holes are drilled, the exit and entry panels are discarded. This is a small gist of what goes happens on the shop floor.

3.6 Drilling Disasters

When the drill bit fails to hit the preferred spot and shifts away in the same axis, the shifts in the drilled hole will give rise to tangency or breakout in annular rings.

Roughness inside the drilled hole:

Roughness leads to non-uniform plating of copper. This results in blow holes and barrel cracks. It can also result in lower insulation resistance by penetration copper plating solution to the hole wall.

Resin smear:

The resin in the board melts due to the heat generated during the drilling. This resin sticks to the hole walls and is called as resin smear. This again results in poor copper plating and leads to conductivity failure between the via and the interior layers of the circuit. The resin smear is removed by a chemical solution.

Presence of entry and exit burrs:

Burr is the unwanted part of copper sticking out of the hole after the drilling process. It is mostly seen both on the top surface of highest stacked of printed circuit board and on the bottom surface of lowest stacked of the printed circuit board.

Nailhead:

Exposed copper of inner layers on through-holes formed the shape of nail heading during drilling. Such a huge burden to hole brings non-uniform surface of through-holes and may cause conductivity failure of plating.

All these irregularities ruin the integrity of a PCB. These problems have been a nightmare for PCB manufacturers. For these reasons, our in-house PCB engineers whimsically define PCB as **"Problems Come Back!"**

In order to eliminate these flaws, scholars have researched on drilling process and PCB design structure and have come up with the following solutions.

THE REMEDIES

Desmear process:

It is a chemical process where the melted resin that is deposited on the hole walls is removed. This process eliminates unwanted resin and enhances electrical conductivity through the vias.

Deburr process:

It is a motorized process that eradicates the elevated ends (crowns) of the metal (copper) called burrs. Any debris that's left out within the holes

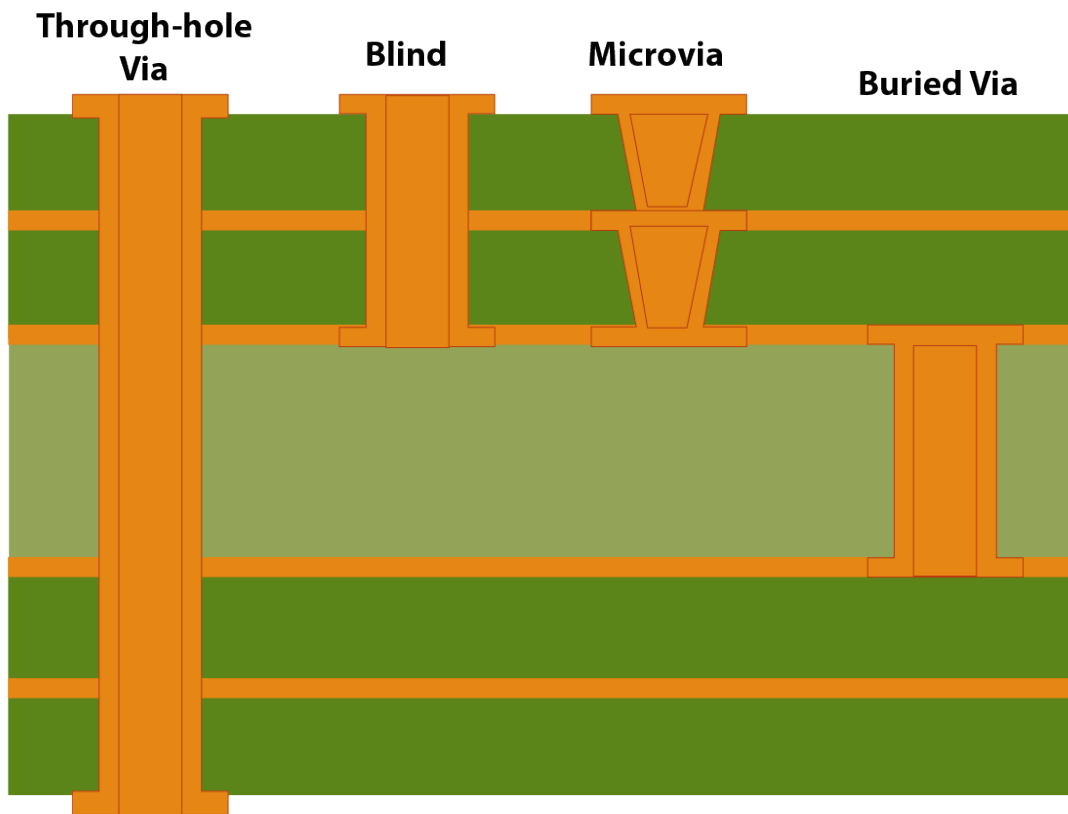
is exterminated through deburring process. The desmearing process is repeated after deburring.

Delamination can be avoided by using laser drills. As mentioned earlier, in laser drilling, the workpiece and the tool do not come under contact thus eliminating delamination.

In recent years, the drilling process has been optimized compared to earlier technologies. With the exponential growth in the PCB industry, the drill precision is reaching close to perfection. We believe now you have a better picture of how the PCB drilling process is done. It looks quite complicated, doesn't it? Don't worry! Just submit your design files (Gerber) to Sierra Circuits. Allow us to drill, while you sit back and watch Netflix and chill!

4 VIAS

4.1 Types Of Vias



Types of vias

Depending on their functionality, there are different types of vias that are drilled into a PCB.

- **Through-hole vias drilled with mechanical drill bits**

The hole penetrates from the top layer to the bottom layer. They can be either PTH or NPTH. For PTH, the connection is established from the top to the bottom layer.

- **Blind vias**

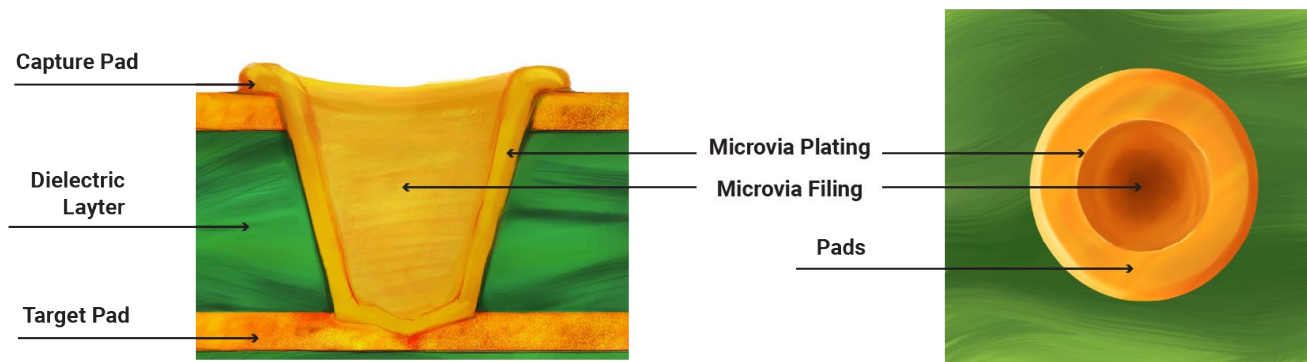
The hole penetrates from an exterior layer and ends at an interior layer. Here, the hole doesn't penetrate through the entire board but connects the PCB's exterior layers to at least one interior layer. Either the connection is from the top layer to a layer in the center or from the bottom layer to some layer in the interior region. The other end of the hole cannot be seen once the lamination is done. Hence, they are called blind vias.

- **Buried vias (hidden vias)**

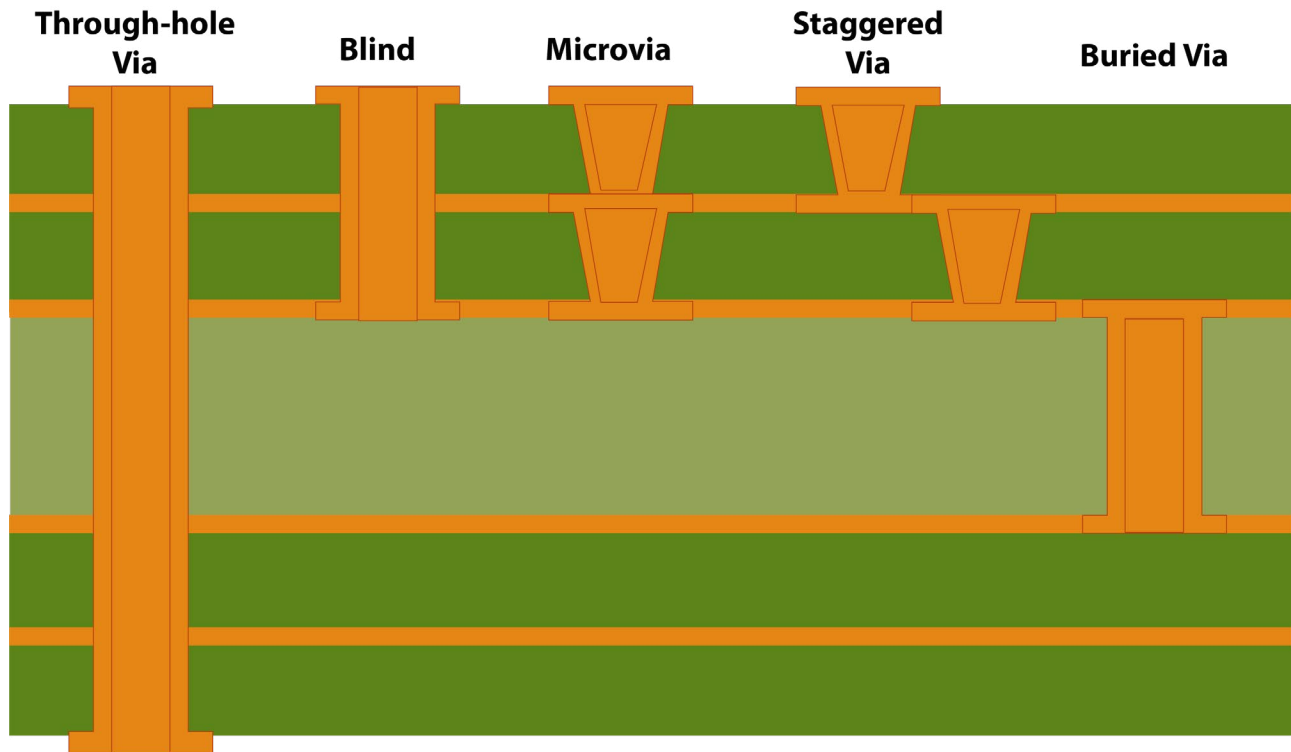
These vias are located in the interior region of the PCB. The buried vias have no paths to the outer layers. They connect the inner layers and stay hidden from sight.

As per IPC standards, buried vias and blind vias must be 6 mils (150 micrometers) in diameter or less.

4.2 Microvias



The most commonly known vias are the microvias (μ vias). During PCB manufacturing, microvias are drilled by lasers and have a smaller diameter compared to the standard through-hole vias. Microvias are generally implemented in High-Density Interconnection (HDI) PCBs. The depth of a microvia isn't usually more than two layers deep since the plating of copper inside these small vias depends on the microvia aspect ratio. The smaller the diameter of a via, the higher should be the throwing power of the plating bath to achieve electroless copper plating. Sierra Circuits uses special microvia plating baths to achieve reliable connections.



Types of microvias:

Microvias can be classified into **stacked vias** and **staggered vias** based on their location in the PCB layers.

Stacked vias are piled on top of one another in different layers.

Staggered vias are offset in the different layers. And they are more reliable than stacked vias. Call us for more details.

Additionally, there is another type of microvias called skipvias. Skipvias skip one layer, meaning, they pass through a layer making no electrical contact with that specific layer. The skipped layer will not form an electric connection with that via. Hence the name.

Microvias improve the electrical characteristics and also allow miniaturization for higher functionality in less space. This, in turn, makes room for large pin-count chips that can be found in smartphones and other mobile devices.

Microvias reduce the layer count in printed circuit board designs and enable higher routing density. This eliminates the need for through-hole vias. The microvias micro size and capabilities have successively increased the processing power. The implementation of microvias

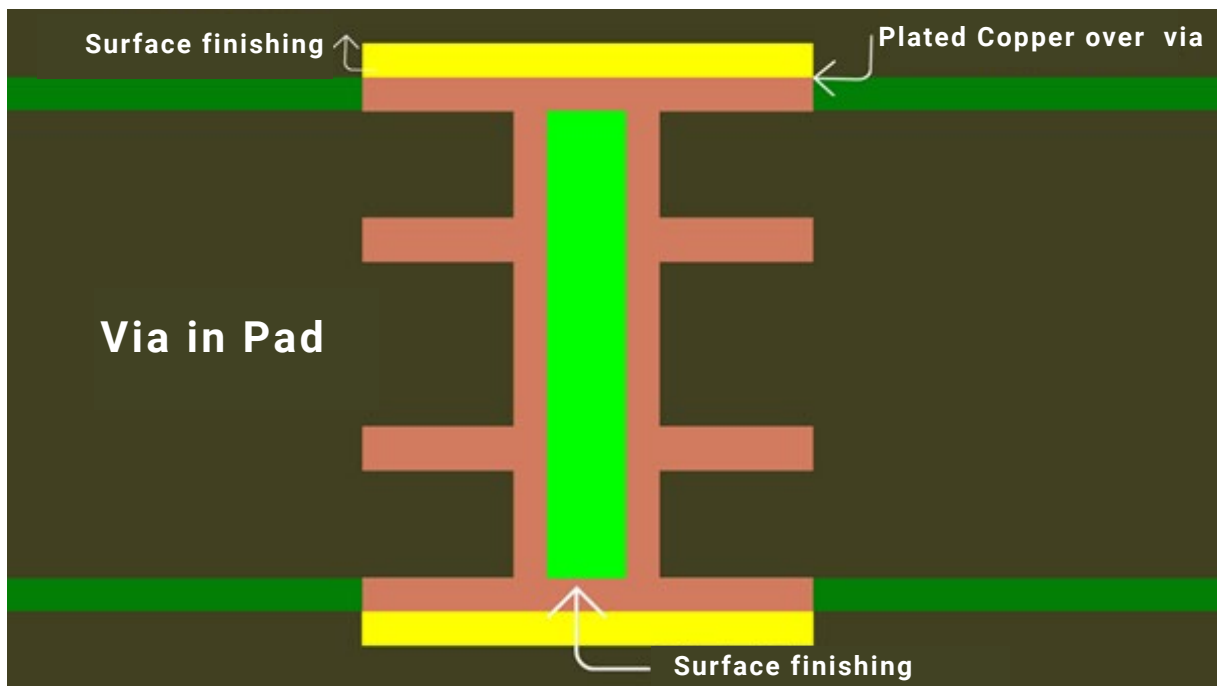
instead of through-holes can reduce the layer count of PCBs and also ease the BGA breakout. Without microvias, you would still be using a big fat cordless phone instead of your sleek little smartphone.

PRO TIP!

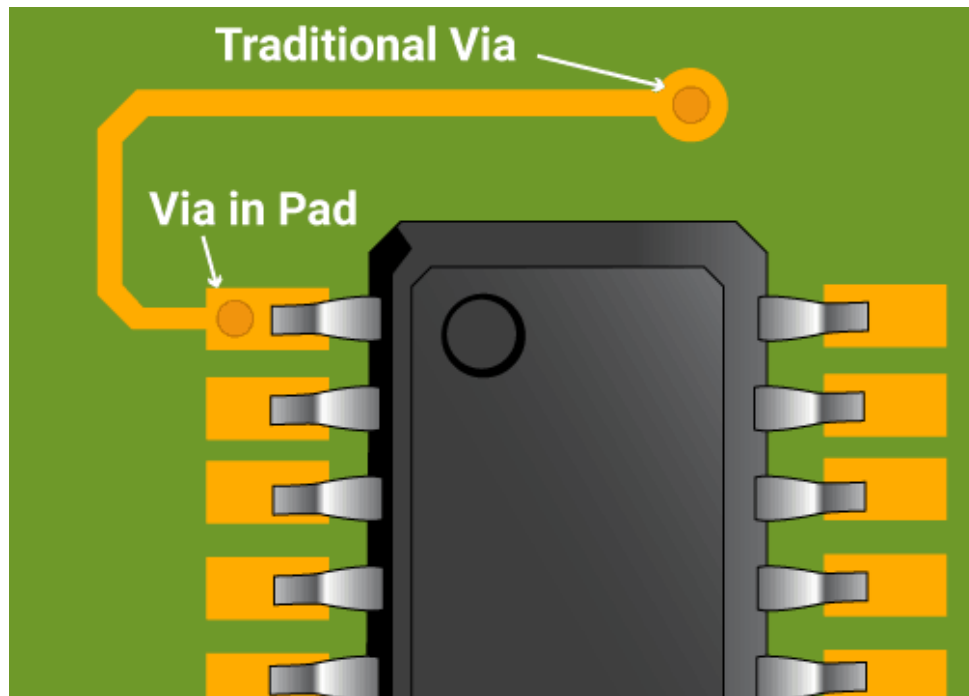
Avoid tented vias. Sometimes a via is covered with soldermask so that it isn't exposed. This is called a tented or a covered via. It most likely requires extra solder mask process steps.

4.3 Via-In-Pad

Implementation of via-in-pad or via-in-pad plated over (VIPPO) in your design:



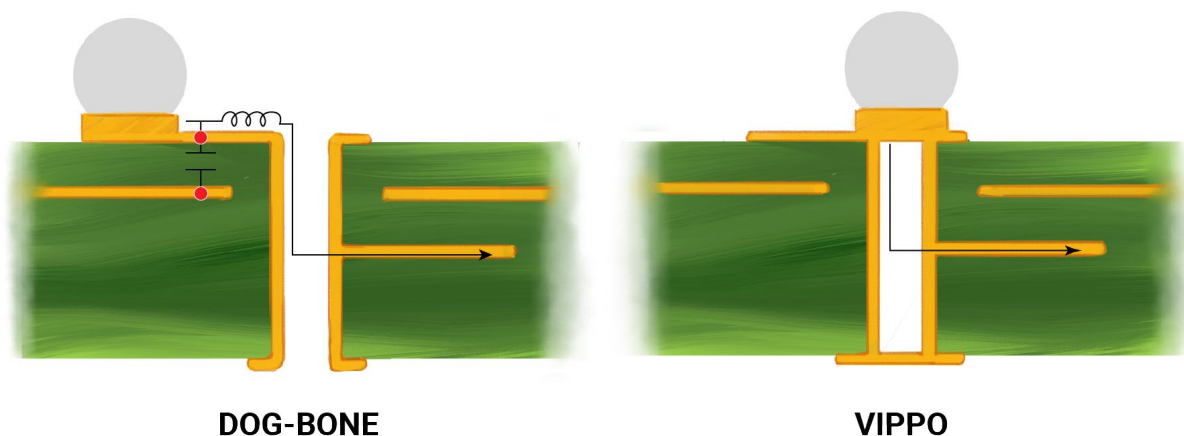
The increasing signal speed, board component density, and PCB thickness have led to the implementation of via-in-pad. The PCB design engineers implement VIPPO along with the conventional via structures in order to achieve routability and signal integrity requirements.



Via-in-pad Vs traditional via

What is a via-in-pad?

In traditional vias, the signal trace is routed away from the pad and then to the via. You can see this in the above diagram. This is done to avoid seepage of the solder paste into the via during the reflow process. In a via-in-pad, the drilled via is present right below a pad. To be precise, the via is placed within the pad of a surface mount component.

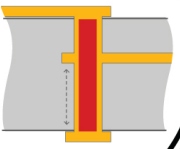


Traditional dog bone and VIPPO – Image credit: Cisco Systems, Inc.

First, the via is filled with non-conductive epoxy depending on the designer's requirement. Later, this via is capped and plated to regain the land area. **This technique shrinks the signal path lengths and as a result eliminates the parasitic inductance and capacitance effect.**

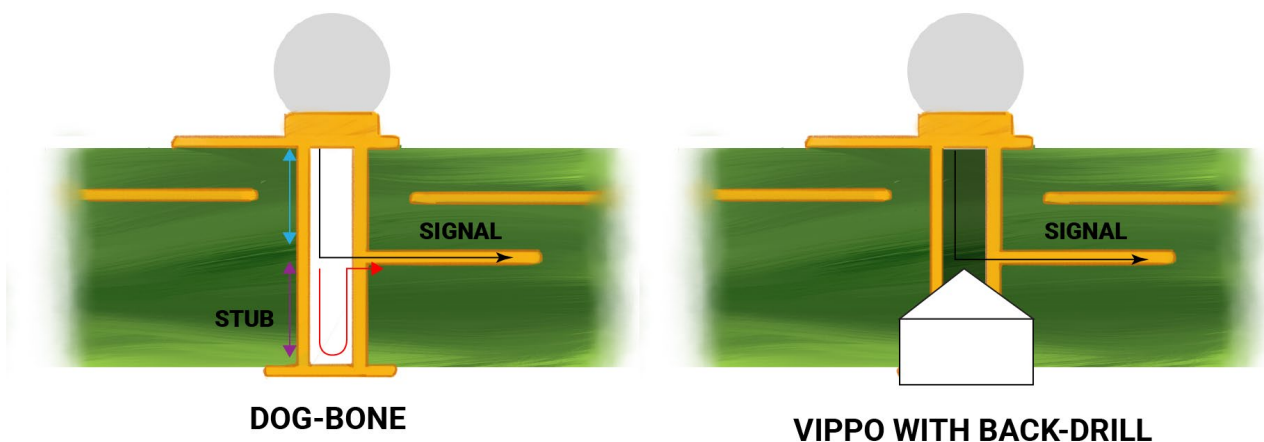
The via-in-pad accommodates tighter component pitch sizes (like .5mm) and shrinks the PCB's overall size. This technology is ideal for BGA footprint components.

To make things better, back-drilling process is implemented along with the via-in-pad. The back drilling is performed to eliminate the signal reflections within the unused portion of the via. The unwanted via stub is drilled to remove any kind of signal reflection. This ensures **signal integrity**.



Maximum Via Stub Length Calculator

[Try Now](#)



Via-in-pad can provide a flat surface for components and can help reduce inductance in high-frequency board.

So, vias are basically wells but not big enough to drop a coin and make a wish. The via technology implemented by your PCB manufacturer could make or break your product. The next time you run into a wishing well, do remember to wish for a perfect via!

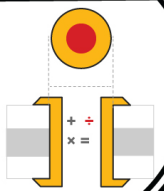
4.4 PCB Design Tips For Vias

Here are a few quick tips that you can consider while employing vias in your design:

- Use maximum micro via structures in your design.
- Stacked and staggered vias: Choose staggered instead of stacked vias since the stacked vias need to be filled and planarized. This process is time consuming and expensive as well.
- Implement smaller vias. This can help you build an efficient HDI PCB since the stray capacitance and inductance gets reduced.
- Via-in-pads must be filled, unless they reside in thermal pads.
- The pad matrix on which a BGA will be installed may include through vias and blind vias, but all of them must be filled and planarized, otherwise solder joints will be compromised.
- Incorporate vias in the thermal pads under QFNs to help solder flow through to conductive planes.
- The vias ensure a secure solder joint for the thermal pad and prevent solder from floating the package during assembly, which could hamper forming good solder joints at the QFN contacts.
- An assembly shop can compensate for a lack of through vias in a thermal pad by adding windowpane-shaped opening in the solder paste stencil above the pad, to relieve solder pooling and outgassing during assembly, but the fix is less effective than if vias were present.
- Check for minimum clearance of traces and vias from the routed/scored edges.
- Check the position of vias for BGA packages.
- Via-in-pad design requires filling. Use non-conductive epoxy as a standard.
- Dog-bone design: Separate each via from its pad with a predefined short trace covered with soldermask. Ensure there is no mask clearance for the vias under BGA.
- The board documentation should include a drill file with tool codes and X-Y coordinates for all holes.
- The fab drawing should include a drill chart with hole symbols on the

drawing and finished hole sizes along with via tolerances.

- The Gerber files should include via plugging holes if required.
- **Tolerance:**
 - Minimum outer layer annular ring: as per IPC standards
 - Minimum inner layer annular ring: as per IPC standards
 - Drill to plane clearance: 8 mils
 - Diameter: ± 3 mils preferred
 - Location: 1 mil
 - Registration: 1 mil
 - Via clearance of soldermask: 2.5 mils bigger than via pad size
 - Encroachment of soldermask onto via: via size + 3 mils
 - Anti-pad: 16 mils bigger than the hole size and plane relief preferred 8 mils

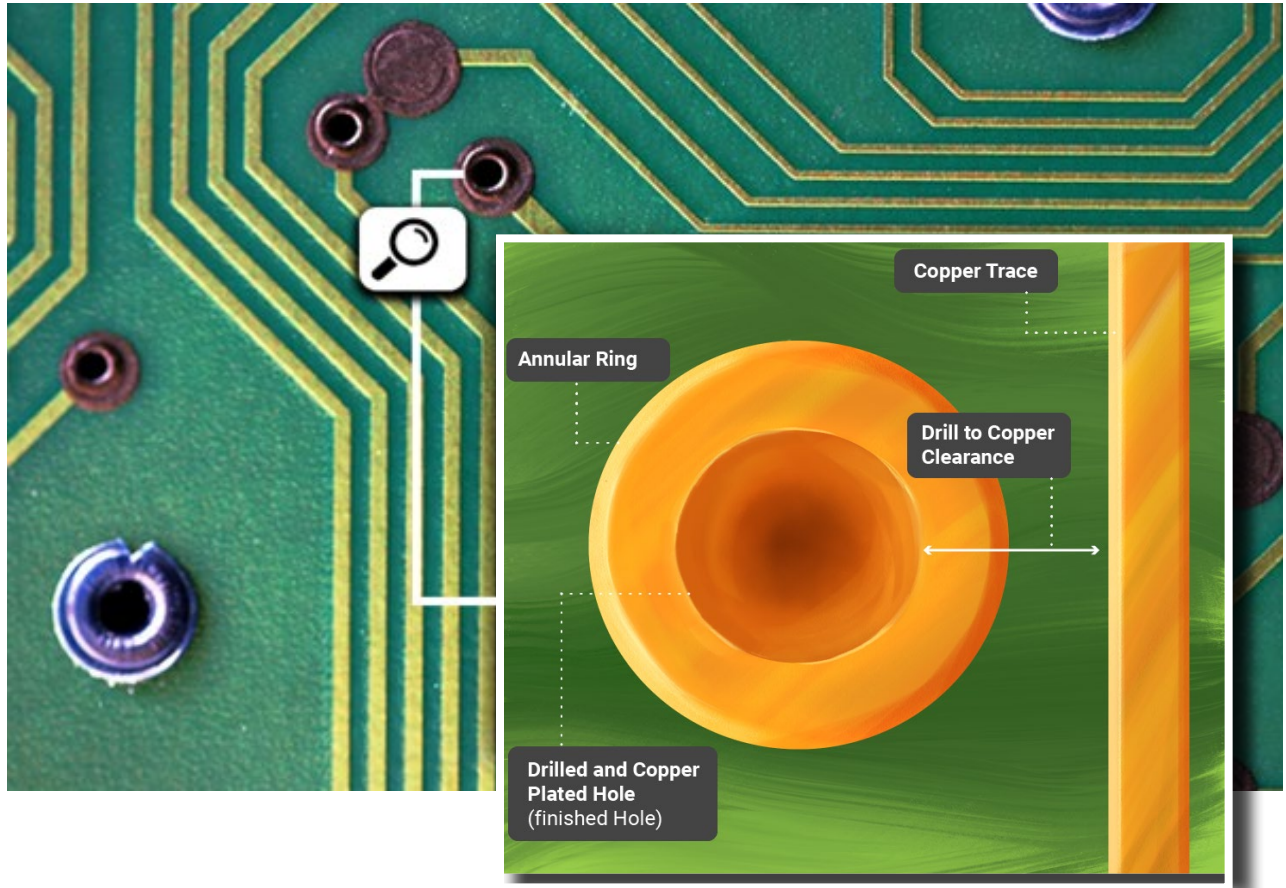


Via Current Capacity and Temperature Rise Calculator

[Try Now](#)

There may be requirements for fabricators to plug, fill, or tent vias on a PCB.

5 ANNULAR RING CHECKS

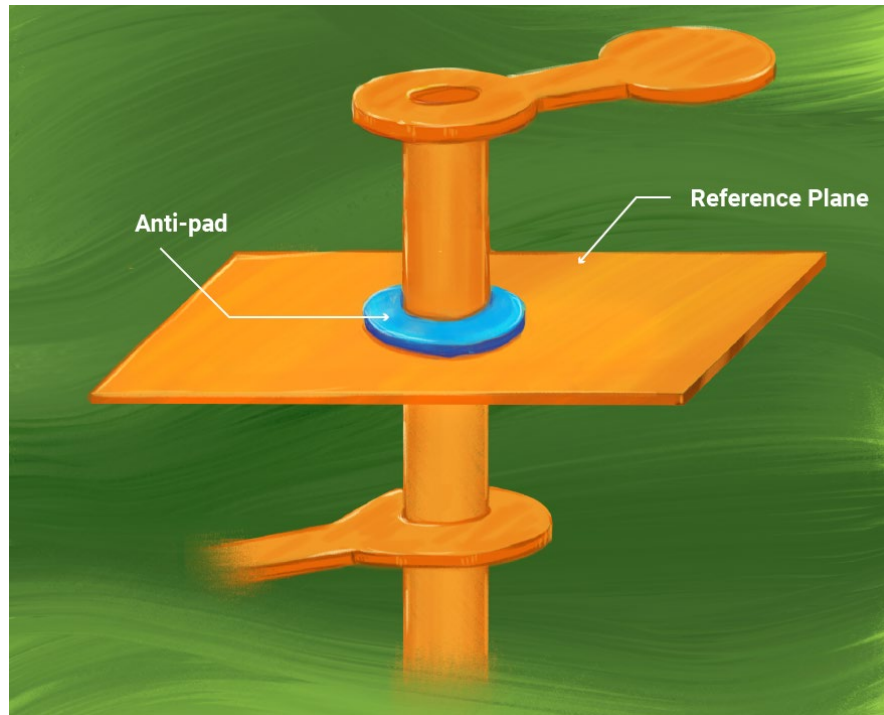


5.1 What Is An Annular Ring?

An annular ring is the area of copper pad around a drilled and finished hole. The finished hole we are talking about here is nothing but a copper plated via. All around this via, there should be enough copper to form a solid connection between the copper traces and the via in a multi-layer PCB. Therefore, the annular ring is a bridge between a via and copper traces to ensure signal flow.

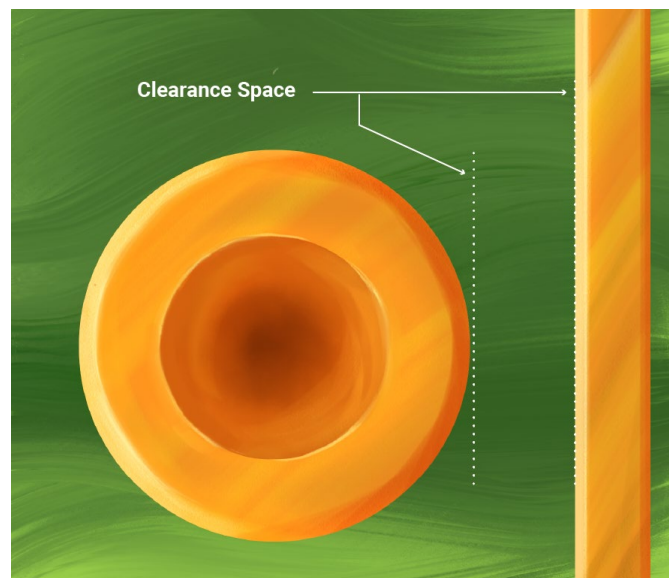
Anti-pad

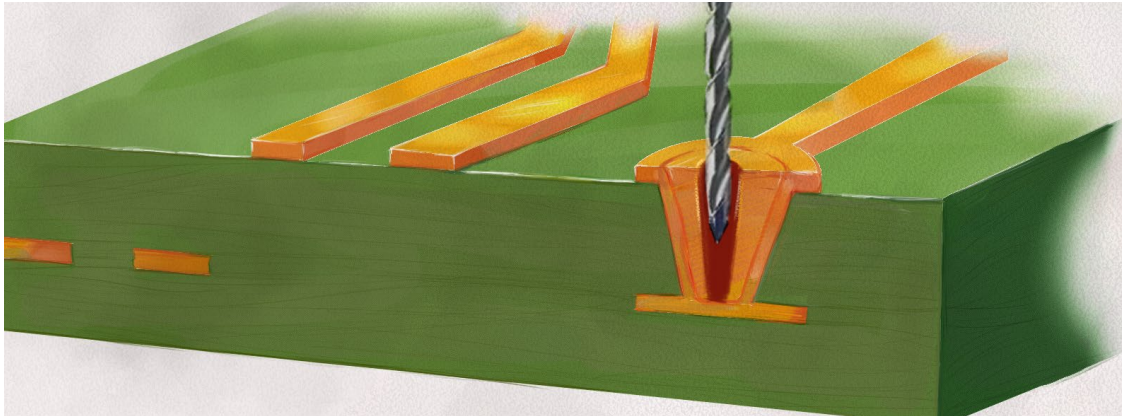
Anti-pads are added to keep unwanted signals away from the ground planes.



Annular ring clearance:

Annular rings are one of the biggest concerns of PCB designers. You know that you may have placed your via right in the middle of the pad in the design files, but in the physical world it might not be easy to get the exact same result.





5.2 Formation of an annular ring through drilling process

When you need to connect traces to another layer in a multi-layered board, you typically have to place a copper pad on your circuit board and drill a via on it to make the connection. The outer ring surrounding the via after the drilling process constitutes the annular ring. Then you plate.

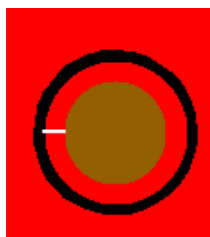
5.3 The Cosy Annular Ring Width

Ideally, designers prefer annular rings with holes located at the dead-center in order to get the best connection possible between the vias and the layers.

The perfect annular ring width is the difference between the diameter of the copper pad and the diameter of the finished hole divided by two.

- **Annular ring width = (diameter of the pad – diameter of the finished hole) / 2**

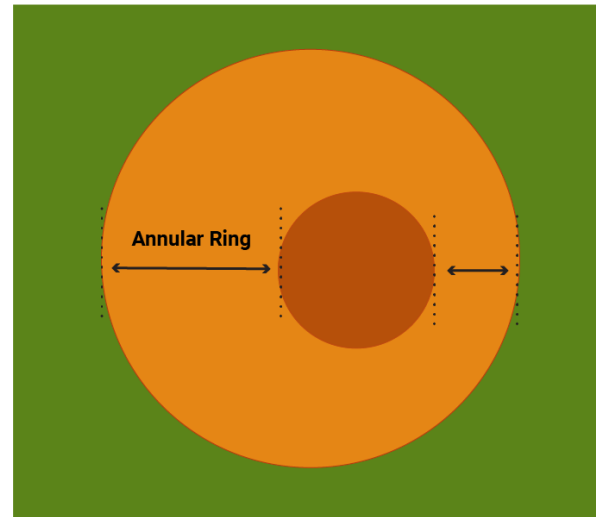
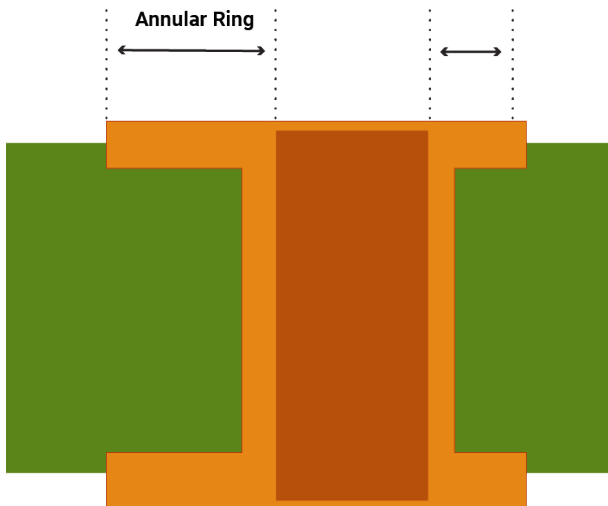
For example, if your pad diameter equals 22 mils and the hole diameter equals 10 mils, then the annular ring width is calculated in this manner: **$(22 - 10) / 2 = 6$ mils.**



Laser via hole = 3mils minimum
Component hole = 4mils

5.4 Annular Ring: The Horror!

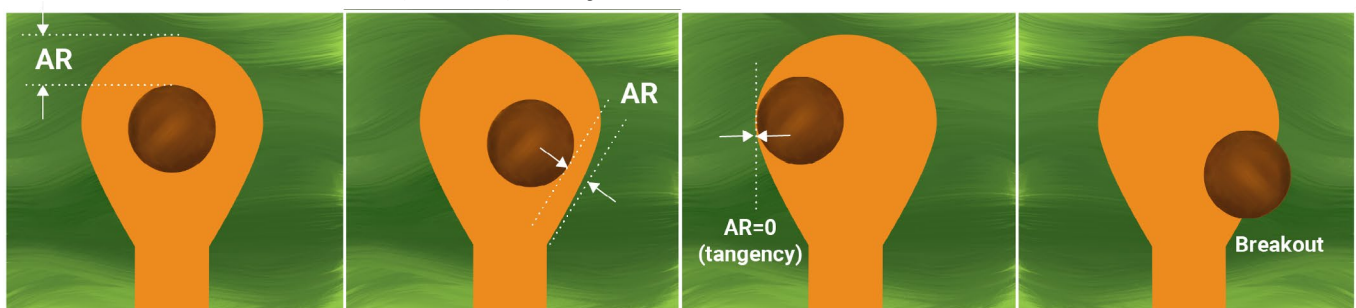
- Undesired annular ring
- Tangency
- Breakout



Cross section of an annular ring with the hole drilled slightly off-center

Even though the designers calculate and place the perfect annular ring in their CAD design, manufacturing issues often cause vias to be drilled off-center. Indeed, the drill bit may slightly wander and miss the middle of the pad. Another explanation could be that some layers may slightly shift during the lamination process. Or, the registration may not be 100% dead-center during the imaging process, and so on. This could lead to an inaccurate circuit and you will be left with a PCB that doesn't meet your Class 2 or Class 3 specs.

Undesired annular ring, tangency, and breakout:



The manufacturing issues mentioned earlier can result in three different problems.

Case 1:

If the PCB designer provides a wide annular ring area, chances are that the via will be drilled approximately in the middle of the pad. Even though it will not be dead-center, this will still retain a good electrical connectivity.

Case 2:

If the PCB designer doesn't provide a wide enough annular ring area, then the hole could almost end up touching the boundaries of the pad. This leads to an annular ring width that equals 0. Here, the drilled hole forms a tangent with the outer rim of the annular ring. This is called tangency. This will lead to connection problems between the via and the copper traces. This violates Class 3 requirements.

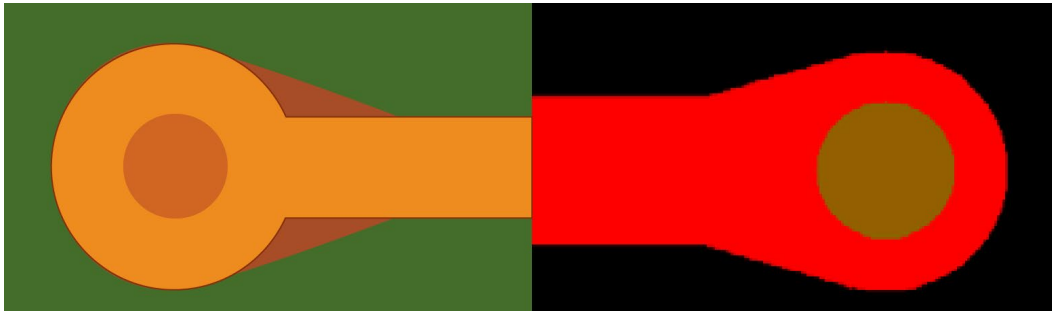
Case 3:

A designer's worst nightmare is when the hole shifts over the copper pad. The drill bit might deviate outside the pad during the drilling process. This is what we call an annular breakout. Annular breakouts can lead to connection problems between the via and the layers. It will also cause problems with component placement, solderability, and so on. If the drill breaks out of the pad, you could've a direct short. This is why you need an 8-mil drill-to-copper.

Special Case (When Karma hits you hard!):

When two vias are placed too close to each other, the current through them can be too high and can short the two vias. This phenomenon is referred to as conductive anodic filament (CAF) formation. One of the best ways to reduce the angular ring irregularities in your PCB is by implementing tear dropping. This trick provides an extra space on the pad for the drilling process. Here the copper pads are elongated towards the copper trace side making it look like a comet. This technique reduces breakout and tearing of copper by providing more pad area to the drill bit. Hence the name.

Tear dropping:



Teardrops are mandatory for designing medical and military boards (IPC Class 3 boards).

5.5 Annular Ring: The Safe Zone!

Getting the perfect annular rings predominantly depends on your PCB manufacturer. The minimum annular ring varies from manufacturer to manufacturer. So, it is always good to find out their capabilities before placing an order. Some manufacturers do offer smaller annular rings at an extra cost. But smaller the annular ring, more problems may arise within the hole. That's something you need to look out for.

For a High-Density Interconnect (HDI) PCB design, a smaller annular ring assists in more component placement and saves more space on the PCB. This leads to efficient real estate utilization. As a result, there will be more room for traces and spaces.

The onus lies on the designer to make sure that there is enough annular ring width that can be manufactured by a manufacturer. Not to forget, sometimes the CAD tool that the designer uses doesn't add an annular ring by default. Hence, these things must be taken care of before the design is sent to the manufacturer.

5.6 Inspection Guide

Here are a few things that can help you achieve a healthy annular ring:

- As a quick inspection, check if the copper pads are present for plated drills on all copper layer.
- Check if the annular ring called out in fab can be maintained by the manufacturer.

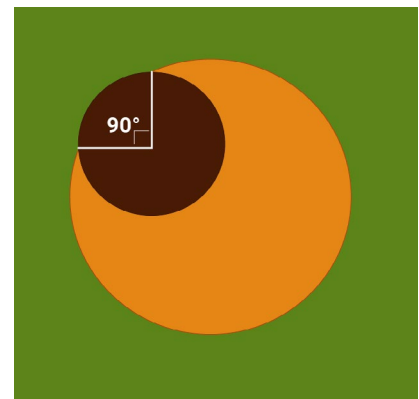
For example, in order to have a minimum 2-mil annular ring, the following must be considered:

2-layer job	4 mils for drilled hole
4-layer job	5 mils for drilled hole
6-layer job	5-6 mils for drilled hole
More than 6-layer job	7 mils for drilled hole

The annular ring plays a critical role in PCB design and manufacturing. Hence, it's a good practice to make sure all your annular rings are carefully craft.

5.7 IPC Class 2 vs Class 3

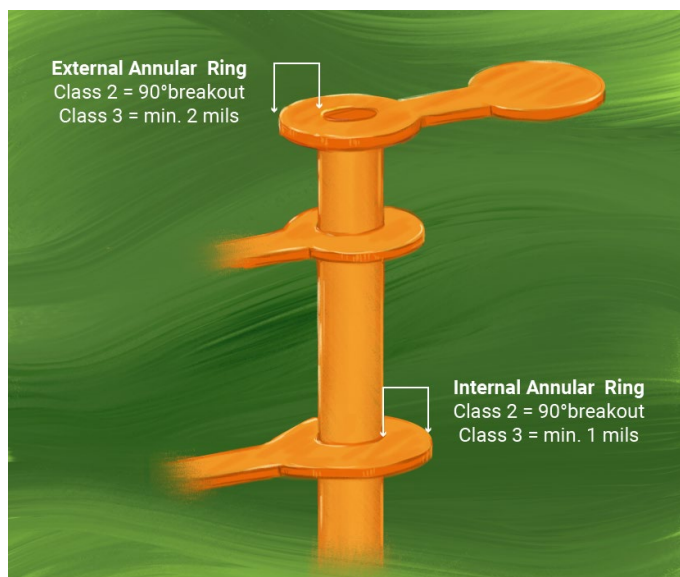
Another topic IPC Class 2 and Class 3 differ on is drill breakouts. Class 2 allows breakouts from the annular ring whereas Class 3 does not accept any lifted or fractured annular rings. Class 3 boards need to be highly reliable and when there is a breakout, it is too difficult to find out how much is really broken out and how much it really affects the connection with the pad. For Class 2, 90 degrees breakout of the hole from land is allowed provided minimum lateral spacing is maintained.



The conductor junction cannot be reduced more than 20% of the minimum conductor width specified on the engineering drawing. The conductor junction should never be less than 2 mils or the minimum line width, whichever is smaller. For Class 3, the minimum internal annular ring cannot be less than 1 mil. The external annular ring cannot be less than 2

mils. It is measured from the inside of the PTH barrel to the edge of the land pad and may have 20% reduction of the minimum annular ring in isolated areas due to defects, like pits, nicks, pinholes, or dents.

There will be a difference between the designed annular ring and the manufactured/actual annular ring. This is due to shifting in materials during the circuit board manufacturing process. To meet the Class 3 requirements, Sierra uses Pleuritic machines to discover the shift in material, software to re-scale the drill locations, and vision drilling to accurately place the drills.



5.8 Design Rules For Annular Rings

To achieve acceptance for Class 2 and Class 3, follow the tables below published by Altium. The first one gives the annular ring requirements for mechanically drilled blind, buried, and through-holes on ½ oz copper:

DRILL & PAD Diameter IPC Class 2 1/2 oz Copper				
Drill	Pad	Anti-Pad	PCB Thickness	Aspect Ratio
0.006"	0.016"	0.026"	up to 0.039"	6.05:1
0.008"	0.018"	0.028"	up to 0.062"	7.75:1
0.010"	0.020"	0.03"	up to 0.100"	10:01
0.012"	0.022"	0.032"	up to 0.120"	10:01
0.0135"	0.024"	0.034"	up to 0.135"	10:01

DRILL & PAD Diameter IPC Class 3 1/2 oz Copper				
Drill	Pad	Anti-Pad	PCB Thickness	Aspect Ratio
0.008"	0.023"	0.033"	up to 0.062"	7.75:1
0.010"	0.025"	0.035"	up to 0.100"	10:01
0.012"	0.027"	0.037"	up to 0.120"	10:01
0.0135"	0.028"	0.038"	up to 0.135"	10:01

And this table is for various copper thicknesses:

DRILL & PAD Diameter IPC Class 2		
	Pad diameter over Drill	
	< 8 Layers	> 8 Layers
1/4 oz copper	0.010"	0.010"
3/8 oz copper	0.010"	0.010"
1/2 oz copper	0.010"	0.010"
1 oz copper	0.012"	0.012"
2 oz copper	0.014"	0.014"
3 oz copper	0.016"	0.016"
4 oz copper	0.018"	0.018"

DRILL & PAD Diameter IPC Class 3		
	Pad diameter over Drill	
	< 8 Layers	> 8 Layers
1/4 oz copper	0.010"	0.010"
3/8 oz copper	0.010"	0.010"
1/2 oz copper	0.010"	0.010"
1 oz copper	0.012"	0.012"
2 oz copper	0.014"	0.014"
3 oz copper	0.016"	0.016"
4 oz copper	0.018"	0.018"

DRILL & PAD Diameter IPC Class 3a		
	Pad diameter over Drill	
	< 8 Layers	> 8 Layers
1/4 oz copper	0.010"	0.010"
3/8 oz copper	0.010"	0.010"
1/2 oz copper	0.010"	0.010"
1 oz copper	0.012"	0.012"
2 oz copper	0.014"	0.014"
3 oz copper	0.016"	0.016"
4 oz copper	0.018"	0.018"

5.9 PCB Through-Hole Plating Requirement

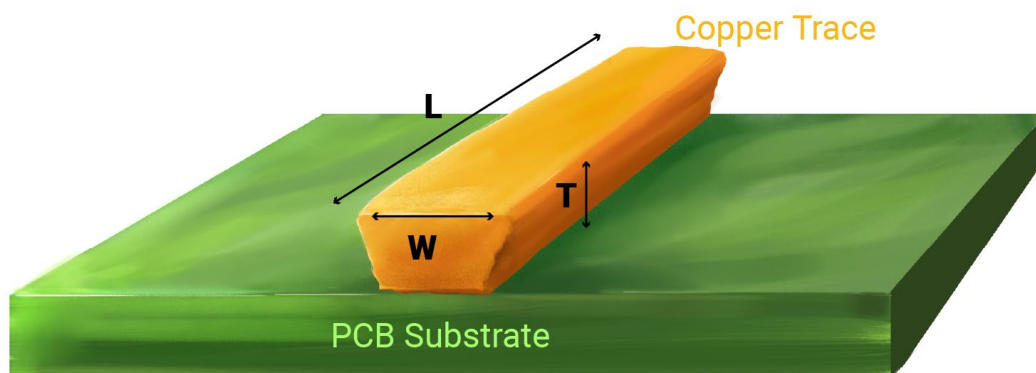
Class 3 requirements are as well more stringent for voids in copper. A copper void is where the copper plating in the barrel of the hole is missing exposing the dielectric material of the drilled hole. Class 2 allows one void in 5% of the holes. Class 3 and 3/A allows no voids. The plating thickness requirement for Class 2 is 0.8 mil as opposed to 1 mil for Class 3.

These are just a few requirements that differ between Class 2 and Class 3. As usual, the best advice we can give you is to communicate with your PCB manufacturer. They will guide you and help you get it right the first time. You should also request a cross-section of your board to make sure that your shop met your Class 2 or Class 3 requirements.

6 SIGNAL CHECKS

The first checklist we like to implement after receiving Gerber files is signal checks. This checklist holds key parameters that include conductor width, spacing requirements, hole registration and many more. As we move forward, we would like to shed some light on some of these parameters.

6.1 Conductor Width



Traces within the PCB are used to connect different components to different connectors. These traces can be identified as continuous paths of copper that exist on the surface of a PCB. The width of the conductor traces becomes crucial as it directly impacts the functionality of a PCB. Additionally, increasing signal flow through PCB traces generates an immense amount of heat. Monitoring trace width also helps to minimize heat build-up that typically occurs on boards. The conductor width also determines the resistance of the traces that directly affect the transmission of a signal.

Many manufacturers opt for their default trace width value available, which may not be suitable for high-frequency applications. Moreover, depending on the application, the trace width is varied, thus affecting the current carrying capacity of the trace. The maximum current carrying capacity for 2 oz copper with temperature rise of 10°C is mentioned in the table.

Maximum Current Capacity (amps)	Trace Width (mil)
2	80
6	150
8	220
10	300

The formula for calculating the trace width for allowable current is published in the IPC-2221 standard section 6.2 as shown below.

$$\text{Width[mils]} = A[\text{mils}^2] / (\text{Thickness[oz]} * 1.378[\text{mils/oz}])$$

As per IPC-2221, for internal layers $k = 0.024$ and for external layers, $k = 0.048$.

The cross-sectional area A is calculated by below formula:

$$A[\text{mils}^2] = (I[\text{Amps}] / (k * (\Delta T[\text{deg. C}]^{0.44}))^{1/0.725}.$$

Where I is the current, k is a constant, ΔT is temperature rise, and A is the cross-sectional area of the trace.

The trace width is considered as one of the most important design parameters during the PCB design. It becomes paramount to decide the adequate trace width to ensure the quality performance of the PCB. This also helps to ensure the safe transmission of current without overheating and damaging the board.

A) Impedance And Trace Calculator

Geometry Information

UNCOATED MICROSTRIP SINGLE ENDED

Diagram showing a microstrip on a PCB with dimensions: $H1$ (dielectric height), W (trace width), and $W1$ (total width). The formula $\Delta W = W - W1$ is shown.

Units (mils):

[Show PCB Dielectric Material construction table](#)

Dielectric Information

Dielectric Height (H1) (mils)

Dielectric Constant (Er1)

Trace Information

Trace Width (W) (mils)

Trace Width (W)

$\Delta W = (W - W1)$ (mils)

Trace Thickness (T) (mils)

Trace Thickness (T)

Impedance Output

Target SE Impedance (Z_o) Ω

Target SE Impedance (Z_o) Ω

Calculated SE Impedance (Z_o) Ω

Calculated SE Impedance (Z_o) Ω

Propagation Delay (Pd) (ps/inch)

Propagation Delay (Pd)

Inductance (Lo) (nH/inch)

Inductance (Lo)

Capacitance (Co) (pF/inch)

Capacitance (Co)

Effective Dielectric Constant (Ereff)

Effective Dielectric Constant

Dielectric Dissipation Factor information

Dissipation Factor (DF1)

Dissipation Factor (DF1)

Signal Loss Input

Frequency (GHz)

Frequency

Surface Roughness (μm)

Length (inches)

Length

[Calculate Loss](#)

Signal Loss Output

Conductor Loss (dB/inch)

Conductor Loss

Dielectric Loss (dB/inch)

Dielectric Loss

Total Insertion Loss (dB/inch)

Total Insertion Loss

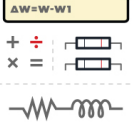
Attenuation factor

Attenuation factor

At Sierra circuits, we have developed an online tool for calculating the overall value of the minimum trace width. The minimum trace width is determined by the amount of required current and copper weight. We offer thicker conductor traces for higher current requirements. We also offer a thicker copper weight allows for thinner traces.

There are various factors that can affect the selection of the right trace width. Some of the key factors include the thickness of the copper layer, the type of bottom or top layer, and the length of the track. Special design guidelines are implemented for traces that are on the inner layer circuit board, for instance heat dissipation. Other factors, such as the dielectric height and dielectric constant Df, will also determine the trace width. We also consider other essential parameters, such as the inductance and capacitance of the trace, and the propagation delay. This allows us to calculate the trace width precisely to a great extent. We also understand the need for improvements in signal integrity of the circuit. This has helped us to develop our Impedance Calculator for single-ended and differential pair signals. Furthermore, maintaining a proper signal integrity in the PCB reduces losses such as copper loss and noise.

Having said all of this, we typically suggest our customers to opt for larger traces in order to prevent broken connection, provided there is availability of larger space on the PCB. In your design, try to assign separate D-code for the traces which have to be impedance control.



Impedance Calculator

Try Now

B) Challenges With Conductor Width

The maximum current carrying capacity of a copper trace usually differs from the theoretical value due to several factors. Some of the factors include number of components, pads and vias. Moreover, super large transient surge can lead to the burning down of a trace between pads during initial supply of power or when modifications are implemented on traces. To avoid such complex issues, we prefer to increase the trace width. Solder mask can be applied on PCB traces to avoid transient surge. The solder paste can also be applied on a surface mount technology (SMT) procedure.

In simple words, it is highly preferred to calculate the PCB trace current carrying capacity in order to decide the precise trace width. However, other external factors, such as dust or contaminant pollution, are also considered in real printed circuit board fabrication or assembly. The excess of pollution leads to partial broken traces.

C) Minimizing Losses And Sierra's Capabilities

The criticality of the trace width calculation also depends on parameters including PCB copper foil cross-sectional area, maximum current carrying capacity and consistent temperature rise.

Additionally, parameters such as conductive material selection and current carrying capacity vary as per types of conductors including internal conductors and external conductors. Also, the maximum current carrying capacity of internal conductors is half of that of external conductors. The copper foil cross-sectional area is directly proportional to the trace width. We can also say that the rising in the temperature and maximum current carrying capacity are dependent on external and internal conductors.

$W = (I_{max} \cdot \Delta T) \cdot Th$

+

÷

×

=

W1

W2

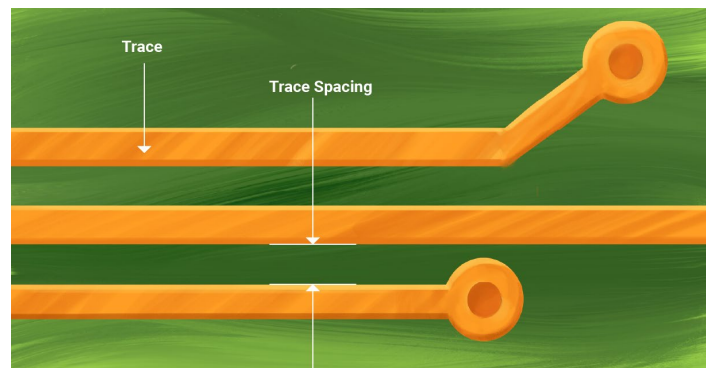
IPC-2152

Trace Width, Current Capacity and Temperature Rise Calculator

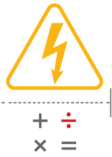
Try Now

The standard trace width is 4 mils. The minimum spacing is done to limit excess of losses. Usually, the size of traces on an outer layer shouldn't be below 4 mils, as plating needs to be performed on these traces.

6.2 Spacing



Spacing between PCB traces is another critical parameter during signal checks. Spacing between traces helps maintain a distance between two traces, thus avoiding flashover or tracking between electrical conductors. The flashover or tracking are defined as an electric breakdown along the surface of the PCB. Flashover can occur along the junction of the conductor trace and insulator. To avoid flashover or tracking between electrical conductors, several industry standards and rules are placed. Factors, such as voltage, application and type of assembly, significantly impact spacing requirements as well. It is difficult to derive a single solution to decide specific spacing requirements to this issue. Various methods and calculations are implemented in order to calculate the proper distance between two two traces.



PCB Conductor Spacing and Voltage Calculator

[Try Now](#)

A) Why Is Spacing Important?

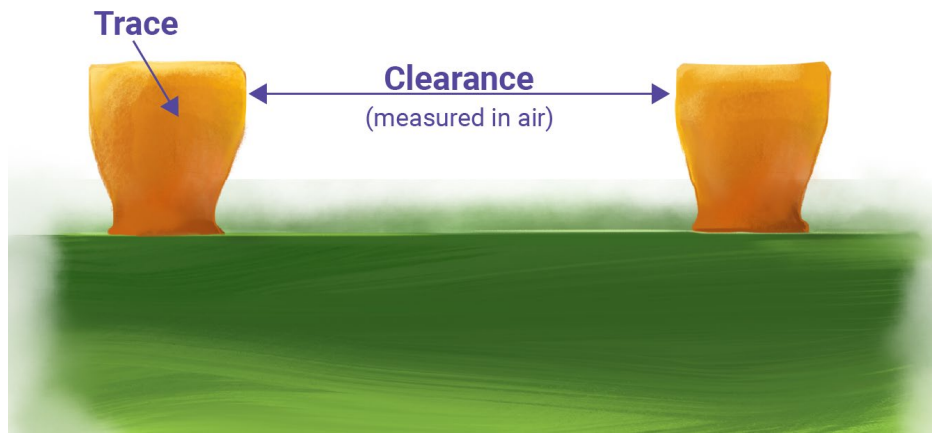
The growing importance of miniaturization in electronic circuitry is driving PCB manufacturers toward reducing size and increasing component density on circuit boards. This helps achieve miniaturization and reduces the costs. This mindset is not only confined to handheld electronic equipment but also prevalent in the entire consumer electronic sector across the globe. The current trend towards miniaturization of electronic circuitry pose substantial challenges to the designer, specifically in mixed technology that includes high-voltage circuits.

Earlier, high-voltage multi-boards like solar energy converters incorporated a separate high-voltage board in the design. With miniaturization, now it is possible to merge multiple boards which allows designers to utilize mixed technologies, including analog, digital, and RF circuits. Design considerations have become a primary concern for PCB manufacturers as high-voltage circuits require additional rules to form increased electrical clear-ances and isolation for operator safety. The development of these rules helps find ways for implementing precise circuit formation and reducing overall product size.

Sierra has developed certain categories in terms of spacing requirement with respect to copper weight:

Start Copper	Minimum Capability in mills (Outer Layers)		Minimum Capability in mills (Inner Layers)	
	Line Width	Spacing Between Conductors	Line Width	Spacing Between Conductors
5 microns	2	3	2	2
9 microns	3	3	2.5	2.5
½ oz	4	4	3	2.25
1 oz	6	6	4	4.25
2 oz	8	8	6	6.25
3 oz	12	12	7	8
4 oz	14	14	8	10

B) Clearance Requirements



Clearance is a crucial parameter while considering spacing between PCB traces. The clearance is defined as the minimum distance through air (medium) between two conductors. Lower clearance among PCB traces can lead to the overhead clearance; overhead clearance may lead to over-voltage. Over-voltage in PCB will result in an arc between neighboring conductive traces on the PCB. This is a virtually instantaneous fault that does not recur until another such over-voltage event. Faults resulting from insufficient spacing for creepage can take much longer to occur.

The trace gets stemmed due to contamination of dust particles and moisture, thus resulting in current leakage from one or two conductors. This can cause a slow breakdown of the surface of the insulating material between them. Breakdown of the surface may be caused due to a voltage spike. The constant high voltage along with an insulating material whose comparative tracking index (CTI) is too low will definitely lead to breakdown of the surface.

The measurement of clearance depends on factors such as the PCB material, applied voltage, and temperature variations. The environmental conditions, such as temperature variations, play a major role in deciding the value for permissible clearance. Additionally, other environmental parameters, such as humidity, decide the breakdown voltage of air and affect the likelihood of arcing. The contamination of dust on the surface of the PCB can cause shortening of the distance between conductors.

C) Creepage Requirement



Creepage is defined as the shortest distance between two conductors on a PCB along the surface of the insulation material. Unlike clearance, which is measured in air (medium), creepage is measured along the surface of the insulation material. Factors such as board material and environment conditions, have an effect on creepage requirements. Moisture and particulate accumulation will shorten creepage distance.

Several errors occur while deciding the creepage distance during a high-density design, owing to the complexity of the design. However, several measures are implemented to avoid these errors, such as moving tracks and increasing the surface distance in your design. Designers can avoid spacing errors by adding a slot between traces or placing vertical barriers of insulation. Designers can increase the creepage distance by various tricks instead of changing the trace layout on the board.

D) Solving Creepage And Clearance Issues

It is quite hard for designers to provide adequate clearance during the layout design stage. But major spacing reduction can be established by adoption of double-sided assembly and by the implementation of insulating materials.

Insulating materials act as a sheet barrier for high-voltage nodes. They also cover overexposed high-voltage leads. As most of the board components are SMDs, the circuits that require clearance can be placed on top and bottom sides of the board. It is also important to maintain clearance from the bounding surface and through-hole connection points.

Usually, the nodes present in the same high-voltage circuits at the same potential do not require increased clearance or creepage between them. But these nodes present within high-voltage circuits, require clearance to low-voltage circuits. With respect to this, try to keep high-voltage circuits on the top and low-voltage circuits at the bottom of the PCB.

Tricks like incorporating V-groove, parallel-sided notch, or placing a slot in your design can effectively solve your creepage issues.

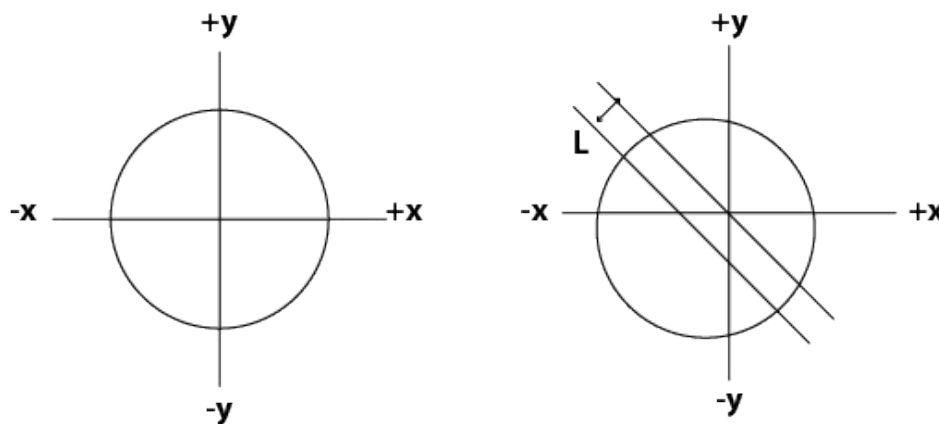
So far, we have understood creepage is the spacing between electrical nodes over an insulating surface. We are treating it as the space between conductors on the surface or internal layers of a PCB.

So far, we have understood creepage is the spacing between electrical nodes over an insulating surface. We are treating it as the space between conductors on the surface or internal layers of a PCB.

6.3 Hole Registration

Why the annular ring you design is not the one you get

The hole registration is another key aspect during the manufacturing process. The hole registration is the displacement of the drilled hole from the target. The accuracy of the hole registration is evaluated by calculating the drilled hole from the target. Various methods are adopted for measuring the hole registration accuracy. This image shows a displacement of the hole registration from its actual position. Figure A shows an ideal hole registration, while Figure B shows a displacement of the hole registration from its actual position. The actual deviation is represented by the symbol 'L' in Figure B. Misregistration of the hole can lead to violation of the minimum annular ring requirement, which should be avoided at any cost.



6.4 Missing Copper

After designers generate an IPC netlist out of a schematic, that list should be purposefully used to avoid missing interconnections. These missing interconnections can result in missing copper that designers must check by themselves. It is expected from designers to generate an IPC netlist. PCB manufacturers can perform mismatch analysis and clarify eventual errors.

6.5 Featured Connection

Featured connection is another important parameter in signal checks. Unconnected nets are not a good idea. It can become a source of electromagnetic noise. Designers should remove unintended ground conductor thin traces in copper flooded areas.

6.6 Unconnected Or Dangling Lines

Unconnected lines may occur due to high level of complexity in a PCB design. It is always difficult to locate unconnected lines. Unconnected lines can result in hairline short defect that incur during PCB manufacturing processes.

However, several design constraints with respect to form factor or manufacturing budget can reduce such defects. The signal checklist allows to identify and correct these issues. Designers can themselves correct such errors by allowing a larger clearance between copper connections and pads.

7 SOLDER MASK CLEARANCE

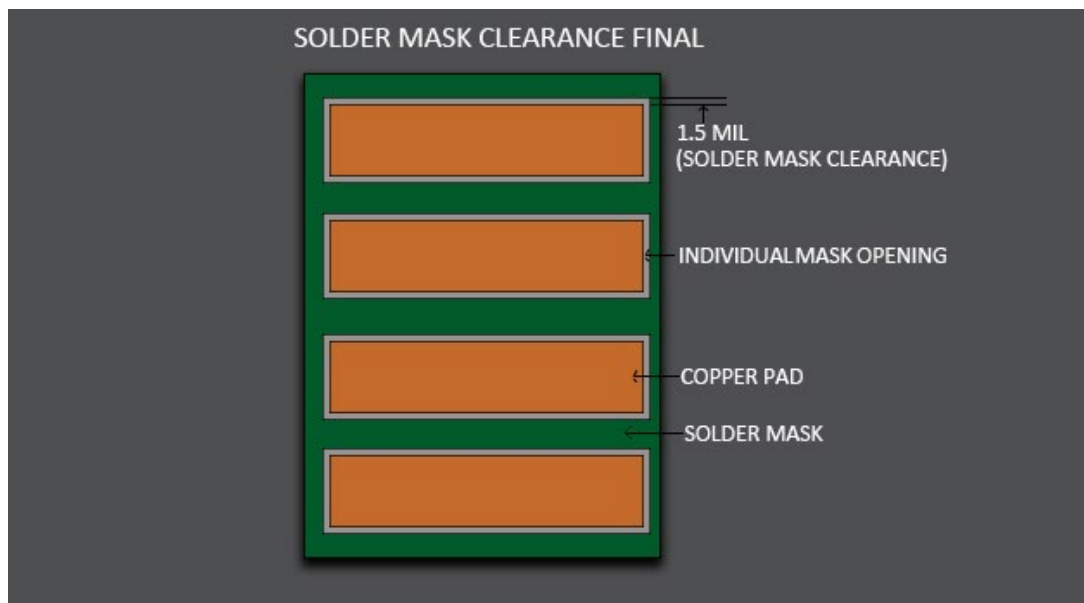
The color green represents the solder mask that protects circuit boards. Most of the surface of the PCB is primarily covered by the solder mask. Solder mask is basically a resin-based covering on the surface of the PCB, which is meant for the protection of your PCB. Protection from contamination and oxidation from external sources, such as manual handling, manufacturing processing, and environmental effects.

But why green? The color green is the most eye-soothing color. It makes the assembly process a little easy and less harmful to the eyes. That's it! Nowadays, solder mask can be of any color you want and it is based on the end product requirement, like white mask for LED lighting applications, black mask for LCD displays, etc.

7.1 Solder Mask Clearance

Ideally speaking, the function of the solder mask is to cover all traces, i.e. to isolate. But in practice, there exists a tolerance that decides how close the solder mask can be to surface elements. Therefore, the clearances in densely-packaged designs cannot be increased arbitrarily. The all-over clearance in general case should be half the conductor spacing width. Only when using fine conductive patterns under $100\mu\text{m}$ can the solder mask clearance be reduced to below $50\mu\text{m}$. This tolerance is known as solder mask clearance. Determining the right tolerance specifications is very significant since it impacts the board's manufacturability.

During PCB assembly, the components are connected by soldering method. To ensure a proper soldering outcome, areas of the board that require solder, like component pads and vias, must be isolated from the areas that do not. This isolation is achieved with solder masking. But there can be situations where it is not advisable or maybe not even possible to apply solder mask. For instance, places where heat sinks are used, where the separation between pads are very small when a component is too close to drilling holes. These areas, where the solder mask is not applied, are usually defined by solder mask clearance restrictions.



Solder mask clearance in a circuit board

The basic reason behind solder mask clearance restrictions is to provide enough spacing or solder dams between surface elements that receive solder. This is to prevent the formation of solder bridges.

Solder bridges may sound something positive, but it's not. It is an unnecessary connection between two surface elements. As the name suggests, it takes place when two or more pads become connected through an excessive application of solder, creating a bridge. Solder bridges hence can result in short circuits or burned components.



Snapshot of a solder bridge taken from CAM

There should, therefore, be a minimum distance between two elements to avoid such connections. Also, different colors in solder mask call for different minimum values.

Coming back to solder mask clearance, we can typically define it as a general isolation recommendation alongside specific details characterized by the kind of surface element(s) being isolated. Particular specifications apply to pads, which may be solder mask defined or non-solder mask defined, and drill holes, which may be plated through-holes or non-plated through-holes.

Let's look into some of the types of surface mask clearance specifications.

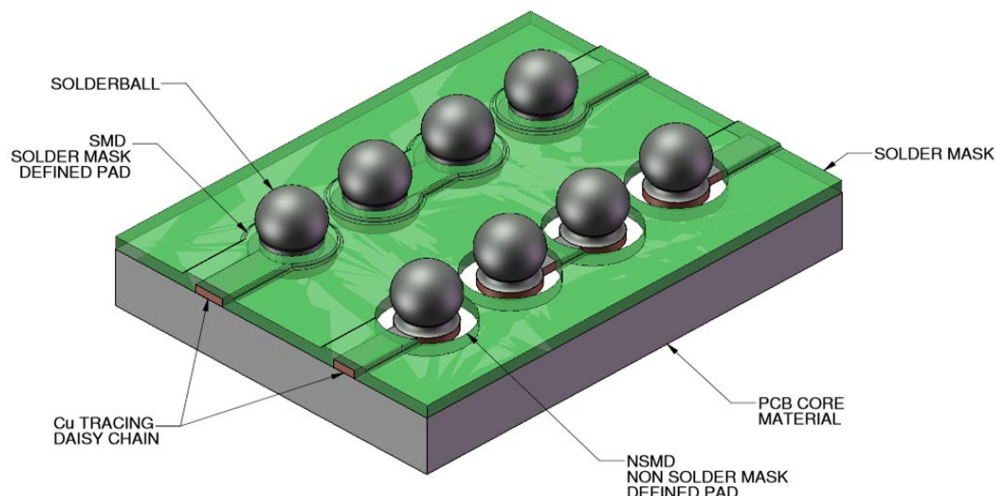
Drill holes:

- A plated through-hole (PTH) is a via that typically carries a signal or provides a ground return.
- A non-plated through-hole (NPTH) is usually a mounting hole that does not carry current.

To ensure the required quality and reliability, it is recommended that the vias in the solder mask have larger clearances than the hole diameter, especially the small vias. This is largely avoided as in some cases the vias remain sealed with mask and the chemical residues can rise onto the solder surface and result in poor solderability.

Pads:

- Solder mask defined pads are pads where the solder mask opening is smaller than the pad or a solder mask defined pad has a solder mask opening that is smaller than the copper pad, so that the solder mask defines the dimensions of the pad widely used in BGAs. Any increase or decrease in solder mask clearance varies the copper pad size.



- Non-solder mask defined pads involve a gap between the pad and the solder mask.

As for the solder mask process, fitting tolerances must be considered, so that the solder mask clearance should always be larger than the solder pads. This is the only way to ensure that the entire pad remains free of solder resist and optimum soldering results can be achieved.

Sometimes, we treat the vias with solder mask for serving different purposes in the board. For instance, we remove the mask clearances from the vias, hence forming a covered via. The main purpose is not to close the opening of a hole as it seems but rather covering the annular ring to prevent exposure to the elements and reduce accidental shorting or contact with the circuit.

To avoid solder bridging and improve the solder mask dams, another option is to encroach the mask opening onto the copper pad and or provide barrel relief (solder mask clearance = drill size + 3mils).

Again, a mask plugged via, (a.k.a. mask filled or non-conductive filled via), is also a type. Here, we ensure plugging and sealing of a via with mask and getting the annular ring covered. This process will avoid the solder from flowing down the intended pad to the via.

In our discussion above, we came across the phrase “solder mask opening”, this is also a significant check for solder mask. Let’s find out how!

7.2 Solder Mask Opening

The place without solder mask is known as solder mask opening. Solder mask opening is basically the removal of the paint layer on the circuit so that the circuit can be exposed to the tin. PCB opening is not a new concept. The most common one is probably the memory stick. The memory stick has gold fingers. This gold fingers here are used for plugging and play.

In some cases, the solder mask may be partially or completely absent around pads. This exposes more than the required copper. And moreover, it can result in solder bridges. We already know how bad solder bridges can be. They can result in short and burning of components. Again, unwanted copper exposure can also consequently lead to corrosion.



CAM snapshots of solder mask opening

PCB manufacturers prefer to have solder mask openings 1:1 with the copper pads which would be edited to suit the manufacturing process.

Green-colored PCBs might still dominate the PCB industry but other vibrant colors have also made their way into the market. Therefore, now solder mask opening has different recommended values for different colors.

Sierra's own set of capabilities:

Solder Mask Colors	Preferred Minimum Solder Mask Opening per side
Green	1.25 mils
Blue	1 mil
Black	1 mil
Red	1 mil
Others	2 mils

So, leaving a lot of clearance is the solution you think?

Remember, it is absolutely not advisable for you to just assume, the bigger the better! Since excessive mask clearance will come with its own set of problems. In this case, maybe the fab will be within your spec, but it can still manage to expose the ground plane right next to your pad. It will still be usable but you would need to be extra cautious about shorts. It's a really nasty trap.

7.3 Solder Mask Coverage or Expansion

Most PCB design software packages allow you to set the distance between the solder mask and surface elements for the entire board or for individual elements. This parameter is usually called the solder mask expansion and may be positive, zero or negative.

Positive solder mask expansion:

When a distance exists between the outer circumference of the pad and the end of the solder mask around it that is uncovered, that is positive solder mask expansion.

Zero solder mask expansion:

When there is no space or gap between where the pad ends and the solder mask begins.

Negative solder mask expansion:

When the solder mask covers a portion of the pad, that is negative solder mask expansion.



CAM snapshot showing solder mask coverage (copper exposure)

Why solder mask expansion?

Usually, it would be ideal to have zero solder mask expansion, which provides the required solder dam and maximum board protection. Therefore, suppose the solder mask expansion is zero, and everything is aligned just perfectly then the board would work fine. But in practice, things never align that perfectly. When your solder mask expansion is too small, then these tiny misalignments can cause the solder mask to partially or even completely overlap SMT pads and through-hole pads. The shift in the solder mask results in the mask on pad which in turn reduces the footprint of the component.

Practically, it is best to specify a minimum tolerance in solder mask expansion that is manufacturable based on your design needs.

Sierra's capabilities based on different colors are:

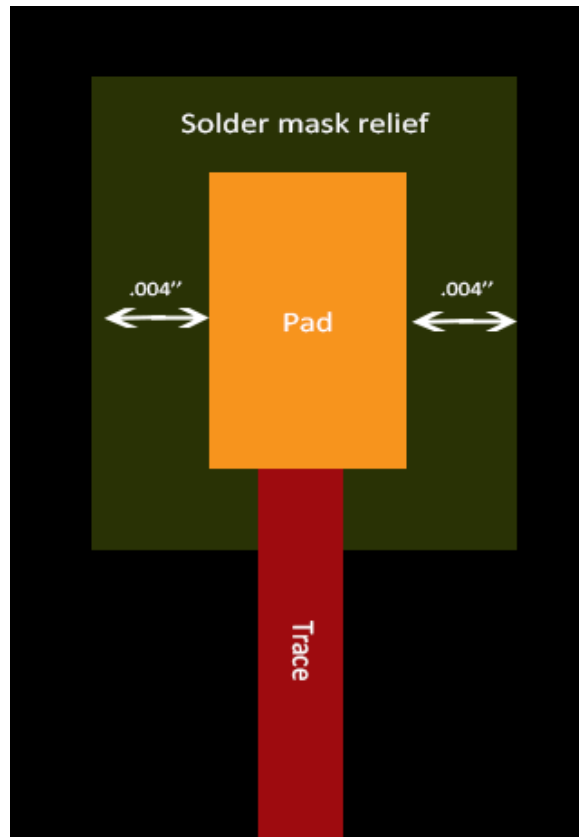
SOLDER MASK COVERS	TOLERANCE IN SOLDER MASK COVERAGE
Green	2 mils
Blue	2 mils
Black	2 mils
Red	2 mils
Others	2 mils

So, leaving a lot of clearance is the solution you think?

Remember, it is absolutely not advisable for you to just assume, the bigger the better! Since excessive mask clearance will come with its own set of problems. In this case, maybe the fab will be within your spec, but it can still manage to expose the ground plane right next to your pad. It will still be usable but you would need to be extra cautious about shorts. It's a really nasty trap.

7.4 Solder Mask Relief Or Solder Mask Web

The area on the surface of the PCB that does not have or doesn't require solder mask is called solder mask relief. These locations are usually surrounding SMT pads, through-hole pads, test points, and vias as a margin of error during fabrication. For instance, by default, design rules in many CADs check for a minimum opening of $8\mu\text{m}$ (0.315 mil) larger than the pad. This comes out to $4\mu\text{m}$ (0.1575 mil) relief per side.



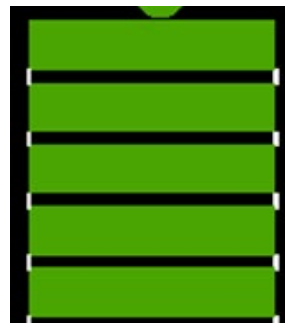
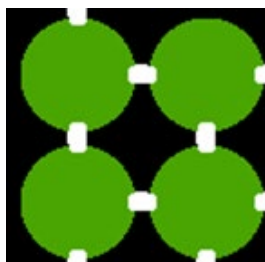
Solder mask relief or web in a PCB

The solder masked distance between two nearby reliefs is the solder mask web also known as the solder mask dam. There is a minimum manufacturable solder mask web measurement, and it depends on what color the mask is. Every color has its own individual chemical composition that affects its ability to adhere to the board below a particular area size.

Sierra's capabilities:

Solder Mask Colors	Tolerance in Solder Mask Webbing
Green	4 mils
Blue	5 mils
Black	5 mils
Red	4 mils
Others	5 mils

Sometimes, designs have large solder mask reliefs. That can end up creating a solder mask web smaller than licensed. In the worst-case scenario, this can lead to undesirable exposure of copper. Typically, this happens with traces, SMT pads or ground copper that have the minimum copper-to-copper spacing from other SMT pads.



CAM snapshots flaunting webbing between round pads and fine pitching

Solder mask web violations make poor solder mask cohesion and eventually this leads to delay in turn-out. In extreme cases, if not caught during DFM check, it can lead to a lot of hustle. With too little relief, SMT pads might get contaminated by solder mask. This might further make the board surface a little uneven and difficult to solder on. Again, with too much relief, the tight components can suffer solder bridging.

On the off chance that there is a test point via or electrical connection via excessively near the SMT pads, this eliminates the solder mask web completely and offers liquid solder a chance to leak through them during assembly, which can cause shorting or tombstoning on the other side of the board.

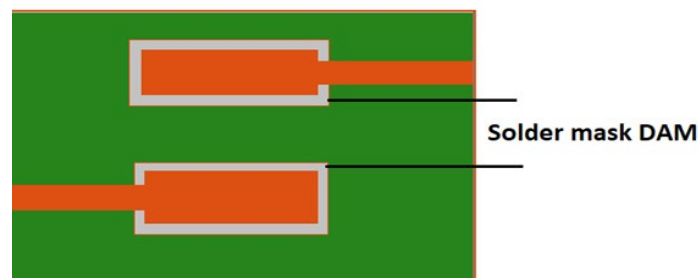
Tombstoning is a component imperfection that happens at the PCB assembly stage because of the solder's surface tension during reflow. Thus, one end of the component is withdrawn from a PCB's copper pad and lifts up vertically, looking like a tombstone. This circumstance came about in light of the fact that solder was flowing into the trace on the grounds that it was a similar size as the pad, and there was development during reflow. The outcome was a mismatched pad measure.

When setting up your design rules at the start of your project, we always recommend setting a relief between .003" to .008" for all of your SMT components. The solder mask color you choose to use is also going to influence how extensive your mask reliefs need to be.

7.5 Solder Mask Dam Or Spacing In Solder Mask

As already been discussed above, the solder masked distance between two nearby reliefs is the solder mask dam. To understand this a little better, think of it as a physical dam. What do dams do?

They can be utilized to gather water or for storage of water which can be equally disseminated between areas. Dams typically serve the purpose of holding water, while different structures, for example, floodgates or levees (otherwise called dikes) are utilized to oversee or avert water stream into explicit land areas. In like manner, on a board, where you don't have a dam keeping the solder contained on a pad, at that point it can very easily overflow onto another pad, causing an unintended solder bridge.



Solder mask dam or the spacing between two solder mask reliefs

As a general rule, we prescribe setting up solder mask dams between every one of the pads on your SMT components. These dams become progressively significant as your board gets smaller and more compact, particularly for integrated circuits (ICs). As an absolute minimum, this dam size ought to be kept up at 2 mils, or it could be too tough for your manufacturer to isolate solder between pads.

Moreover, there might be times when you realize that you need a solder mask dam between two solder mask pads, but you just don't have enough space. You might face this kind of problem when working with very tightly spaced pads. In such instances, you can use a solder mask defined pad which provides a solder mask relief that is the same size as the copper pad it is protecting.

7.6 Solder Mask Slivers

During the PCB manufacturing process, some narrow wedges of copper or solder mask are produced, they are called slivers. Slivers can be either conductive (copper) or non-conductive (solder mask) and can be avoided with a proper DFM review. Slivers can cause serious problems during the fabrication of circuit boards.

Traditionally, there are two ways of producing slivers. Firstly, when an extremely long, thin feature of the copper or solder mask is etched away. In some cases, this sliver detaches before it fully dissolves. Conductive slivers that break off can create an electrical short either at the fabricator or worse, in the field. These detached slivers might just float around in the chemical, and land on another board, potentially adding an unintended connection.

Another approach to produce slivers is to cut a section of the PCB design too narrowly or too deeply. Regardless of whether they are proposed to remain attached to the board if an etched area is thin enough or the etching is deep enough, a sliver of material can totally or mostly detach, either creating a floating sliver or a peeled off sliver. Both of these alternatives can have genuine negative ramifications for the circuit board's functions.



CAM snapshots showing copper slivers



Solder mask slivers as seen from CAM

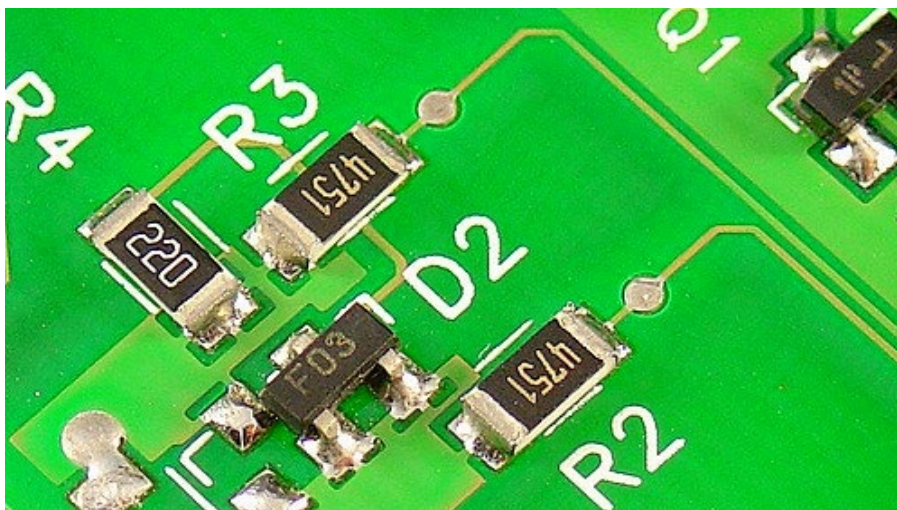
All the above check points for solder mask would be categorized as DFF or design for fabrication. All these checks will be done before we start fabricating a PCB.

7.7 Reflow Soldering

Component placement is one of the most important aspects of assembly. Once that is done, the PCB assembly moves into the reflow soldering oven, where all the electrical solder connections are formed between the components and the PCB. This is done by heating the assembly to a sufficient temperature.

This seems quite simple, right? So why do we need to have a check point for this? Well, a correct reflow profile is very important and DFM is the key to it. It ensures proper solder joints, even distribution of heat in the oven, hence, no damage to the parts or assembly due to excessive heat.

8 SILKSCREEN CHECKS



The first look of a PCB can put a question mark on any onlooker's face. Believe it or not, a PCB designer is no exception. Silkscreen will help readers understand the ins and outs of the PCBs, both literally and figuratively. For instance, it is easier to read and understand a programmer's complex code with structured annotation or a comment section. Silkscreen performs a similar function. The symbols or text on a PCB, which is printed with a permanent non-conductive ink, is commonly termed as a silkscreen. It is established by IPC standard to use permanent legend and marking ink for silkscreening process.

Silkscreen helps identify PCB components and their orientations, various test points, marks, etc. The key information, like identifiers, component labels and logos, can be conveyed via silkscreen layer to the user. It is important that silkscreen should be in a readable format for its effectiveness and usefulness. For quality inspection and PCB assembly processes, silkscreen is highly recommended as well. It is the responsibility of every PCB manufacturer to employ silkscreen guidelines as part of their DFM checklist.

Materials used for silkscreen include epoxy resin, PF resin (XPC, FR1, FR2), polyester resin, etc. However, the selection of material varies as per application of a PCB or its operating conditions. Defects occurring due to the selection of silkscreen materials is almost unheard-of, except for some cases involving high-reflow temperatures that require RoHS compliant soldering. Most of the errors are incurred during PCB designing. It is important to lay out a few guidelines for designers to avoid silkscreen errors.

Design consideration for silkscreen:

- Designers should avoid overlapping component reference designator marks. These component reference marks are essential during PCB assembly and troubleshooting processes. It is preferred that component marking should be next to the component itself.
- Designers should avoid printing silkscreen over via holes, even though there is limited space for it. In some cases, designers can print on tented via; as these vias are covered with solder mask. However, these holes are not allowed to be used as a test point. So, if space is available next to the component, it should be utilized completely.
- Designers are not supposed to put component reference marks under PCB components. These marks will be completely invisible after component placement. Additionally, reference marks help us understand the polarity of the component and are a great help for the PCB assembly team.

- Designers should define the polarity for the components such as inductors and capacitors. These polarity marks need to be printed beside component reference marks.
- Designers should place measurement marks that include the number of pins of the IC or the number of lines on the microchip.
- Designers should opt for standard colors and larger shapes to make the silkscreen easier to read, while considering all other parameters that are discussed.
- Designers need to keep in mind tolerances during machine printing processes to avoid common printing errors.

Here are a few silkscreen checks that we follow at Sierra Circuits:

8.1 Silkscreen To Mask Spacing

The ink used for silkscreen formation should not be printed over pads or on the PCB surface. If the ink is applied over pads, there is a possibility that it will be melted into the solder joint. Mostly, a silkscreen layer is placed over the solder mask. The designers often forget to keep the component outlines away from the pins, which creates more confusion. It is the responsibility of the designer to check whether the silkscreen graphic is suitable for the design layout of the board.

8.2 Silkscreen To Copper Spacing

Copper spacing is defined as the minimum air gap between any two adjacent copper features or traces. Silkscreen should not be overprinted, as it can lead to several problems during soldering, assembly, and inspection tests. The silkscreen checklist will detect an overprinted silkscreen on copper features; it will highlight the marking print at this location. The marking print is usually automatically clipped as minimum spacing requirement.

8.3 Silkscreen To Hole Spacing And Rout Spacing

Designers must place silkscreen outlines within defined boundaries to avoid overlapping with minimum hole spacing and profile spacing. While implementing silkscreen outlines, designers need to ensure that the silkscreen should not overlay the maximum component body.

8.4 Line Width And Text Height

There is no recognized standard for deciding the line width and text height. Sierra Circuits can print lines with a minimum of 4 mils. Additionally, higher line width and text height will be fine, considering it meets all of the above silkscreen checklist parameters. We also recommend using a minimum text height of 25 mils, for a good readability. It is highly recommended for PCB designers as well as manufacturers not to place silkscreen text on top of the copper layer without a solder mask layer.

Silkscreen Checks	Recommended (mils)
Silkscreen to Mask Spacing	4
Silkscreen to Copper Spacing	6
Text Height	25
Silkscreen to Hole Spacing	Minimum 8
Silkscreen to Rout Spacing	10
Line Width	4

9 PCB MANUFACTURING TOLERANCES

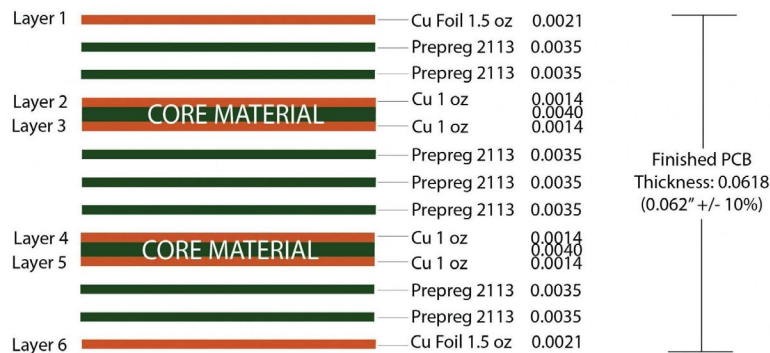
While placing an order, you convey your PCB requirements to your manufacturer and expect your boards to be as per your specifications. However, there is always a certain tolerance that's added to your specs. This is due to variations in the operating environment, equipment, and material.

The acceptable deviation from the nominal values without affecting the overall functionality of a PCB is called tolerance. Usually, tolerance ranges between a maximum and minimum range like $\pm 10\%$, $\pm 1\text{mm}$, etc.

9.1 Board thickness tolerances

31 mils, 62 mils, 93 mils, and 125 mils are the industry standards for PCB thickness. But the final boards come with a minute thickness variation. This variation depends on factors like material, copper thickness, operating environment, and layer count. The standard board thickness tolerances are mentioned below.

Thickness	Standard board thickness tolerance
Boards thickness - 31 mils and above	$\pm 10\%$
Boards thickness - lower than 31 mils	$\pm 0.003''$



Tolerance in PCB thickness

9.2 Copper thickness tolerances

Usually, we measure the copper thickness in ounces (oz). This means we are spreading **1oz** of copper (28.35 g) over a 1 square foot (0.093 sq.m) surface area. **1oz** copper thickness will be approximately **1.4 mils**.

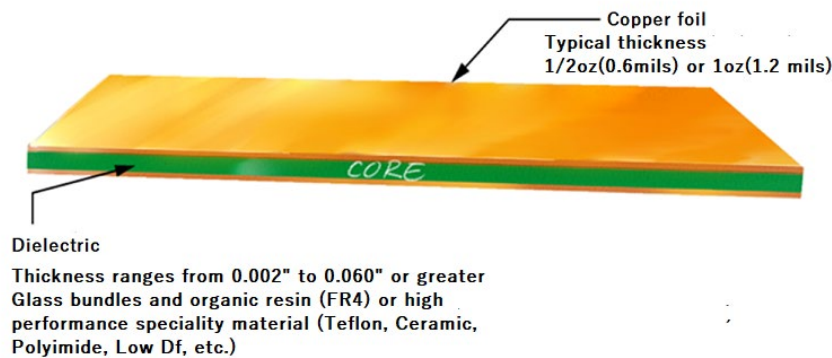
In the below table, the equivalent of copper weight in oz and thickness in mils are depicted.

Copper weight (in oz)	Copper thickness (in mils)
1	1.4
2	2.8
3	4.2
4	5.6

The major factors impacting the copper thickness on board are material and manufacturing processes.

9.2.1 Start copper thickness

IPC- 4562 standard allows a maximum of **10%** reduction in start copper of the base material.



Base material copper thickness

9.2.2 End copper thickness

- Inner layer processing (without via):

If the inner layer has no plated via, then the copper on the core is printed and etched. Hence, you can define the inner layer copper thickness according to the base copper thickness. Based on the start copper, the minimum finished copper thickness after processing is mentioned below.

Start Copper (in μm)	Minimum finished copper thickness as per IPC-A-600j-class 2 (in μm)
12	9.3
18	11.4
35	24.9
70	55.7
105	86.6

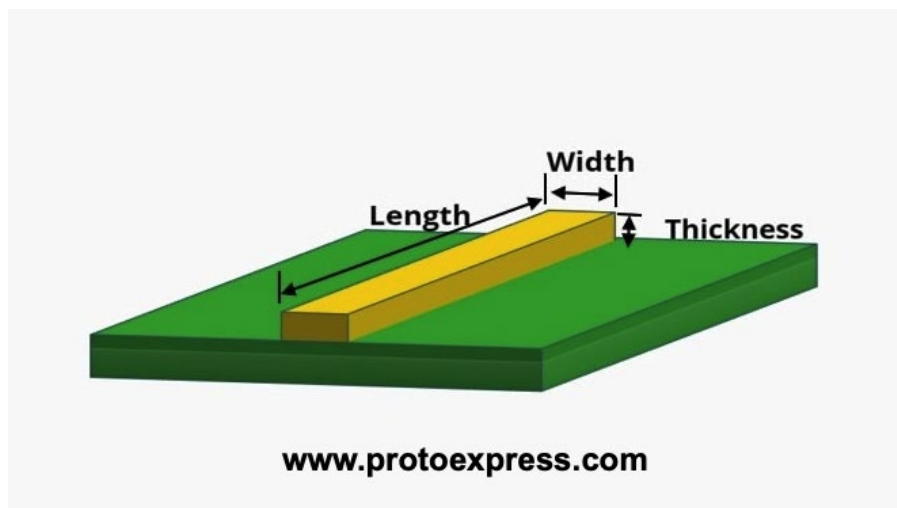
- **Outer-layer and plated holes:**

For layers with buried, blind, or plated through holes, the barrel should be plated with a minimum thickness of **18 μm** as per the IPC-A-600 standard.

Similarly, manufacturers deposit a copper layer on the board during the outer layer preparation. Copper balance and distribution are essential in depositing a uniform copper layer. The cleaning and etching process will also reduce the copper thickness. Based on the start copper, the minimum finished copper thickness after plating and processing is mentioned below.

Industry defined copper thickness (in μm)	Minimum finished copper thickness as per IPC-A-600j-class 2 (in μm)
30	29.3
35	33.4
70	47.9
105	78.7
140	108.6

9.3 Copper trace width tolerances



Copper trace width

Trace width influences the current carrying capacity, controlled impedance, and also signal integrity of a printed circuit board. So, maintaining the correct trace width is essential.

However, variations in imaging, etching, copper balance, and base copper thickness can impact the width of the trace.

Also, the trace width and the isolation gap are interlinked. If the trace width decreases, then the isolation gap increases. Hence, **the tolerances of conductor width and isolation gap are the same**. IPC A – 600 allows a tolerance of **20%** on the final copper trace width.

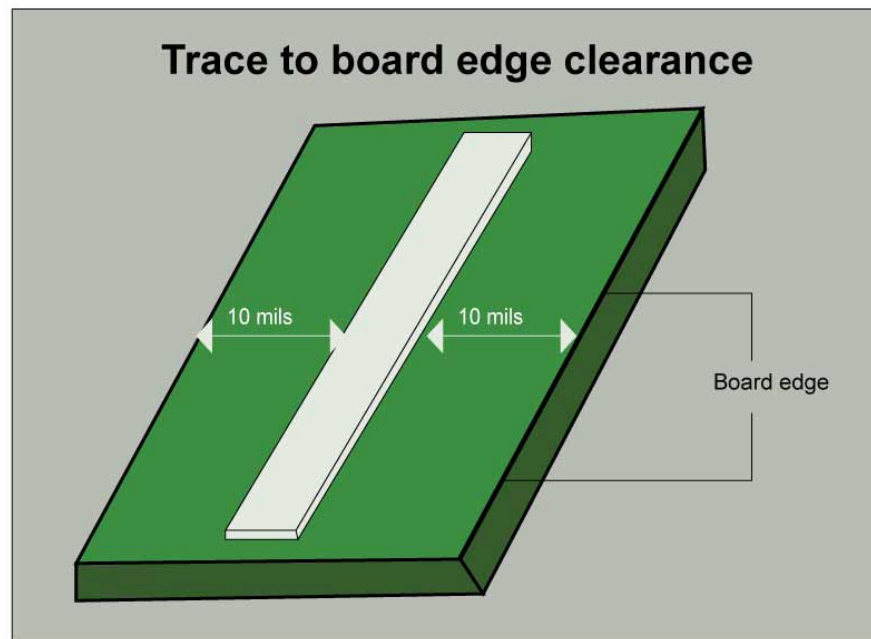
Based on the copper weight, the minimum line width required for the proper functioning of PCB is shown below.

Start Copper	Minimum copper trace width on the outer layer (in mils)	Minimum copper trace width on the inner layer (in mils)
5 microns	2	2
9 microns	3	2.5
½ oz	4	3
1 oz	6	4
2 oz	8	6
3 oz	12	7
4 oz	14	8

9.4 Copper trace spacing tolerances

9.4.1 Trace to edge spacing

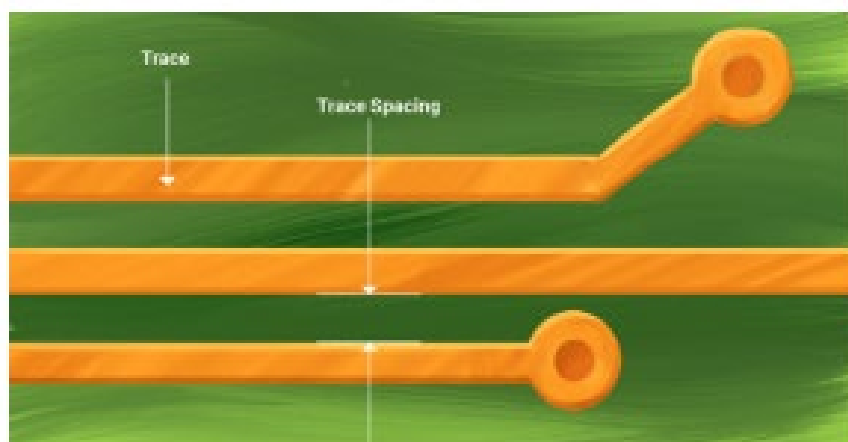
This is the distance between the conductor and the edge of the board. If you do not maintain a minimum trace-to-edge spacing, the outer conductor can get exposed, making it susceptible to corrosion. Additionally, the trace can get partially chipped off during mechanical routing (depanelization).



Copper trace to edge spacing

9.4.3 Trace-to-trace-spacing

As you know, it is essential to maintain a minimum distance between two conductors to avoid flashovers and crosstalk between the conductors. Things that influence the conductor spacing are the applied voltage and the type of assembly.



Copper trace to trace spacing

Based on the copper weight, the minimum spacing between the conductors on the outer layer and inner layers of PCB can be defined as below.

Start copper	Minimum spacing between the conductors on the outer layer (in mils)	Minimum spacing between the conductors on the inner layer (in mils)
5 microns	3	2
9 microns	3	2.5
½ oz	4	2.25
1 oz	6	4.25
2 oz	8	6.25
3 oz	12	8
4 oz	14	10

9.5 Drilling tolerances



PCB drilling

Sometimes, the hole/via size specified in your design may not reflect in the manufactured board because of the following reasons:

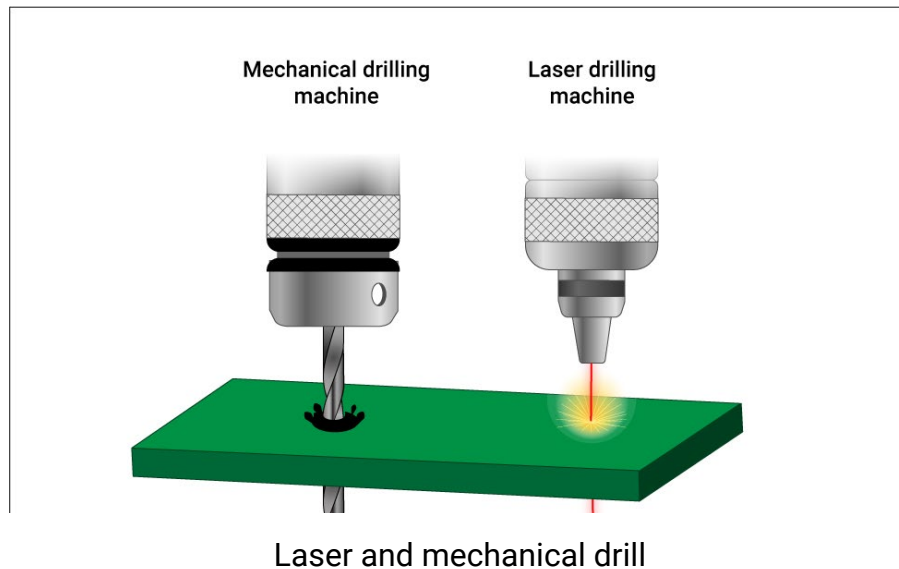
- **Drill bit size:** The drill bit used may vary in size due to its own tolerance or wear. Also, the drill size comes in multiples of 0.05, so drilling the exact hole of 0.37 may not be possible.
- **Drill wander:** When the drilling machine is slightly off from its actual placement, it is called a drill wander. A maximum allowed tolerance for drilling is ± 2 mils.
- **Copper plating:** For plated holes, the deposition of the copper impacts the drilled hole size, which in turn depends on copper balance. If a hole/via is placed in a full copper area, copper plating on the barrel will be thinner (electroless and electroplating), making the hole diameter larger. On the other hand, the copper plating will be thicker when a hole/via is placed in an isolated area. The standard tolerance for the plated hole and the non-plated hole is ± 3 mils.
- **Drill to copper:** This is the distance between the drilled hole edge to the nearest copper feature. Maintaining a minimum tolerance in the drill to copper spacing is essential as it could disrupt the circuit.

Creating the hole size close to your specification depends on the manufacturer's capability. The following are Sierra Circuits drilling tolerances.

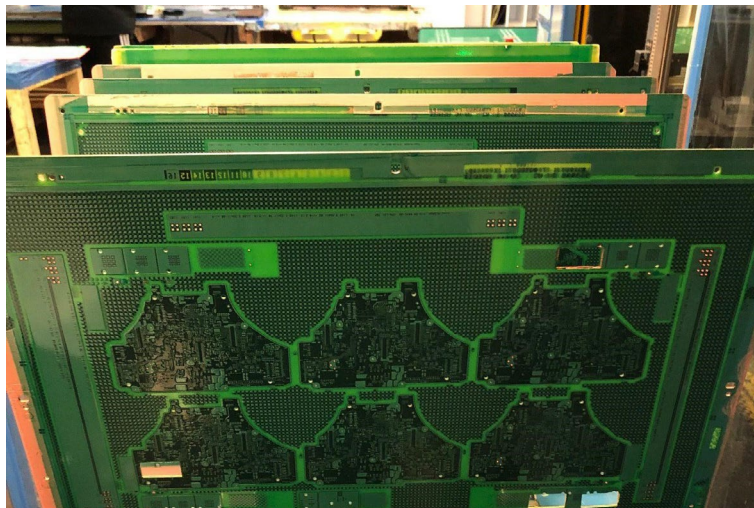
Features	Tolerance
Tolerance for PTH and NPTH drills	± 3 mils (0.003")
Drill to copper	Min. 8 mils (0.008")
Drilled hole registration tolerance	1 mil (0.001")
Drill to drill clearance	6 mils (0.006")
Drill (hole) to the board edge	6 mils (0.006")
Laser hole registration tolerances	5 mils (0.005")

9.6 Annular ring tolerance

As discussed earlier, the drilled holes don't exactly match your specification. The CAM tool considers the specified drill size mentioned in your design and not the finished hole size with tolerance. You can expect a drill tolerance of **2 mils** on a finished hole, so make sure that the annular ring is more than **2 mils for laser drilled holes** and **4 mils for mechanically drilled holes**. This will help avoid the discontinuity in annular rings.



9.7 Solder mask feature tolerances



Solder mask layer

It is essential to have proper clearance between the solder mask and the surface elements like pads, footprints, test points, etc., to avoid solder bridges.

But during the application of the solder mask, it can expand and overflow onto the pad, and this can cause difficulties during the assembly process. Thus, fabricators maintain a minimum tolerance in solder mask coverage. We also provide a solder mask relief or a web for this purpose.

Sierra's capabilities based on different colors of solder masks are mentioned below.

Solder mask covers	Tolerance in solder mask coverage (in mils)	Tolerance in solder mask webbing (in mils)
Green	2	4
Blue	2	5
Black	2	5
Red	2	4
Others	2	5

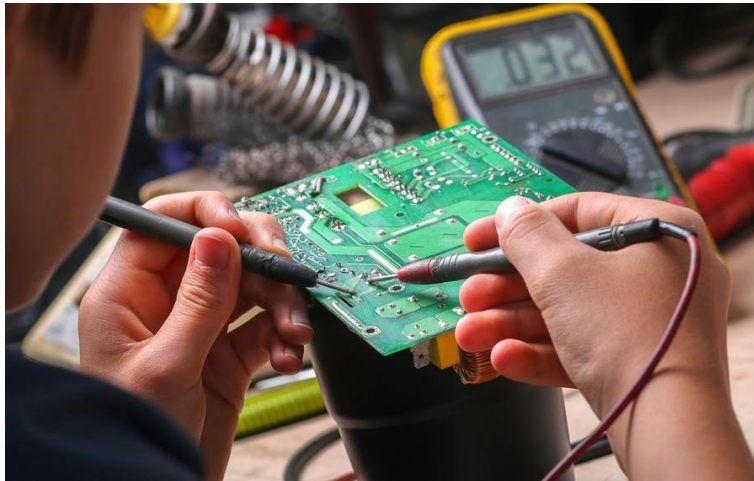
Other solder mask tolerance can occur due to the improper registration of the solder layer with the rest of the layers.

Product Features	Solder mask registration tolerance
Standard fab	0.002"
Advanced fab	0.001"
Micro fab	0.001"

9.8 Layer-to-layer registration tolerances

Getting a hundred percent accuracy in the alignment of all layers is challenging. Manufacturers take many precautions like fiducial holes, registration holes, optical alignment, direct imaging, etc., to minimize the errors in the registration. However, the layer alignment can slightly change in dimension during the pressing and curing cycles. Hence, a **maximum of 50 μm tolerance is acceptable in the layer-to-layer registration.**

9.9 Controlled impedance tolerances



Controlled impedance

If the trace impedance varies from point to point, it creates reflection causing the signal to distort. Hence, maintaining a uniform impedance is crucial. You can do this by establishing a uniform trace width or by varying the dielectric properties of the selected substrate. The standard tolerance for controlled impedance is **+/-10% tolerance.**

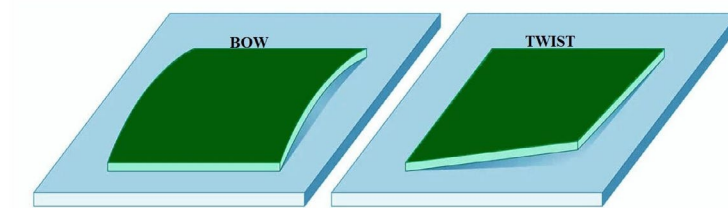
Controlled impedance tolerances at Sierra Circuits:

Product features	Controlled impedance tolerance
Standard fab	10%
Advanced fab	5%
Micro fab	5%

9.10 Bow and twist tolerances

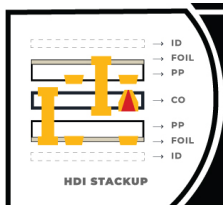
The manufactured circuit board must be flat to facilitate the assembly and final installation process. However, during the preparation of stack-up, if there is an asymmetry in layers or the copper distribution is imbalanced, it can cause a bend in the fabricated board. This bend will be in the form of a bow or twist.

In a twist, one of the board's corners will deform and be off the plane from the other three corners. In a bow, all four corners of the board will be on a single plane, but there will be a cylindrical/spherical curve in the middle, as shown in the image.



Bow and twist in the PCB

Feature	Tolerance (IPC 2422-1 and IPC 2422-2)
Max. bow and twist with SMD	0.75%
Max. bow and twist without SMD	1.5%



PCB Stackup Designer

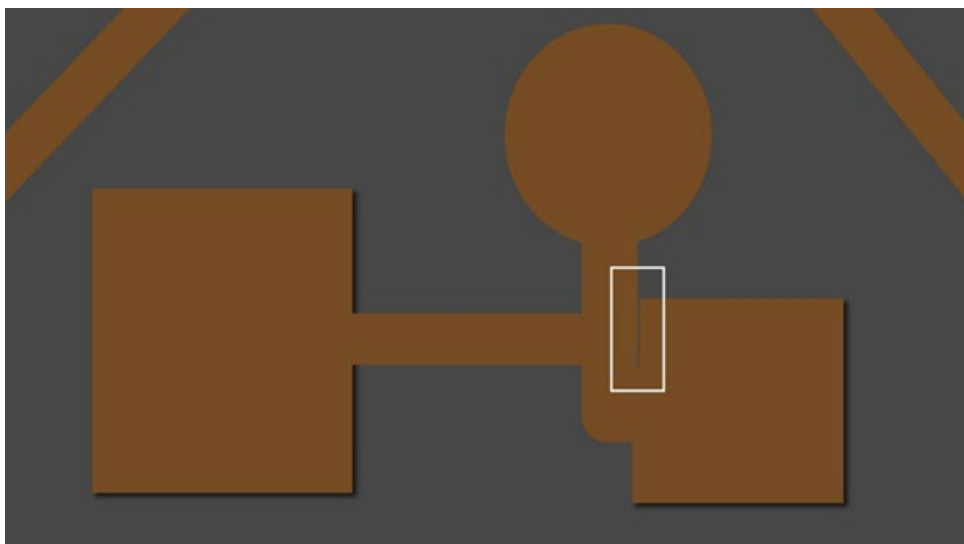
Try Now

10 OUTPUTTING YOUR DATA/ POLARITY!

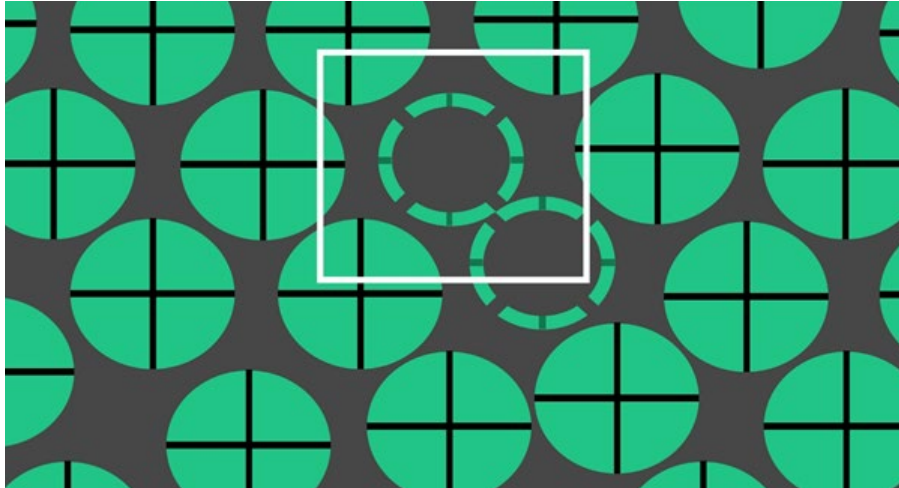
- o Annular ring waiver when called out on fab drawing or IPC Class 3 annular ring waiver
- o Fab drawing requirements not matching with the data – example: Fab calls out cutouts, data does not show cutouts
- o Waiver on location of vendor markings as against called out in the customer documents
- o Missing or extra solder mask clearances
- o Solder mask clearances exposing traces, copper pour
- o Trace width/spacing not supporting the copper weight
- o Waiver for lesser copper weight
- o Stubs in copper layers (stubs are features that are connected on one side and unterminated on the other side)
- o For online orders, the data not meeting the online specs (example: Multi part data, slots, cutouts more than 3 numbers, etc.)
- o Close holes (distance between edge of the hole to edge of another hole is less than 7 mils)
- o Holes very close to board profile
- o Board thickness called out on fab drawing cannot be met as given in the stack-up drawing

10.1 Designer Tips for Signal checks

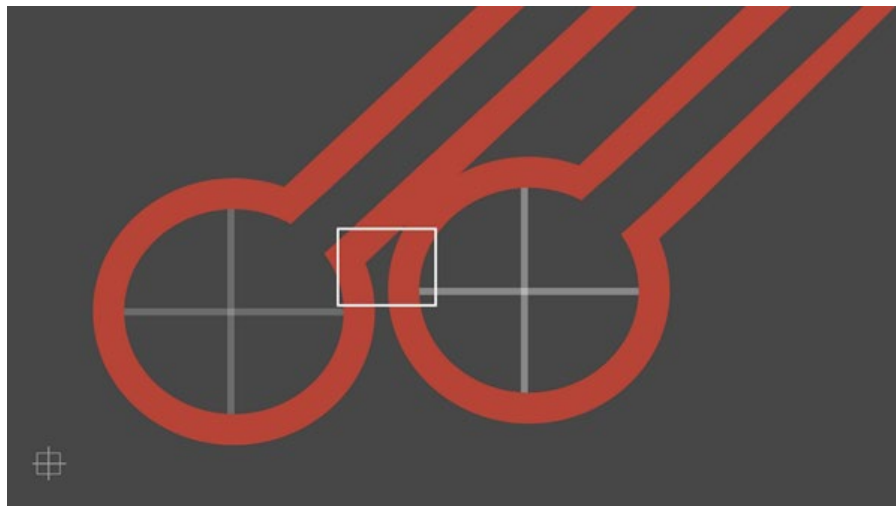
Avoid acid traps: Designs that incorporate acute angles will attract acid concentration in that region. This might lead to over-etched traces and will result in open circuits.



Starved thermal: Thermals allow pads to dissipate heat. Starved thermals might yield undesired results during the soldering process.

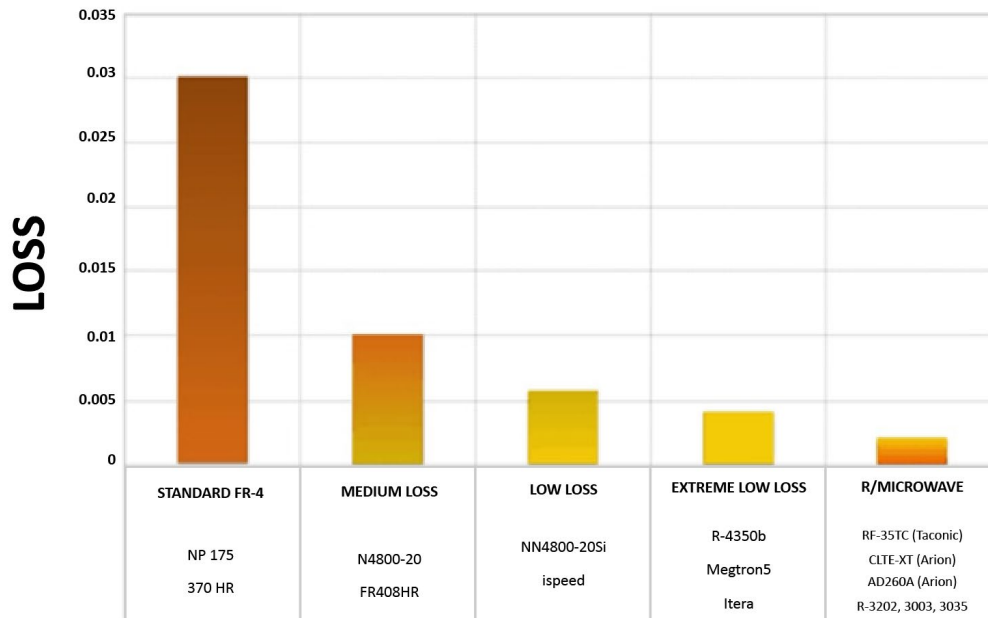


Copper slivers: Small copper slivers might detach themselves during assembly, float around during soldering and reconnect themselves anywhere on the PCB. Narrow wedges of copper or solder mask that can peel off and either reconnect to other pieces of copper or expose copper that should be covered with solder mask.

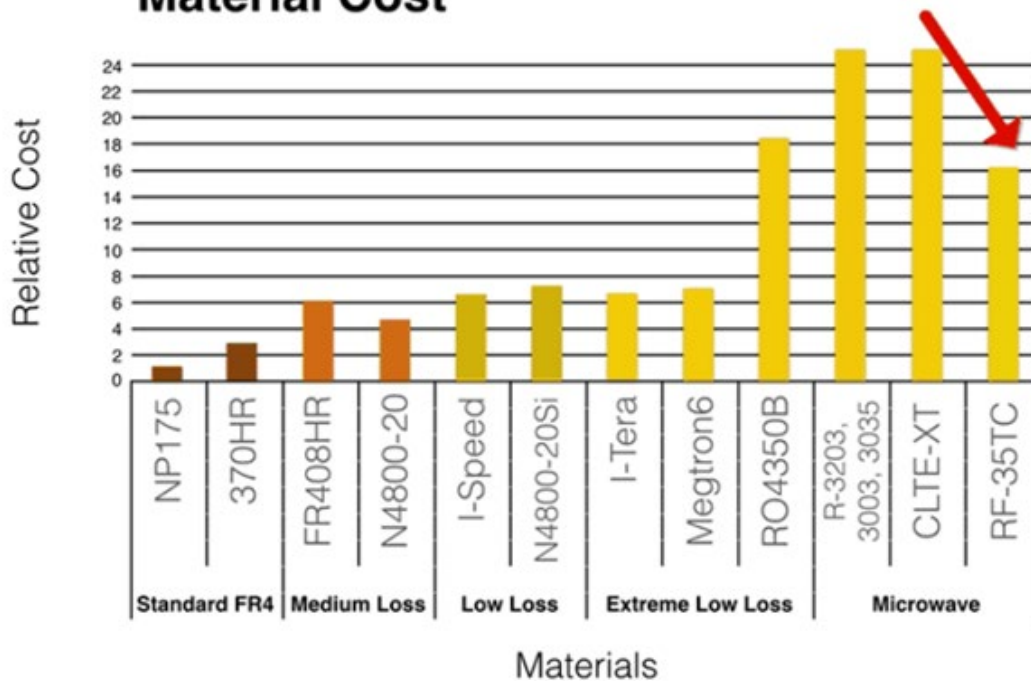


Missing clearance pads on planes: Pins that are missing a clearance pad will connect to a plane layer. If clearance pads are missing from all plane layers for the pin, it will connect all of the voltage planes.

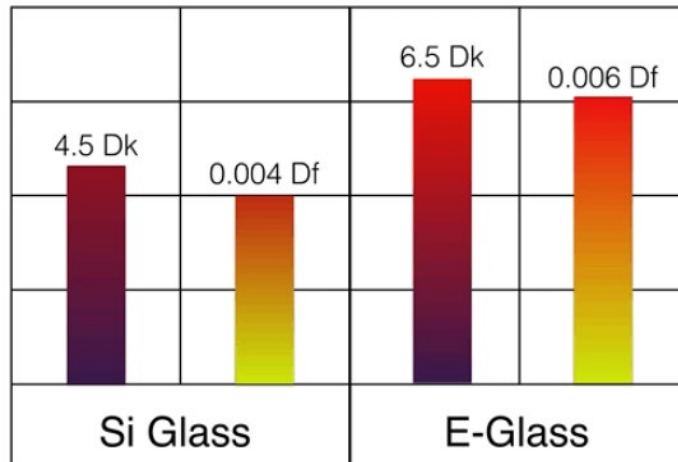
The 5 Basic PCB Material Categories



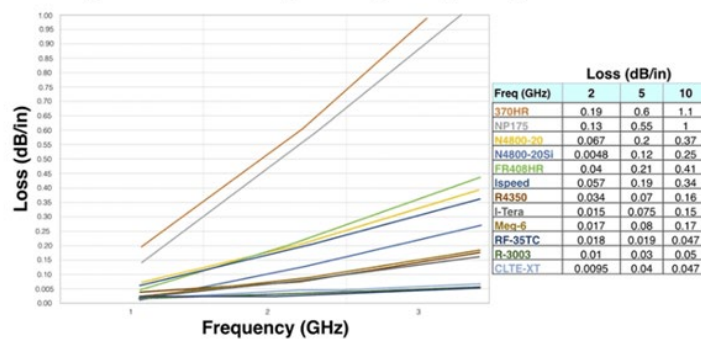
Material Cost



Si Glass versus E-Glass at 5 Ghz



Signal Loss and Operating Frequency



Things to look out for!

Annular ring: You can specify if you want our Better DFM tool (learn more in the Better DFM section) to test against tangency or breakout or some specified annular ring minimum width.

Check your netlist with IPC-D-356A and IPC-D-356.

We provide a full netlist compare. If you load your IPC-356 format netlist with your files, we will create a netlist from your Gerber files and compare it with your IPC netlist. Check if there are any unintentional shorts and opens.

If you are using multiple drill files, indicate which holes are plated or non-plated, and which layers they go through.

11 BETTER DFM

Sierra Circuits understands numerous issues faced by PCB designers, while following and implementing DFM checklists. We have decided to simplify these complex issues by developing a highly reliable and sophisticated DFM tool. Better DFM is an online design tool to check the manufacturability of an electronic circuit design. The primary purpose of the Better DFM tool includes simplifying the product designing and improving functional yield of the electronic circuit, thus making it easier to manufacture a PCB. The use of design for manufacturability tools has become common practice among PCB manufacturers over the past few years. However, the rising complexity level associated with PCBs and increasing number of manufacturing technologies have driven a demand for high-end design for manufacturing tools. Better DFM not only describes but also simplifies the process of designing, thus limiting the overall manufacturing cost.

The Better DFM tool is operated on PCB design files, like Gerber file format. The tool provides in-depth insights on design issues in PCB design files. Better DFM is capable of identifying design inaccuracies. For instance, a 6-mil trace will be identified and reported for correction, if you mentioned that your traces are supposed to be 5 mils.

The Better DFM tool strictly follows core manufacturability rules along with several design specific rules provided by Sierra. We also offer customers the opportunity to customize specific design parameters, as per their requirements.

The design rules are determined by comparing the full netlist with your files, which are set by our industry experts. Better DFM allows users to load their IPC-356 format netlist along with Gerber files. The Better DFM tool will create a netlist and compare it with the IPC netlist. Any errors in design nets, such as any shorts and opens, are identified in a report.

Better DFM offers accurate analysis by determining the exact location of the particular issue with detailed graphics. Thus, users can easily point out design faults and correct them accordingly. Several drill files can be added into Better DFM. This allows users to assign holes that are to be plated or non-plated. The tool also showcases similarity between PCB layers. A report is submitted to the user in PDF format for every Gerber files. The Better DFM tool is capable of fixing any alignment issues that may occur.

11.1 Operation And Design Characteristics

Better DFM is operated by three simple steps:

1. The first step is to log in our website:

LOGIN

LOG IN

2. The second step is to add up the required design specifications:

Quote Help

Hover over items to get quick help. To freeze this click on an item when hovering

Unfreeze Pane

Outer Layer Finish Copper: Number of ounces of copper per square foot on outer layers. Specify this as "finished" copper weight. 1 oz is most commonly used weight. Note that when you choose 1oz finished copper from the list it typically means we will start with 0.5 oz copper foil and plate up 1 oz, to end up with about 1.5 oz actual finished copper.

Enter specifications for your DFM

Part Number

Revision

Layers

Are your boards in Arrays? ☒ Yes ☐ No

How many boards per array?

Array Dimension (inches) X Y

Individual Board Dimensions (inches) X Y

ITAR? ☐ Yes ☒ No

Surface Finish

Minimum Trace (Outer layer)

Minimum Space (Outer layer)

Minimum Trace (Inner layer)

Minimum Space (Inner layer)

Outer Layer Finish Copper

Inner Copper

Minimum Hole Size

0.5 oz Inners

1 oz Inners

2 oz Inners

3 oz Inners

Not Applicable

Upload File

Browse...

Show Advanced Options

☒ I only need Better DFM report, no need to give me Quote

☐ I need Better DFM report and ALSO a Quote with it

Run Better DFM!

3. The Third step is to upload your Gerber files:

Better DFM - Experience the Difference

<u>TopPaste.GBX</u> /	Top Solder Paste	Positive	0
<u>TopPrint.GBX</u> /	Top Silkscreen	Positive	0
<u>TopSMask.GBX</u> /	Top Soldermask	Positive	0
<u>Top.GBX</u> /	Top Copper Layer(Signal)	Positive	1
<u>Bottom.GBX</u> /	Bottom Copper Layer(Mixed)	Positive	2
<u>BotSMask.GBX</u> /	Bottom Soldermask	Positive	0
<u>BotPrint.GBX</u> /	Bottom Silkscreen	Positive	0
<u>Drill_Plated_NC</u>	NC Drill	Positive	0

Click on magnifying glass to view file to help with assignment

You must assign Drill files

Assign Polarity here

Assign Layer# here

Better DFM helps you identify critical design faults by presenting a full-fledged report. The tool first unzips your Gerber files and ask you to verify the design specs. However, the following parameters are considered to be taken into account before operating Better DFM:

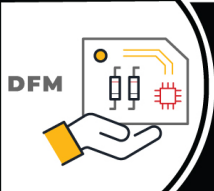
1. Determine the type of layer to be assigned while adding the design specifications. For instance, sm1.gbr has to be identified as solder mask top layer and rotator1.gbr has to be identified as Layer 1.
2. Add the required drill information in order to identify which holes are vias, plated or non-plated.
3. Make sure Gerber packages are not corrupted or missing.
4. In some cases, Gerber files have not been assigned correctly and users must assign copper layers as top layers on the layer assignment screen.
5. Provide the entire board outline as crop marks are not taken into account. The board outline must be on one of the layers, preferably on the solder mask layer.
6. Align layers in accordance with the circuit design.
7. Check if the drill file is corrupt or incomplete.
8. Drill holes are not supposed to lie outside or at the board outline. Check for NO drill holes.
9. Gerber file data is expected to be in 274x format. Additionally, Gerber files are supposed to be 1:1 of its true size.
10. Enter the actual dimensions of the board.

A detailed report is generated consisting of every design faults and explaining in detail.

The following example showcases content in the Better DFM report:

```
Sierra Circuits, Inc.  
Better DFM Netlist Compare Summary  
www.protoexpress.com/betterdfm  
  
PN: TES22323  
Rev: 21  
File: R97645X-set1.zip  
Better DFM Number: afvbdxg-3356  
  
DATE : 17 Mar 2010  
TIME : 16:45:58  
-----  
HOW TO INTERPRET THIS REPORT  
  
In the Shorted Nets section it shows customer's CAD netlists that are shorted.  
The Shorted Nets are displayed with the same Item number in the table.  
  
In the Open Nets section it shows customer's CAD netlists that are open.  
The individual disconnected Nets are displayed with the same Item number in the table.  
  
ALSO SEE TIPS & HINTS AT BOTTOM OF REPORT.  
-----  
  
SHORTED NETS  
  
ITEM    CAD NET                GERBER NET  
-----  
Total : 0  
-----  
  
OPEN NETS  
  
ITEM    CAD NET                GERBER NET  
-----  
1        0V(1)                NET00276  
1        "                    NET00314  
1        "                    NET00303  
1        "                    NET00315  
1        "                    NET00264  
1        "                    NET00277  
1        "                    NET00317  
1        "                    NET00308  
  
2        0V(2)                NET00295  
2        "                    NET00297  
2        "                    NET00305  
2        "                    NET00304  
  
3        3.3V                NET00145  
3        "                    NET00183  
3        "                    NET00185  
3        "                    NET00333  
3        "                    NET00062  
3        "                    NET00332  
3        "                    NET00061  
3        "                    NET00156  
3        "                    NET00158  
3        "                    NET00334  
3        "                    NET00151  
3        "                    NET00336  
3        "                    NET00174
```

Better DFM is capable of identifying key issues that affect manufacturability, thus helps save your money. Better DFM can identify both critical and common manufacturing problems existing in your Gerber files. The tool pinpoints design inaccuracies and fixes any violations.

**Better DFM**

Try Now

SPECIAL THANKS!

A big shout out to the Sierra team who worked hard to make this DFM handbook happen!

Our wonderful writers:

Rahul Shashikanth
Taisha Chattopadhyay
Pankaj Shrotre

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