8-Bit, 8-Channel Sampling ANALOG-TO-DIGITAL CONVERTER with I²C™ Interface

FEATURES

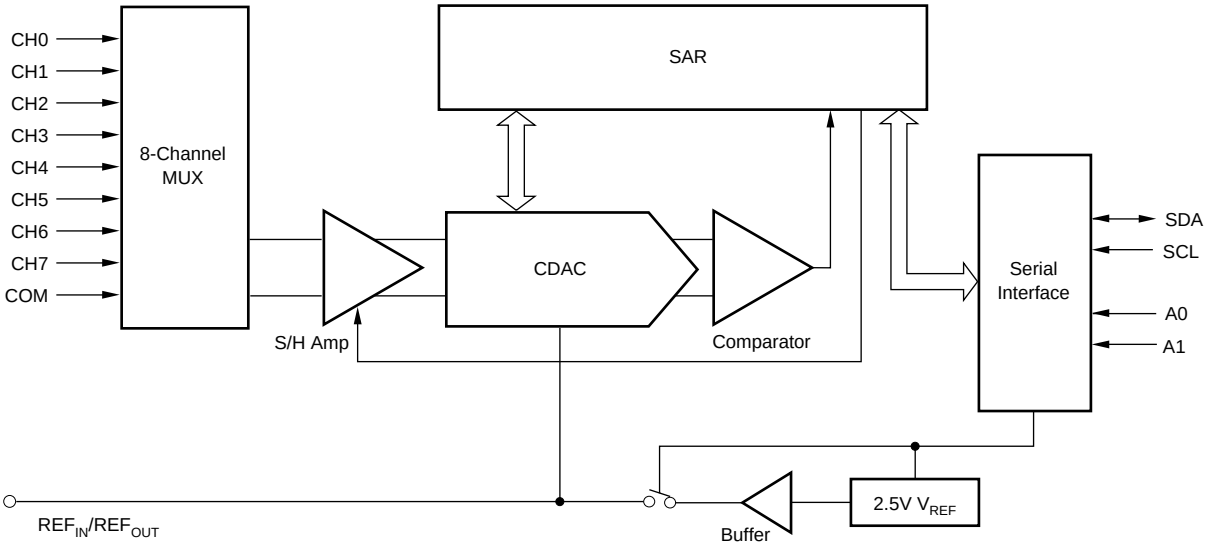
- 70kHz SAMPLING RATE
- ±0.5LSB INL/DNL
- 8 BITS NO MISSING CODES
- 4 DIFFERENTIAL/8 SINGLE-ENDED INPUTS
- 2.7V TO 5V OPERATION
- BUILT-IN 2.5V REFERENCE/BUFFER
- SUPPORTS ALL THREE I²C MODES: Standard, Fast, and High-Speed
- LOW POWER:
  180μW (Standard Mode)
  300μW (Fast Mode)
  675μW (High-Speed Mode)
- DIRECT PIN COMPATIBLE WITH ADS7828
- TSSOP-16 PACKAGE

APPLICATIONS

- VOLTAGE-SUPPLY MONITORING
- ISOLATED DATA ACQUISITION
- TRANSDUCER INTERFACE
- BATTERY-OPERATED SYSTEMS
- REMOTE DATA ACQUISITION

DESCRIPTION

The ADS7830 is a single-supply, low-power, 8-bit data acquisition device that features a serial I²C interface and an 8-channel multiplexer. The Analog-to-Digital (A/D) converter features a sample-and-hold amplifier and internal, asynchronous clock. The combination of an I²C serial, 2-wire interface and micropower consumption makes the ADS7830 ideal for applications requiring the A/D converter to be close to the input source in remote locations and for applications requiring isolation. The ADS7830 is available in a TSSOP-16 package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

$+V_{DD}$ to GND	–0.3V to +6V
Digital Input Voltage to GND	–0.3V to $+V_{DD}$ + 0.3V
Operating Temperature Range	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature (T_J max)	+150°C
TSSOP Package	
Power Dissipation	(T_J max – T_A)/θ_{JA}
θ_{JA} Thermal Impedance	240°C/W
Lead Temperature, Soldering	
Vapor Phase (60s)	+215°C
Infrared (15s)	+220°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

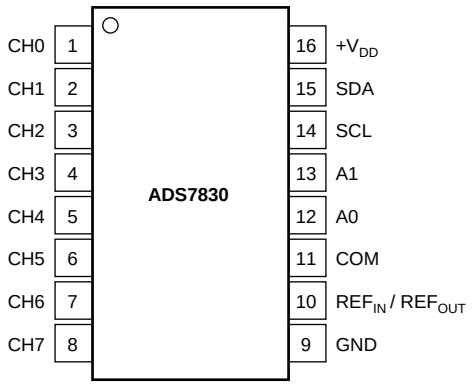
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS7830I	±0.5	TSSOP-16	PW	–40°C to +85°C	ADS7830IPWT	Tape and Reel, 250
"	"	"	"	"	ADS7830IPWR	Tape and Reel, 2500

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

PIN CONFIGURATION

Top View **TSSOP**



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CH0	Analog Input Channel 0
2	CH1	Analog Input Channel 1
3	CH2	Analog Input Channel 2
4	CH3	Analog Input Channel 3
5	CH4	Analog Input Channel 4
6	CH5	Analog Input Channel 5
7	CH6	Analog Input Channel 6
8	CH7	Analog Input Channel 7
9	GND	Analog Ground
10	REF_{IN} / REF_{OUT}	Internal +2.5V Reference, External Reference Input
11	COM	Common to Analog Input Channel
12	A0	Slave Address Bit 0
13	A1	Slave Address Bit 1
14	SCL	Serial Clock
15	SDA	Serial Data
16	$+V_{DD}$	Power Supply, 3.3V Nominal

ELECTRICAL CHARACTERISTICS: +2.7V

At T_A = –40°C to +85°C, $+V_{DD}$ = +2.7V, V_{REF} = +2.5V, SCL Clock Frequency = 3.4MHz (High-Speed Mode), unless otherwise noted.

PARAMETER	CONDITIONS	ADS7830E MIN	ADS7830E TYP	ADS7830E MAX	UNITS
ANALOG INPUT					
Full-Scale Input Scan	Positive Input - Negative Input	0		V_{REF}	V
Absolute Input Range	Positive Input	–0.2		$+V_{DD}$ + 0.2	V
	Negative Input	–0.2		+0.2	V
Capacitance			25		pF
Leakage Current			±1		µA
SYSTEM PERFORMANCE					
No Missing Codes		8			Bits
Integral Linearity Error			±0.1	±0.5	LSB(1)
Differential Linearity Error			±0.1	±0.5	LSB
Offset Error			+0.5	+1	LSB
Offset Error Match			±0.05	±0.25	LSB
Gain Error			±0.1	±0.5	LSB
Gain Error Match			±0.05	±0.25	LSB
Noise			100		µVRMS
Power-Supply Rejection			72		dB
SAMPLING DYNAMICS					
Throughput Frequency	High-Speed Mode: SCL = 3.4MHz			70	kSPS(2)
	Fast Mode: SCL = 400kHz			10	kSPS
	Standard Mode, SCL = 100kHz			2.5	kSPS
Conversion Time			5		µs
AC ACCURACY					
Total Harmonic Distortion	V_{IN} = 2.5V_{PP} at 1kHz		–72		dB(3)
Signal-to-Ratio	V_{IN} = 2.5V_{PP} at 1kHz		50		dB
Signal-to-(Noise+Distortion) Ratio	V_{IN} = 2.5V_{PP} at 1kHz		49		dB
Spurious-Free Dynamic Range	V_{IN} = 2.5V_{PP} at 1kHz		68		dB
Isolation Channel-to-Channel			90		dB
VOLTAGE REFERENCE OUTPUT					
Range		2.475	2.5	2.525	V
Internal Reference Drift			15		ppm/°C
Output Impedance	Internal Reference ON		110		Ω
	Internal Reference OFF		1		GΩ
Quiescent Current	Internal Reference ON, SCL and SDA pulled HIGH		850		µA
VOLTAGE REFERENCE INPUT					
Range		0.05		V_{DD}	V
Resistance			1		GΩ
Current Drain	High-Speed Mode: SCL= 3.4MHz		20		µA
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Levels: V_{IH}		$+V_{DD}$ • 0.7		$+V_{DD}$ + 0.5	V
V_{IL}		–0.3		$+V_{DD}$ • 0.3	V
V_{OL}	Minimum 3mA Sink Current			0.4	V
Input Leakage: I_{IH}	V_{IH} = $+V_{DD}$ +0.5			10	µA
I_{IL}	V_{IL} = -0.3	-10			µA
Data Format			Straight Binary		
ADS7830 HARDWARE ADDRESS			10010		Binary
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage, $+V_{DD}$	Specified Performance	2.7		3.6	V
Quiescent Current	High-Speed Mode: SCL = 3.4MHz		225	320	µA
	Fast Mode: SCL = 400kHz		100		µA
	Standard Mode, SCL = 100kHz		60		µA
Power Dissipation	High-Speed Mode: SCL = 3.4MHz		675	1000	µW
	Fast Mode: SCL = 400kHz		300		µW
	Standard Mode, SCL = 100kHz		180		µW
Power-Down Mode	High-Speed Mode: SCL = 3.4MHz		70		µA
w/Wrong Address Selected	Fast Mode: SCL = 400kHz		25		µA
	Standard Mode, SCL = 100kHz		6		µA
Full Power-Down	SCL Pulled HIGH, SDA Pulled HIGH		400	3000	nA
TEMPERATURE RANGE					
Specified Performance		–40		85	°C

NOTES: (1) LSB means least significant bit. When V_{REF} = 2.5V, 1LSB is 9.8mV.
(2) kSPS means kilo samples-per-second.
(3) THD measured out to the 9th-harmonic.

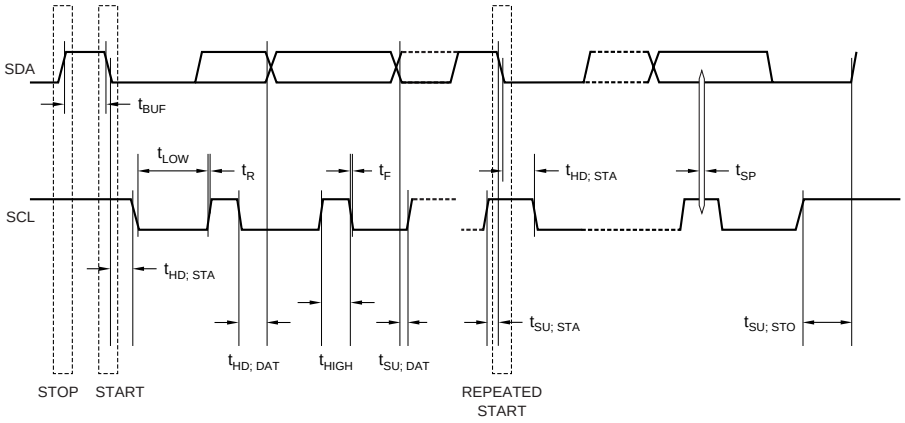
ELECTRICAL CHARACTERISTICS: +5V

At T_A = –40°C to +85°C, $+V_{DD}$ = +5.0V, V_{REF} = External +5.0V, SCL Clock Frequency = 3.4MHz (High-Speed Mode), unless otherwise noted.

PARAMETER	CONDITIONS	ADS7830E MIN	ADS7830E TYP	ADS7830E MAX	UNITS
ANALOG INPUT					
Full-Scale Input Scan	Positive Input - Negative Input	0		V_{REF}	V
Absolute Input Range	Positive Input	–0.2		$+V_{DD}$ + 0.2	V
	Negative Input	–0.2		+0.2	V
Capacitance			25		pF
Leakage Current			±1		µA
SYSTEM PERFORMANCE					
No Missing Codes		8			Bits
Integral Linearity Error			±0.1	±0.5	LSB(1)
Differential Linearity Error			±0.1	±0.5	LSB
Offset Error			+0.5	+1	LSB
Offset Error Match			±0.05	±0.25	LSB
Gain Error			±0.1	±0.5	LSB
Gain Error Match			±0.05	±0.25	LSB
Noise			100		µVRMS
Power-Supply Rejection			72		dB
SAMPLING DYNAMICS					
Throughput Frequency	High-Speed Mode: SCL = 3.4MHz			70	kSPS(2)
	Fast Mode: SCL = 400kHz			10	kSPS
	Standard Mode, SCL = 100kHz			2.5	kSPS
Conversion Time			5		µs
AC ACCURACY					
Total Harmonic Distortion	V_{IN} = $5V_{PP}$ at 1kHz		–72		dB(3)
Signal-to-Ratio	V_{IN} = $5V_{PP}$ at 1kHz		50		dB
Signal-to-(Noise+Distortion) Ratio	V_{IN} = $5V_{PP}$ at 1kHz		49		dB
Spurious-Free Dynamic Range	V_{IN} = $5V_{PP}$ at 1kHz		68		dB
Isolation Channel-to-Channel			90		dB
VOLTAGE REFERENCE OUTPUT					
Range		2.475	2.5	2.525	V
Internal Reference Drift			15		ppm/°C
Output Impedance	Internal Reference ON		110		Ω
	Internal Reference OFF		1		GΩ
Quiescent Current	Int. Ref. ON, SCL and SDA pulled HIGH		1300		µA
VOLTAGE REFERENCE INPUT					
Range		0.05		V_{DD}	V
Resistance			1		GΩ
Current Drain	High-Speed Mode: SCL = 3.4MHz		20		µA
DIGITAL INPUT/OUTPUT					
Logic Family			CMOS		
Logic Levels: V_{IH}		$+V_{DD}$ • 0.7		$+V_{DD}$ + 0.5	V
V_{IL}		–0.3		$+V_{DD}$ • 0.3	V
V_{OL}	Minimum 3mA Sink Current			0.4	V
Input Leakage: I_{IH}	V_{IH} = $+V_{DD}$ +0.5			10	µA
I_{IL}	V_{IL} = -0.3	-10			µA
Data Format			Straight Binary		
ADS7830 HARDWARE ADDRESS			10010		Binary
POWER-SUPPLY REQUIREMENTS					
Power-Supply Voltage, $+V_{DD}$	Specified Performance	4.75	5	5.25	V
Quiescent Current	High-Speed Mode: SCL = 3.4MHz		750	1000	µA
	Fast Mode: SCL = 400kHz		300		µA
	Standard Mode, SCL = 100kHz		150		µA
Power Dissipation	High-Speed Mode: SCL = 3.4MHz		3.75	5	mW
	Fast Mode: SCL = 400kHz		1.5		mW
	Standard Mode, SCL = 100kHz		0.75		mW
Power-Down Mode	High-Speed Mode: SCL = 3.4MHz		400		µA
w/Wrong Address Selected	Fast Mode: SCL = 400kHz		150		µA
	Standard Mode, SCL = 100kHz		35		µA
Full Power-Down	SCL Pulled HIGH, SDA Pulled HIGH		400	3000	nA
TEMPERATURE RANGE					
Specified Performance		–40		85	°C

NOTES: (1) LSB means Least Significant Bit. When V_{REF} = 5.0V, 1LSB is 19.5mV.
(2) kSPS means kilo samples-per-second.
(3) THD measured out to the 9th-harmonic.

TIMING DIAGRAM



TIMING CHARACTERISTICS(1)

At T_A = –40°C to +85°C, $+V_{DD}$ = +2.7V, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
SCL Clock Frequency	f_{SCL}	Standard Mode		100	kHz
		Fast Mode		400	kHz
		High-Speed Mode, C_B = 100pF max		3.4	MHz
		High-Speed Mode, C_B = 400pF max		1.7	MHz
Bus Free Time Between a STOP and START Condition	t_{BUF}	Standard Mode	4.7		µs
		Fast Mode	1.3		µs
Hold Time (Repeated) START Condition	$t_{HD;\ STA}$	Standard Mode	4.0		µs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
LOW Period of the SCL Clock	t_{LOW}	Standard Mode	4.7		µs
		Fast Mode	1.3		µs
		High-Speed Mode, C_B = 100pF max(2)	160		ns
		High-Speed Mode, C_B = 400pF max(2)	320		ns
HIGH Period of the SCL Clock	t_{HIGH}	Standard Mode	4.0		µs
		Fast Mode	600		ns
		High-Speed Mode, C_B = 100pF max(2)	60		ns
		High-Speed Mode, C_B = 400pF max(2)	120		ns
Setup Time for a Repeated START Condition	$t_{SU;\ STA}$	Standard Mode	4.7		µs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
Data Setup Time	$t_{SU;\ DAT}$	Standard Mode	250		ns
		Fast Mode	100		ns
		High-Speed Mode	10		ns
Data Hold Time	$t_{HD;\ DAT}$	Standard Mode	0	3.45	µs
		Fast Mode	0	0.9	µs
		High-Speed Mode, C_B = 100pF max(2)	0(3)	70	ns
		High-Speed Mode, C_B = 400pF max(2)	0(3)	150	ns
Rise Time of SCL Signal	t_{RCL}	Standard Mode		1000	ns
		Fast Mode	$20 + 0.1C_B$	300	ns
		High-Speed Mode, C_B = 100pF max(2)	10	40	ns
		High-Speed Mode, C_B = 400pF max(2)	20	80	ns
Rise Time of SCL Signal After a Repeated START Condition and After an Acknowledge Bit	t_{RCL1}	Standard Mode		1000	ns
		Fast Mode	$20 + 0.1C_B$	300	ns
		High-Speed Mode, C_B = 100pF max(2)	10	80	ns
		High-Speed Mode, C_B = 400pF max(2)	20	160	ns
Fall Time of SCL Signal	t_{FCL}	Standard Mode		300	ns
		Fast Mode	$20 + 0.1C_B$	300	ns
		High-Speed Mode, C_B = 100pF max(2)	10	40	ns
		High-Speed Mode, C_B = 400pF max(2)	20	80	ns

NOTES: (1) All values referred to V_{IHMIN} and V_{ILMAX} levels.
(2) For bus line loads C_B between 100pF and 400pF the timing parameters must be linearly interpolated.
(3) A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

TIMING CHARACTERISTICS(1) (Cont.)

At T_A = –40°C to +85°C, +V_{DD} = +2.7V, unless otherwise noted.

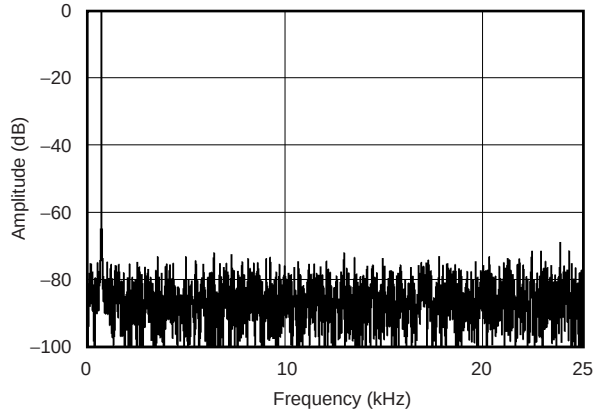
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Rise Time of SDA Signal	t_{RDA}	Standard Mode		1000	ns
		Fast Mode	20 + 0.1C_B	300	ns
		High-Speed Mode, C_B = 100pF max(2)	10	80	ns
		High-Speed Mode, C_B = 400pF max(2)	20	160	ns
Fall Time of SDA Signal	t_{FDA}	Standard Mode		300	ns
		Fast Mode	20 + 0.1C_B	300	ns
		High-Speed Mode, C_B = 100pF max(2)	10	80	ns
		High-Speed Mode, C_B = 400pF max(2)	20	160	ns
Setup Time for STOP Condition	$t_{SU;\,STO}$	Standard Mode	4.0		µs
		Fast Mode	600		ns
		High-Speed Mode	160		ns
Capacitive Load for SDA and SCL Line	C_B			400	pF
Pulse Width of Spike Suppressed	t_{SP}	Fast Mode		50	ns
		High-Speed Mode		10	ns
Noise Margin at the HIGH Level for Each Connected Device (Including Hysteresis)	V_{NH}	Standard Mode Fast Mode High-Speed Mode	0.2V_{DD}		V
Noise Margin at the LOW Level for Each Connected Device (Including Hysteresis)	V_{NL}	Standard Mode Fast Mode High-Speed Mode	0.1V_{DD}		V

NOTES: (1) All values referred to V_{IHMIN} and V_{ILMAX} levels.
(2) For bus line loads C_B between 100pF and 400pF the timing parameters must be linearly interpolated.
(3) A device must internally provide a data hold time to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of the SCLH signal. An input circuit with a threshold as low as possible for the falling edge of the SCLH signal minimizes this hold time.

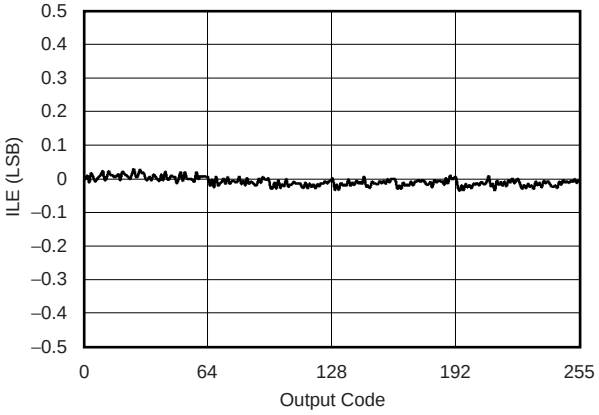
TYPICAL CHARACTERISTICS

T_A = +25°C, V_{DD} = +2.7V, V_{REF} = External +2.5V, f_{SAMPLE} = 50kHz, unless otherwise noted.

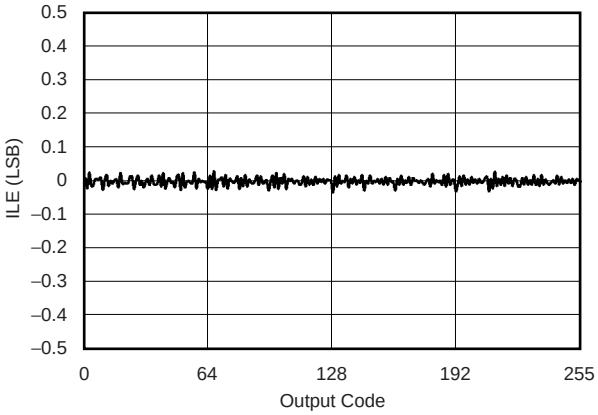
FFT vs FREQUENCY



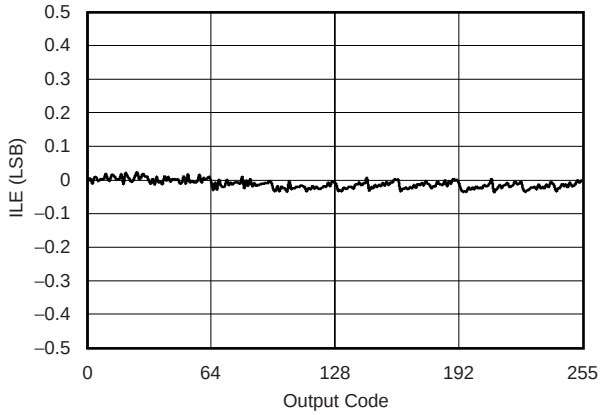
INTEGRAL LINEARITY ERROR vs CODE
(2.5V Internal Reference)



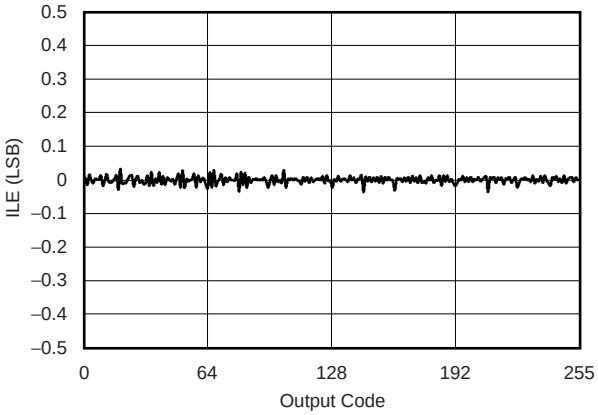
DIFFERENTIAL LINEARITY ERROR vs CODE
(2.5V Internal Reference)



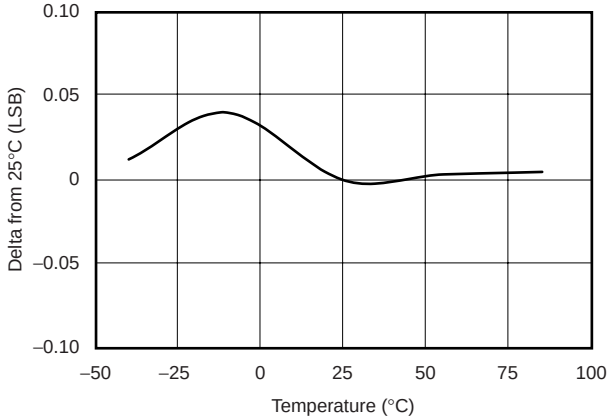
INTEGRAL LINEARITY ERROR vs CODE
(2.5V External Reference)



DIFFERENTIAL LINEARITY ERROR vs CODE
(2.5V External Reference)



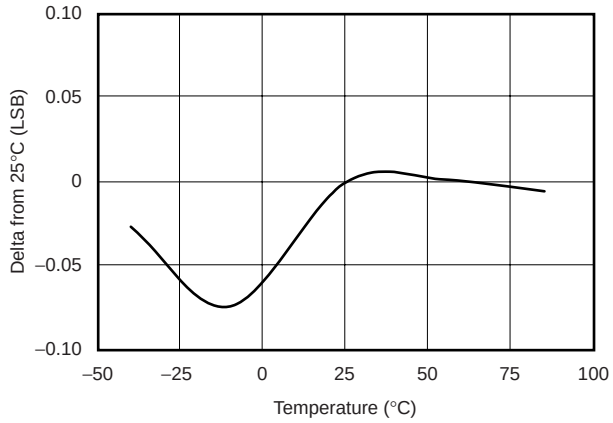
CHANGE IN OFFSET vs TEMPERATURE



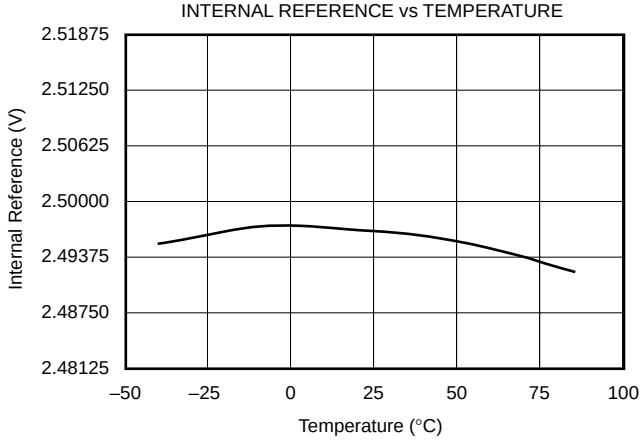
TYPICAL CHARACTERISTICS (Cont.)

T_A = +25°C, V_{DD} = +2.7V, V_{REF} = External +2.5V, f_{SAMPLE} = 50kHz, unless otherwise noted.

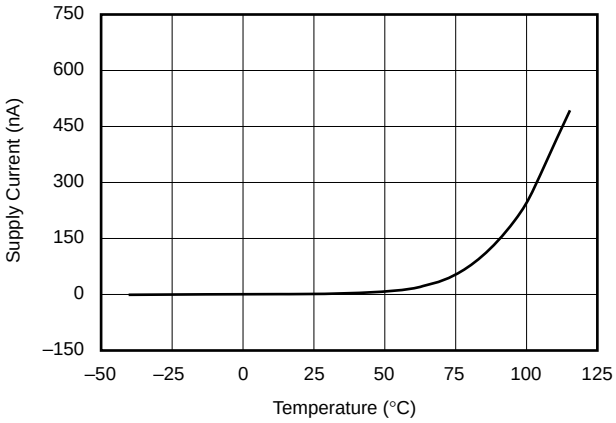
CHANGE IN GAIN vs TEMPERATURE



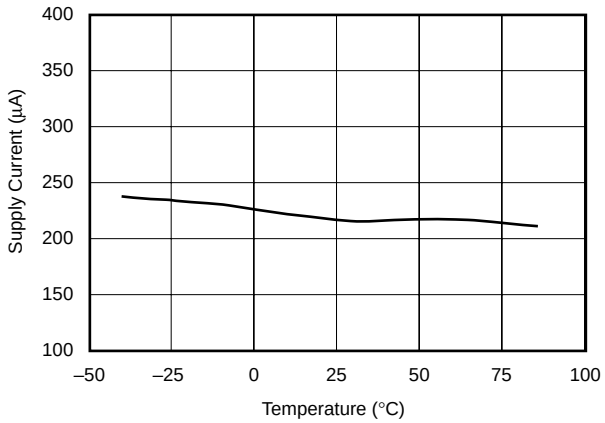
INTERNAL REFERENCE vs TEMPERATURE



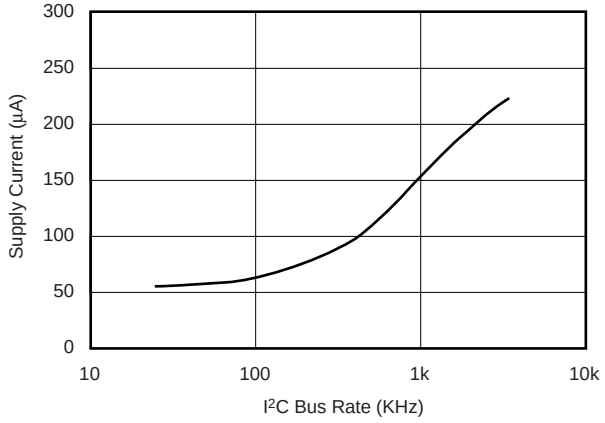
POWER-DOWN SUPPLY CURRENT vs TEMPERATURE



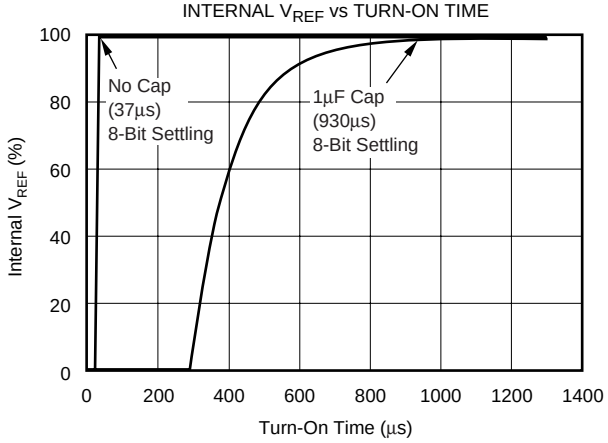
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs I²C BUS RATE



INTERNAL V_{REF} vs TURN-ON TIME



THEORY OF OPERATION

The ADS7830 is a classic Successive Approximation Register (SAR) A/D converter. The architecture is based on capacitive redistribution which inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µ CMOS process.

The ADS7830 core is controlled by an internally generated free-running clock. When the ADS7830 is not performing conversions or being addressed, it keeps the A/D converter core powered off, and the internal clock does not operate.

The simplified diagram of input and output for the ADS7830 is shown in Figure 1.

ANALOG INPUT

When the converter enters the hold mode, the voltage on the selected CHx pin is captured on the internal capacitor array. The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The amount of charge transfer from the analog source to the converter is a function of conversion rate.

REFERENCE

The ADS7830 can operate with an internal 2.5V reference or an external reference. If a +5V supply is used, an external +5V reference is required in order to provide full dynamic range for a 0V to $+V_{DD}$ analog input. This external reference can be as low as 50mV. When using a +2.7V supply, the internal +2.5V reference will provide full dynamic range for a 0V to $+V_{DD}$ analog input.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the LSB (least significant bit) size and is equal to the reference voltage divided by 256. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced.

The noise inherent in the converter will also appear to increase with lower LSB size. With a 2.5V reference, the internal noise of the converter typically contributes only 0.02LSB peak-to-peak of potential error to the output code. When the external reference is 50mV, the potential error contribution from the internal noise will be 50 times larger—1LSB. The errors due to the internal noise are Gaussian in nature and can be reduced by averaging consecutive conversion results.

DIGITAL INTERFACE

The ADS7830 supports the I^2C serial bus and data transmission protocol, in all three defined modes: standard, fast, and high-speed. A device that sends data onto the bus is defined as a transmitter, and a device receiving data as a receiver. The device that controls the message is called a “master.” The devices that are controlled by the master are “slaves.” The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions. The ADS7830 operates as a slave on the I^2C bus. Connections to the bus are made via the open-drain I/O lines SDA and SCL.

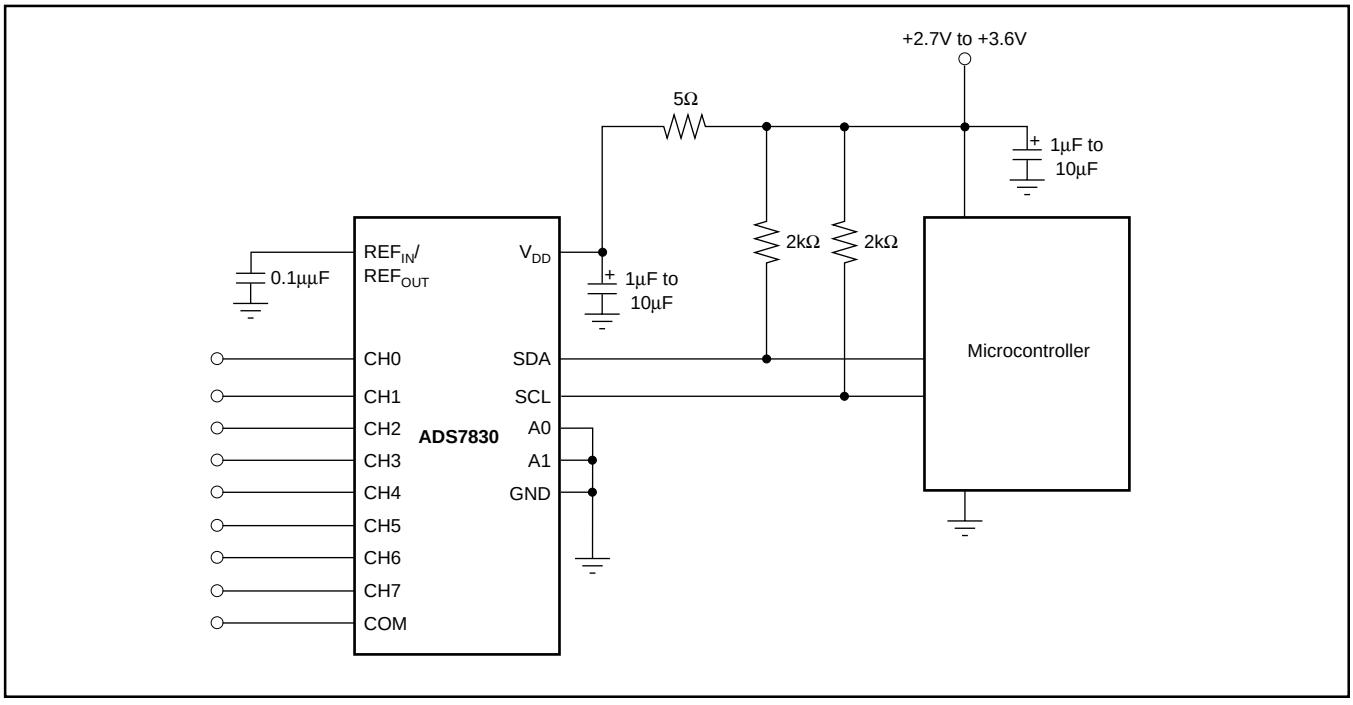


FIGURE 1. Simplified I/O of the ADS7830.

The following bus protocol has been defined (as shown in Figure 2):

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is HIGH. Changes in the data line while the clock line is HIGH will be interpreted as control signals.

Accordingly, the following bus conditions have been defined:

Bus Not Busy: Both data and clock lines remain HIGH.

Start Data Transfer: A change in the state of the data line, from HIGH to LOW, while the clock is HIGH, defines a START condition.

Stop Data Transfer: A change in the state of the data line, from LOW to HIGH, while the clock line is HIGH, defines the STOP condition.

Data Valid: The state of the data line represents valid data, when, after a START condition, the data line is stable for the duration of the HIGH period of the clock signal. There is one clock pulse per bit of data.

Each data transfer is initiated with a START condition and terminated with a STOP condition. The number of data bytes transferred between START and STOP conditions is not limited and is determined by the master device. The information is transferred byte-wise and each receiver acknowledges with a ninth-bit.

Within the I^2C bus specifications a standard mode (100kHz clock rate), a fast mode (400kHz clock rate), and a high-speed mode (3.4MHz clock rate) are defined. The ADS7830 works in all three modes.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge after the reception of each byte. The master device must generate an extra clock pulse that is associated with this acknowledge bit.

A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable LOW during the HIGH period of the acknowledge clock pulse. Of course, setup and hold times must be taken into account. A master must signal an end of data to the slave by not generating an acknowledge bit on the last byte that has been clocked out of the slave. In this case, the slave must leave the data line HIGH to enable the master to generate the STOP condition.

Figure 2 details how data transfer is accomplished on the I^2C bus. Depending upon the state of the R/$\overline{W}$ bit, two types of data transfer are possible:

1. **Data transfer from a master transmitter to a slave receiver.** The first byte transmitted by the master is the slave address. Next follows a number of data bytes. The slave returns an acknowledge bit after the slave address and each received byte.
2. **Data transfer from a slave transmitter to a master receiver.** The first byte, the slave address, is transmitted by the master. The slave then returns an acknowledge bit. Next, a number of data bytes are transmitted by the slave to the master. The master returns an acknowledge bit after all received bytes other than the last byte. At the end of the last received byte, a not-acknowledge is returned.

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or a repeated START condition. Since a repeated START condition is also the beginning of the next serial transfer, the bus will not be released.

The ADS7830 may operate in the following two modes:

- **Slave Receiver Mode:** Serial data and clock are received through SDA and SCL. After each byte is received, an acknowledge bit is transmitted. START and STOP conditions are recognized as the beginning and end of a serial transfer. Address recognition is performed by hardware after reception of the slave address and direction bit.
- **Slave Transmitter Mode:** The first byte (the slave address) is received and handled as in the slave receiver mode. However, in this mode the direction bit will indicate that the transfer direction is reversed. Serial data is transmitted on SDA by the ADS7830 while the serial clock is input on SCL. START and STOP conditions are recognized as the beginning and end of a serial transfer.

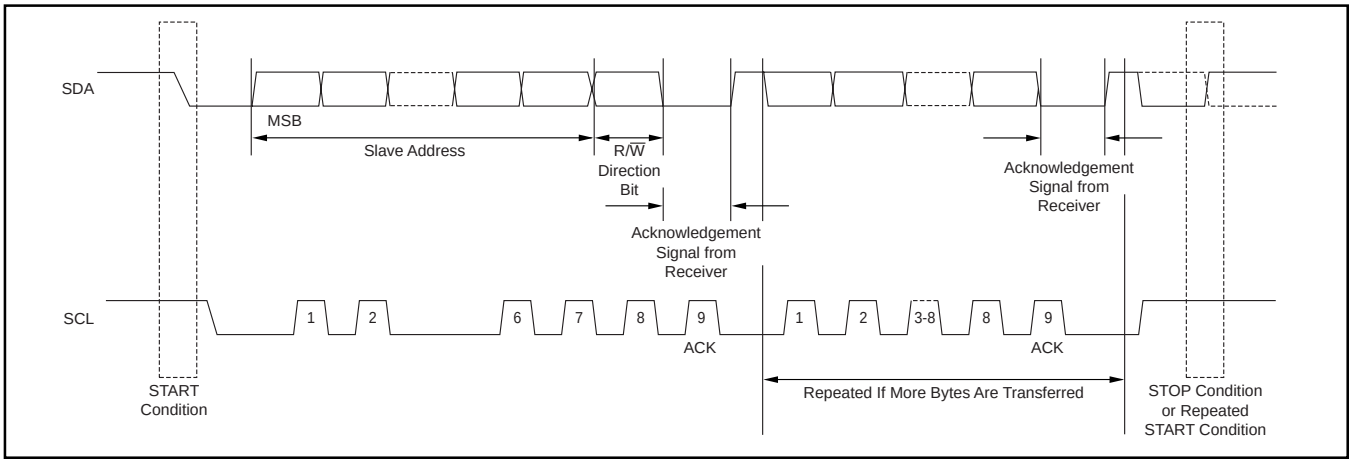


FIGURE 2. Basic Operation of the ADS7830.

Address Byte

MSB	6	5	4	3	2	1	LSB
1	0	0	1	0	A1	A0	R/$\overline{W}$

The address byte is the first byte received following the START condition from the master device. The first five bits (MSBs) of the slave address are factory pre-set to 10010. The next two bits of the address byte are the device select bits, A1 and A0. Input pins (A1-A0) on the ADS7830 determine these two bits of the device address for a particular ADS7830. A maximum of four devices with the same pre-set code can therefore be connected on the same bus at one time.

The A1-A0 Address Inputs can be connected to V_{DD} or digital ground. The device address is set by the state of these pins upon power-up of the ADS7830.

The last bit of the address byte (R/$\overline{W}$) defines the operation to be performed. When set to a '1' a read operation is selected; when set to a '0' a write operation is selected. Following the START condition the ADS7830 monitors the SDA bus, checking the device type identifier being transmitted. Upon receiving the 10010 code, the appropriate device select bits, and the R/$\overline{W}$ bit, the slave device outputs an acknowledge signal on the SDA line.

Command Byte

MSB	6	5	4	3	2	1	LSB
SD	C2	C1	C0	PD1	PD0	X	X

The ADS7830 operating mode is determined by a command byte which is illustrated above.

SD: Single-Ended/Differential Inputs
0: Differential Inputs
1: Single-Ended Inputs

C2 - C0: Channel Selections

PD1 - 0: Power-Down Selection
X: Unused

See Table I for a power-down selection summary.

See Table II for a channel selection control summary.

PD1	PD0	DESCRIPTION
0	0	Power Down Between A/D Converter Conversions
0	1	Internal Reference OFF and A/D Converter ON
1	0	Internal Reference ON and A/D Converter OFF
1	1	Internal Reference ON and A/D Converter ON

TABLE I. Power-Down Selection

CHANNEL SELECTION CONTROL												
SD	C2	C1	C0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	0	+IN	–IN	—	—	—	—	—	—	—
0	0	0	1	—	—	+IN	–IN	—	—	—	—	—
0	0	1	0	—	—	—	—	+IN	–IN	—	—	—
0	0	1	1	—	—	—	—	—	—	+IN	–IN	—
0	1	0	0	–IN	+IN	—	—	—	—	—	—	—
0	1	0	1	—	—	–IN	+IN	—	—	—	—	—
0	1	1	0	—	—	—	—	–IN	+IN	—	—	—
0	1	1	1	—	—	—	—	—	—	–IN	+IN	—
1	0	0	0	+IN	—	—	—	—	—	—	—	–IN
1	0	0	1	—	—	+IN	—	—	—	—	—	–IN
1	0	1	0	—	—	—	—	+IN	—	—	—	–IN
1	0	1	1	—	—	—	—	—	—	+IN	—	–IN
1	1	0	0	—	+IN	—	—	—	—	—	—	–IN
1	1	0	1	—	—	—	+IN	—	—	—	—	–IN
1	1	1	0	—	—	—	—	—	+IN	—	—	–IN
1	1	1	1	—	—	—	—	—	—	—	+IN	–IN

TABLE II. Channel Selection Control Addressed by Command BYTE.

INITIATING CONVERSION

Provided the master has write-addressed it, the ADS7830 turns on the A/D converter section and begins conversions when it receives BIT 4 of the command byte shown in the Command Byte. If the command byte is correct, the ADS7830 will return an ACK condition.

READING DATA

Data can be read from the ADS7830 by read-addressing the part (LSB of address byte set to '1') and receiving the transmitted byte. Converted data can only be read from the ADS7830 once a conversion has been initiated as described in the preceding section.

Each 8-bit data word is returned in one byte, as shown below, where D7 is the MSB of the data word, and D0 is the LSB.

	MSB	6	5	4	3	2	1	LSB
DATA	D7	D6	D5	D4	D3	D2	D1	D0

READING IN F/S MODE

Figure 3 describes the interaction between the master and the slave ADS7830 in Fast or Standard (F/S) mode. At the end of reading conversion data the ADS7830 can be issued a repeated START condition by the master to secure bus operation for subsequent conversions of the A/D converter. This would be the most efficient way to perform continuous conversions.

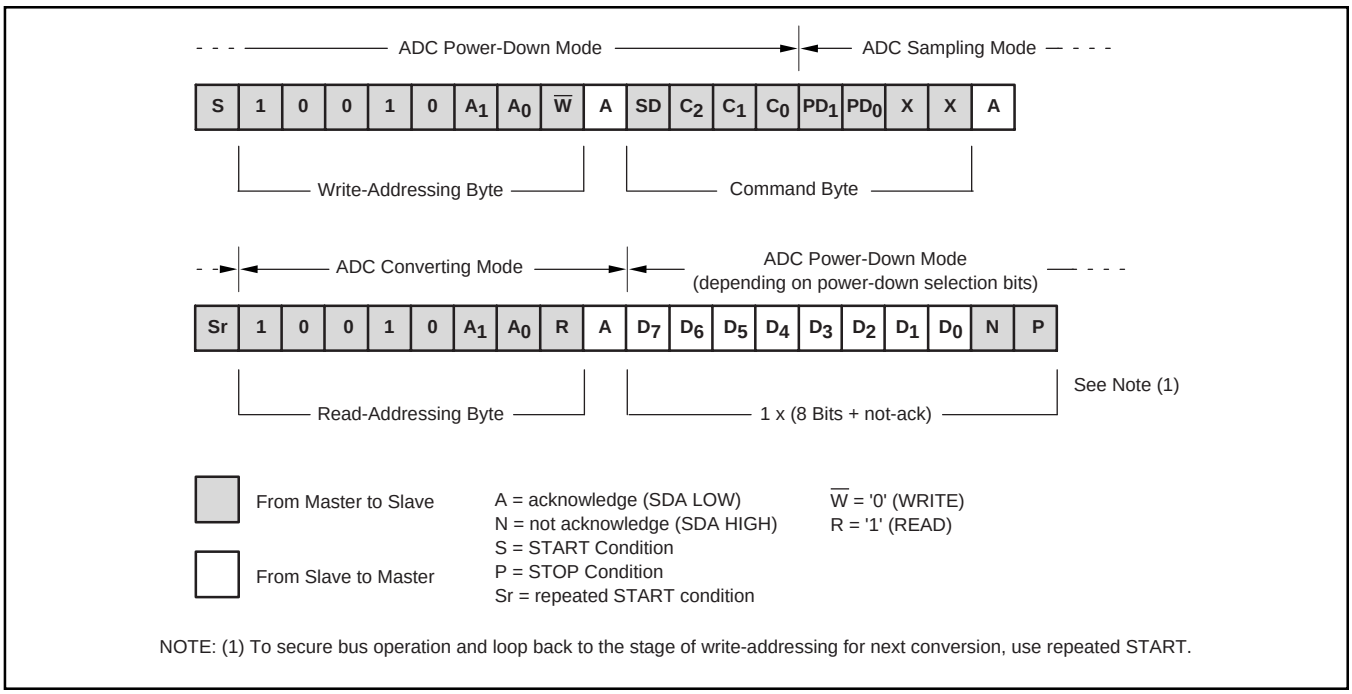


FIGURE 3. Typical Read Sequence in F/S Mode.

READING IN HS MODE

High Speed (HS) mode is fast enough that codes can be read out one at a time. In HS mode, there is not enough time for a single conversion to complete between the reception of a repeated START condition and the read-addressing byte, so the ADS7830 stretches the clock after the read-addressing byte has been fully received, holding it LOW until the conversion is complete.

See Figure 4 for a typical read sequence for HS mode. Included in the read sequence is the shift from F/S to HS modes. It may be desirable to remain in HS mode after reading a conversion; to do this, issue a repeated START instead of a STOP at the end of the read sequence, since a STOP causes the part to return to F/S mode.

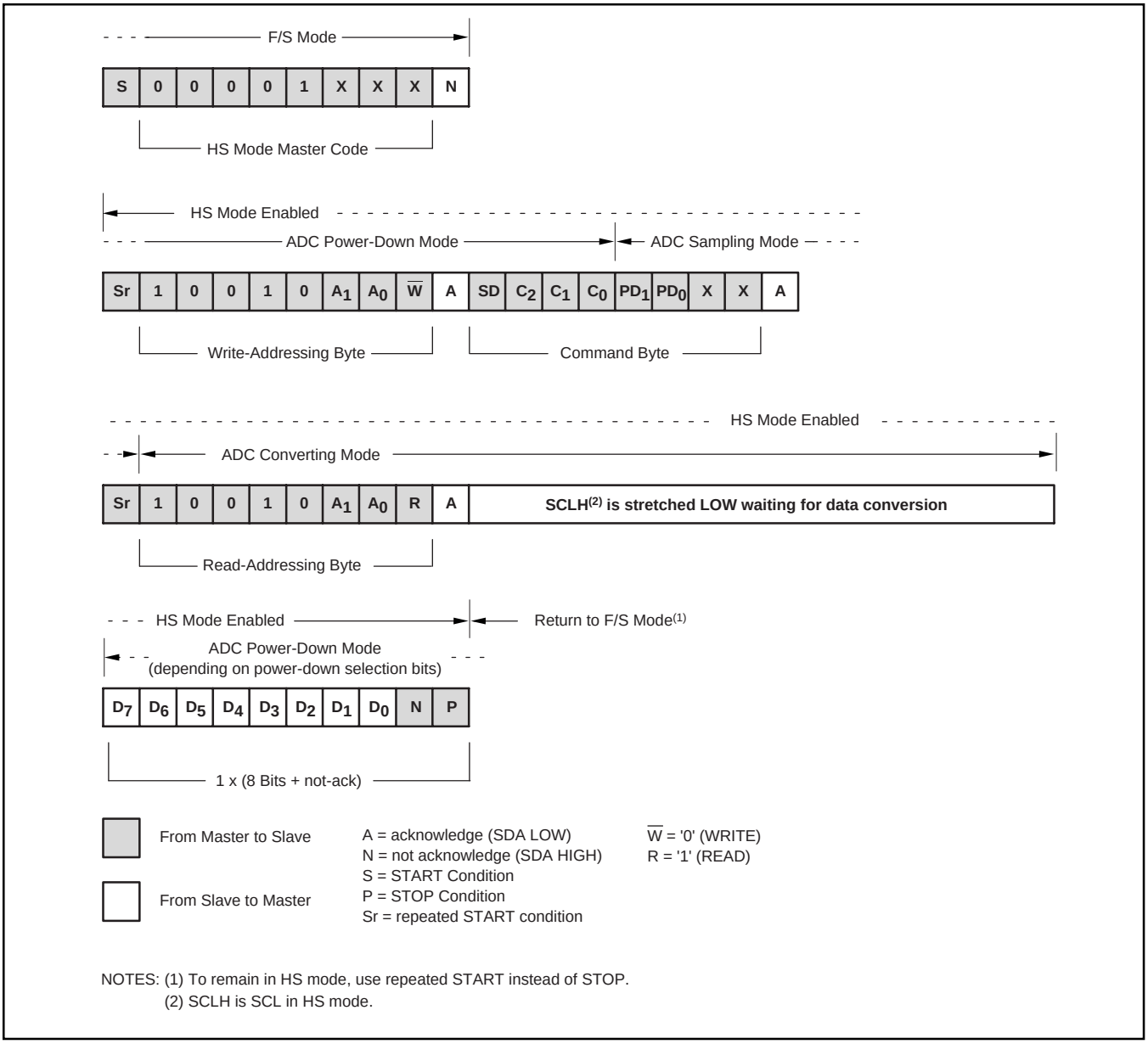


FIGURE 4. Typical Read Sequence in HS Mode.

READING WITH REFERENCE ON/OFF

The internal reference defaults to off when the ADS7830 power is on. To turn the internal reference on or off, see Table I. If the reference (internal or external) is constantly turned on and off, a proper amount of settling time must be added before a normal conversion cycle can be started. The exact amount of settling time needed varies depending on the configuration.

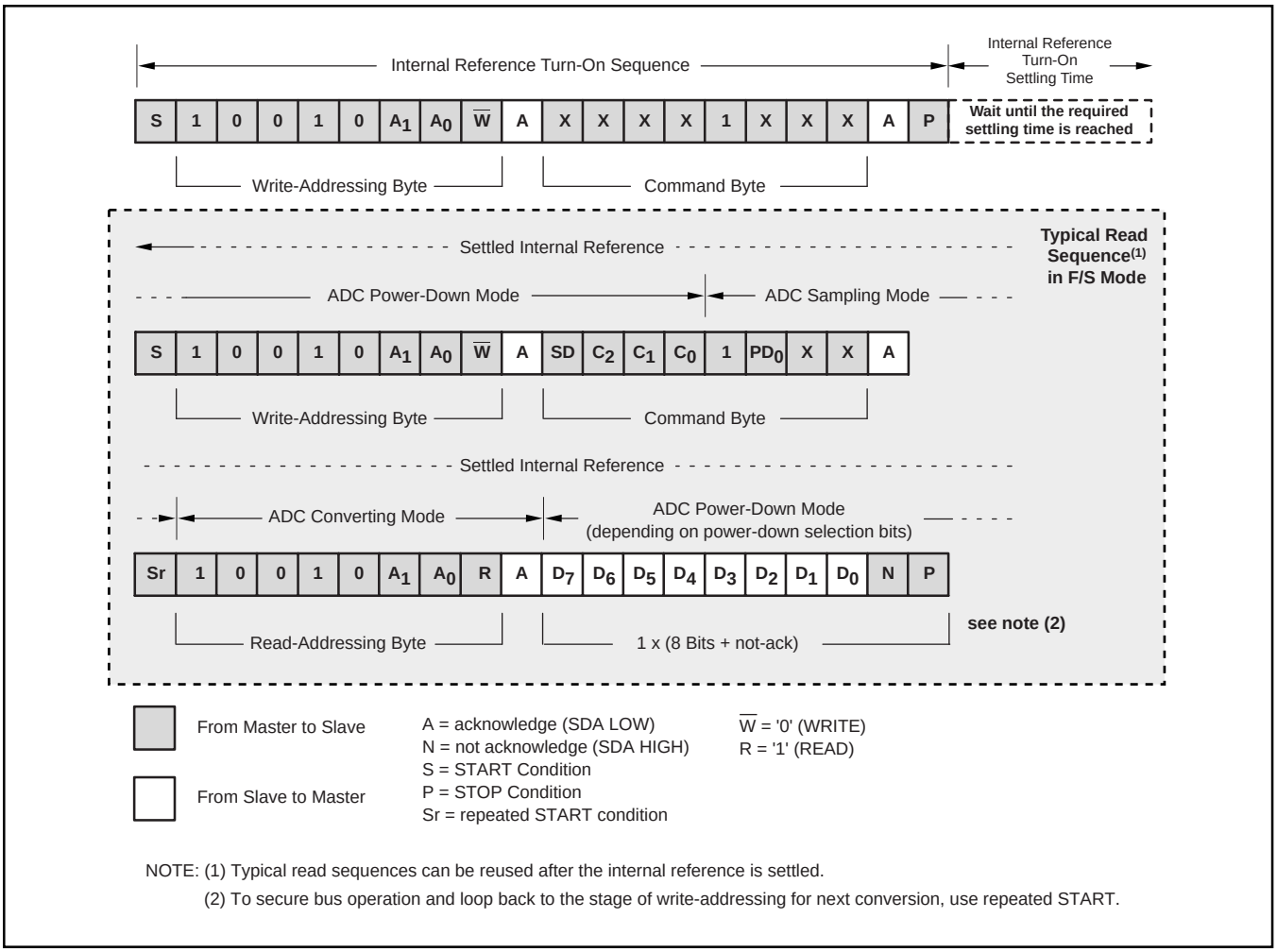
See Figure 5 for an example of the proper internal reference turn-on sequence before issuing the typical read sequences required for the F/S mode when an internal reference is used.

When using an internal reference, there are three things that must be done:

1) In order to use the internal reference, the PD1 bit of Command Byte must always be set to logic '1' for each sample conversion that is issued by the sequence, as shown in Figure 3.
2) In order to achieve 8-bit accuracy conversion when using the internal reference, the internal reference settling time must be considered, as shown in the *Internal V_{REF} vs Turn-On Time* Typical Characteristic plot. If the PD1 bit has been set to logic '0' while using the ADS7830, then the settling time must be reconsidered after PD1 is set to logic '1'. In other words, whenever the internal reference is turned on after it has been turned off, the settling time must be long enough to get 8-bit accuracy conversion.
3) When the internal reference is off, it is not turned on until both the first Command Byte with PD1 = '1' is sent *and then* a STOP condition or repeated START condition is issued. (The actual turn-on time occurs once the STOP or repeated START condition is issued.) Any Command Byte with PD1 = '1' issued after the internal reference is turned on serves only to keep the internal reference on. Otherwise, the internal reference would be turned off by any Command Byte with PD1 = '0'.

The example in Figure 5 can be generalized for a HS mode conversion cycle by simply swapping the timing of the conversion cycle.

If using an external reference, PD1 must be set to '0', and the external reference must be settled. The typical sequence in Figure 3 or Figure 4 can then be used.



NOTE: (1) Typical read sequences can be reused after the internal reference is settled.
(2) To secure bus operation and loop back to the stage of write-addressing for next conversion, use repeated START.

FIGURE 5. Internal Reference Turn-On Sequence and Typical Read Sequence (F/S mode shown).

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS7830 circuitry. The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Therefore, during any single conversion for an “n-bit” SAR converter, there are n “windows” in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices.

With this in mind, power to the ADS7830 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. A 1µF to 10µF capacitor may also be needed if the impedance of the connection between $+V_{DD}$ and the power supply is high.

The ADS7830 architecture offers no inherent rejection of noise or voltage variation in regards to using an external reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the “analog” ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
4/08	B	1	Features	Changed *Low Power* sub-bullets to show correct values; High Speed and Fast modes were reversed (typo).

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
ADS7830IPWR	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS7830IPWRG4	ACTIVE	TSSOP	PW	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS7830IPWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
ADS7830IPWTG4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

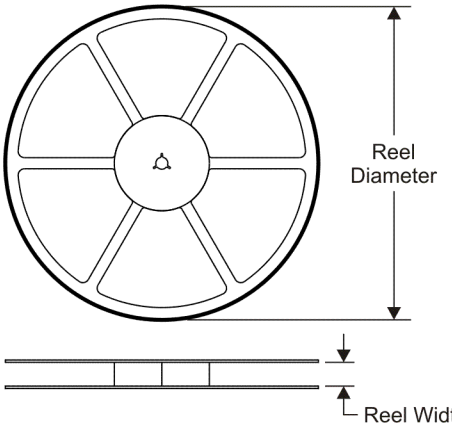
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

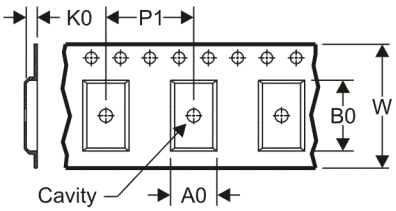
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

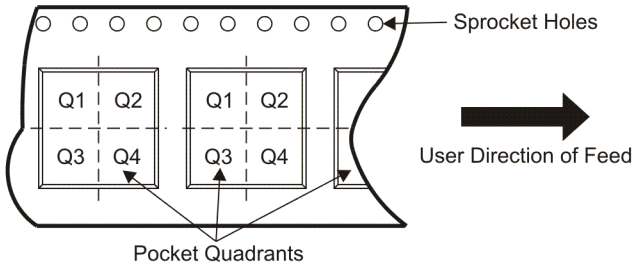


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

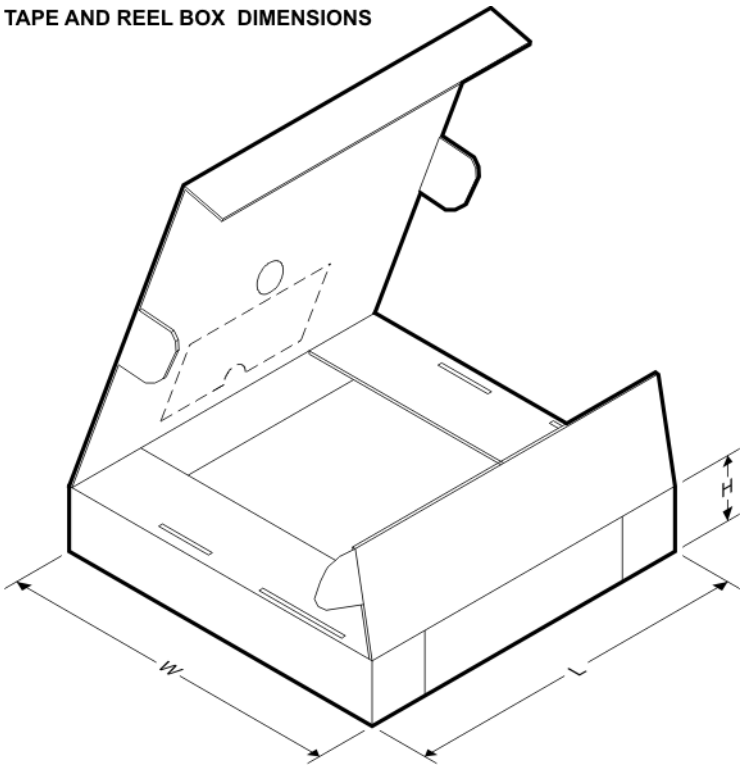
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS7830IPWR	TSSOP	PW	16	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
ADS7830IPWT	TSSOP	PW	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

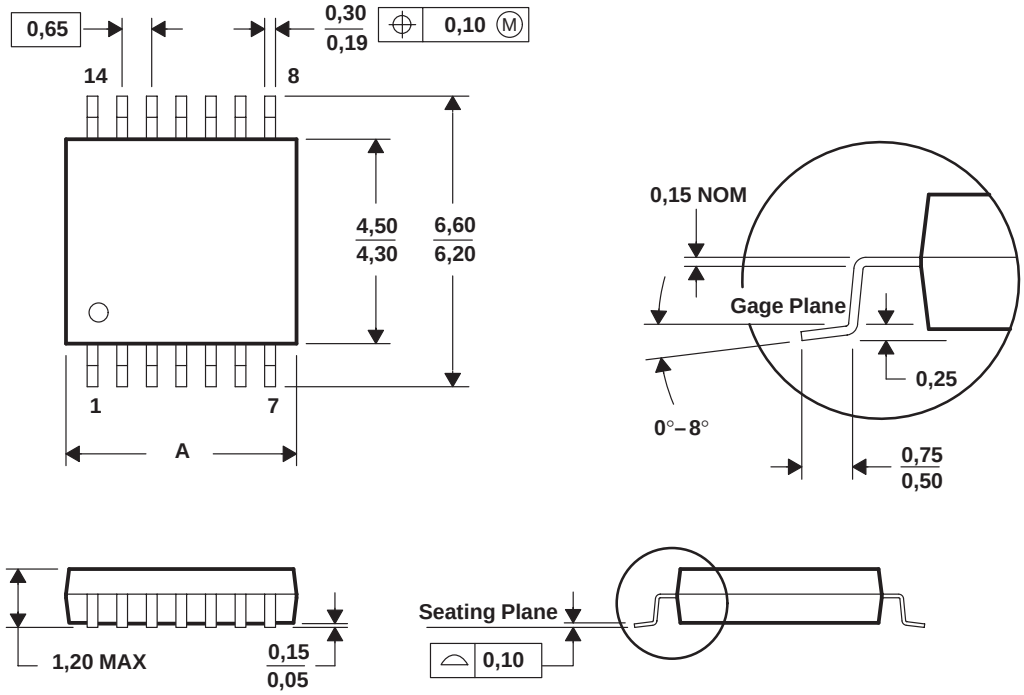


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS7830IPWR	TSSOP	PW	16	2500	346.0	346.0	29.0
ADS7830IPWT	TSSOP	PW	16	250	190.5	212.7	31.8

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN

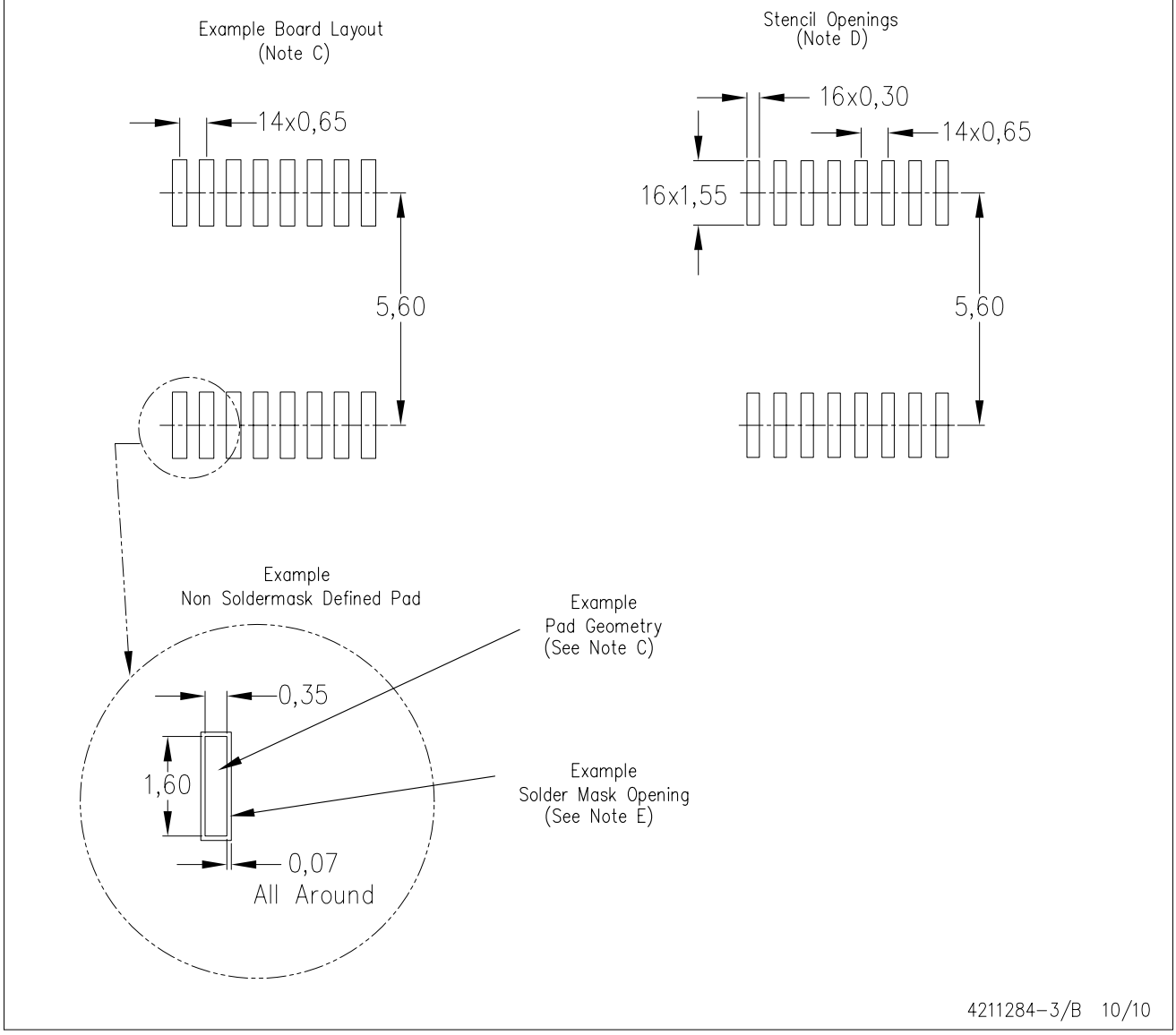


DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

PW (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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