MOOS Controller Overview

"The key to innovation is not thinking up new things, but learning to forget old ideas that are no longer valuable."

-Tom Peters, A Passion for Excellence

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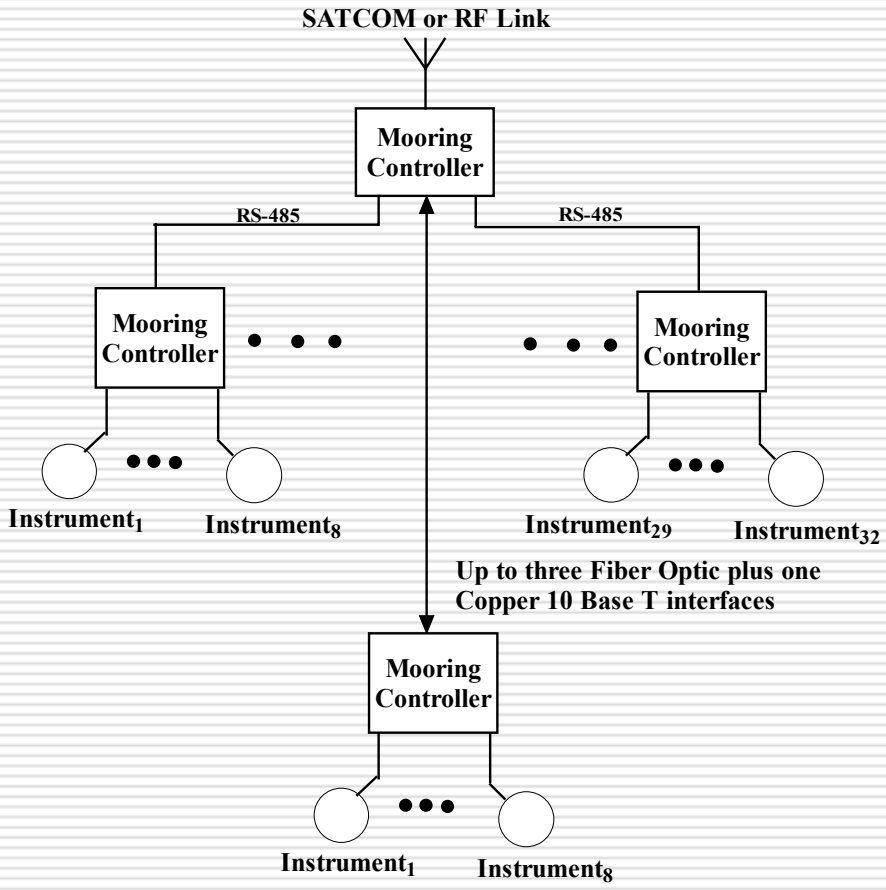
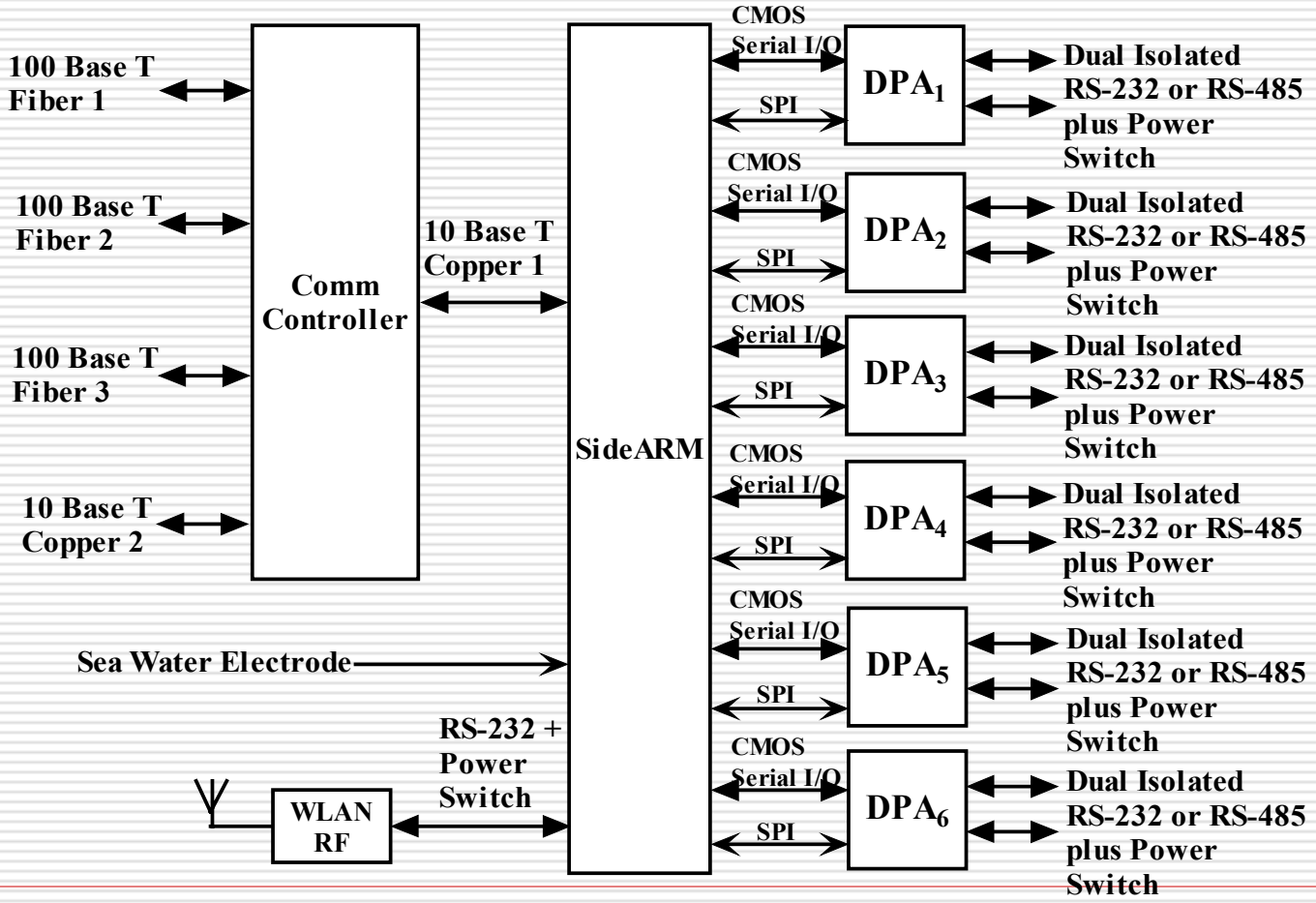
Over Simplified MOOS System



MOOS Controller Components

- "SideARM"
  - Runs SIAM application code via a Java JVM
  - Up to twelve instruments may be directly attached
  - Connects to shore based assets using a RF link or satellites
- "Communications Controller"
  - Permits a number of moorings controller to be connected together over fiber or copper.
  - Monitors network health and provides some tolerance of link failures.
- "DPA" (Dual Port Adapter)
  - Level Shifters and Isolation
  - Power Switches / Power Monitoring
  - Over current protection

MOOS Controller Block Diagram



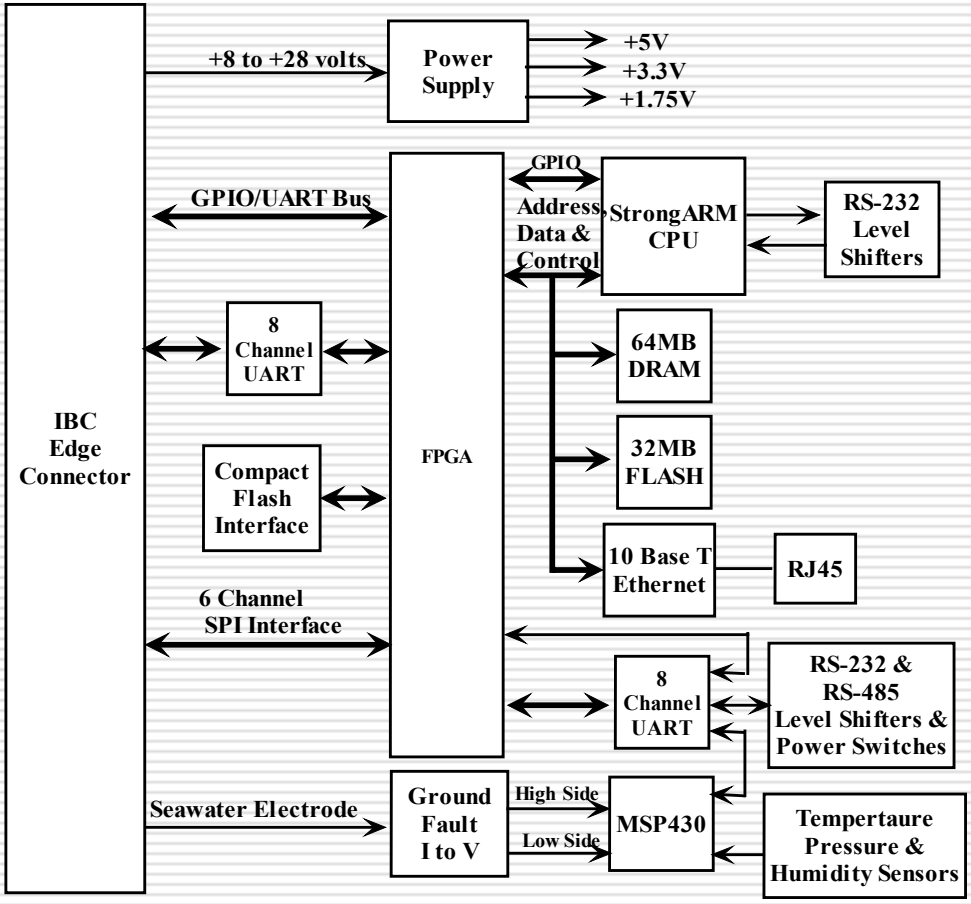
SideARM

- Dual CPU architecture
  - Application processor runs Linux and Java using
    - 206 MHz operation, 16 MB Flash, 64 MB SDRAM
    - Support for 10 Base T ethernet and 18 UARTs
    - Compact flash socket for up to 4GB of mass storage
    - FPGA for glue and time keeping logic
  - Environmental processor runs continuously even when application processor is “powered down” monitoring
    - Ground fault current
    - Temperature, Barometric pressure, and relative humidity inside mooring enclosure

Power Consumption

- Operational
  - 1.5 watts with CPU running and Ethernet at 200 Mhz
  - 1.0 watts with CPU running without Ethernet at 200 MHz
  - 0.3 watts with CPU running without Ethernet at 60 MHz
- Idle Mode: 200 milliwatts
- Sleep Mode: 50 milliwatts

SideARM Block Diagram



Time Keeping and Distribution

- The next revision of the SideARM will keep better time, with the following additional hardware:
  - A DCXO accurate to +/- 1 minute per year
  - A 64 bit counter that increments once per microsecond for measuring time delays and duration
  - A 32 bit numerically controller oscillator (NCO) whose 1 Megahertz output frequency can be controlled to better than a part per billion
  - The ability to phase lock the NCO to the 1 PPS output of a GPS receiver
- MBARI plans to implement IEEE-1588 using the hardware mentioned above to limit the time skew among mooring controller clocks to less than one millisecond.

Lessons Learned

- Adding power management to existing Linux drivers was difficult.
- Application CPU's Phase Locked Loop was challenging to use:
  - 60 MHz to 206 MHz in 60 MHz steps is too coarse to minimize overall power consumption.
  - 150 millisecond lock time limits the usefulness of sleep mode
- Generating all the required voltages, efficiently and in the smallest possible area was difficult.
- SDRAM still is power hungry, but things are improving.
- FPGA technology is ideal for hardware flexibility but the quiescent current is very high. SideARM was limited to using less dense CPLD like devices.