DPA SPI interface Specification

The purpose of this document is to describe the interface of the DPA board. This board communicates with its controller via a SPI interface. The bus uses a 16 bit word with positive edge sampled data. The basic data format is as follows:

Bit	Description
15:12	Command
11:0	Arguments

The defined commands are given in Table 1.

Table 1 DPA commands

Commands	Function
0	Channel 1 Dpot write
1	Channel 2 Dpot write
2	Channel 1 relays
3	Channel 2 relays
4	Start ADC
5	Set interrupt flags
6	Set channel 1 controls
7	Set channel 2 controls
8	Unused
9	Read channel 1 relay positions
10	Read channel 2 relay positions
11	Read ADC value
12	Read Interrupt flags
13	Read channel 1 controls
14	Read channel 2 controls
15	Busy

Each of these commands is described in the following sections. The interface uses a simple single instruction, processing scheme in which each command must be completed before the next can be processed. This is accomplished with a busy indicator. The busy indicator may be read through the busy command (15) and will be returned on any command attempted while the interface is busy. The busy response is defined as hex 7FFF. If at any time a read or write is performed, the busy string is returned the interface is busy and will have ignored the incoming information. The basic algorithm for accessing the DPA is shown in figure 1.

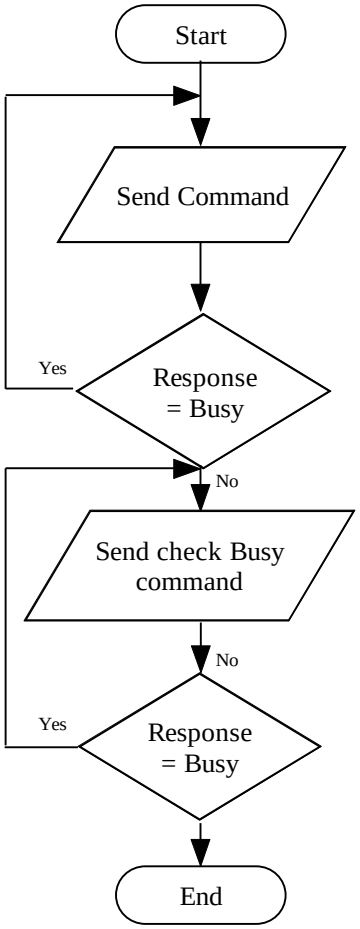

Start
Send Command
Response
= Busy
Yes
No
Send check Busy
command
No
Response
= Busy
Yes
End

Figure 1

DPA initialization

Upon power-up there are a few items which need to be completed to synchronize the state of the host, DPA interface and the latching relays. This section describes these steps and the order in which they should be preformed. At power up the interface sets up each channel as shown in table x.

Function	**State**
Power	Off
Communications power	Off
Slew rate	Slow
Duplex	Full
Mode	RS-232
Interrupts	All disabled
ADC	TBD
DPOTS	Loaded from EEPROM
Relays	In last state (unknown, assume state value of 0)

The suggested initialization steps are as follows:

1) Set ADC to Stand-By mode, command 4 argument 58 hex, (4058). This generates a conversion on channel 0, which may be ignored.
2) Set relay Positions for Channel 0 and 1.
3) Set the over current threshold value in Dpot. Use dpot command and run all to full 0, command 0 argument 64, command 0 with number of counts up to desired level. Repeat for channel 2, command 1 argument 64, and then command 1 argument to move up required counts.
4) Configure communications to required configuration. Set mode, duplex, and slew rate.
5) Enable required interrupts
6) At this point the attached instrument is ready to be powered. To do this the instrument isolation relay must be first closed and then power may be applied, along with the communications power.

Dpot

The Dpot commands provides control of the two dpots on the DPA. The wiper position may be moved to any of its 100 locations by specifying the number of position to move and the direction (up/down). This position may be saved at the end by moving the wiper and asserting the save bit. This will, at the end of the move causes the dpot to store its current location in to its EEPROM. Further power cycles will cause the dpot to reload this value automatically. The dpots generate the overcurrent trip level for the channel. This value is calculated with the following equation:

$$I_{trip} = 0.12A/count.$$

There is no feedback as to the current position of the Dpot. This must be kept track of by the host.

Channel 1Dpot Write (CMND = 0)
Channel 2Dpot Write (CMND = 1)

Table 2 Dpot command arguments

Bit	Arguments
11:9	Unused
8	Up/Down (Up = 1, Down = 0)
7	Save position (Save = 1)
6:0	Count (Range = 0 to 100)

Set and read Relay commands

These two command types allow the host to set the position of the 6 latching relays on the DPA board and query their positions. Since these relays are latching a single pulse is required to switch them from one state to the other. Due to this setup there in no way of knowing the current state of the relay, and because of this the DPA does not know the state of the relay at power but assumes a zero state. To ensure the relay is in the correct position the relay must be toggled away from the desired position and then back which will then synchronize the internal state machines with the relay. The interface will only generate pulses if the new state differs from the current position the interface believes the relay to be in.

Set channel 1 relays (CMND = 2)
Set channel 2 relays (CMND = 3)
Read channel 1 relays (CMND = 10)
Read channel 2 relays (CMND = 11)

Table 3 Set and Read Relay commands

Bit	Arguments
11:3	Unused
2	485 Terminators (1 = terminators connected)
1	Communications (1 = Isolated)
0	Instrument Power (1= Isolated)

Channel Control Commands

The state of the channels may be read and writing using these commands. These commands provide for configuring the communications and instrument power.

Set channel 1 (CMND = 6)
Set channel2 (CMND = 7)
Read channel 1 (CMND = 13)
Read channel 2 (CMND = 14)

Bit	Arguments
11:6	0
5	Serial direction (1= on, 0 = Low Power)
4	Comm Fast (Fast = 1, SRL = 0)
3	Comm Mode (485 = 1, 232 = 0)

2	Comm Duplex (Half = 1, Full = 0)
1	Communications power (On = 1, Off = 0)
0	Instrument Power (1 = on)

ADC control

ADC control is provided by these commands. The ADC is a 12-bit 8 channel parallel converter. The PLD on the DPA, with a start command, starts the ADC and then reads the values from it and stores it internally. At the end of this conversion the DPA port is released and the value may be read at any time from the port using the read ADC command. The ADC's input voltage range is:

0 to 2.5V in Unipolar Mode,
-1.25 to +1.25 in Biploar Mode.

The ADC may be run in one of two modes, Internal or External acquisition mode. This is controlled by bit 5 (ACQMOD) of the control word. Using external acquisition mode the ADC selects the requested channel and then waits for an internal acquisition command to do the actual conversion. This is to allow a channel time to settle.

ADC start (CMND = 4)

Bit	Arguments
11:8	0
7	PD1
6	PD0
5	ACQMOD (Ext = 1, Int = 0)
4	SGL/DIF (Single = 1, Differential = 0)
3	Uni/Bi (Unipolar = 1, Bipolar = 0)
2	Ch Address 2
1	Ch Address 1
0	Ch Address 0

Refer to following table for definitions of the ADC configuration bits.

BIT	NAME	FUNCTION		
D7, D6	PD1, PD0	**PD1** and **PD0** select the various clock and power-down modes.		
		0	**0**	Full Power-Down Mode. Clock mode is unaffected.
		0	**1**	Standby Power-Down Mode. Clock mode is unaffected.
		1	**0**	Normal Operation Mode. Internal clock mode selected.
		1	**1**	Normal Operation Mode. External clock mode selected.
D5	ACQMOD	ACQMOD = 0: Internal Acquisition Mode ACQMOD = 1: External Acquisition Mode		
D4	SGL/$\overline{DIF}$	SGL/$\overline{DIF}$ = 0: Pseudo-Differential Analog Input Mode SGL/$\overline{DIF}$ = 1: Single-Ended Analog Input Mode In single-ended mode, input signals are referred to COM. In pseudo-differential mode, the voltage difference between two channels is measured (see Tables 2, 3).		
D3	UNI/$\overline{BIP}$	UNI/$\overline{BIP}$ = 0: Bipolar Mode UNI/$\overline{BIP}$ = 1: Unipolar Mode In unipolar mode, an analog input signal from 0 to V_{REF} can be converted; in bipolar mode, the signal can range from $-V_{REF}/2$ to $+V_{REF}/2$.		
D2, D1, D0	A2, A1, A0	Address bits A2–A0 select which of the 8/4 (MAX1291/MAX1293) channels are to be converted (see Tables 3, 4).		

ADC Read (CMND = 11)

Bit	Arguments
11:0	ADC value

The ADC channel assignments are given below

Channel	Function
7	Battery Supply Voltage Vbat=5.8*Vin
6	Channel 2 voltage Sense Vinstr = 6*Vin
5	Channel 2 trip level sense
4	Channel 2 current sense
3	Heat-sink Temperature
2	Channel 1 voltage Sense Vinstr = 6*Vin
1	Channel 1 trip level sense
0	Channel 1 current sense

Interrupt

The interrupt register provides control of the interrupt subsystem. There are two sources of interrupts on the DPA, Channel 1 and 2 overcurrent. Each of these interrupts may be enabled or disabled individually, along with the global interrupt. If a system interrupt has been received a read interrupt command will return the current flag settings along with the interrupt flags to determine the source and cause of the interrupt. A read will not reset the interrupt. To clear the interrupt, either the interrupt must be disable or the power to the overcurrented channel must be turned off. This action is much like a mechanical breaker, which must be reset before powering on.

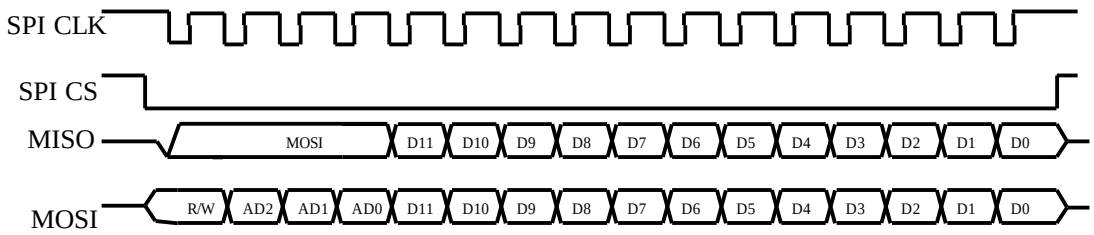
Set Interrupt flags (CMND = 5)
Read Interrupt Flags (CMND = 12)

Bit	Read command	Write command
11:6	0	0

5	CH1 overcurrent enable	CH1 overcurrent enable
4	CH2 overcurrent enable	CH2 overcurrent enable
3	Global enable	Global enable
2	CH1 overcurrent flag	0
1	CH2 overcurrent flag	0
0	Global flag	0

Hardware interface protocol

The hardware interface assumes that the data from the master is available to be clocked in on the rising of the spi clock signal. The interface provides valid data to the master updated on the falling edge, and to be clocked in on the rising edge of the spi clock.



Revision History

11/29/01 – original Document
12/07/01 – Update command format table to match rest of document
- Changed Initialization to reflect that relays do not need to be flopped to sync
- Changed Dpot write arguments to swap Save and UD.

3/05/03 - Corrected misspellings