P-Channel 30-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.0075 @ V_{GS} = -10 V	-17

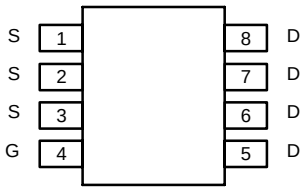
FEATURES

- TrenchFET® Power MOSFETS
- 100% R_g Tested

APPLICATIONS

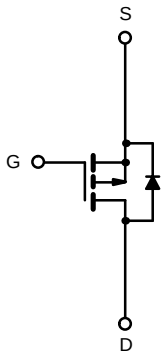
- Battery and Load Switching
  - Notebook Computers
  - Notebook Battery Packs

SO-8



Top View

Ordering Information: Si4405DY
Si4405DY-T1 (with Tape and Reel)



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C UNLESS OTHERWISE NOTED)					
Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V_{DS}	-30		V
Gate-Source Voltage		V_{GS}	±20		
Continuous Drain Current (T_J = 150°C)[a]	T_A = 25°C	I_D	-17	-11	A
	T_A = 70°C		-13	-9	
Pulsed Drain Current		I_{DM}	-60		
continuous Source Current (Diode Conduction)[a]		I_S	-2.9	-1.30	
Maximum Power Dissipation[a]	T_A = 25°C	P_D	3.5	1.6	W
	T_A = 70°C		2.1	1.0	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient[a]	t ≤ 10 sec	R_{thJA}	29	35	°C/W
	Steady State		67	80	
Maximum Junction-to-Foot (Drain)	Steady State	R_{thJF}	13	16	

Notes
a. Surface Mounted on 1" x 1" FR4 Board.

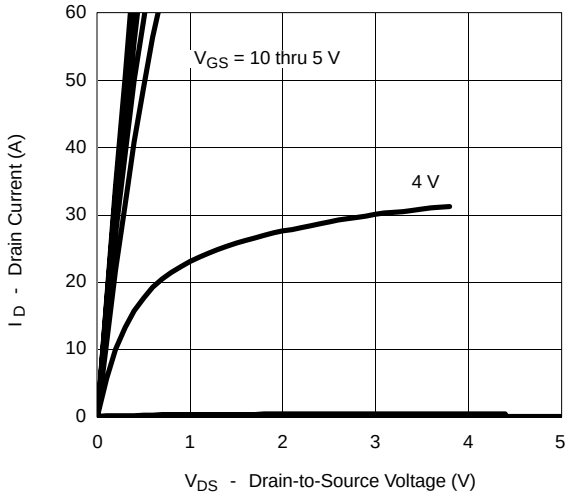
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = -250 μA	-1.0		-3.0	V
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -24 V, V_{GS} = 0 V			-1	μA
		V_{DS} = -24 V, V_{GS} = 0 V, T_J = 70°C			-10	
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = -5 V, V_{GS} = -10 V	-30			A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = -10 V, I_D = -17 A		0.006	0.0075	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = -15 V, I_D = -17 A		47		S
Diode Forward Voltage[a]	V_{SD}	I_S = -2.9 A, V_{GS} = 0 V		-0.75	-1.1	V
Dynamic[b]						
Total Gate Charge	Q_g	V_{DS} = -15 V, V_{GS} = -10 V, I_D = -17 A		105	160	nC
Gate-Source Charge	Q_{gs}			17.5		
Gate-Drain Charge	Q_{gd}			29.5		
Gate Resistance	R_g		3	4	6.5	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -15 V, R_L = 15 Ω I_D ≅ -1 A, V_{GEN} = -10 V, R_G = 6 Ω		25	40	ns
Rise Time	t_r			15	25	
Turn-Off Delay Time	$t_{d(off)}$			190	285	
Fall Time	t_f			80	120	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = -2.9 A, di/dt = 100 A/μs		70	110	

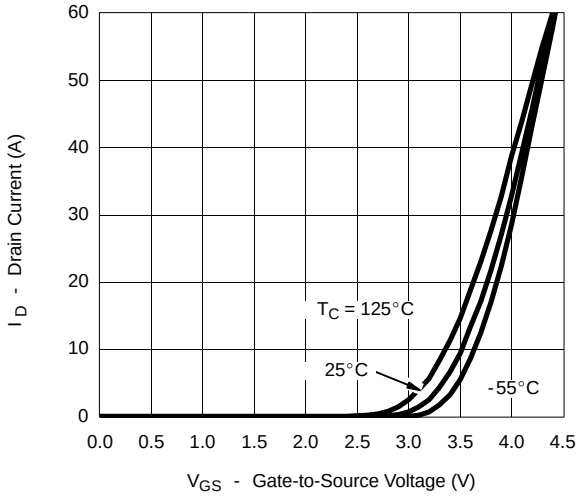
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Output Characteristics

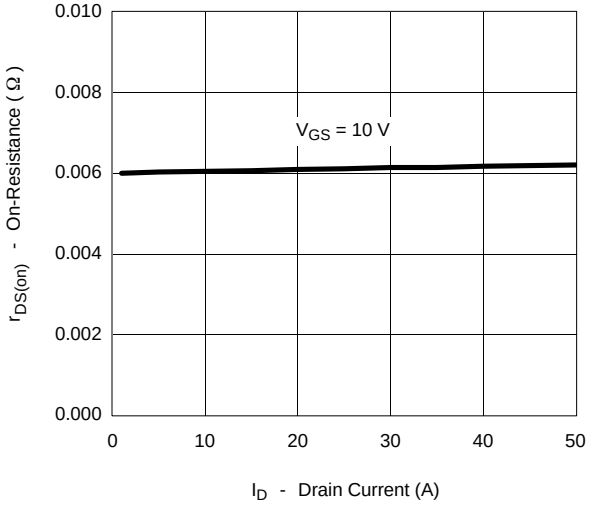


Transfer Characteristics

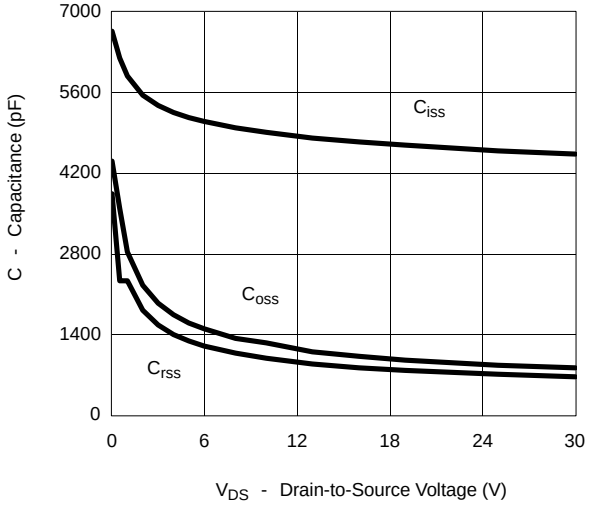


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

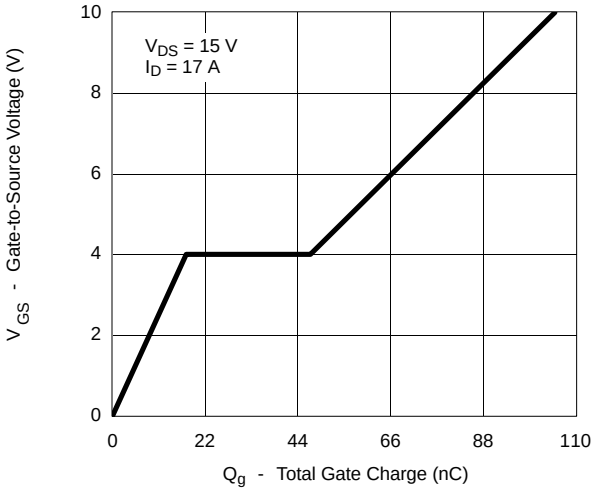
On-Resistance vs. Drain Current



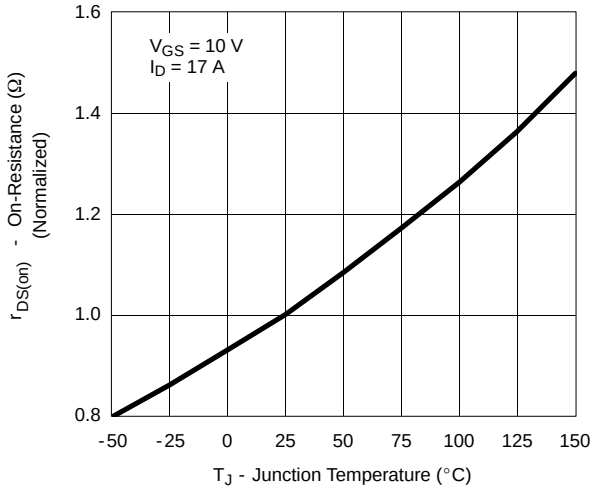
Capacitance



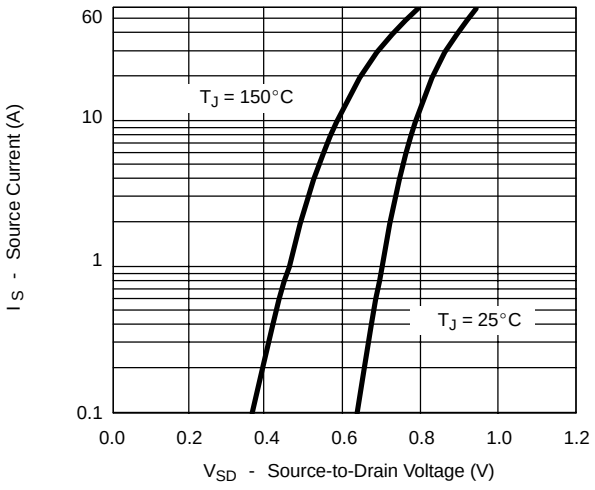
Gate Charge



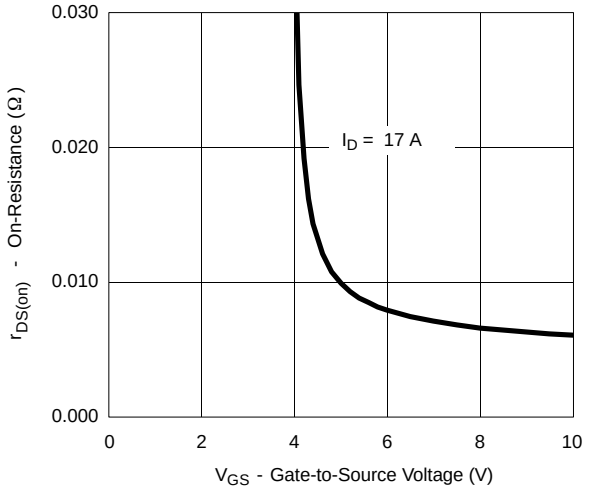
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

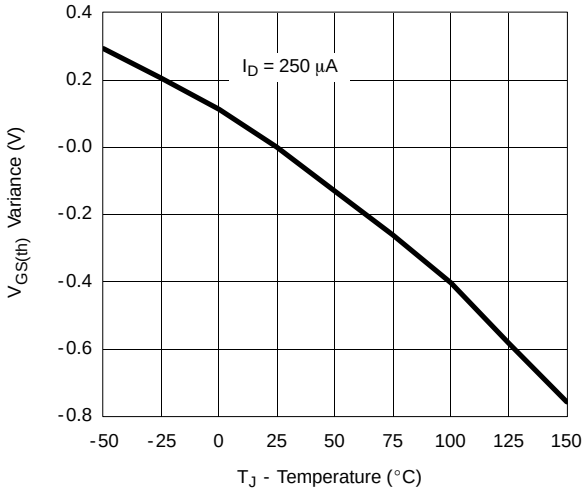


On-Resistance vs. Gate-to-Source Voltage

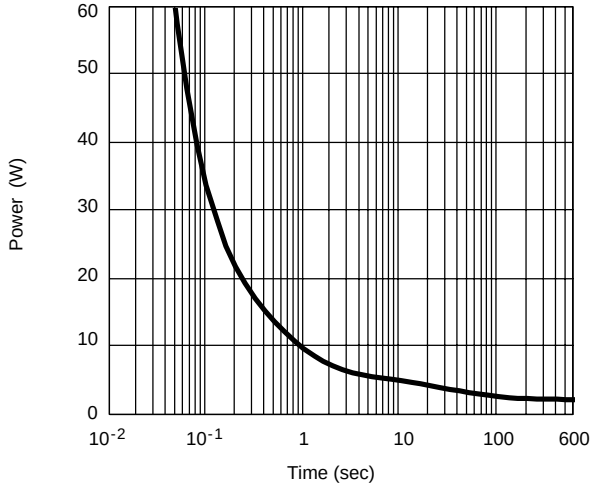


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

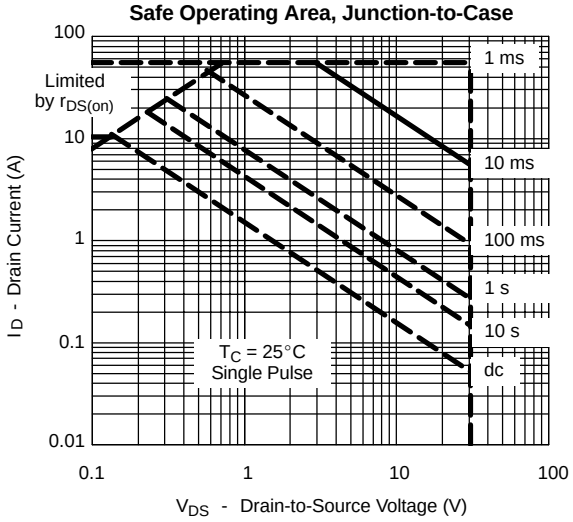
Threshold Voltage



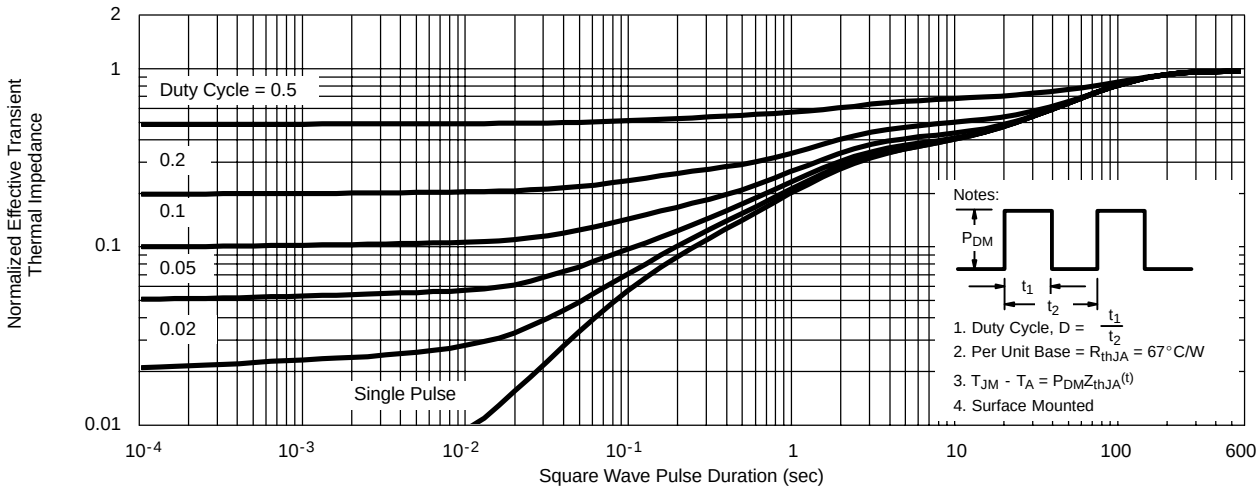
Single Pulse Power



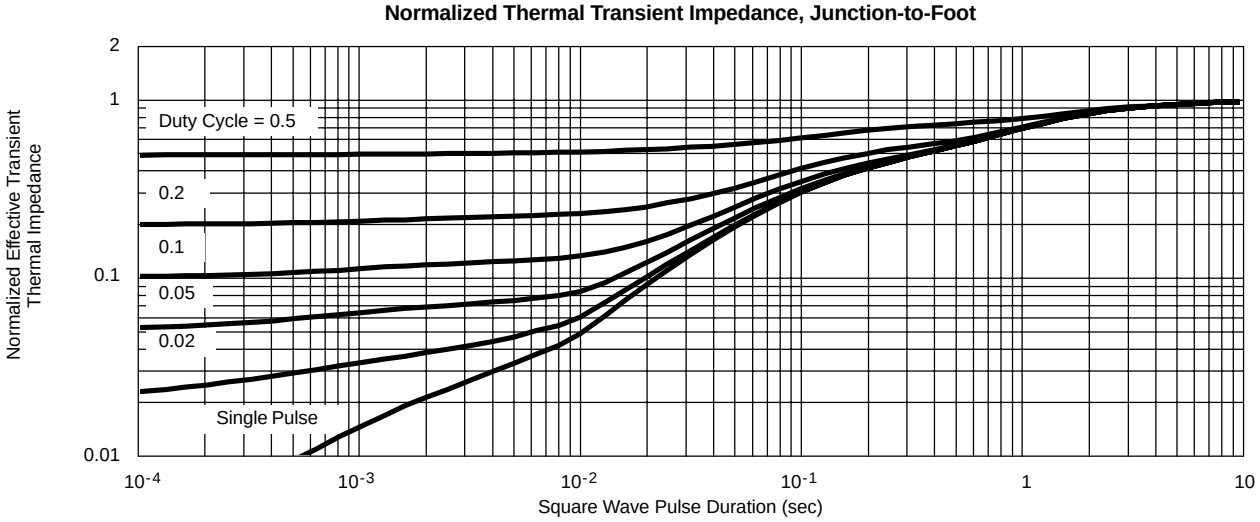
Safe Operating Area, Junction-to-Case



Normalized Thermal Transient Impedance, Junction-to-Ambient



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



ENVIRONMENTAL AND PACKAGE TESTING DATA FOR SO-8 SOLDER PROCESS					
Stress	**Sample Size**	**Device Hr./Cyc**	**Condition**	**Total Fails**	**Fail Percentage**
BOND INT	300	150,000	200°C + N2	0	0.00
HAST	2,102	207,450	130°C, 85%RH	0	0.00
Power Cycle	306	4,204,320	DELTA T_j = 100	0	0.00
Pressure Pot	7,514	754,764	121°, 15 PSIG	0	0.00
Solder DUNK	1,000	3,000	260°C, 10SEC	0	0.00
Solderability	255	2,040	883 M2003	0	0.00
Temp Cycle	15,170	6,357,500	–65°C–150°C	0	0.00
Thermal Shock	200	20,000	–60°C–150°C	0	0.00

P-CHANNEL ACCELERATED OPERATING LIFE TEST RESULT	
Sample Size	42,968
Equivalent Device Hours	5,074,566,845
Number of Total Failures	0
Failure Rate in FIT	0.179

Failure Rate in FIT is calculated according to JEDEC Standard JESD85, *Methods for Calculating Failure Rates in Units of FITs*, based on accelerated high temperature operating life test results by using an apparent activation energy of 0.7 eV. The junction temperature of the device at use is assumed to be 55°C. A constant failure rate distribution is assumed. The upper confidence bound of the failure rate is 60%.

P-Channel 30-V (D-S) MOSFET

CHARACTERISTICS

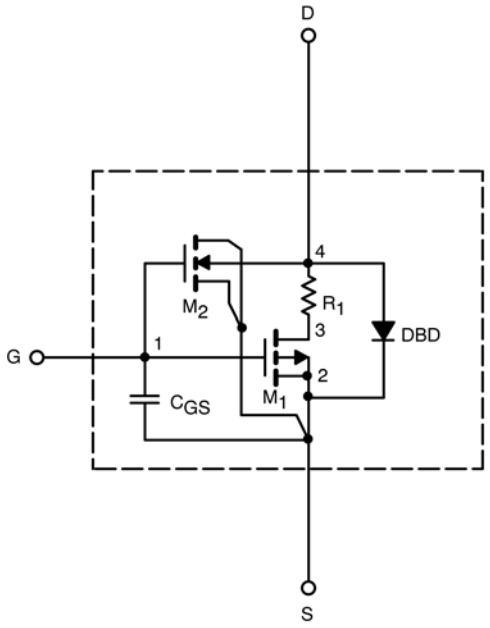
- P-Channel Vertical DMOS
- Macro Model (Subcircuit Model)
- Level 3 MOS
- Apply for both Linear and Switching Application
- Accurate over the −55 to 125°C Temperature Range
- Model the Gate Charge, Transient, and Diode Reverse Recovery Characteristics

DESCRIPTION

The attached spice model describes the typical electrical characteristics of the p-channel vertical DMOS. The subcircuit model is extracted and optimized over the −55 to 125°C temperature ranges under the pulsed 0-V to 10-V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched C_{gd} model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

SUBCIRCUIT MODEL SCHEMATIC

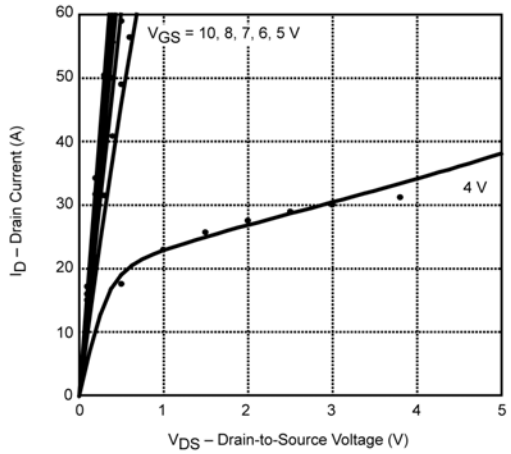


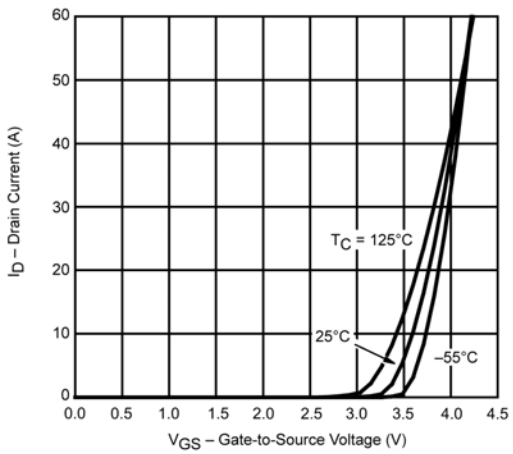
This document is intended as a SPICE modeling guideline and does not constitute a commercial product data sheet. Designers should refer to the appropriate data sheet of the same number for guaranteed specification limits.

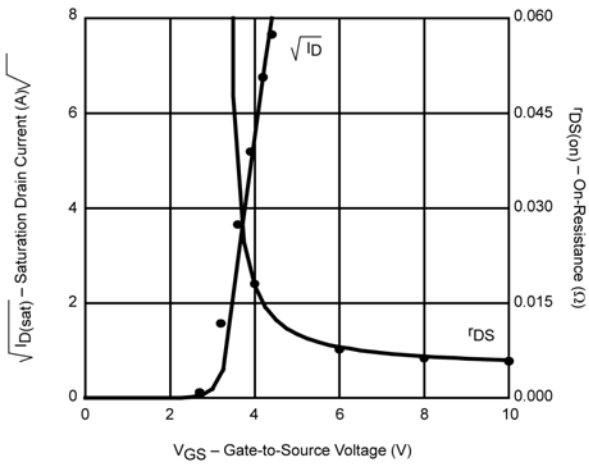
SPECIFICATIONS (T_J = 25°C UNLESS OTHERWISE NOTED)					
Parameter	**Symbol**	**Test Condition**	**Simulated Data**	**Measured Data**	**Unit**
Static					
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = –250 μA	2.5		V
On-State Drain Current[a]	$I_{D(on)}$	V_{DS} = –5 V, V_{GS} = –10 V	780		A
Drain-Source On-State Resistance[a]	$r_{DS(on)}$	V_{GS} = –10 V, I_D = –17 A	0.006	0.006	Ω
Forward Transconductance[a]	g_{fs}	V_{DS} = –15 V, I_D = –17 A	84	47	S
Diode Forward Voltage[a]	V_{SD}	I_S = –2.9 A, V_{GS} = 0 V	–0.82	–0.75	V
Dynamic[b]					
Total Gate Charge	Q_g	V_{DS} = –15 V, V_{GS} = –10 V, I_D = –17 A	100	105	nC
Gate-Source Charge	Q_{gs}		17.5	17.5	
Gate-Drain Charge	Q_{gd}		29.5	29.5	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = –15 V, R_L = 10 Ω I_D ≅ –1 A, V_{GEN} = –10 V, R_G = 6 Ω	43	25	ns
Rise Time	t_r		29	15	
Turn-Off Delay Time	$t_{d(off)}$		184	190	
Fall Time	t_f		60	80	
Source-Drain Reverse Recovery Time	t_{rr}	I_F = –2.9 A, di/dt = 100 A/μs	49	70	

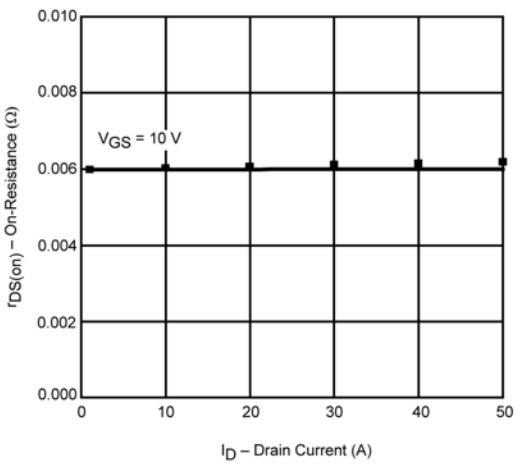
Notes
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
b. Guaranteed by design, not subject to production testing.

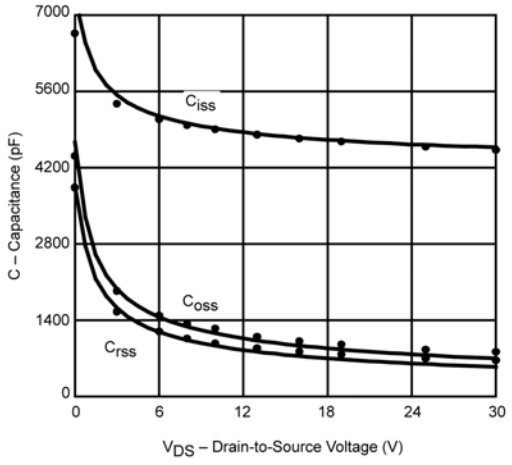
COMPARISON OF MODEL WITH MEASURED DATA (T_J=25°C UNLESS OTHERWISE NOTED)

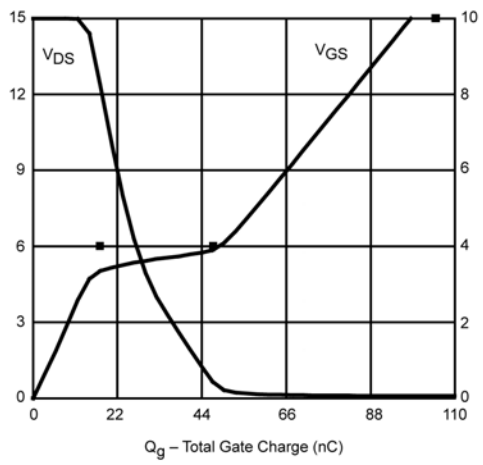








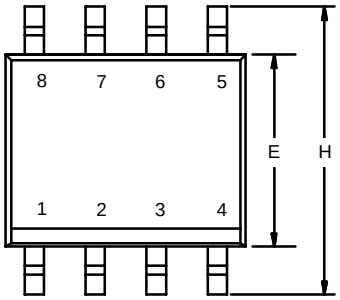




Note: Dots and squares represent measured data.

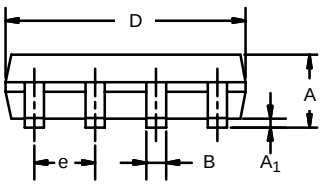
SOIC (NARROW): 8-LEAD

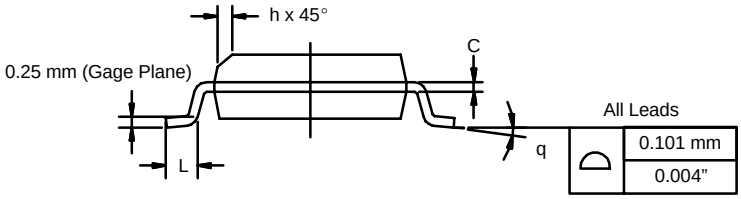
JEDEC Part Number: MS-012



Dim	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A_1	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°

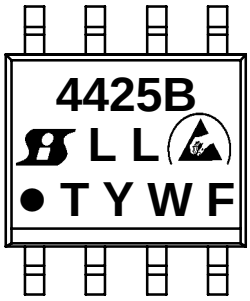
ECN: T-04451—Rev. H, 30-Aug-04
DWG: 5498





DEVICE: SO-8

SO-8 Devices



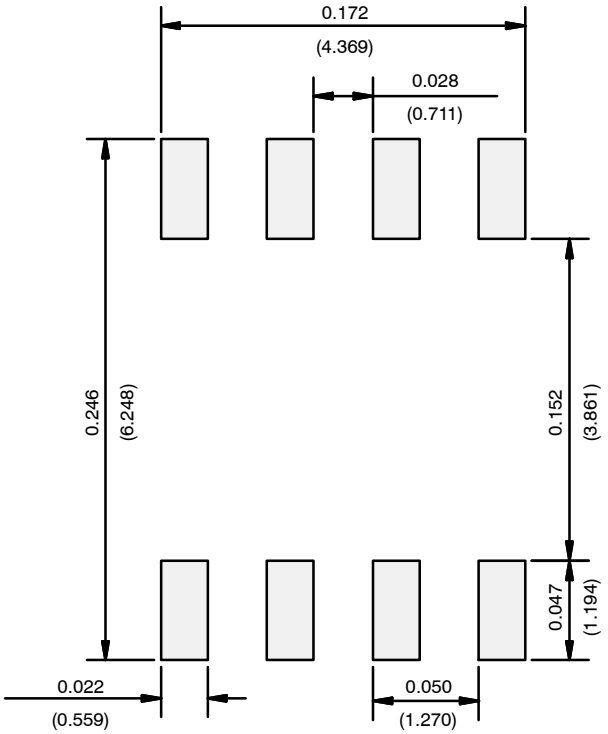
4425	**=**	**Example Base Part Number** [1]
B	**=**	**Revision if applicable, where part number format is Si4425BDY for example.**
	=	**Siliconix Logo**
LL	**=**	**Lot Code**
	=	**ESD Symbol**
●	**=**	**Pin 1 Indicator**
T	**=**	**Assembly Factory Code**
Y	**=**	**Year Code**
W	**=**	**Week Code**
F	**=**	**Wafer Fab Code**

NOTE:

1. For analog switches base part includes DG prefix. Package suffix may or may not be present, depending on room available.

The current marking strategy is reflected. Contact your local sales representative for historical marking strategies for these packages.

RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads
Dimensions in Inches/(mm)

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Mounting LITTLE FOOT® SO-8 Power MOSFETs

Wharton McDaniel

Surface-mounted LITTLE FOOT power MOSFETs use integrated circuit and small-signal packages which have been been modified to provide the heat transfer capabilities required by power devices. Leadframe materials and design, molding compounds, and die attach materials have been changed, while the footprint of the packages remains the same.

See Application Note 826, *Recommended Minimum Pad Patterns With Outline Drawing Access for Vishay Siliconix MOSFETs*, (http://www.vishay.com/doc?72286), for the basis of the pad design for a LITTLE FOOT SO-8 power MOSFET. In converting this recommended minimum pad to the pad set for a power MOSFET, designers must make two connections: an electrical connection and a thermal connection, to draw heat away from the package.

In the case of the SO-8 package, the thermal connections are very simple. Pins 5, 6, 7, and 8 are the drain of the MOSFET for a single MOSFET package and are connected together. In a dual package, pins 5 and 6 are one drain, and pins 7 and 8 are the other drain. For a small-signal device or integrated circuit, typical connections would be made with traces that are 0.020 inches wide. Since the drain pins serve the additional function of providing the thermal connection to the package, this level of connection is inadequate. The total cross section of the copper may be adequate to carry the current required for the application, but it presents a large thermal impedance. Also, heat spreads in a circular fashion from the heat source. In this case the drain pins are the heat sources when looking at heat spread on the PC board.

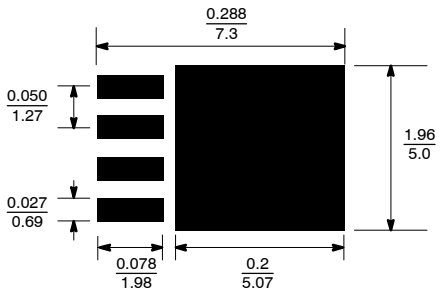

FIGURE 1. Single MOSFET SO-8 Pad Pattern With Copper Spreading

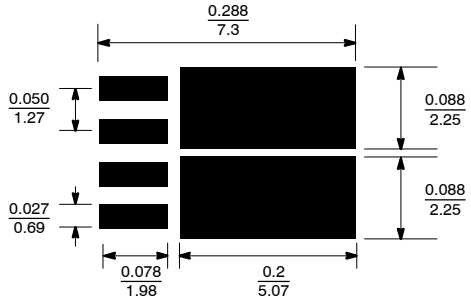

FIGURE 2. Dual MOSFET SO-8 Pad Pattern With Copper Spreading

The minimum recommended pad patterns for the single-MOSFET SO-8 with copper spreading (Figure 1) and dual-MOSFET SO-8 with copper spreading (Figure 2) show the starting point for utilizing the board area available for the heat-spreading copper. To create this pattern, a plane of copper overlies the drain pins. The copper plane connects the drain pins electrically, but more importantly provides planar copper to draw heat from the drain leads and start the process of spreading the heat so it can be dissipated into the ambient air. These patterns use all the available area underneath the body for this purpose.

Since surface-mounted packages are small, and reflow soldering is the most common way in which these are affixed to the PC board, “thermal” connections from the planar copper to the pads have not been used. Even if additional planar copper area is used, there should be no problems in the soldering process. The actual solder connections are defined by the solder mask openings. By combining the basic footprint with the copper plane on the drain pins, the solder mask generation occurs automatically.

A final item to keep in mind is the width of the power traces. The absolute minimum power trace width must be determined by the amount of current it has to carry. For thermal reasons, this minimum width should be at least 0.020 inches. The use of wide traces connected to the drain plane provides a low impedance path for heat to move away from the device.