

File: g:\VSS_Projects\work\sjensen\DPA\HDL_project\src\Dpot_counter.v

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1  *****
2  ****//
3  // file : c:\projects\nmc\DPA\hdl\DPainterface\src\Dpot_counter.v
4  // created Tue Oct 30 06:46:09 2001
5  // by ITF2V generator version 1.0
6  *****
7  ****//
8
9  //{{ Section below this comment is automatically maintained
10 // and may be overwritten
11 //{module {Dpot_counter}}
12 module Dpot_counter ( Count ,Counter_Zero ,Enable_count ,
13 Load_counter ,clk ,reset );
14
15 input [6:0] Count ;
16 wire [6:0] Count ;
17 input Enable_count ;
18 wire Enable_count ;
19 input Load_counter ;
20 wire Load_counter ;
21 input clk ;
22 wire clk ;
23 input reset ;
24 wire reset ;
25
26 output Counter_Zero ;
27 wire Counter_Zero ;
28
29 //}} End of automatically maintained section
30 // -- Enter your statements here -- //
31
32 reg [7:0] counter;
33
34 assign Counter_Zero = (counter <= 7'd1); //this flags end of
35 counting to dpot control
36
37 always @ (posedge reset or posedge clk)
38 begin
39     if (reset) counter <= 7'd0; //reset counter
40     else if (Load_counter) counter <= {Count, 1'b0}; //if it is
41 load time then load with 2n+1
42     else if (Enable_count) //if counter is enabled count to zero
43 and hold
44         if (counter != 7'd0) counter <= counter - 7'b1;
45         else counter <= 7'd0;
46     else counter <= counter; //just hold till enable counter
47 end
48
49 endmodule
50
```