

File: g:\VSS_Projects\work\sjensen\DPA\HDL_project\src\Pulse_generator.v

```
1  *****
   ****//
2  // file : c:\projects\nmc\DPA\hdl\DPAinterface\src\Pulse_generator.v
3  // created Tue Oct 30 08:18:00 2001
4  // by ITF2V generator version 1.0
5  *****
   ****//
6
7  `timescale 1ps / 1ps
8
9  //{{ Section below this comment is automatically maintained
10 // and may be overwritten
11 //{module {Pulse_generator}}
12 module Pulse_generator ( Pulse ,Pulse_end ,Pulse_request ,reset ,clk
   );
13
14 input Pulse_request ;
15 wire Pulse_request ;
16 input reset ;
17 wire reset ;
18 input clk ;
19 wire clk ;
20
21 output Pulse ;
22 reg Pulse ;
23 output Pulse_end ;
24 reg Pulse_end ;
25
26 //}} End of automatically maintained section
27
28 // -- Enter your statements here -- //
29 parameter Pulse_start = 11'd1638;
30
31 reg [10:0] count;
32
33 //Whe count == 0 and Pulse_request is true then load counter with
Pulse_start
34 //and start counting down to 0 and then hold.
35 always @ (posedge reset or posedge clk)
36     begin
37         if (reset) count <= 11'b0;
38         else if ((count == 11'b0) && (Pulse_request)) count <=
Pulse_start;
39         else if (count != 11'b0) count <= count - 1'b1;
40         else count <= 11'b0;
41     end
42
43 //as long as count does not equal zero then pulse is true
44 always @ (posedge reset or posedge clk)
45     begin
46         if (reset) Pulse <= 1'b0;
47         else if (count > 11'b1) Pulse <= 1'b1;
48         else Pulse <= 1'b0;
49     end
50
51 //Pulse end is one clock long and is used to update the relay
position
```

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```
52  // and clear the DAVE flag
53  always @ (posedge reset or posedge clk)
54      begin
55          if (reset) Pulse_end <= 1'b0;
56          else if (count != 11'd2) Pulse_end <= 1'b0;
57          else Pulse_end <= 1'b1;
58      end
59  endmodule
60
```