

File: g:\VSS_Projects\work\sjensen\DPA\HDL_project\src\interrupt_generator.v

```
1  //*****
   ****//
2  // file : G:\VSS_Projects\work\sjensen\DPA\hdl\DPainterface\src\interrupt_gene
   rator.v
3  // created Wed Oct 31 13:17:43 2001
4  // by ITF2V generator version 1.0
5  //*****
   ****//
6
7  `timescale 1ps / 1ps
8
9  /**{ Section below this comment is automatically maintained
10   and may be overwritten
11 /**module {interrupt_generator}}
12 module interrupt_generator ( ch1_oc ,ch2_oc ,flags_in ,flags_out ,
   intr ,rd_intr ,reset );
13
14 input ch1_oc ;
15 wire ch1_oc ;
16 input ch2_oc ;
17 wire ch2_oc ;
18 input [5:3] flags_in ;
19 wire [5:3] flags_in ;
20 input reset ;
21 wire reset ;
22
23 output [2:1] flags_out ;
24 wire [2:1] flags_out ;
25 output intr ;
26 wire intr ;
27 output rd_intr ;
28 wire rd_intr ;
29
30 /**} End of automatically maintained section
31
32 // -- Enter your statements here -- //
33
34 wire interim;
35
36 assign flags_out[1] = (!ch1_oc);
37 assign flags_out[2] = (!ch2_oc);
38 assign rd_intr = (flags_out[1] | flags_out[2]);
39 assign intr = ((flags_in[3]==1'b1) && ((flags_out[1] & flags_in[4])
   || (flags_out[2] & flags_in[5]))) ? 1'b0 : 1'bz;
40
41
42 endmodule
43
```