



Magnetic-Less Ethernet

Point-to-Point Ethernet over a Backplane

Application Note

March 2001

Order Number: [249490-001](#)



Information in this document is provided in connection with Intel® products. No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document. Except as provided in Intel's Terms and Conditions of Sale for such products, Intel assumes no liability whatsoever, and Intel disclaims any express or implied warranty, relating to sale and/or use of Intel products including liability or warranties relating to fitness for a particular purpose, merchantability, or infringement of any patent, copyright or other intellectual property right. Intel products are not intended for use in medical, life saving, or life sustaining applications.

Intel may make changes to specifications and product descriptions at any time, without notice.

Designers must not rely on the absence or characteristics of any features or instructions marked "reserved" or "undefined." Intel reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

The Intel Ethernet Transceivers may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

Contact your local Intel sales office or your distributor to obtain the latest specifications and before placing your product order.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature may be obtained by calling 1-800-548-4725 or by visiting Intel's website at <http://www.intel.com>.

Copyright © Intel Corporation, 2001

*Third-party brands and names are the property of their respective owners.

Contents

1.0	Introduction	5
1.1	Intel Fast Ethernet Products	5
1.1.1	Single-Port Transceivers	5
1.1.2	Multi-Port Transceivers	5
1.1.3	Repeaters	5
1.2	Twisted-Pair Interface	6
2.0	Magnetic-Less Termination Networks	7
2.1	LXT971A/972A, LXT9761/62/63, LXT9781/82, LXT9860/80, and LXT9863/83	7
2.2	LXT9784 Fast-Ethernet, Octal Transceiver with RMII/SMII and Auto-MDIX	9
2.3	LXT9785 Fast-Ethernet, Octal Transceiver with RMII, SMII, SS/SMII, and Auto-MDIX	10
2.4	Hybrid Configuration	13
3.0	Validation Testing	13
3.1	Testing Summary	14
4.0	Recommendations	15
5.0	Summary	15

Figures

1	Typical Twisted-Pair Transceiver Interface	6
2	Point-to-Point Ethernet	7
3	LXT971A/972A, LXT9761/62/63, LXT9781/82, LXT9860/80, and LXT9863/83 Receiver Termination	8
4	LXT971A/972A, LXT9761/62/63, LXT9781/82, LXT9860/80, and LXT9863/83 Transmitter Termination	8
5	LXT9784 Typical Ethernet Interface	9
6	LXT9784 Receiver Termination	10
7	LXT9784 Transmitter Terminations	10
8	LXT9785 Typical Ethernet Interface	11
9	LXT9785 Receiver Termination	12
10	LXT9785 Transmitter Termination	12
11	Hybrid Interface Representing LXT971A/972A, LXT9761/62/63, LXT9781/82 and LXT98xxx	13
12	100 Mbps Eye Pattern at LXT971A Transmitter Output Terminated into 100Ω	14
13	100 Mbps Eye Pattern at LXT971A Receiver Input at 1-Meter Cable End	14

Revision History

Date	Revision	Page #	Description
March 2001	001		Initial Release.

1.0 Introduction

This application note provides information and design-specific considerations for system designers interested in implementing point-to-point Ethernet over proprietary, printed circuit board (PCB) backplanes. The typical application configurations shown are implemented using Intel's most recent and popular IEEE 802.3-compliant, 10/100 Fast Ethernet Transceivers.

This application note assumes the reader is familiar with Fast Ethernet, and focuses on the twisted-pair interface and interoperability between the selected transceivers.

Since the Ethernet transceiver applications described here are non-standard, the reader should understand that the resulting configurations are not meant to imply that the magnetic-less interface meets the full intent of compliance to the IEEE 802.3 specification.

1.1 Intel Fast Ethernet Products

This application note covers the following, newer generation of Intel Fast Ethernet products:

1.1.1 Single-Port Transceivers

- LXT971A — 3.3V Single Fast Ethernet Transceiver with support for Fiber
- LXT972A — 3.3V Single Fast Ethernet Transceiver

1.1.2 Multi-Port Transceivers

- LXT9761 — 3.3V Hex Fast Ethernet Transceiver with RMII
- LXT9762 — 3.3V Hex Fast Ethernet Transceiver with SMII
- LXT9763 — 3.3V Hex Fast Ethernet Transceiver with MII
- LXT9781 — 3.3V Octal Fast Ethernet Transceiver with RMII
- LXT9782 — 3.3V Octal Fast Ethernet Transceiver with SMII
- LXT9784 — 3.3/3.0V Octal Fast Ethernet Transceiver with RMII/SMII and Auto-MDIX
- LXT9785 — 2.5V Octal Fast Ethernet Transceiver with RMII, SMII, SS/SMII, and Auto-MDIX

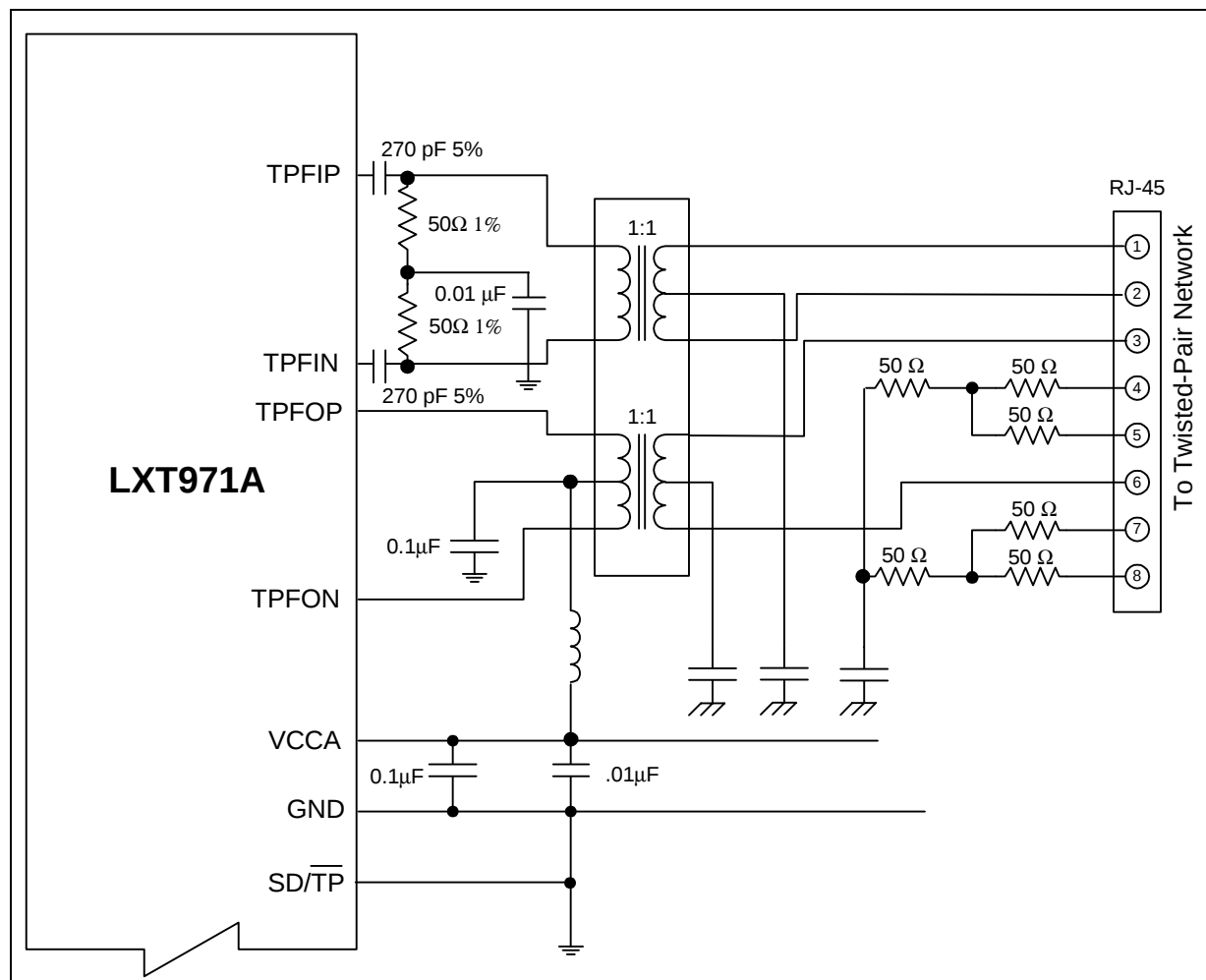
1.1.3 Repeaters

- LXT9860 — 3.3V Advanced 10/100 Repeater with Integrated Management (Hex)
- LXT9880 — 3.3V Advanced 10/100 Repeater with Integrated Management (Octal)
- LXT9863 — 3.3V Advanced 10/100 Unmanaged Repeater (Hex)
- LXT9883 — 3.3V Advanced 10/100 Unmanaged Repeater (Octal)

1.2 Twisted-Pair Interface

The transceivers described here are IEEE-compliant, Fast-Ethernet, physical layer (PHY) devices that directly support 100BASE-TX or 10BASE-T applications. In a typical Ethernet application, connections between PHYs are made over unshielded, twisted-pair (UTP), 100 Ω , category 5 cable. Figure 1 shows a typical representation of this complete interface. The front-end interface components consist of a transformer, an RJ-45 connector, as well as several termination resistors and bypass capacitors.

Figure 1. Typical Twisted-Pair Transceiver Interface

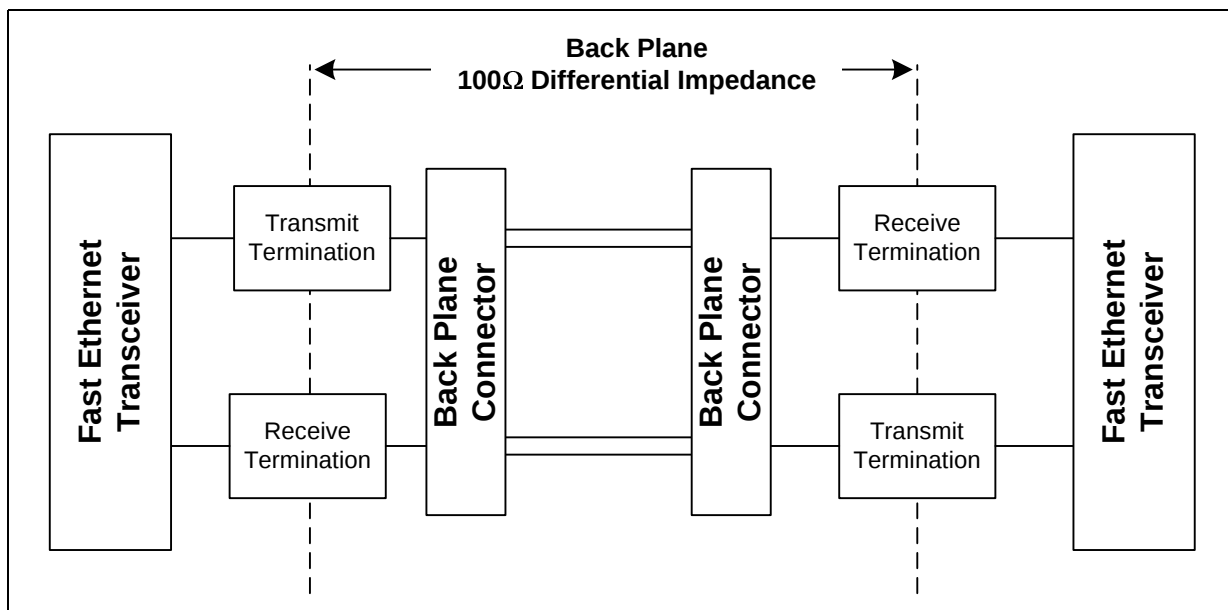


For purposes of this application note, the front-end, twisted-pair interface components are replaced as follows:

- A suitable termination network specific to the device (detailed later by device type) replaces the 1:1 transformer.
- A connector and PCB traces replace the RJ-45 connector and category 5 cable, respectively. To optimize signal integrity, the user must maintain a 100 Ω differential impedance by choosing the appropriate connector and PCB layout.

Figure 2 illustrates the resulting configuration.

Figure 2. Point-to-Point Ethernet



2.0 Magnetic-Less Termination Networks

The termination networks referenced for the devices listed in “[Intel Fast Ethernet Products](#)” on [page 5](#) were developed under the following constraints:

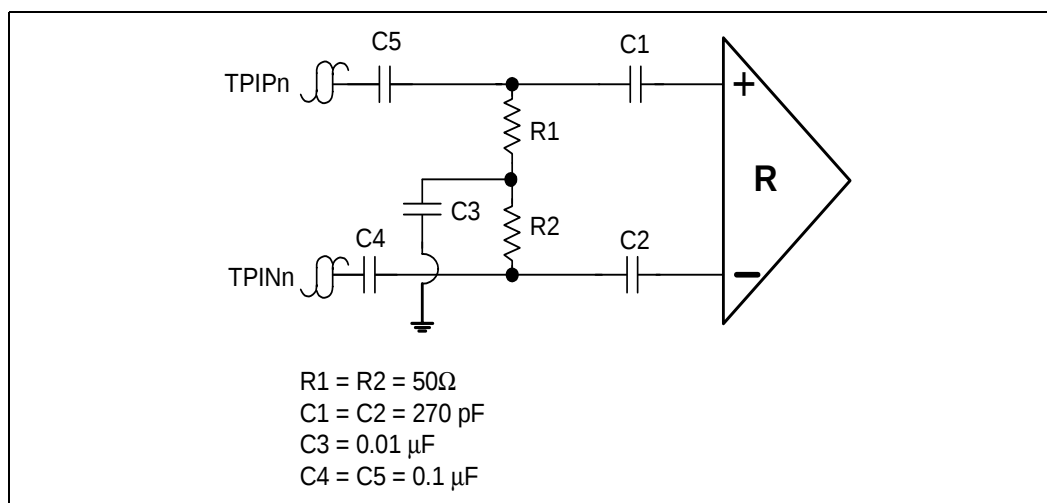
- Magnetic-less PCB interface is over a 100Ω differential-impedance backplane.
- PCB backplane does not exceed one meter.
- Point-to-point interface is supported (multi-drop and multi-point are not supported).
- 100BASE-TX or 10BASE-T applications are supported.
- Full-duplex and half-duplex data transmissions are supported.
- Auto-negotiation is not supported.
- Auto-MDIX is not supported.

2.1 LXT971A/972A, LXT9761/62/63, LXT9781/82, LXT9860/80, and LXT9863/83

The transmitter and receiver termination-network designs are key to the magnetic-less interface. Figures 3 and 4 show the receiver and transmitter termination networks for the LXT971A/972A, LXT9761/62/63, LXT9781/82, LXT9860/80, and LXT9863/83 devices.

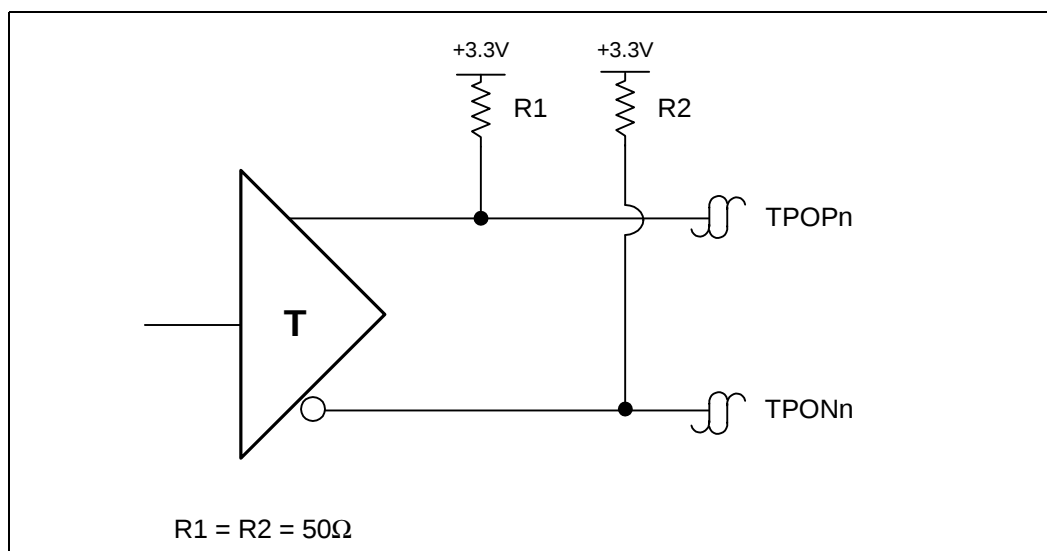
In Figure 3, the 100Ω receiver termination is placed across the TPINn/TPIPn input pair using two 50Ω resistors (R1 and R2) with a 0.01 μF common-mode bypass capacitor (C3) to ground. The 270 pF coupling capacitors (C1 and C2) work with the receiver circuitry to improve the receiver signal-to-noise ratio. The receiver termination uses two series 0.1 μF capacitors (C4 and C5) to achieve AC coupling.

Figure 3. LXT971A/972A, LXT9761/62/63, LXT9781/82, LXT9860/80, and LXT9863/83 Receiver Termination



The transmitter design for the LXT971A/972A, LXT9761/62/63, LXT9781/82, LXT9860/80, and LXT9863/83 devices incorporates a current-driven output stage, and therefore, requires 50Ω pull-up resistors (see Figure 4) to replace the pull-up supplied by the magnetics center tap as depicted in Figure 1. Additionally, a review of Figure 1 shows the absence of the transmitter's 100Ω termination resistor typically found in older generation PHYS. These termination resistors are integrated into this grouping of devices.

Figure 4. LXT971A/972A, LXT9761/62/63, LXT9781/82, LXT9860/80, and LXT9863/83 Transmitter Termination



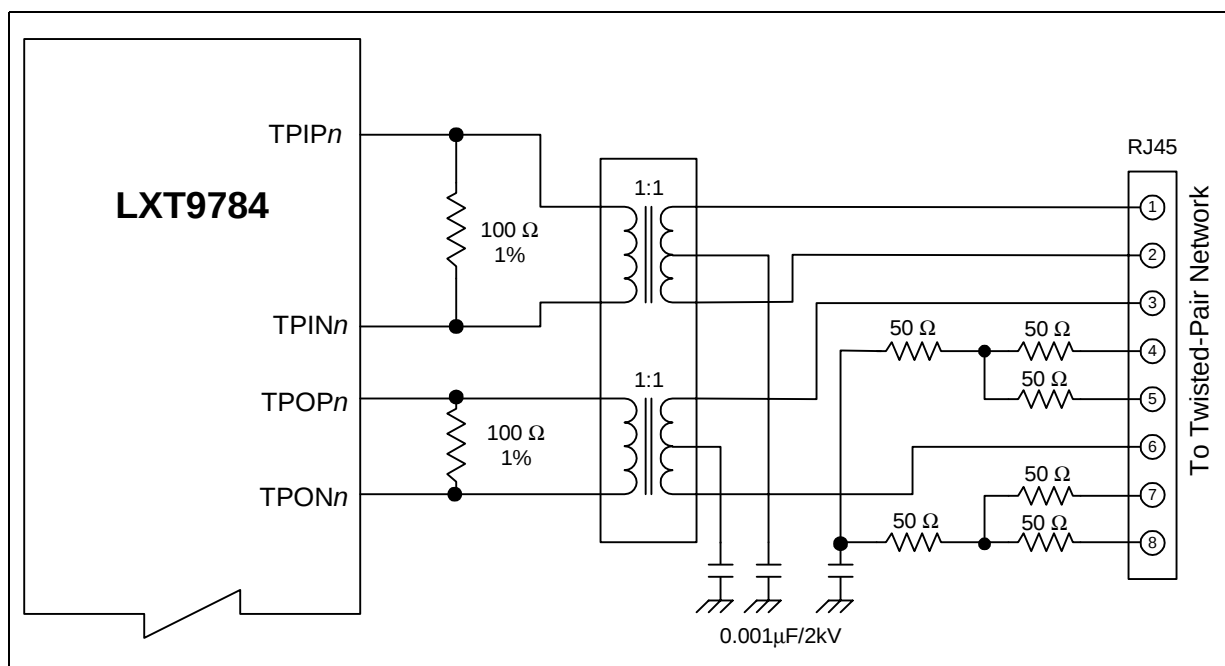
2.2 LXT9784 Fast-Ethernet, Octal Transceiver with RMII/SMII and Auto-MDIX

The LXT9784 and the LXT9785 (see [Section 2.3](#)) offer Auto-MDIX. However, this feature is not supported in magnetic-less applications.

The Auto-MDIX feature allows automatic selection of driver and receiver pairs independent of the cable (straight-through or cross-over) used in normal LAN applications. Auto-MDIX also requires that the magnetics for both transmit and receive functions be identical to allow either pair to be a transmitter or a receiver.

[Figure 5](#) illustrates the magnetic connections to the LXT9784 in a typical LAN application. As illustrated, the primary and secondary windings are identical to satisfy the Auto-MDIX requirement, as well as the line termination.

Figure 5. LXT9784 Typical Ethernet Interface



With the removal of the magnetic interface for the backplane application, the Auto-MDIX feature must be disabled since the termination networks now required are specific to the transmitter and receiver pairs. Thus, Auto-MDIX is not supported in magnetic-less applications.

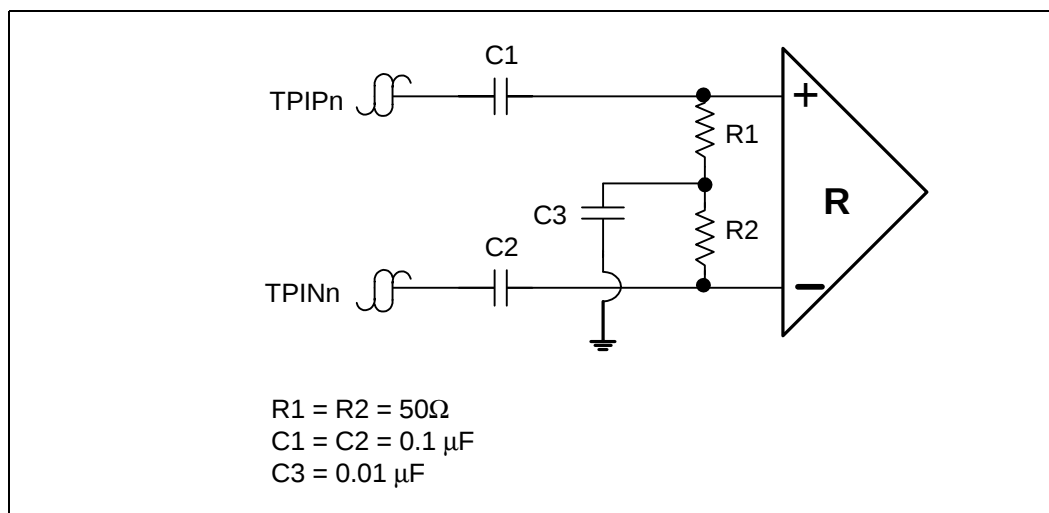
Figures [6](#) and [7](#) illustrate the termination networks for the LXT9784 receiver and transmitter, respectively. Because of differences in the PHY design, the termination networks are slightly different than the previous series of PHY transceivers. However, interoperability is maintained.

In [Figure 6](#), the 100Ω receiver termination is placed across the TPINN/TPIPN input pair by using two 50Ω resistors (R1 and R2) with a 0.01 μF, common-mode, bypass capacitor (C3) to ground. Two series 0.1 μF capacitors (C1 and C2) achieve AC coupling.

Application Note

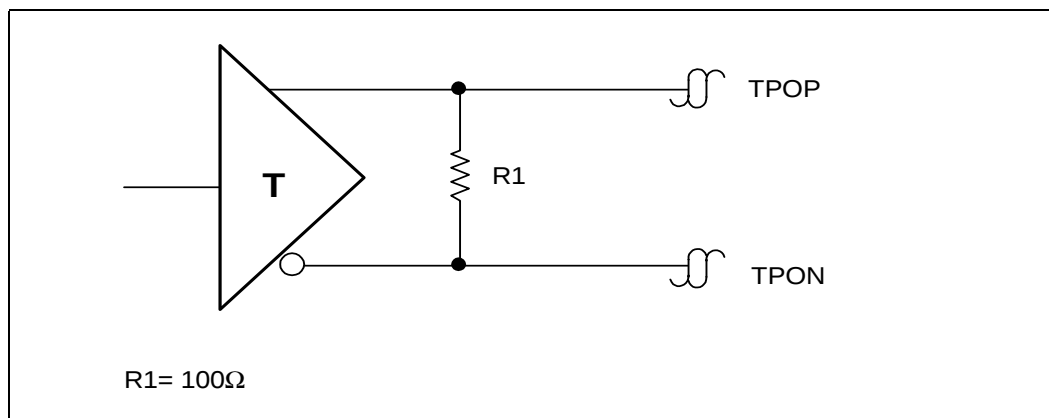
Document #: 249490
Revision #: 001
Rev. Date: 03/07/01

Figure 6. LXT9784 Receiver Termination



The transmit driver of the LXT9784 is also implemented differently than the previously described transmitters. The equivalent circuitry only requires a 100Ω termination resistor across the TPOPn and TPONn pins for line impedance matching.

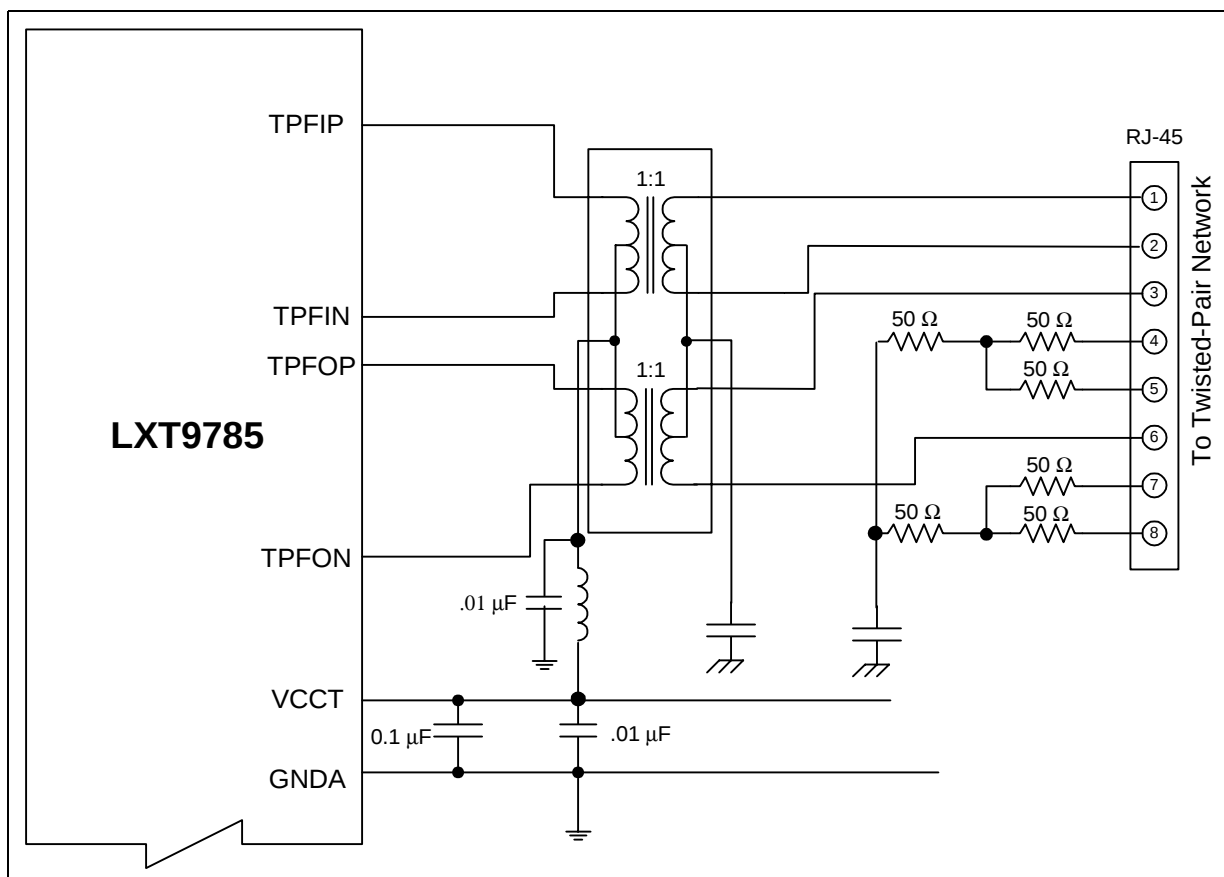
Figure 7. LXT9784 Transmitter Terminations



2.3 LXT9785 Fast-Ethernet, Octal Transceiver with RMII, SMII, SS/SMII, and Auto-MDIX

Unlike the previous generations of transceivers discussed, the LXT9785 does not require the external-load termination to match the 100Ω characteristics impedance of the UTP cable or backplane. The external resistors typically required on both transmit and receive pairs for impedance matching have been integrated into the device. This absence of the termination resistors is reflected in the LXT9785 typical-Ethernet interface shown in Figure 8.

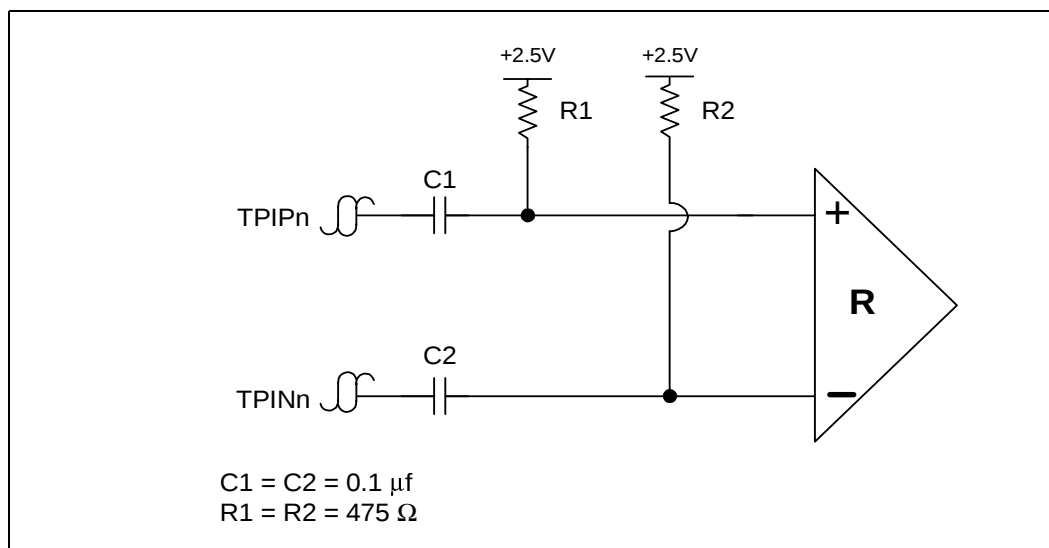
Figure 8. LXT9785 Typical Ethernet Interface



Since the LXT9785 includes the Auto-MDIX feature, the magnetics requirements for a typical LAN application are the same as in [Section 2.2](#) covering the LXT9784. Again, with the removal of the magnetic interface for the backplane application, the Auto-MDIX feature must be disabled.

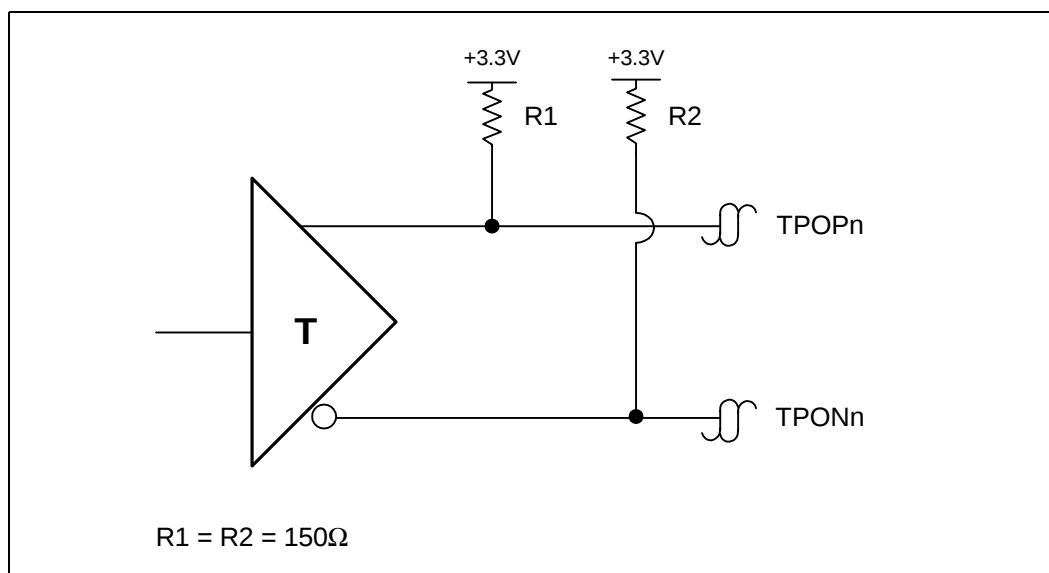
The resulting termination networks for the LXT9785 receiver and transmitter are illustrated in [Figures 9 and 10](#). In [Figure 9](#), C1 and C2 provide the AC coupling to the receiver, and R1 and R2 establish the common-mode operating voltage for the receiver in conjunction with the receiver input circuitry.

Figure 9. LXT9785 Receiver Termination



LXT9785 transmitter outputs are designed with current-driven output stages similar to the LXT971 device. One major difference is that the LXT9785 transmitter circuitry is designed to operate with a 2.5V supply, and only the transmitter outputs are compatible with 3.3V. The magnetic-less interface shown in Figure 10 requires that the resistors on the TPOPn and TPONn outputs be pulled up to 3.3V. Due to the voltage drop across these resistors, the transmitter operates in a safe region during normal operation. However, device damage could occur if the internal circuitry is disabled while the 3.3V supply remains active, which could happen if the 2.5V supply fails, the LXT9785 is held in an extended period of reset, or the software power down of the LXT9785 is enabled.

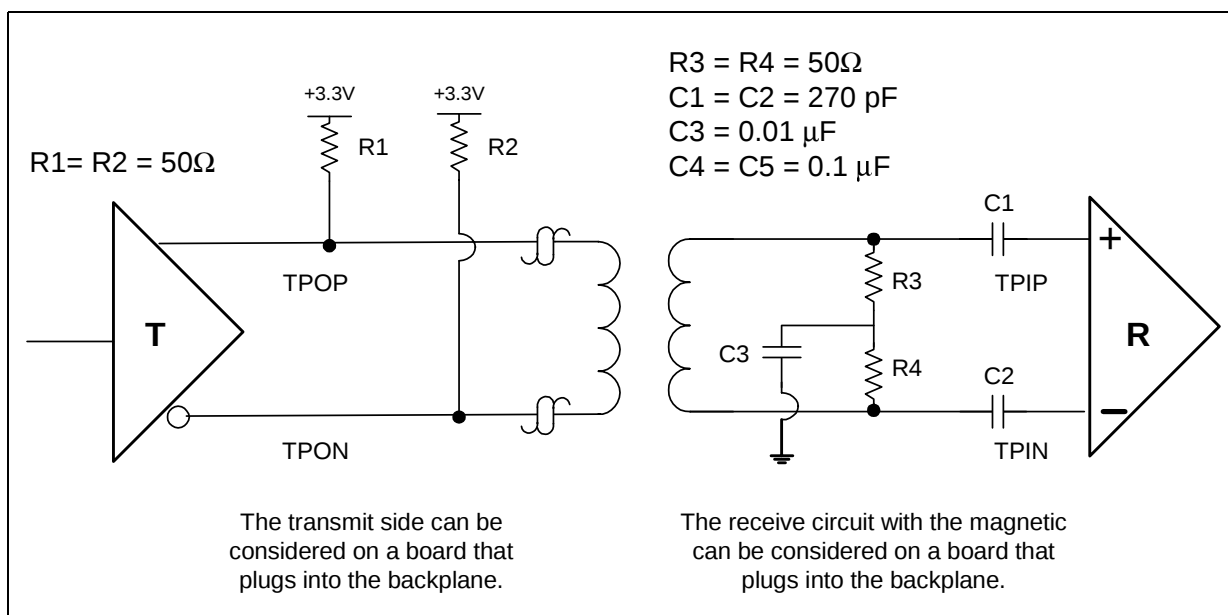
Figure 10. LXT9785 Transmitter Termination



2.4 Hybrid Configuration

Although this application note focuses on how to implement a magnetic-less Ethernet interface, it is possible to build a “hybrid” configuration. Figure 11 shows an example of a LXT971A magnetic-less transmitter to a LXT971A receiver with the standard recommended transformer configuration. Again it should be recognized that the transmitter configuration will not necessarily meet the full intent of compliance to the IEEE 802.3 standard, and therefore, it is not recommended when the link partner may be unknown and is expecting Ethernet signaling levels.

Figure 11. Hybrid Interface Representing LXT971A/972A, LXT9761/62/63, LXT9781/82 and LXT98xxx



3.0 Validation Testing

Testing of all Fast Ethernet devices listed in Section 1.1 was performed in two phases. The first phase was as a stand-alone interface, meaning a specific device transmitted to another of the same device type as a link partner. In the second phase, testing was completed across the full matrix of transmitters to receivers to demonstrate full interoperability, independent of combinations used.

Because of variables and time limitations in actually designing a PCB-backplane evaluation board, testing was completed on modified demo boards. The magnetic interface was replaced with the appropriate AC termination network, and the RJ-45 connector and category 5 cable were used to emulate the backplane.

During validation testing, the following variables were considered:

- Variable packet length (64-byte\1514-byte)
- Variable cable length (0 to >2 meters)
- VCC supplies — full range of operation

3.1 Testing Summary

Validation testing completed in Intel's lab clearly demonstrated that the magnetic-less interfaces operated 100% error free from minimum length (< 1.5 inches) to greater than 2 meters of category 5 cable. Bit-error-rate (BER) testing was terminated at greater than 10 million packets based upon signal integrity and error-free operation.

Figures 12 and 13 show typical examples of the eye patterns captured for the LXT971A in the recommended magnetic-less circuit configuration. All other PHYs tested had similar signaling results.

Figure 12. 100 Mbps Eye Pattern at LXT971A Transmitter Output Terminated into 100Ω

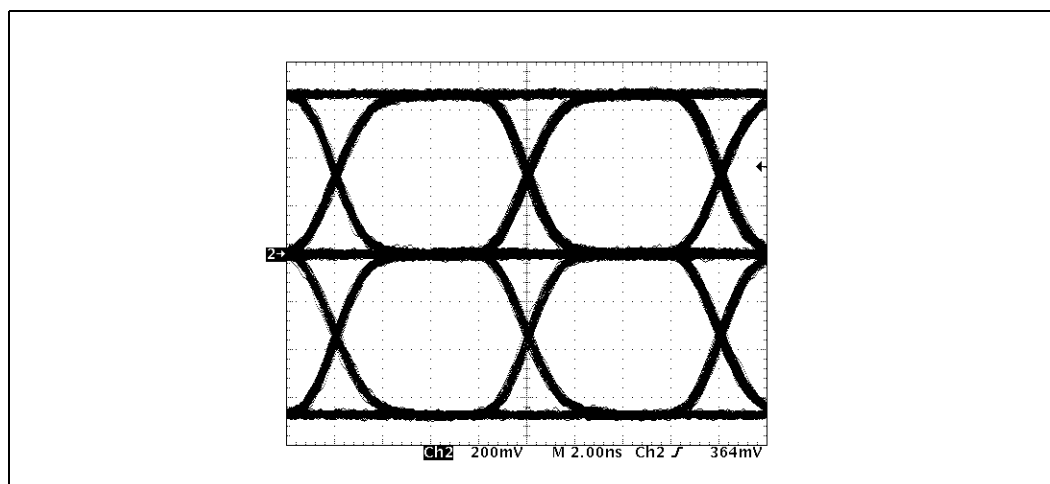
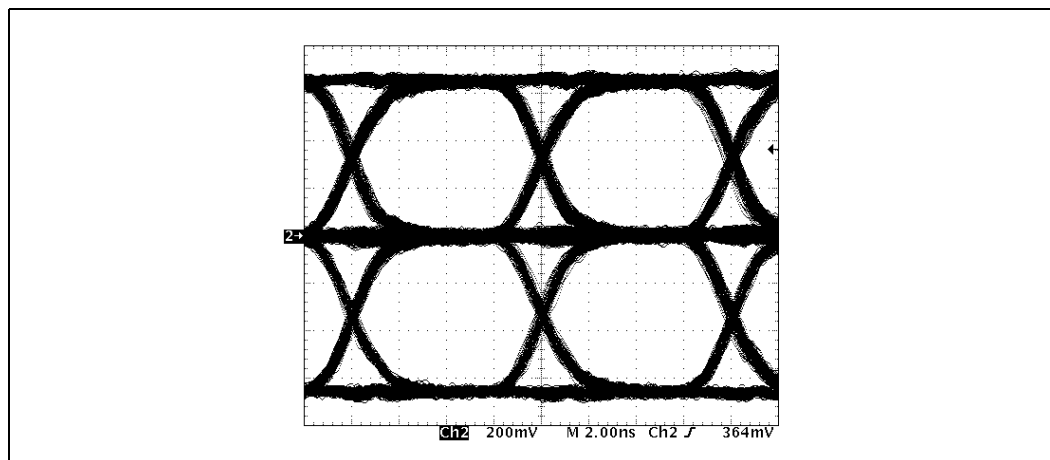


Figure 13. 100 Mbps Eye Pattern at LXT971A Receiver Input at 1-Meter Cable End



4.0 Recommendations

In all figures defining the receiver and transmitter termination networks, it is highly recommended that a minimum distance be maintained between the PHY and the actual connectors used on the PCB. Components shown in the termination networks should be placed as close as possible to the transceiver pins, thereby placing the termination networks as close to ports as possible for all circuit configurations.

It is recommended that system designers layout the PCB backplane such that it matches the characteristics of the category 5 cable, as follows:

- Use a 100Ω differential impedance across the differential pairs.
- Impedance match the connectors used in the backplane. (Please note that depending on the layout, additional termination may be required at the connector.)
- Allow sufficient spacing on adjacent differential pairs to minimize crosstalk. (Layout-tool design rules should be sufficient.)
- Place termination circuitry close to the device.
- Keep backplane traces as short as possible.
- Minimize vias.

5.0 Summary

Ethernet over a backplane is gaining in popularity because it provides the high reliability and data integrity of Ethernet and is achieved at high speed without yet another protocol to implement. Selected Intel Fast Ethernet Transceivers provide engineers that develop fast and complex proprietary-bus systems with a high-performance alternative particularly suitable for the design of current systems.

Circuit configurations outlined in this document have been tested and should provide system designers a high degree of confidence with its basic implementation.

