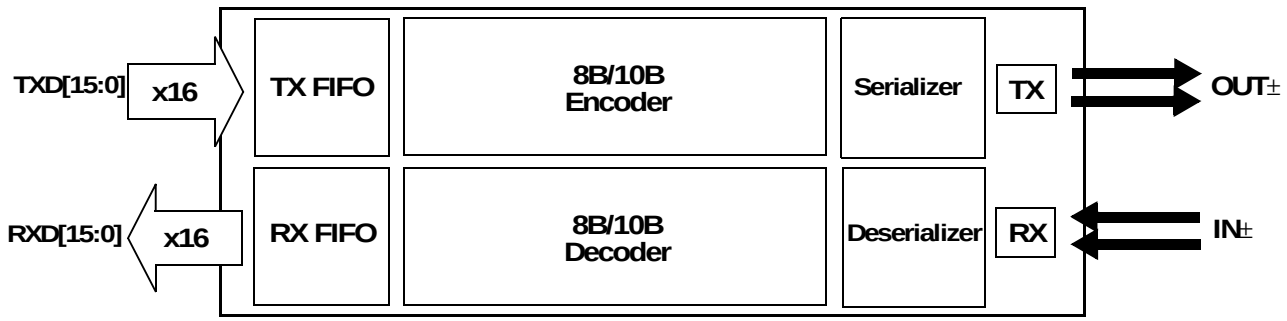
InfiniPHY™ Transceiver

Features

- InfiniBand™ Operation
- 2.5--GBaud serial signaling rate
- Multiple selectable loopback/loop-through modes
- Single 125-MHz reference clock
- Transmit FIFO for flexible data interface clocking
- 16-bit parallel-to-serial conversion in transmit path
- Serial to 16-bit parallel conversion in receive path
- Synchronous HSTL parallel interface
- Internal transmit and receive PLLs
- Differential CML serial input with internal termination
- Differential CML serial output with source matched 50-ohm transmission lines
- Direct interface to standard fiberoptic modules
- Compatible with
  - fiberoptic modules
  - copper cables
  - circuit board traces
- 456-Ball Thermally Enhanced BGA packaging
- Built-In Self-Test (BIST) for at-speed link testing
- Power down feature
- Comma detect
- 8B/10B encoding and decoding
- Clock tolerance compensation logic
- Polarity inversion
- PRBS idle data transmission

CY7B9260V InfiniPHY Transceiver Logic Block Diagram



General Description

The CY7B9260V InfiniBand™ Transceiver is a building block for InfiniBand based data communications systems. It provides complete parallel-to-serial and serial-to-parallel conversion in a single chip. The transmit channel accepts parallel characters in an input register, encodes each character for transport and converts it to serial data. The receive channel accepts serial data and converts it to parallel data, decodes the data into characters, and presents these characters to the output register. In accordance with the InfiniBand standard, the transceiver is compatible with optical modules, copper cable connections and PCB traces.

Figure 1 and *Figure 2* illustrate typical connections between InfiniBand Channel Adapters (Target Channel Adapter (TCA) or Host channel Adapter (HCA)) and CY7B9260V in optical and copper applications.

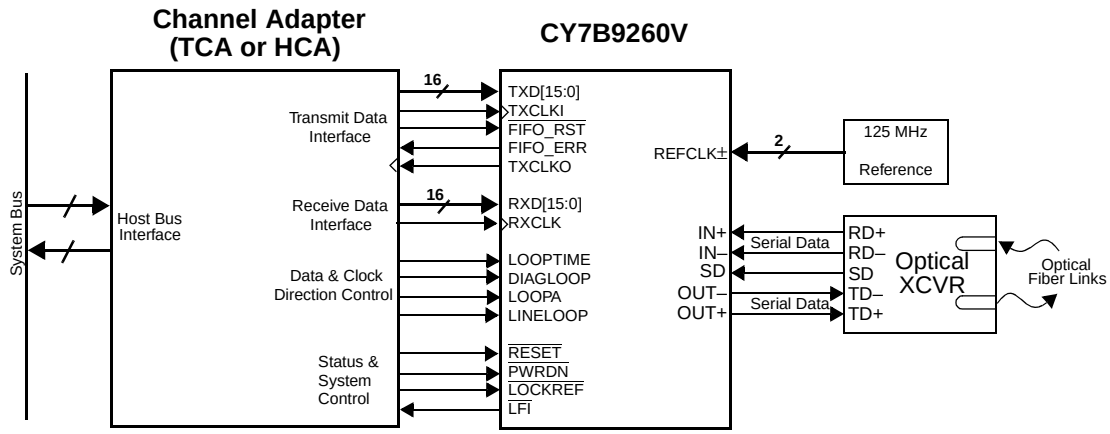


Figure 1. CY7B9260V System Connections with an Optical Interface.

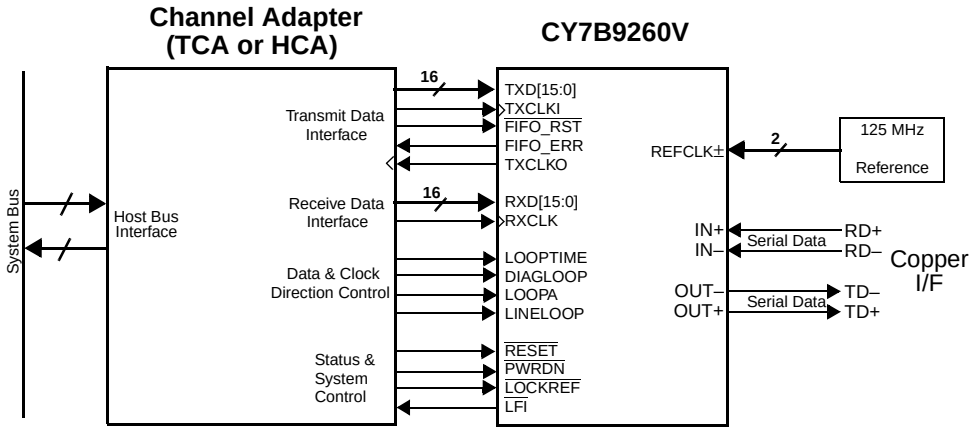


Figure 2. CY7B9260V System Connections with a Copper Interface.

Device Interface and Pin Functionality

Name	I/O	Description
TXD	Input	Parallel data transmit bus[15:0]
TXCLKI	Input	Parallel transmit data input clock
TXCLKO	Output	Parallel transmit data output clock
$\overline{\text{FIFO\_RST}}$	Input	Transmit FIFO reset
FIFO_ERR	Output	Transmit FIFO error
RXD	Output	Data Receive Bus [15:0]
RXCLK	Input	Receive clock input
TIMELOOP	Input	Loop control signal (1)
DIAGLOOP	Input	Loop control signal (2)
LOOPA	Input	Loop control signal (3)
LINELOOP	Input	Loop control signal (4)
$\overline{\text{RESET}}$	Input	Reset for logic functions
$\overline{\text{PWRDN}}$	Input	Device power down
$\overline{\text{LOCKREF}}$	Input	Receive PLL lock to reference
$\overline{\text{LFI}}$	Output	Line fault indicator
REFCLK±	Input	Reference clock (differential LVPECL) input
SD	Input	Signal detect
IN±	Input	Differential serial data input
OUT±	Output	Differential serial data output

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