Multiformat SDTV Video Decoder

ADV7183A

FEATURES

- Multiformat video decoder supports NTSC-(M, N, 4.43), PAL-(B/D/G/H/I/M/N), SECAM
- Integrates three 54 MHz, 10-bit ADCs
- Clocked from a single 27 MHz crystal
- Line-locked clock compatible (LLC)
- Adaptive Digital Line Length Tracking (ADLLT™)
- 5-line adaptive comb filters
- Proprietary architecture for locking to weak, noisy, and unstable video sources such as VCRs and tuners
- Subcarrier frequency lock and status information output
- Integrated AGC with adaptive peak white mode
- Macrovision® copy protection detection
- CTI (chroma transient improvement)
- DNR (digital noise reduction)
- Multiple programmable analog input formats:
  - CVBS (composite video)
  - S-Video (Y/C)
  - YPrPb component (VESA, MII, SMPTE, and BetaCam)
- 12 analog video input channels
- Automatic NTSC/PAL/SECAM identification
- Digital output formats (8-bit or16-bit):
  - ITU-R BT.656 YCrCb 4:2:2 output + HS, VS, and FIELD
- 0.5 V to 1.6 V analog signal input range
- Differential gain: 0.5% typ
- Differential phase: 0.5° typ
- Programmable video controls:
  - Peak-white/hue/brightness/saturation/contrast
- Integrated on-chip video timing generator
- Free run mode (generates stable video ouput with no I/P)
- VBI decode support for
  - Close captioning, WSS, CGMS, EDTV, Gemstar® 1×/2×
- Power-down mode
- 2-wire serial MPU interface (I²C® compatible)
- 3.3 V analog, 1.8 V digital core; 3.3 V IO supply
- 2 temperature grades: –25°C to +70°C and –40°C to +85°C
- 80-lead LQFP Pb-free package

APPLICATIONS

- DVD recorders
- Video projectors
- HDD-based PVRs/DVDRs
- LCD TVs
- Set-top boxes
- Security systems
- Digital televisions
- AVR receiver

GENERAL DESCRIPTION

The ADV7183A integrated video decoder automatically detects and converts a standard analog baseband television signal compatible with worldwide standards NTSC, PAL, and SECAM into 4:2:2 component video data compatible with 16-/8-bit CCIR601/CCIR656.

The advanced and highly flexible digital output interface enables performance video decoding and conversion in line-locked clock based systems. This makes the device ideally suited for a broad range of applications with diverse analog video characteristics, including tape based sources, broadcast sources, security/surveillance cameras, and professional systems.

The 10-bit accurate A/D conversion provides professional quality video performance and is unmatched. This allows true 8-bit resolution in the 8-bit output mode.

The 12 analog input channels accept standard Composite, S-Video, YPrPb video signals in an extensive number of combinations. AGC and clamp restore circuitry allow an input video signal peak-to-peak range of 0.5 V up to 1.6 V. Alternatively, these can be bypassed for manual settings.

The fixed 54 MHz clocking of the ADCs and datapath for all modes allows very precise, accurate sampling and digital filtering. The line-locked clock output allows the output data rate, timing signals, and output clock signals to be synchronous, asynchronous, or line locked even with ±5% line length variation. The output control signals allow glueless interface connections in almost any application. The ADV7183A modes are set up over a 2-wire, serial, bidirectional port (I²C compatible).

The ADV7183A is fabricated in a 3.3 V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation.

The ADV7183A is packaged in a small 80-lead LQFP Pb-free package.

Rev. A

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REVISION HISTORY

Revision A

6/04—Changed from Rev. 0 to Rev. A.

Addition to Applications List.....1

Changes to Table 3 8

Changes to Table 5 8

Change to Drive Strength Selection (Data) Section 17

Changes to Figure 42 103

Revision 0

5/04—Revision 0: Initial Version

INTRODUCTION

The ADV7183A is a high quality, single chip, multiformat video decoder that automatically detects and converts PAL, NTSC, and SECAM standards in the form of composite, S-Video, and component video into a digital ITU-R BT.656 format.

The advanced and highly flexible digital output interface enables performance video decoding and conversion in line-locked clock based systems. This makes the device ideally suited for a broad range of applications with diverse analog video characteristics, including tape based sources, broadcast sources, security/surveillance cameras, and professional systems.

ANALOG FRONT END

The ADV7183A analog front end comprises three 10-bit ADCs that digitize the analog video signal before applying it to the standard definition processor. The analog front end employs differential channels to each ADC to ensure high performance in mixed-signal applications.

The front end also includes a 12-channel input mux that enables multiple video signals to be applied to the ADV7183A. Current and voltage clamps are positioned in front of each ADC to ensure that the video signal remains within the range of the converter. Fine clamping of the video signals is performed downstream by digital fine clamping within the ADV7183A. The ADCs are configured to run in 4× oversampling mode.

STANDARD DEFINITION PROCESSOR

The ADV7183A is capable of decoding a large selection of baseband video signals in composite, S-Video, and component formats. The video standards supported by the SDP include PAL B/D/I/G/H, PAL60, PAL M, PAL N, PAL Nc, NTSC M/J, NTSC 4.43, and SECAM B/D/G/K/L. The ADV7183A can automatically detect the video standard and process it accordingly.

The ADV7183A has a 5-line, superadaptive, 2D comb filter that gives superior chrominance and luminance separation when decoding a composite video signal. This highly adaptive filter automatically adjusts its processing mode according to video standard and signal quality with no user intervention required. Video user controls such as brightness, contrast, saturation, and hue are also available within the ADV7183A.

The ADV7183A implements a patented adaptive digital line-length tracking (ADLLT) algorithm to track varying video line lengths from sources such as a VCR. ADLLT enables the ADV7183A to track and decode poor quality video sources such as VCRs, noisy sources from tuner outputs, VCD players, and camcorders. The ADV7183A contains a chroma transient improvement (CTI) processor that sharpens the edge rate of chroma transitions, resulting in sharper vertical transitions.

The SDP can process a variety of VBI data services, such as closed captioning (CC), wide screen signaling (WSS), copy generation management system (CGMS), EDTV, Gemstar 1×/2×, and extended data service (XDS). The ADV7183A is fully Macrovision certified; detection circuitry enables Type I, II, and III protection levels to be identified and reported to the user. The decoder is also fully robust to all Macrovision signal inputs.

FUNCTIONAL BLOCK DIAGRAM

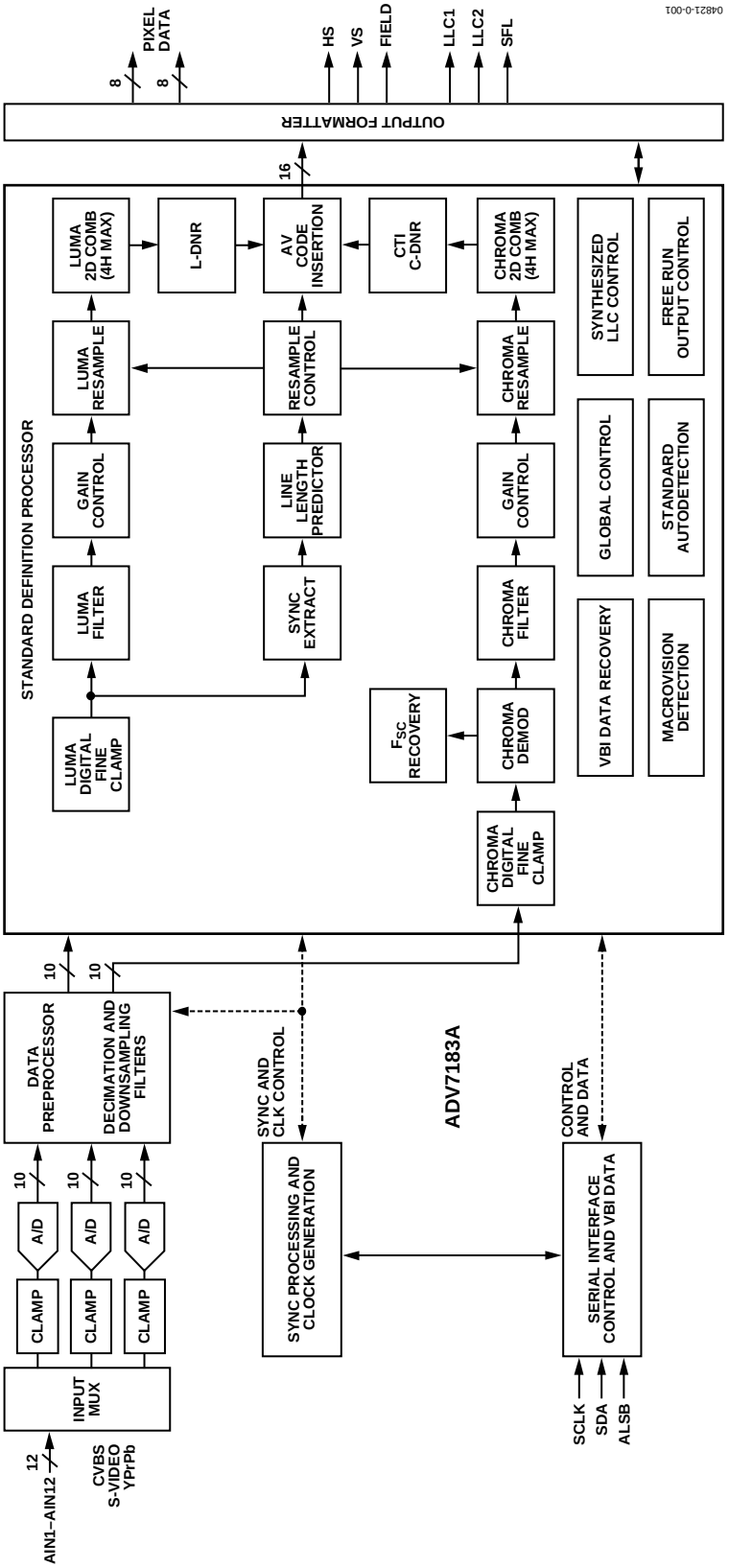

Figure 1.

SPECIFICATIONS

Temperature range: T_{MIN} to T_{MAX}, –40°C to +85°C. The min/max specifications are guaranteed over this range.

ELECTRICAL CHARACTERISTICS

At A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V (operating temperature range, unless otherwise noted).

Table 1.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
STATIC PERFORMANCE						
Resolution (Each ADC)	N				10	Bits
Integral Nonlinearity	INL	BSL at 54 MHz		–0.475/+0.6	±3	LSB
Differential Nonlinearity	DNL	BSL at 54 MHz		–0.25/+0.5	–0.7/+2	LSB
DIGITAL INPUTS						
Input High Voltage	V_{IH}		2			V
Input Low Voltage	V_{IL}				0.8	V
Input Current	I_{IN}	Pins listed in Note 1	–50		+50	µA
		All other pins	–10		+10	µA
Input Capacitance	C_{IN}				10	pF
DIGITAL OUTPUTS						
Output High Voltage	V_{OH}	I_{SOURCE} = 0.4 mA	2.4			V
Output Low Voltage	V_{OL}	I_{SINK} = 3.2 mA			0.4	V
High Impedance Leakage Current	I_{LEAK}	Pins listed in Note 2			50	µA
		All other pins			10	µA
Output Capacitance	C_{OUT}				20	pF
POWER REQUIREMENTS[3]						
Digital Core Power Supply	D_{VDD}		1.65	1.8	2	V
Digital I/O Power Supply	D_{VDDIO}		3.0	3.3	3.6	V
PLL Power Supply	P_{VDD}		1.65	1.8	2.0	V
Analog Power Supply	A_{VDD}		3.15	3.3	3.45	V
Digital Core Supply Current	I_{DVDD}			72		mA
Digital I/O Supply Current	I_{DVDDIO}			2		mA
PLL Supply Current	I_{PVDD}			10.5		mA
Analog Supply Current	I_{AVDD}	CVBS input[4]		85		mA
		YPrPb input[5]		180		mA
Power-Down Current	I_{PWRDN}			1.5		mA
Power-Up Time	t_{PWRUP}			20		ms

[1] Pins 36 and 79.
[2] Pins 1, 2, 5, 6, 7, 8, 12, 17, 18, 19, 20, 21, 22, 23, 24, 32, 33, 34, 35, 73, 74, 75, 76, and 80.
[3] Guaranteed by characterization.
[4] ADC1 powered on.
[5] All three ADCs powered on.

VIDEO SPECIFICATIONS

Guaranteed by characterization. At A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V (operating temperature range, unless otherwise noted).

Table 2.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
NONLINEAR SPECIFICATIONS						
Differential Phase	DP	CVBS I/P, modulate 5-step		0.5	0.7	°
Differential Gain	DG	CVBS I/P, modulate 5-step		0.5	0.7	%
Luma Nonlinearity	LNL	CVBS I/P, 5-step		0.5	0.7	%
NOISE SPECIFICATIONS						
SNR Unweighted		Luma ramp	54	56		dB
		Luma flat field	58	60		dB
Analog Front End Crosstalk				60		dB
LOCK TIME SPECIFICATIONS						
Horizontal Lock Range			–5		+5	%
Vertical Lock Range			40		70	Hz
Fsc Subcarrier Lock Range				±1.3		Hz
Color Lock In Time				60		Lines
Sync Depth Range			20		200	%
Color Burst Range			5		200	%
Vertical Lock Time				2		Fields
Autodetection Switch Speed				100		Lines
CHROMA SPECIFICATIONS						
Hue Accuracy	HUE			1		°
Color Saturation Accuracy	CL_AC			1		%
Color AGC Range			5		400	%
Chroma Amplitude Error				0.5		%
Chroma Phase Error				0.4		°
Chroma Luma Intermodulation				0.2		%
LUMA SPECIFICATIONS						
Luma Brightness Accuracy		CVBS, 1 V I/P		1		%
Luma Contrast Accuracy		CVBS, 1 V I/P		1		%

TIMING SPECIFICATIONS

Guaranteed by characterization. At A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V (operating temperature range, unless otherwise noted).

Table 3.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
SYSTEM CLOCK AND CRYSTAL						
Nominal Frequency				27.00		MHz
Frequency Stability					±50	ppm
I^2C PORT						
SCLK Frequency					400	kHz
SCLK Min Pulse Width High	t_1		0.6			µs
SCLK Min Pulse Width Low	t_2		1.3			µs
Hold Time (Start Condition)	t_3		0.6			µs
Setup Time (Start Condition)	t_4		0.6			µs
SDA Setup Time	t_5		100			ns
SCLK and SDA Rise Time	t_6				300	ns
SCLK and SDA Fall Time	t_7				300	ns
Setup Time for Stop Condition	t_8			0.6		µs
RESET FEATURE						
Reset Pulse Width			5			ms
CLOCK OUTPUTS						
LLC1 Mark Space Ratio	t_9:t_{10}		45:55		55:45	% Duty Cycle
LLC1 Rising to LLC2 Rising	t_{11}			0.5		ns
LLC1 Rising to LLC2 Falling	t_{12}			0.5		ns
DATA AND CONTROL OUTPUTS						
Data Output Transitional Time	t_{13}	$t_{ACCESS} = t_{10} - t_{13}$			6	ns
Data Output Transitional Time	t_{14}	$t_{HOLD} = t_9 + t_{14}$			−0.6	ns
Propagation Delay to Hi-Z	t_{15}			6		ns
Max Output Enable Access Time	t_{16}			7		ns
Min Output Enable Access Time	t_{17}			4		ns

ANALOG SPECIFICATIONS

Guaranteed by characterization. At A_{VDD} = 3.15 V to 3.45 V, D_{VDD} = 1.65 V to 2.0 V, D_{VDDIO} = 3.0 V to 3.6 V, P_{VDD} = 1.65 V to 2.0 V (operating temperature range, unless otherwise noted).

Table 4.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
CLAMP CIRCUITRY						
External Clamp Capacitor				0.1		µF
Input Impedance		Clamps switched off		10		MΩ
Large Clamp Source Current				0.75		mA
Large Clamp Sink Current				0.75		mA
Fine Clamp Source Current				60		µA
Fine Clamp Sink Current				60		µA

THERMAL SPECIFICATIONS

Table 5.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
THERMAL CHARACTERISTICS						
Junction-to-Case Thermal Resistance	θ_{JC}	4-layer PCB with solid ground plane		7.6		°C/W
Junction-to-Ambient Thermal Resistance (Still Air)	θ_{JA}	4-layer PCB with solid ground plane		38.1		°C/W

TIMING DIAGRAMS

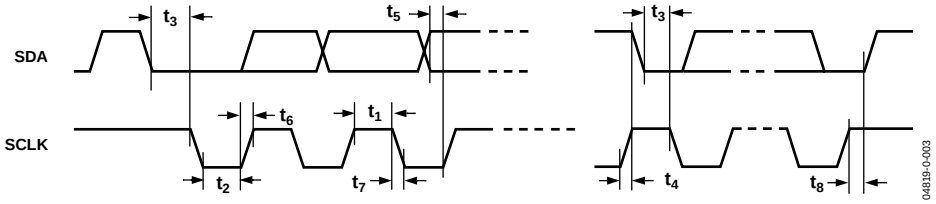

Figure 2. I²C Timing

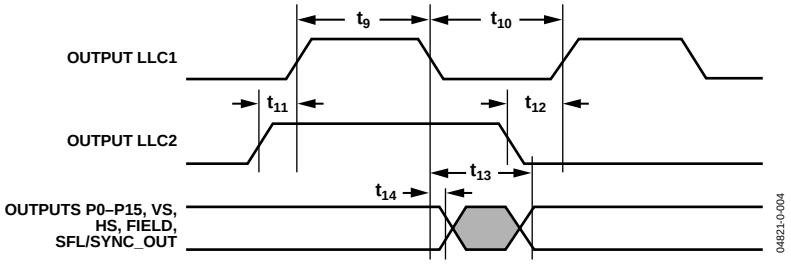

Figure 3. Pixel Port and Control Output Timing

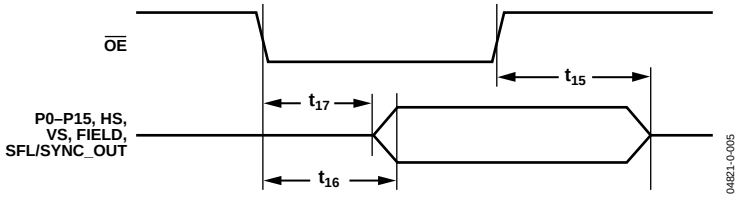

Figure 4. $\overline{OE}$ Timing

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
A_{VDD} to GND	4 V
A_{VDD} to AGND	4 V
D_{VDD} to DGND	2.2 V
P_{VDD} to AGND	2.2 V
D_{VDDIO} to DGND	4 V
D_{VDDIO} to AVDD	–0.3 V to +0.3 V
P_{VDD} to D_{VDD}	–0.3 V to +0.3 V
D_{VDDIO} – P_{VDD}	–0.3V to +2 V
D_{VDDIO} – D_{VDD}	–0.3V to +2 V
A_{VDD} – P_{VDD}	–0.3V to +2 V
A_{VDD} – D_{VDD}	–0.3V to +2 V
Digital Inputs Voltage to DGND	–0.3V to D_{VDDIO} + 0.3 V
Digital Output Voltage to DGND	–0.3V to D_{VDDIO} + 0.3 V
Analog Inputs to AGND	AGND – 0.3 V to A_{VDD} + 0.3 V
Maximum Junction Temperature (T_{JMAX})	150°C
Storage Temperature Range	–65°C to +150°C
Infrared Reflow Soldering (20 s)	260°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

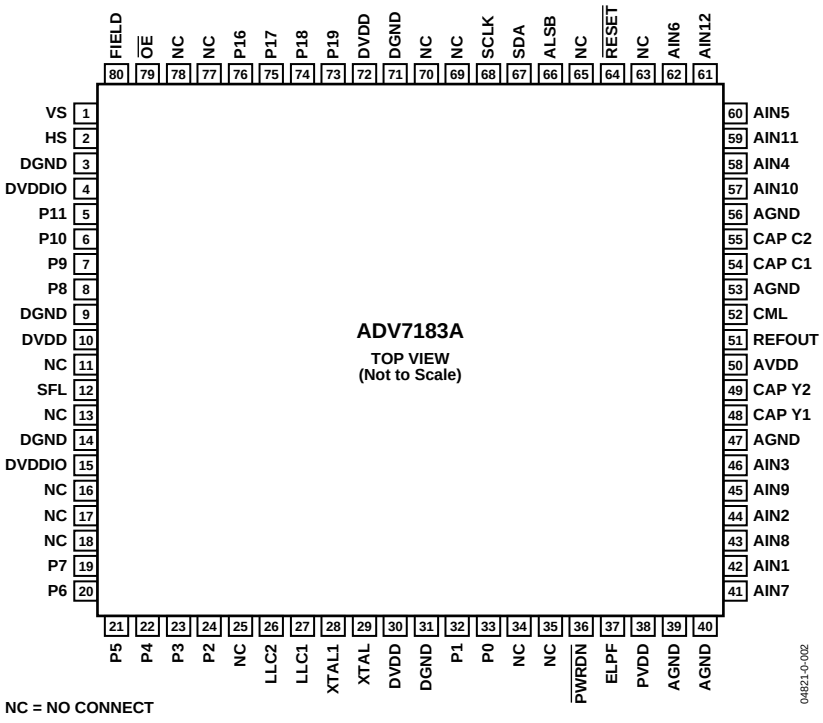

Figure 5. 80-Lead LQFP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Type	Function
3, 9, 14, 31, 71	DGND	G	Digital Ground.
39, 40, 47, 53, 56	AGND	G	Analog Ground.
4, 15	DVDDIO	P	Digital I/O Supply Voltage (3.3 V).
10, 30, 72	DVDD	P	Digital Core Supply Voltage (1.8 V).
50	AVDD	P	Analog Supply Voltage (3.3 V).
38	PVDD	P	PLL Supply Voltage (1.8 V).
41–46, 57–62	AIN1–AIN12	I	Analog Video Input Channels.
11, 13, 16–18, 25, 34, 35, 63, 65, 69, 70, 77, 78	NC		No Connect Pins.
5–8, 19–24, 32, 33, 73–76	P0–P15	O	Video Pixel Output Port.
2	HS	O	HS is a horizontal synchronization output signal.
1	VS	O	VS is a vertical synchronization output signal.
80	FIELD	O	FIELD is a field synchronization output signal.
67	SDA	I/O	I^2C Port Serial Data Input/Output Pin.
68	SCLK	I	I^2C Port Serial Clock Input (Max Clock Rate of 400 kHz).
66	ALSB	I	This pin selects the I^2C address for the ADV7183A. ALSB set to Logic 0 sets the address for a write as 0x40; for ALSB set to logic high, the address selected is 0x42.
64	$\overline{\text{RESET}}$	I	System Reset Input, Active Low. A minimum low reset pulse width of 5 ms is required to reset the ADV7183A circuitry.
27	LLC1	O	This is a line-locked output clock for the pixel data output by the ADV7183A. Nominally 27 MHz, but varies up or down according to video line length.
26	LLC2	O	This is a divide-by-2 version of the LLC1 output clock for the pixel data output by the ADV7183A. Nominally 13.5 MHz, but varies up or down according to video line length.

Pin No.	Mnemonic	Type	Function
29	XTAL	I	This is the input pin for the 27 MHz crystal, or can be overdriven by an external 3.3 V, 27 MHz clock oscillator source. In crystal mode, the crystal must be a fundamental crystal.
28	XTAL1	O	This pin should be connected to the 27 MHz crystal or left as a no connect if an external 3.3 V, 27 MHz clock oscillator source is used to clock the ADV7183A. In crystal mode, the crystal must be a fundamental crystal.
36	$\overline{\text{PWRDN}}$	I	A logic low on this pin places the ADV7183A in a power-down mode. Refer to the I2C Control Register Map for more options on power-down modes for the ADV7183A.
79	$\overline{\text{OE}}$	I	When set to a logic low, $\overline{\text{OE}}$ enables the pixel output bus, P15–P0 of the ADV7183A. A logic high on the $\overline{\text{OE}}$ pin places Pins P15–P0, HS, VS, SFL/SYNC_OUT into a high impedance state.
37	ELPF	I	The recommended external loop filter must be connected to this ELPF pin, as shown in Figure 42.
12	SFL	O	Subcarrier Frequency Lock. This pin contains a serial output stream that can be used to lock the subcarrier frequency when this decoder is connected to any Analog Devices, Inc. digital video encoder.
51	REFOUT	O	Internal Voltage Reference Output. Refer to Figure 42 for a recommended capacitor network for this pin.
52	CML	O	The CML pin is a common-mode level for the internal ADCs. Refer to Figure 42 for a recommended capacitor network for this pin.
48, 49	CAPY1, CAPY2	I	ADC's Capacitor Network. Refer to Figure 42 for a recommended capacitor network for this pin.
54, 55	CAPC1, CAPC2	I	ADC's Capacitor Network. Refer to Figure 42 for a recommended capacitor network for this pin.

ANALOG FRONT END

ANALOG INPUT MUXING

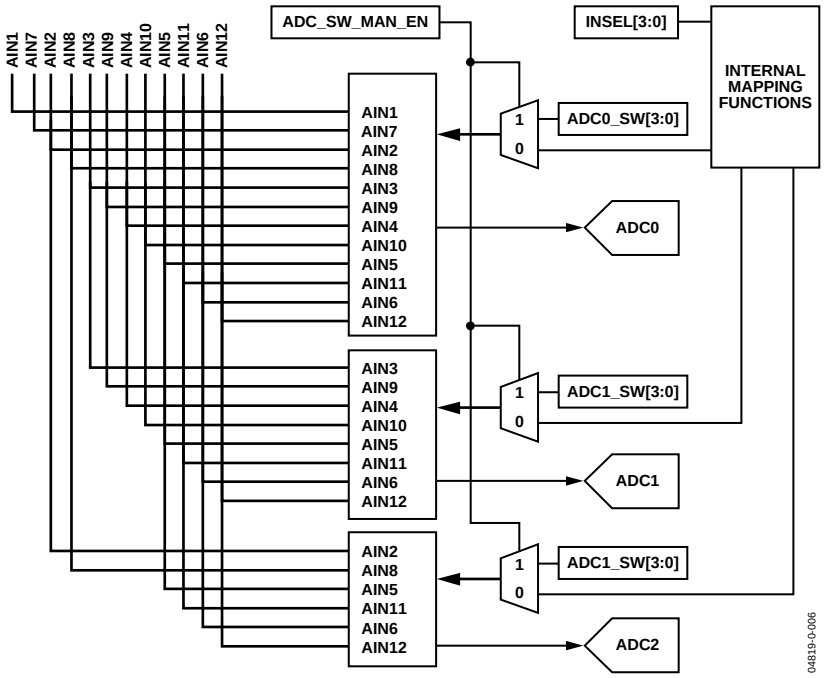

Figure 6. Internal Pin Connections

The ADV7183A has an integrated analog muxing section that allows more than one source of video signal to be connected to the decoder. Figure 6 outlines the overall structure of the input muxing provided in the ADV7183A.

As can be seen in Figure 6, there are two different ways in which the analog input muxes can be controlled:

1. Control via functional registers (INSEL).
   Using INSEL[3:0] simplifies the setup of the muxes, and minimizes crosstalk between channels by pre-assigning the input channels. This is referred to as ADI recommended input muxing.

2. Control via an I²C manual override (ADC_sw_man_en, ADC0_sw, ADC1_sw, ADC2_sw).
   This is provided for applications with special requirements (e.g., number/combinations of signals) that would not be served by the pre-assigned input connections. This is referred to as manual input muxing.

Please refer to Figure 7 for an overview of the two methods of controlling the ADV7183A's input muxing.

ADI Recommended Input Muxing

A maximum of 12 CVBS inputs can be connected and decoded by the ADV7183A. As can be seen from Figure 5, this means the sources will have to be connected to adjacent pins on the IC. This calls for a careful design of the PCB layout (e.g., ground shielding between all signals routed through tracks that are physically close together).

INSEL[3:0] Input Selection, Address 0x00, [3:0]

The INSEL bits allow the user to select an input channel as well as the input format. Depending on the PCB connections, only a subset of the INSEL modes are valid. Please note that the INSEL[3:0] does not only switch the analog input muxing, it also configures the standard definition processor core to process CVBS (Comp), S-video (Y/C), or component (YPbPr) format.

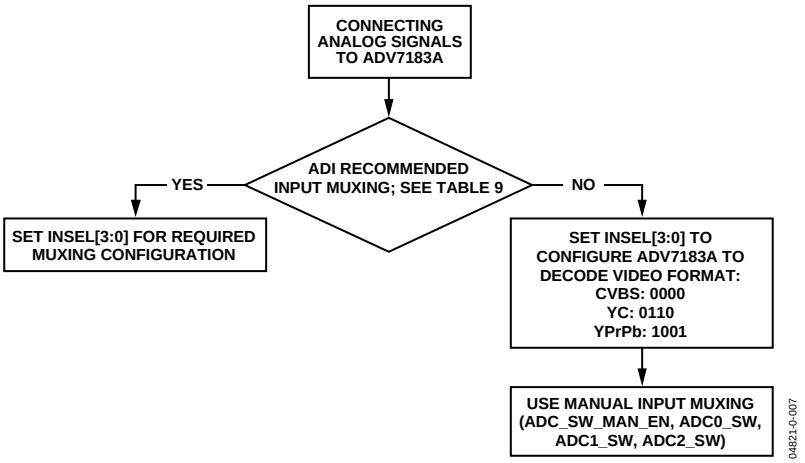

Figure 7. Input Muxing Overview

Table 8. Input Channel Switching Using INSEL[3:0]

	Description	
INSEL[3:0]	**Analog Input Pins**	**Video Format (SDP)**
0000*	CVBS1 = AIN1	Composite
0001	CVBS2 = AIN2	Composite
0010	CVBS3 = AIN3	Composite
0011	CVBS4 = AIN4	Composite
0100	CVBS5 = AIN5	Composite
0101	CVBS6 = AIN6	Composite
0110	Y1 = AIN1	YC
	C1 = AIN4	YC
0111	Y2 = AIN2	YC
	C2 = AIN5	YC
1000	Y3 = AIN3	YC
	C3 = AIN6	YC
1001	Y1 = AIN1	YPrPb
	PR1 = AIN4	YPrPb
	PB1 = AIN5	YPrPb
1010	Y2 = AIN2	YPrPb
	PR2 = AIN3	YPrPb
	PB2 = AIN6	YPrPb
1011	CVBS7 = AIN7	Composite
1100	CVBS8 = AIN8	Composite
1101	CVBS9 = AIN9	Composite
1110	CVBS10 = AIN10	Composite
1111	CVBS11 = AIN11	Composite

*Default value.

Table 9. Input Channel Assignments

Input Channel	Pin No.	ADI Recommended Input Muxing Control INSEL[3:0]		
AIN7	41	CVBS7		
AIN1	42	CVBS1	YC1-Y	YPrPb1-Y
AIN8	43	CVBS8		
AIN2	44	CVBS2	YC2-Y	YPrPb2-Y
AIN9	45	CVBS9		
AIN3	46	CVBS3	YC3-Y	YPrPb2-Pb
AIN10	57	CVBS10		
AIN4	58	CVBS4	YC1-C	YPrPb1-Pb
AIN11	59	CVBS11		
AIN5	60	CVBS5	YC2-C	YPrPb1-Pr
AIN12	61	Not Available		
AIN6	62	CVBS6	YC3-C	YPrPb2-Pr

ADI recommended input muxing is designed to minimize crosstalk between signal channels and to obtain the highest level of signal integrity. Table 9 summarizes how PCB layout should connect analog video signals to the ADV7183A.

Notes

- It is strongly recommended to connect any unused analog input pins to AGND to act as a shield.
- Inputs AIN7 to AIN11 should be connected to AGND in cases where only six input channels are used. This will improve the quality of the sampling due to better isolation between the channels.
- AIN12 is not under the control of INSEL[3:0]. It can only be routed to ADC0/ADC1/ADC2 by manual muxing. See Table 10 for further details.

Manual Input Muxing

By accessing a set of manual override muxing registers, the analog input muxes of the ADV7183A can be controlled directly. This is referred to as manual input muxing.

Notes

- Manual input muxing overrides other input muxing control bits (e.g., INSEL)
- The manual muxing is activated by setting the ADC_SW_MAN_EN bit. It only affects the analog switches in front of the ADCs.

  This means if the settings of INSEL and the manual input muxing registers (ADC0/1/2_sw) contradict each other, the ADC0/ADC1/ADC2_sw settings apply and INSEL is ignored.
- Manual input muxing only controls the analog input muxes. INSEL[3:0] still has to be set so the follow-on blocks process the video data in the correct format.

  This means INSEL must still be used to tell the ADV7183A whether the input signal is of component, YC, or CVBS format.

There are restrictions in the channel routing imposed by the analog signal routing inside the IC; every input pin cannot be routed to each ADC. Please refer to Figure 6 for an overview on the routing capabilities inside the chip. The three mux sections can be controlled by the reserved control signal buses ADC0/ADC1/ADC2_sw[3:0]. Table 10 explains the control words used.

SETADC_sw_man_en, Manual Input Muxing Enable, Address 0xC4, [7]

ADC0_sw[3:0], ADC0 mux configuration, Address 0xC3, [3:0]

ADC1_sw[3:0], ADC1 mux configuration, Address 0xC3, [7:4]

ADC2_sw[3:0], ADC2 mux configuration, Address 0xC4, [3:0]

Table 10. Manual Mux Settings for All ADCs

SETADC_sw_man_en = 1					
ADC0_sw[3:0]	**ADC0 Connected to:**	**ADC1_sw[3:0]**	**ADC1 Connected to:**	**ADC2_sw[3:0]**	**ADC2 Connected to:**
0000	No Connection	0000	No Connection	0000	No Connection
0001	AIN1	0001	No Connection	0001	No Connection
0010	AIN2	0010	No Connection	0010	AIN2
0011	AIN3	0011	AIN3	0011	No Connection
0100	AIN4	0100	AIN4	0100	No Connection
0101	AIN5	0101	AIN5	0101	AIN5
0110	AIN6	0110	AIN6	0110	AIN6
0111	No Connection	0111	No Connection	0111	No Connection
1000	No Connection	1000	No Connection	1000	No Connection
1001	AIN7	1001	No Connection	1001	No Connection
1010	AIN8	1010	No Connection	1010	AIN8
1011	AIN9	1011	AIN9	1011	No Connection
1100	AIN10	1100	AIN10	1100	No Connection
1101	AIN11	1101	AIN11	1101	AIN11
1110	AIN12	1110	AIN12	1110	AIN12
1111	No Connection	1111	No Connection	1111	No Connection

GLOBAL CONTROL REGISTERS

Register control bits listed in this section affect the whole chip.

POWER-SAVE MODES

Power-Down

PDBP, Address 0x0F, [2]

There are two ways to shut down the digital core of the ADV7183A: a pin ($\overline{\text{PWRDN}}$) and a bit (PWRDN see below). The PDBP controls which of the two has the higher priority. The default is to give the pin ($\overline{\text{PWRDN}}$) priority. This allows the user to have the ADV7183A powered down by default.

Table 11. PDBP Function

PDBP	Description
0*	Digital core power controlled by the $\overline{\text{PWRDN}}$ pin (bit is disregarded).
1	Bit has priority (pin is disregarded).

*Default value.

PWRDN, Address 0x0F, [5]

Setting the PWRDN bit switches the ADV7183A into a chip-wide power-down mode. The power-down stops the clock from entering the digital section of the chip, thereby freezing its operation. No I^2C bits are lost during power-down. The PWRDN bit also affects the analog blocks and switches them into low current modes. The I^2C interface itself is unaffected, and remains operational in power-down mode.

The ADV7183A leaves the power-down state if the PWRDN bit is set to 0 (via I^2C), or if the overall part is reset using Pin $\overline{\text{RESET}}$.

Note that PDBP must be set to 1 for the PWRDN bit to power down the ADV7183A.

Table 12. PWRDN Function

PWRDN	Description
0*	Chip operational.
1	ADV7183A in chip-wide power-down.

*Default value.

ADC Power-Down Control

The ADV7183A contains three 10-bit ADCs (ADC 0, ADC 1, and ADC 2). If required, it is possible to power down each ADC individually.

When should the ADCs be powered down?

- CVBS mode. ADC 1 and ADC 2 should be powered down to save on power consumption.
- S-Video mode. ADC 2 should be powered down to save on power consumption.

PWRDN_ADC_0, Address 0x3A, [3]

Table 13. PWRDN_ADC_0 Function

PWRDN_ADC_0	Description
0*	ADC normal operation.
1	Power down ADC 0.

*Default value.

PWRDN_ADC_1, Address 0x3A, [2]

Table 14. PWRDN_ADC_1 Function

PWRDN_ADC_1	Description
0*	ADC normal operation.
1	Power down ADC 1.

*Default value.

PWRDN_ADC_2, Address 0x3A, [1]

Table 15. PWRDN_ADC_2 Function

PWRDN_ADC_2	Description
0*	ADC normal operation.
1	Power down ADC 2.

*Default value.

RESET CONTROL

Chip Reset (RES), Address 0x0F, [7]

Setting this bit, equivalent to controlling the $\overline{\text{RESET}}$ pin on the ADV7183A, issues a full chip reset. All I^2C registers get reset to their default values[6]. After the reset sequence, the part immediately starts to acquire the incoming video signal.

Notes

- After setting the RES bit (or initiating a reset via the pin), the part returns to the default mode of operation with respect to its primary mode of operation. All I^2C bits are loaded with their default values, making this bit self-clearing.
- Executing a software reset takes approximately 2 ms. However, it is recommended to wait 5 ms before any further I^2C writes are performed.
- The I^2C master controller receives a no acknowledge condition on the ninth clock cycle when Chip Reset is implemented. See the MPU Port Description section.

Table 16. RES Function

RES	Description
0*	Normal operation.
1	Start reset sequence.

*Default value.

[6] Some register bits do not have a reset value specified. They keep their last written value. Those bits are marked as having a reset value of x in the register table.

GLOBAL PIN CONTROL

Three-State Output Drivers

TOD, Address 0x03, [6]

This bit allows the user to three-state the output drivers of the ADV7183A.

Upon setting the TOD bit, the P15–P0, HS, VS, FIELD, and SFL pins are three-stated.

Note that the timing pins (HS/VS/FIELD) can be forced active via the TIM_OE bit. For more information on three-state control, refer to the following sections:

- Three-State LLC Driver
- Timing Signals Output Enable

Individual drive strength controls are provided via the DR_STR_XX bits.

Note that the ADV7183A supports three-stating via a dedicated pin. When set high, the $\overline{OE}$ pin three-states the output drivers for P15–P0, HS, VS, FIELD, and SFL. The output drivers are three-stated if the TOD bit or the $\overline{OE}$ pin is set high.

Table 17. TOD Function

TOD	Description
0*	Output drivers enabled.
1	Output drivers three-stated.

*Default value.

Three-State LLC Driver

TRI_LLC, Address 0x0E, [6]

This bit allows the output drivers for the LLC1 and LLC2 pins of the ADV7183A to be three-stated. For more information on three-state control, refer to the following sections:

- Three-State Output Drivers
- Timing Signals Output Enable

Individual drive strength controls are provided via the DR_STR_XX bits.

Table 18. TRI_LLC Function

TRI_LLC	Description
0*	LLC pin drivers working according to the DR_STR_C[1:0] setting (pin enabled).
1	LLC pin drivers three-stated.

*Default value.

Timing Signals Output Enable

TIM_OE, Address 0x04, [3]

The TIM_OE bit should be regarded as an addition to the TOD bit. Setting it high forces the output drivers for HS, VS, and FIELD into the active (i.e., driving) state even if the TOD bit is set. If set to low, the HS, VS, and FIELD pins are three-stated dependent on the TOD bit. This functionality is useful if the decoder is to be used as a timing generator only. This may be the case if only the timing signals are to be extracted from an incoming signal, or if the part is in free-run mode where a separate chip can output, for instance, a company logo.

For more information on three-state control, refer to the following sections:

- Three-State Output Drivers
- Three-State LLC Driver

Individual drive strength controls are provided via the DR_STR_XX bits.

Table 19. TIM_OE Function

TIM_OE	Description
0*	HS, VS, FIELD three-stated according to the TOD bit.
1	HS, VS, FIELD are forced active all the time. The DR_STR_S[1:0] setting determines drive strength.

*Default value.

Drive Strength Selection (Data)

DR_STR[1:0] Address 0x04, [5:4]

For EMC and crosstalk reasons, it may be desirable to strengthen or weaken the drive strength of the output drivers. The DR_STR[1:0] bits affect the P[15:0] output drivers.

For more information on three-state control, refer to the following sections:

- Drive Strength Selection (Clock)
- Drive Strength Selection (Sync)

Table 20. DR_STR Function

DR_STR[1:0]	Description
00	Low drive strength (1×).
01*	Medium low drive strength (2×).
10	Medium high drive strength (3×).
11	High drive strength (4×).

*Default value.

Drive Strength Selection (Clock)

DR_STR_C[1:0] Address 0x0E, [3:2]

The DR_STR_C[1:0] bits can be used to select the strength of the clock signal output driver (LLC pin). For more information, refer to the following sections:

- Drive Strength Selection (Sync)
- Drive Strength Selection (Data)

Table 21. DR_STR Function

DR_STR[1:0]	Description
00	Low drive strength (1×).
01*	Medium low drive strength (2×).
10	Medium high drive strength (3×).
11	High drive strength (4×).

*Default value.

Drive Strength Selection (Sync)

DR_STR_S[1:0] Address 0x0E, [1:0]

The DR_STR_S[1:0] bits allow the user to select the strength of the synchronization signals with which HS, VS, and F are driven. For more information, refer to the following sections:

- Drive Strength Selection (Clock)
- Drive Strength Selection (Data)

Table 22. DR_STR Function

DR_STR[1:0]	Description
00	Low drive strength (1×).
01*	Medium low drive strength (2×).
10	Medium high drive strength (3×).
11	High drive strength (4×).

*Default value.

Enable Subcarrier Frequency Lock Pin

EN_SFL_PIN Address 0x04, [1]

The subcarrier frequency lock pin (SDP, output only) has a double function: it can also output raw sync-related information (SogOut). The EN_SFL_PIN bit enables the output of subcarrier lock information (also known as GenLock) from the SDP core to an encoder in a decoder-encoder back-to-back arrangement.

Table 23. EN_SFL_PIN

EN_SFL_PIN	Description
0*	Subcarrier frequency lock output is disabled.
1	Subcarrier frequency lock information is presented on the SFL pin.

*Default value.

Polarity LLC Pin

PCLK Address 0x37, [0]

The polarity of the clock that leaves the ADV7183A via the LLC1 and LLC2 pins can be inverted using the PCLK bit. Note that this inversion affects the clock for SDP.

Changing the polarity of the LLC clock output may be necessary to meet the setup-and-hold time expectations of follow-on chips.

Note that this bit also inverts the polarity of the LLC2 clock.

Table 24. PCLK Function

PCLK	Description
0	Invert LLC output polarity.
1*	LLC output polarity normal (as per the Timing Diagrams)

*Default value.

GLOBAL STATUS REGISTERS

There are four registers that provide summary information about the video decoder. The IDENT register allows the user to identify the revision code of the ADV7183A. The other three registers contain status bits from the SDP.

IDENTIFICATION

IDENT[7:0] Address 0x11, [7:0]

Provides identification of the revision of the ADV7183A. Please review the list of IDENT code readback values for the various versions shown in Table 25.

Table 25. IDENT Function

IDENT[7:0]	Description
0x0D	ADV7183A-ES1
0x0E	ADV7183A-ES2
0x0F or 0x10	ADV7183A-FT
0x11	ADV7183A (Version 2)

STATUS 1

STATUS_1[7:0] Address 0x10, [7:0]

This read-only register provides information about the internal status of the ADV7183A.

Please see CIL[2:0] Count Into Lock (SDP), Address 0x51, [2:0] and COL[2:0] Count Out of Lock (SDP), Address 0x51, [5:3] for information on the timing.

Depending on the setting of the FSCLE bit, the Status[0] and Status[1] are based solely on horizontal timing info or on the horizontal timing and lock status of the color subcarrier. See the FSCLE Fsc Lock Enable (SDP), Address 0x51, [7] section.

SDP Autodetection Result

AD_RESULT[2:0] Address 0x10, [6:4]

The AD_RESULT[2:0] bits report back on the findings from the SDP autodetection block. Consult the SDP General Setup section for more information on enabling the autodetection block, and the Autodetection of SDP Modes section to find out how to configure it.

Table 26. AD_RESULT Function

AD_RESULT[2:0]	Description
000	NTSM-MJ
001	NTSC-443
010	PAL-M
011	PAL-60
100	PAL-BGHID
101	SECAM
110	PAL-Combination N
111	SECAM 525

Table 27. STATUS 1 Function

STATUS 1 [7:0]	Bit Name	Block	Description
0	IN_LOCK	SDP	In lock (right now).
1	LOST_LOCK	SDP	Lost lock (since last read of this register).
2	FSC_LOCK	SDP	Fsc locked (right now).
3	FOLLOW_PW	SDP	AGC follows peak white algorithm.
4	AD_RESULT.0	SDP	Result of SDP autodetection.
5	AD_RESULT.1	SDP	Result of SDP autodetection.
6	AD_RESULT.2	SDP	Result of SDP autodetection.
7	COL_KILL	SDP	Color kill active.

STATUS 2

STATUS_2[7:0], Address 0x12, [7:0]

Table 28. STATUS 2 Function

STATUS 2 [7:0]	Bit Name	Block	Description
0	MVCS DET	SDP	Detected Macrovision color striping.
1	MVCS T3	SDP	Macrovision color striping protection. Conforms to Type 3 (if high), and Type 2 (if low).
2	MV_PS DET	SDP	Detected Macrovision pseudo Sync pulses.
3	MV_AGC DET	SDP	Detected Macrovision AGC pulses.
4	LL_NSTD	SDP	Line length is nonstandard.
5	FSC_NSTD	SDP	Fsc frequency is nonstandard.
6	Reserved		
7	Reserved		

STATUS 3

STATUS_3[7:0], Address 0x13, [7:0]

Table 29. STATUS 3 Function

STATUS 3 [7:0]	Bit Name	Block	Description
0	INST_HLOCK	SDP	Horizontal lock indicator (instantaneous).
1			Reserved for future use.
2			Reserved for future use.
3			Reserved for future use.
4	FREE_RUN_ACT	SDP	SDP outputs a blue screen (see theDEF_VAL_AUTO_EN Default Value Automatic Enable (SDP), Address 0x0C, [1] section).
5	STD_FLD_LEN	SDP	Field length is correct for currently selected video standard.
6	INTERLACED	SDP	Interlaced video detected (field sequence found).
7	PAL_SW_LOCK	SDP	Reliable sequence of swinging bursts detected.

STANDARD DEFINITION PROCESSOR (SDP)

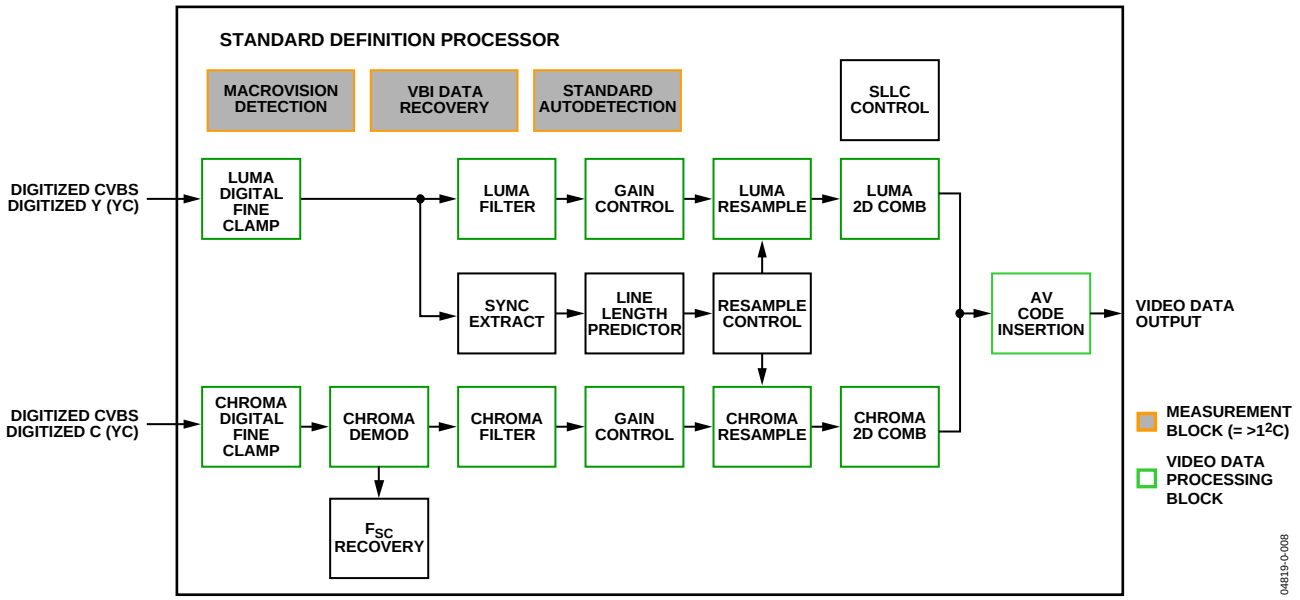

Figure 8. Block Diagram of the Standard Definition Processor

A block diagram of the ADV7183A's standard definition processor (SDP) is shown in Figure 8.

The SDP block can handle standard definition video in CVBS, YC, and YPrPb formats. It can be divided into a luminance and chrominance path. If the input video is of a composite type (CVBS), both processing paths are fed with the CVBS input.

SD LUMA PATH

The input signal is processed by the following blocks:

- Digital Fine Clamp. This block uses a high precision algorithm to clamp the video signal.
- Luma Filter Block. This block contains a luma decimation filter (YAA) with a fixed response, and some shaping filters (YSH) that have selectable responses.
- Luma Gain Control. The automatic gain control (AGC) can operate on a variety of different modes, including gain based on the depth of the horizontal sync pulse, peak white mode, and fixed manual gain.
- Luma Resample. To correct for line-length errors as well as dynamic line-length changes, the data is digitally resampled.
- Luma 2D Comb. The two-dimensional comb filter provides YC separation.
- AV Code Insertion. At this point, the decoded luma (Y) signal is merged with the retrieved chroma values. AV codes (as per ITU-R. BT-656) can be inserted.

SD CHROMA PATH

The input signal is processed by the following blocks:

- Digital Fine Clamp. This block uses a high precision algorithm to clamp the video signal.
- Chroma Demodulation. This block employs a color subcarrier (Fsc) recovery unit to regenerate the color subcarrier for any modulated chroma scheme. The demodulation block then performs an AM demodulation for PAL and NTSC ,and an FM demodulation for SECAM.
- Chroma Filter Block. This block contains a chroma decimation filter (CAA) with a fixed response, and some shaping filters (CSH) that have selectable responses.
- Gain Control. Automatic gain control (AGC) can operate on several different modes, including gain based on the color subcarrier's amplitude, gain based on the depth of the horizontal sync pulse on the luma channel, or fixed manual gain.
- Chroma Resample. The chroma data is digitally resampled to keep it perfectly aligned with the luma data. The resampling is done to correct for static and dynamic line-length errors of the incoming video signal.
- Chroma 2D Comb. The two-dimensional, 5-line, superadaptive comb filter provides high quality YC separation in case the input signal is CVBS.
- AV Code Insertion. At this point, the demodulated chroma (Cr and Cb) signal is merged with the retrieved luma values. AV codes (as per ITU-R. BT-656) can be inserted.

SDP SYNC PROCESSING

The SDP extracts syncs embedded in the video data stream. There is currently no support for external HS/VS inputs. The sync extraction has been optimized to support imperfect video sources (e.g., videocassette recorders with head switches). The actual algorithm used employs a coarse detection based on a threshold crossing followed by a more detailed detection using an adaptive interpolation algorithm. The raw sync information is sent to a line-length measurement and prediction block. The output of this is then used to drive the digital resampling section to ensure that the SDP outputs 720 active pixels per line.

The sync processing on the ADV7183A also includes two specialized postprocessing blocks that filter and condition the raw sync information retrieved from the digitized analog video.

- VSYNC Processor. This block provides extra filtering of the detected VSYNCs to give improved vertical lock.
- HSYNC Processor. The HSYNC processor is designed to filter incoming HSYNCs that have been corrupted by noise, providing much improved performance for video signals with stable time base but poor SNR.

SDP VBI DATA RECOVERY

The SDP can retrieve the following information from the input video:

- Wide-screen signaling (WSS)
- Copy generation management system (CGMS)
- Closed caption (CC)
- Macrovision protection presence
- EDTV data
- Gemstar compatible data slicing

The SDP is also capable of automatically detecting the incoming video standard with respect to

- Color subcarrier frequency
- Field rate
- Line rate

and can configure itself to support PAL-BGHID, PAL-M/N, PAL-combination N, NTSC-M, NTSC-J, SECAM 50 Hz/60 Hz, NTSC4.43, and PAL60.

SDP GENERAL SETUP

Video Standard Selection (SDP)

The VID_SEL[3:0] register allows the user to force the digital core into a specific video standard. Under normal circumstances, this should not be necessary. The VID_SEL[3:0] bits default to an autodetection mode that supports PAL, NTSC, SECAM, and variants thereof.

Refer to the Autodetection of SDP Modes section for more information on the autodetection system.

Autodetection of SDP Modes

In order to guide the autodetect system of the SDP block, individual enable bits are provided for each of the supported video standards. Setting the relevant bit to 0 inhibits the standard from being detected automatically. Instead, the system picks the closest of the remaining enabled standards. The results of SDP autodetection can be read back via the status registers. See the Global Status Registers section for more information.

Table 30. VID_SEL Function

VID_SEL[3:0] Address 0x00 [7:4]	Description
0000*	Autodetect (PAL BGHID) <–> NTSC J.
0001	Autodetect (PAL BGHID) <–> NTSC M.
0010	Autodetect (PAL N) <–> NTSC J.
0011	Autodetect (PAL N) <–> NTSC M.
0100	NTSC J (1)
0101	NTSC M (1).
0110	PAL 60.
0111	NTSC 4.43 (1).
1000	PAL BGHID.
1001	PAL N (= PAL BGHID (with pedestal)).
1010	PAL M (without pedestal).
1011	PAL M.
1100	PAL combination N.
1101	PAL combination N (with pedestal).
1110	SECAM.
1111	SECAM (with pedestal).

*Default value.

AD_SEC525_EN Enable Autodetection of SECAM 525 line video (SDP), Address 0x07, [7]

Table 31. AD_SEC525_EN Function

AD_SEC525_EN	Description
0*	Disable the autodetection of a 525-line system with a SECAM style, FM-modulated color component.
1	Enable the detection.

*Default value.

AD_SECAM_EN Enable Autodetection of SECAM (SDP), Address 0x07, [6]

Table 32. AD_SECAM_EN Function

AD_SECAM_EN	Description
0	Disable the autodetection of SECAM.
1*	Enable the detection.

*Default value.

AD_N443_EN Enable Autodetection of NTSC 443 (SDP), Address 0x07, [5]

Table 33. AD_N443_EN Function

AD_N443_EN	Description
0	Disable the autodetection of NTSC style systems with a 4.43 MHz color subcarrier.
1*	Enable the detection.

*Default value.

AD_P60_EN Enable Autodetection of PAL60 (SDP), Address 0x07, [4]

Table 34. AD_P60_EN Function

AD_P60_EN	Description
0	Disable the autodetection of PAL systems with a 60 Hz field rate.
1*	Enable the detection.

*Default value.

AD_PALN_EN Enable Autodetection of PAL N (SDP), Address 0x07, [3]

Table 35. AD_PALN_EN Function

AD_PALN_EN	Description
0	Disable the detection of the PAL N standard.
1*	Enable the detection.

*Default value.

AD_PALM_EN Enable Autodetection of PAL M (SDP), Address 0x07, [2]

Table 36. AD_PALM_EN Function

AD_PALM_EN	Description
0	Disable the autodetection of PAL M.
1*	Enable the detection.

*Default value.

AD_NTSC_EN Enable Autodetection of NTSC (SDP), Address 0x07, [1]

Table 37. AD_NTSC_EN Function

AD_NTSC_EN	Description
0	Disable the detection of standard NTSC.
1*	Enable the detection.

*Default value.

AD_PAL_EN Enable Autodetection of PAL (SDP), Address 0x07, [0]

Table 38. AD_PAL_EN Function

AD_PAL_EN	Description
0	Disable the detection of standard PAL.
1*	Enable the detection.

*Default value.

SFL_INV Subcarrier Frequency Lock Inversion (SDP)

This bit controls the behavior of the PAL switch bit in the SFL (GenLock Telegram) data stream. It was implemented to solve some compatibility issues with video encoders. It solves two problems:

1. The PAL switch bit is only meaningful in PAL. Some encoders (including Analog Devices encoders) also look at the state of this bit in NTSC.
2. There was a design change in Analog Devices encoders from ADV717x to ADV719x. The older versions used the SFL (GenLock Telegram) bit directly, while the later ones invert the bit prior to using it. The reason for this is that the inversion compensated for the 1-line delay of an SFL (GenLock Telegram) transmission.

As a result:

1. ADV717x encoders need the PAL switch bit in the SFL (GenLock Telegram) to be 1 for NTSC to work.
2. ADV7190/ADV7191/ADV7194 encoders need the PAL switch bit in the SFL to be 0 to work in NTSC.

If the state of the PAL switch bit is wrong, a 180°phase shift occurs.

In a decoder/encoder back-to-back system in which SFL is used, this bit must be set up properly for the specific encoder used.

Table 39. SFL_INV Function

SFL_INV Address 0x41, [6]	Description
0	SFL compatible with ADV7190/ADV7191/ ADV7194 encoders.
1*	SFL compatible with ADV717x/ADV7173x encoders.

*Default value.

Lock Related Controls (SDP)

Lock information is presented to the user through Bits [1:0] of the Status 1 register. See the STATUS_1[7:0] Address 0x10, [7:0] section. Figure 9 outlines the signal flow and the controls available to influence the way the lock status information is generated.

SRLS Select Raw Lock Signal (SDP), Address 0x51, [6]

Using the SRLS bit, the user can choose between two sources for determining the lock status (per Bits [1:0] in the Status 1 register).

- The time_win signal is based on a line-to-line evaluation of the horizontal synchronization pulse of the incoming video. It reacts quite quickly.
- The free_run signal evaluates the properties of the incoming video over several fields, and takes vertical synchronization information into account.

Table 40. SRLS Function

SRLS	Description
0*	Select the free_run signal.
1	Select the time_win signal.

*Default value.

FSCLE Fsc Lock Enable (SDP), Address 0x51, [7]

The FSCLE bit allows the user to choose whether the status of the color subcarrier loop is taken into account when the overall lock status is determined and presented via Bits [1:0] in Status Register 1. This bit must be set to 0 when operating the SDP in YPrPb component mode in order to generate a reliable HLOCK status bit.

Table 41. FSCLE Function

FSCLE	Description
0	Overall lock status only dependent on horizontal sync lock.
1*	Overall lock status dependent on horizontal sync lock and Fsc Lock.

*Default value.

CIL[2:0] Count Into Lock (SDP), Address 0x51, [2:0]

CIL[2:0] determines the number of consecutive lines for which the into lock condition must be true before the system switches into the locked state, and reports this via Status 0 [1:0].

Table 42. CIL Function

CIL[2:0]	Description (Count Value in Lines of Video)
000	1
001	2
010	5
011	10
100*	100
101	500
110	1000
111	100000

*Default value.

COL[2:0] Count Out of Lock (SDP), Address 0x51, [5:3]

COL[2:0] determines the number of consecutive lines for which the out of lock condition must be true before the system switches into unlocked state, and reports this via Status 0 [1:0].

Table 43. COL Function

COL[2:0]	Description (Count Value in Lines of Video)
000	1
001	2
010	5
011	10
100*	100
101	500
110	1000
111	100000

*Default value.

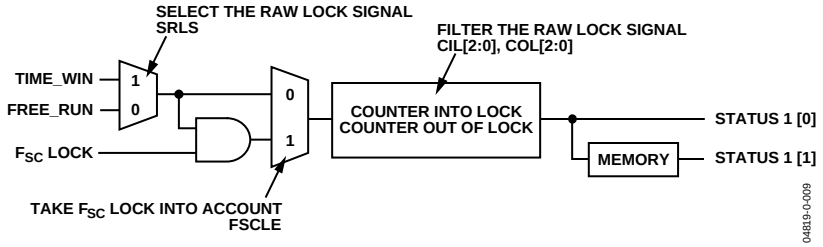

Figure 9. SDP Lock Related Signal Path

SDP COLOR CONTROLS

The following registers provide user control over the picture appearance, including control of the active data in the event of video being lost. They are independent of any other controls. For instance, brightness control is independent from picture clamping, although both controls affect the signal's dc level.

CON[7:0] Contrast Adjust (SDP), Address 0x08, [7:0]

This is the user control for contrast adjustment for the SDP block only.

Table 44. CON Function

CON[7:0]	Description (Adjust Contrast of the Picture)
0x80*	Gain on luma channel = 1.
0x00	Gain on luma channel = 0.
0xFF	Gain on luma channel = 2.

*Default value.

SAT[7:0] Saturation Adjust (SDP), Address 0x09, [7:0]

The user can adjust the saturation of the color output using this register. This registers affects the SDP core only.

ADI encourages users not to use the SAT[7:0] register, which may be removed in future revisions of the ADV7183A. Instead, the SD_SAT_Cb and SD_SAT_Cr registers should be used.

Table 45. SAT Function

SAT[7:0]	Description (Adjust Saturation of the Picture)
0x80*	Chroma gain = 0 dB.
0x00	Chroma gain = –42 dB.
0xFF	Chroma gain = 6 dB.

*Default value.

SD_SAT_Cb[7:0] SD Saturation Cb Channel (SDP), Address 0xE3, [7:0]

This register allows the user to control the gain of the Cb channel only.

For this register to be active , SAT[7:0] must be programmed with its default value of 0x80. If SAT[7:0] is programmed with a different value, SD_SAT_Cb[7:0] and SD_SAT_Cr[7:0] are inactive.

Table 46. SD_SAT_Cb Function

SD_SAT_Cb[7:0]	Description (Adjust Saturation of the Picture)
0x80*	Chroma gain = 0 dB.
0x00	
0xFF	

*Default value.

SD_SAT_Cr[7:0] SD Saturation Cr Channel (SDP), Address 0xE4, [7:0]

This register allows the user to control the gain of the Cr channel only. This register affects the SDP core only.

For this register to be active, SAT[7:0] must be programmed with its default value of 0x80. If SAT[7:0] is programmed with a different value, SD_SAT_Cb[7:0] and SD_SAT_Cr[7:0] are inactive.

Table 47. SD_SAT_Cr Function

SD_SAT_Cr[7:0]	Description (Adjust Saturation of the Picture)
0x80*	Chroma gain = 0 dB
0x00	
0xFF	

*Default value.

SD_OFF_Cb[7:0] SD Offset Cb Channel (SDP), Address 0xE1, [7:0]

This register allows the user to select an offset for the Cb channel only. This register affects the SDP core only. There is a functional overlap with the Hue [7:0] register.

Table 48.SD_OFF_Cb Function

SD_OFF_Cb[7:0]	Description (Adjust Hue of the Picture by Selecting an Offset for Data on the Cb Channel)
0x80*	
0x7F	
0xFF	

*Default value.

SD_OFF_Cr [7:0] SD Offset Cr Channel (SDP), Address 0xE2, [7:0]

This register allows the user to select an offset for the Cr channel only. This register affects the SDP core only. There is a functional overlap with the Hue [7:0] register.

Table 49. SD_OFF_Cr Function

SD_OFF_Cr[7:0]	Description (Adjust Hue of the Picture by Selecting an Offset for Data on Cr Channel)
0x80*	
0x7F	
0xFF	

*Default value.

BRI[7:0] Brightness Adjust (SDP), Address 0x0A, [7:0]

This register controls the brightness of the video signal through the SDP core.

Table 50. BRI Function

BRI[7:0]	Description (Adjust Brightness of the Picture)
0x00*	Offset of the luma channel = 0IRE.
0x7F	Offset of the luma channel = 100IRE.
0xFF	Offset of the luma channel = –100IRE.

*Default value.

HUE[7:0] Hue Adjust (SDP), Address 0x0B, [7:0]

This register contains the value for the color hue adjustment.

HUE[7:0] has a range of ±90°, with 0x00 equivalent to an adjustment of 0°. The resolution of HUE[7:0] is 1 bit = 0.7°.

The hue adjustment value is fed into the AM color demodulation block. Therefore, it only applies to video signals that contain chroma information in the form of an AM modulated carrier (CVBS or Y/C in PAL or NTSC). It does not affect SECAM and does not work on component video inputs (YPrPb).

Table 51. HUE Function

HUE[7:0]	Description (Adjust Hue of the Picture)
0x00*	Phase of the chroma signal = 0°.
0x7F	Phase of the chroma signal = –90°.
0xFF	Phase of the chroma signal = +90°.

*Default value.

DEF_Y[5:0] Default Value Y (SDP), Address 0x0C, [7:2]

In cases where the ADV7183A loses lock on the incoming video signal or where there is no input signal, the DEF_Y[5:0] register allows the user to specify a default luma value to be output.

This value is used under the following conditions:

- If DEF_VAL_AUTO_EN bit is set to high and the ADV7183A lost lock to the input video signal. This is the intended mode of operation (automatic mode).
- The DEF_VAL_EN bit is set, regardless of the lock status of the video decoder.
- This is a forced mode that may be useful during configuration.

The DEF_Y[5:0] values define the 6 MSBs of the output video. The remaining LSBs are padded with 0s. For example, in 8-bit mode, the output is Y[7:0] = {DEF_Y[5:0], 0, 0}.

Table 52. DEF_Y Function

DEF_Y[5:0]	Description
0x36 (Blue)*	Default value of Y.

*Default value.

DEF_C[7:0] Default Value C (SDP), Address 0x0D, [7:0]

The DEF_C[7:0] register complements the DEF_Y[5:0] value. It defines the 4 MSBs of Cr and Cb values to be output if

- The DEF_VAL_AUTO_EN bit is set to high and the ADV7183A can't lock to the input video (automatic mode).
- DEF_VAL_EN bit is set to high (forced output).

The data that is finally output from the ADV7183A for the chroma side is Cr[7:0] = {DEF_C[7:4], 0, 0, 0, 0}, Cb[7:0] = {DEF_C[3:0], 0, 0, 0, 0}.

Table 53. DEF_C Function

DEF_C[7:0]	Description
0x7C (blue)*	Default values for Cr and Cb.

*Default value.

DEF_VAL_EN Default Value Enable (SDP), Address 0x0C, [0]

This bit forces the use of the default values for Y, Cr, and Cb. Refer to the descriptions for DEF_Y and DEF_C for additional information. The decoder also outputs a stable 27 MHz clock, HS, and VS in this mode.

Table 54. DEF_VAL_EN Function

DEF_VAL_EN	Description
0*	Don't force the use of default Y, Cr, and Cb values. Output colors dependent on DEF_VAL_AUTO_EN.
1	Always use default Y, Cr, and Cb values. Override picture data even if the video decoder is locked.

*Default value.

DEF_VAL_AUTO_EN Default Value Automatic Enable (SDP), Address 0x0C, [1]

This bit enables the automatic usage of the default values for Y, Cr, and Cb in cases where the ADV7183A cannot lock to the video signal.

Table 55. DEF_VAL_AUTO_EN Function

DEF_VAL_AUTO_EN	Description
0	Don't use default Y, Cr, and Cb values. If unlocked, output noise.
1*	Use default Y, Cr, and Cb values when decoder loses lock.

*Default value.

SDP CLAMP OPERATION

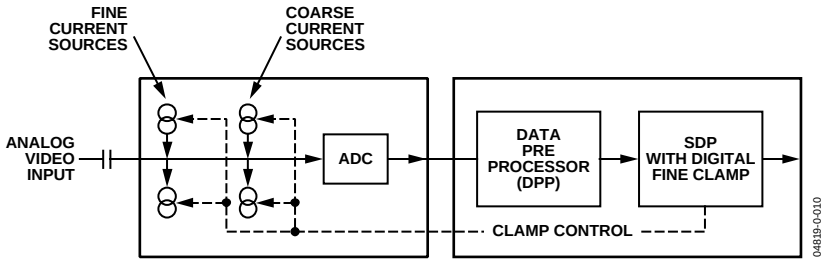

Figure 10. SDP Clamping Overview

The input video is ac-coupled into the ADV7183A. Therefore, its dc value needs to be restored. This process is referred to as clamping the video. This section explains the general process of clamping on the ADV7183A for the SDP, and shows the different ways in which a user can configure its behavior.

The SDP block uses a combination of current sources and a digital processing block for clamping, as shown in Figure 10. The analog processing channel shown is replicated three times inside the IC. While only one single channel (and only one ADC) would be needed for a CVBS signal, two independent channels are needed for YC (S-VHS) type signals, and three independent channels are needed to allow component signals (YPrPb) to be processed.

The clamping can be divided into two sections:

- Clamping before the ADC (analog domain): current sources.
- Clamping after the ADC (digital domain): digital processing block.

The ADCs can digitize an input signal only if it resides within the ADC's 1.6 V input voltage range. An input signal with a dc level that is too large or too small is clipped at the top or bottom of the ADC range.

The primary task of the analog clamping circuits is to ensure that the video signal stays within the valid ADC input window so the analog-to-digital conversion can take place. It is not necessary to clamp the input signal with a very high accuracy in the analog domain as long as the video signal fits the ADC range.

After digitization, the digital fine clamp block corrects for any remaining variations in dc level. Since the dc level of an input video signal refers directly to the brightness of the picture transmitted, it is important to perform a fine clamp with high accuracy; otherwise, brightness variations may occur. Furthermore, dynamic changes in the dc level will almost certainly lead to visually objectionable artifacts, and must therefore be prohibited.

The clamping scheme has to complete two tasks: it must be able to acquire a newly connected video signal with a completely unknown dc level, and it must maintain the dc level during normal operation.

For a fast acquiring of an unknown video signal, the large current clamps may be activated[7]. Control of the coarse and fine current clamp parameters is performed automatically by the decoder.

Standard definition video signals may have excessive noise on them. In particular, CVBS signals transmitted by terrestrial broadcast and demodulated using a tuner usually show very large levels of noise (>100 mV). A voltage clamp would be unsuitable for this type of video signal. Instead, the ADV7183A employs a set of four current sources that can cause coarse (>0.5 mA) and fine (<0.1 mA) currents to flow into and away from the high impedance node that carries the video signal (see Figure 10).

The following sections describe the I^2C signals that can be used to influence the behavior of SDP clamping.

Previous revisions of the ADV7183A had controls (FACL/FICL, fast and fine clamp length) to allow configuration of the length for which the coarse (fast) and fine current sources are switched on. These controls were removed on the ADV7183A-FT and replaced by an adaptive scheme.

CCLEN Current Clamp Enable (SDP), Address 0x14, [4]

The current clamp enable bit allows the user to switch off the current sources in the analog front end altogether. This may be useful if the incoming analog video signal is clamped externally.

Table 56. CCLEN Function

CCLEN	Description
0	Current sources switched off.
1*	Current sources enabled.

*Default value.

[7] It is assumed that the amplitude of the video signal at this point is of a nominal value.

DCT[1:0] Digital Clamp Timing (SDP), Address 0x15, [6:5]

The Clamp Timing register determines the time constant of the digital fine clamp circuitry. It is important to realize that the digital fine clamp reacts very fast since it is supposed to immediately correct any residual dc level error for the active line. The time constant of the digital fine clamp must be much quicker than the one from the analog blocks.

By default, the time constant of the digital fine clamp is adjusted dynamically to suit the currently connected input signal.

Table 57. DCT Function

DCT[1:0]	Description
00	Slow (TC = 1 sec).
01	Medium (TC = 0.5 sec).
10*	Fast (TC = 0.1 sec).
11	Determined by ADV7183A dependent on video parameters.

*Default value.

DCFE Digital Clamp Freeze Enable (SDP), Address 0x15, [4]

This register bit allows the user to freeze the digital clamp loop at any time. It is intended for users who would like to do their own clamping. Users should disable the current sources for analog clamping via the appropriate register bits, wait until the digital clamp loop settles, and then freeze it via the DCFE bit.

Table 58.

DCFE	Description
0*	Digital clamp operational.
1	Digital clamp loop frozen.

*Default value.

SDP LUMA FILTER

Data[8] from the digital fine clamp block is processed by four sets of filters:

- Luma antialias filter (YAA). The SDP received video at a rate of 27 MHz[9]. The ITU-R BT.601 recommends a sampling frequency of 13.5 MHz. The luma antialias filter decimates the oversampled video using a high quality, linear phase, low-pass filter that preserves the luma signal while at the same time attenuating out-of-band components. The luma antialias filter (YAA) has a fixed response.
- Luma shaping filters (YSH). The shaping filter block is a programmable low-pass filter with a wide variety of responses. It can be used to selectively reduce the luma video signal bandwidth (needed prior to scaling, for example). For some video sources that contain high frequency noise, reducing the bandwidth of the luma signal improves visual picture quality. A follow-on video compression stage may work more efficiently if the video is low-pass filtered.

  The ADV7183A allows selection of two responses for the shaping filter: one that is used for good quality CVBS, component, and S-VHS type sources, and a second for nonstandard CVBS signals.

  The YSH filter responses also include a set of notches for PAL and NTSC. However, it is recommended to use the comb filters for YC separation.
- Luma peaking filter. This filter can be manually enabled. The user can select to boost or attenuate the midregion of the Y spectrum around 3 MHz. The peaking filter may visually improve the picture by showing more definition on those picture details that contain frequency components around 3 MHz. The peaking filter compensates for the effects of a wide notch filter: Where the notch starts to fall off, the peaking filter lifts the overall response back on.
- Digital resampling filter. This block is used to allow dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system with no requirement for user intervention.

Figure 12 through Figure 15 show the overall response of all filters together. Unless otherwise noted, the filters are set into a typical wideband mode, and the peaking function is disabled.

Y Shaping Filter

For input signals in CVBS format, the luma shaping filters play an essential role in removing the chroma component from a composite signal. YC separation must aim for best possible crosstalk reduction while still retaining as much bandwidth (especially on the luma component) as possible. High quality YC separation can be achieved by using the internal comb filters of the ADV7183A. Comb filtering, however, relies on the frequency relationship of the luma component (multiples of the video line rate) and the color subcarrier (Fsc). For good quality CVBS signals, this relationship is known; the comb filter algorithms can be used to separate out luma and chroma with high accuracy.

In the case of nonstandard video signals, the frequency relationship may be disturbed and the comb filters may not be able to remove all crosstalk artifacts in an optimum fashion without the assistance of the shaping filter block.

[8] The data format at this point is CVBS for CVBS input or luma only for Y/C and YPrPb input formats.

[9] In the case of 4× oversampled video, the ADCs sample at 54 MHz, and the first decimation is performed inside the DPP filters. Therefore, the data rate into the SDP core is always 27 MHz.

An automatic mode is provided. Here, the ADV7183A evaluates the quality of the incoming video signal and selects the filter responses in accordance with the signal quality and video standard. YFSM, WYSFMOVR, and WYSFM allow the user to manually override the automatic decisions in part or in full.

The luma shaping filter has three control registers:

- YSFM[4:0] allows the user to manually select a shaping filter mode (applied to all video signals) or to enable an automatic selection (dependent on video quality and video standard).
- WYSFMOVR allows the user to manually override the WYSFM decision.
- WYSFM[4:0] allows the user to select a different shaping filter mode for good quality CVBS, component (YPrPb), and S-VHS (YC) input signals.

In automatic mode, the system preserves the maximum possible bandwidth for good CVBS sources (since they can successfully be combed) as well as for luma components of YPrPb and YC sources, since they need not be combed. For poor quality signals, the system selects from a set of proprietary shaping filter responses that complements comb filter operation in order to reduce visual artifacts.

The decisions of the control logic are shown in Figure 11.

YSFM[4:0] Y Shaping Filter Mode (SDP), Address 0x17, [4:0]

The Y shaping filter mode bits allow the user to select from a wide range of low-pass and notch filters. When switched in automatic mode, the filter is selected based on other register selections (e.g., detected video standard) as well as properties extracted from the incoming video itself (e.g., quality, time base stability). The automatic selection always picks the widest possible bandwidth for the video input encountered.

- If the YSFM settings specify a filter (i.e., YSFM is set to values other than 00000 or 00001), the chosen filter is applied to all video, regardless of its quality.
- In automatic selection mode, the notch filters are only used for bad quality video signals. For all other video signals, wideband filters are used.

WYSFMOVR Wideband Y Shaping Filter Override (SDP), Address 0x18,[7]

Setting the WYSFMOVR bit enables the use of the WYSFM[4:0] settings for good quality video signals. For more information, refer to the general discussion of the luma shaping filters in the Y Shaping Filter section and the flowchart shown in Figure 11.

Table 59.

WYSFMOVR	Description
0	Automatic selection of shaping filter for good quality video signals.
1*	Enable manual override via WYSFM[4:0].

*Default value.

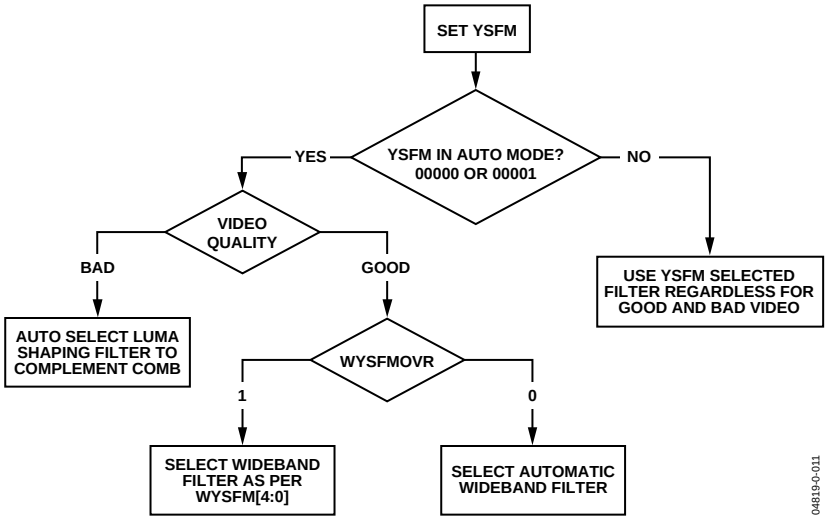

Figure 11. YSFM and WYSFM Control Flowchart

Table 60. YSFM Function

YSFM[4:0]	Description
0'0000	Automatic selection including a wide notch response (PAL/NTSC/SECAM)
0'0001*	Automatic selection including a narrow notch response (PAL/NTSC/SECAM)
0'0010	SVHS 1
0'0011	SVHS 2
0'0100	SVHS 3
0'0101	SVHS 4
0'0110	SVHS 5
0'0111	SVHS 6
0'1000	SVHS 7
0'1001	SVHS 8
0'1010	SVHS 9
0'1011	SVHS 10
0'1100	SVHS 11
0'1101	SVHS 12
0'1110	SVHS 13
0'1111	SVHS 14
1'0000	SVHS 15
1'0001	SVHS 16
1'0010	SVHS 17
1'0011	SVHS 18 (CCIR 601)
1'0100	PAL NN 1
1'0101	PAL NN 2
1'0110	PAL NN 3
1'0111	PAL WN 1
1'1000	PAL WN 2
1'1001	NTSC NN 1
1'1010	NTSC NN 2
1'1011	NTSC NN 3
1'1100	NTSC WN 1
1'1101	NTSC WN 2
1'1110	NTSC WN 3
1'1111	Reserved

*Default value.

WYSFM[4:0] Wide Band Y Shaping Filter Mode (SDP), Address 0x18, [4:0]

The WYSFM[4:0] bits allow the user to manually select a shaping filter for good quality video signals (e.g., CVBS with stable time base, luma component of YPrPb, luma component of YC). The WYSFM bits are only active if the WYSFMOVR bit is set to 1. See the general discussion of the shaping filter settings in the Y Shaping Filter section.

Table 61. WYSFM Function

WYSFM[4:0]	Description
0'0000	Do not use
0'0001	Do not use
0'0010	SVHS 1
0'0011	SVHS 2
0'0100	SVHS 3
0'0101	SVHS 4
0'0110	SVHS 5
0'0111	SVHS 6
0'1000	SVHS 7
0'1001	SVHS 8
0'1010	SVHS 9
0'1011	SVHS 10
0'1100	SVHS 11
0'1101	SVHS 12
0'1110	SVHS 13
0'1111	SVHS 14
1'0000	SVHS 15
1'0001	SVHS 16
1'0010	SVHS 17
1'0011*	SVHS 18 (CCIR 601)
1'0100–1'1111	Do not use

*Default value.

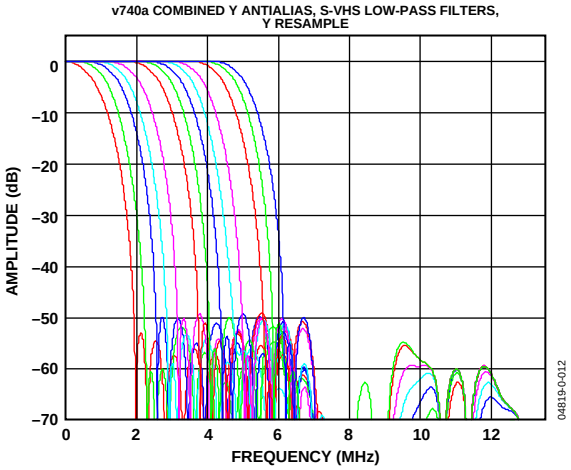

Figure 12. SDP Y S-VHS Combined Responses

The filter plots in Figure 12 show the S-VHS 1 (narrowest) to S-VHS 18 (widest) shaping filter settings. Figure 14 shows the PAL notch filter responses. The NTSC compatible notches are shown in Figure 15.

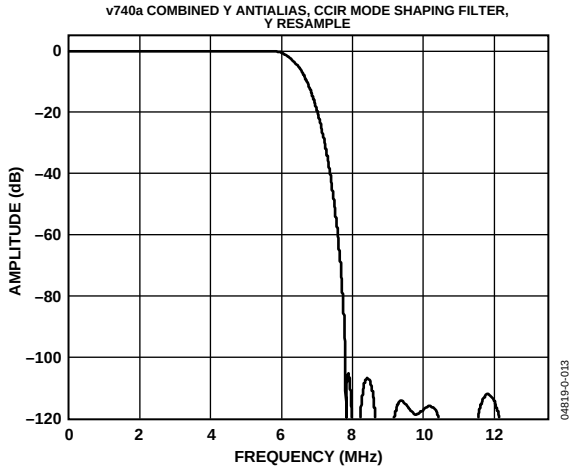

Figure 13. SDP Y S-VHS 18 Extra Wideband Filter (CCIR 601 Compliant)

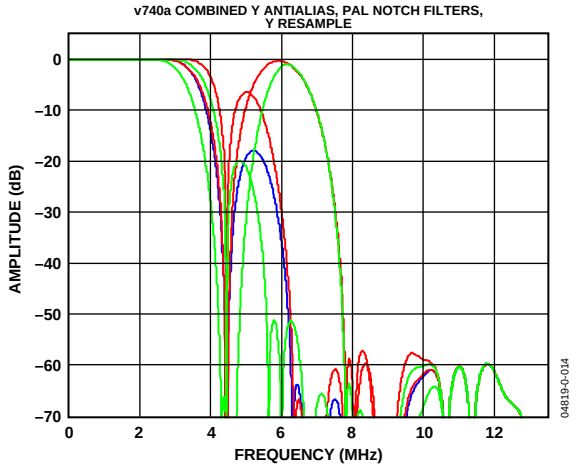

Figure 14. SDP Y S-VHS 18 Extra Wideband Filter (CCIR 601 Compliant)

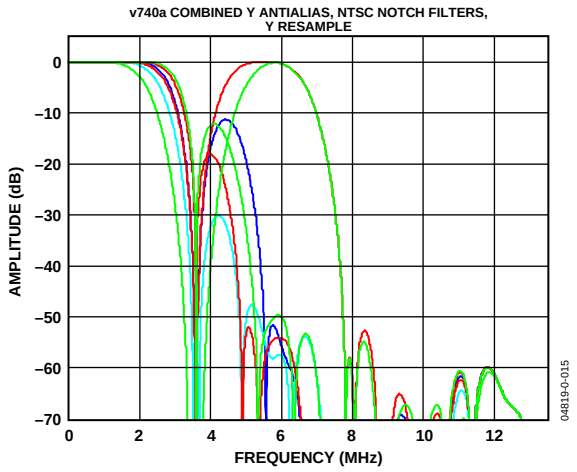

Figure 15. SDP Y S-VHS 18 Extra Wideband Filter (601)

YPM[2:0] Y Peaking Filter Mode (SDP), Address 0x02, [2:0]

Allows the user to select peaking. This function allows the user to boost/attenuate luma signals around the color subcarrier frequency. Selecting YPM = 000,001,010,011 sharpens the image; YPM = 101,110,111 attenuates the luma around the color subcarrier. In cases of incomplete cancellation in the Y comb filter, this could be used to attenuate any residual C components (hanging dots) in the Y output at the cost of a softer image.

Table 62. YPM Function

	Filter Response (Peak Position)	
YPM[2:0]	**Composite (2.6 MHz)**	**S-VHS (3.75 MHz)**
000	+4.5 dB	+9.25 dB
001	+4.5 dB	+9.25 dB
010	+4.5 dB	+5.75 dB
011	+1.25 dB	+3.3 dB
100*	0	0
101	–1.25 dB	–3.0 dB
110	–1.75 dB	–8.0 dB
111	–3.0 dB	–8.0 dB

*Default value.

SDP CHROMA FILTER

Data[10] from the digital fine clamp block is processed by two sets of filters:

- Chroma Antialias Filter (CAA). The ADV7183A oversamples the CVBS by a factor of 2 and the Chroma/PrPb by a factor of 4. A decimating filter (CAA) is used to preserve the active video band and remove any out-of-band components. The CAA filter has a fixed response.
- Chroma Shaping Filters (CSH). The shaping filter block (CSH) can be programmed to perform a variety of low-pass responses. It can be used to selectively reduce the bandwidth of the chroma signal for scaling or compression.
- Digital Resampling Filter. This block is used to allow dynamic resampling of the video signal to alter parameters such as the time base of a line of video. Fundamentally, the resampler is a set of low-pass filters. The actual response is chosen by the system with no requirement for user intervention.

The plots in Figure 16 show the overall response of all filters together.

[10] The data format at this point is CVBS for CVBS inputs, chroma only for Y/C, or U/V interleaved for YPrPb input formats.

CSFM[2:0] C Shaping Filter Mode (SDP), Address 0x17, [7]

The C shaping filter mode bits allow the user to select from a range of low-pass filters for the chrominance signal. When switched in automatic mode, the widest filter is selected based on the video standard/format and user choice (see settings 000 and 001 in Table 63).

Table 63. CSFM Function

CSFM[2:0]	Description
000*	Autoselect 1.5 MHz bandwidth
001	Autoselect 2.17 MHz bandwidth
010	SH1
011	SH2
100	SH3
101	SH4
110	SH5
111	Wideband Mode

*Default value.

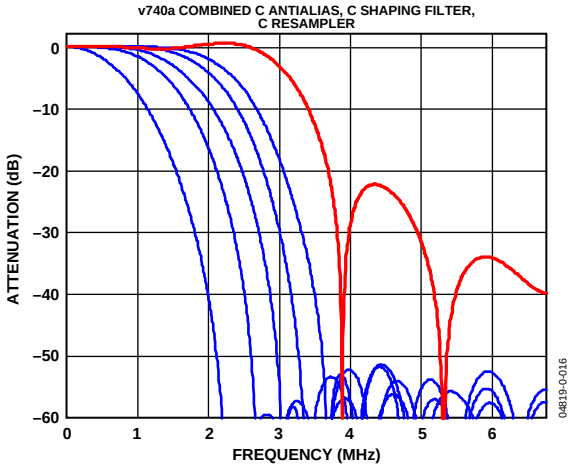

Figure 16. SDP Chroma Shaping Filter Responses

Figure 16 shows the responses of SH1 (narrowest) to SH5 (widest) in addition to the wideband mode (in red).

SDP GAIN OPERATION

The gain control within the ADV7183A is done on a purely digital basis. The input ADCs support a 10-bit range, mapped into a 1.6 V analog voltage range. Gain correction takes place after the digitization in the form of a digital multiplier.

There are several advantages of this architecture over the commonly used PGA (programmable gain amplifier) before the ADCs; among them is the fact that the gain is now completely independent of supply, temperature, and process variations.

As shown in Figure 17, the ADV7183A can decode a video signal as long as it fits into the ADC window. There are two components to this: the amplitude of the input signal and the dc level it resides on. The dc level is set by the clamping circuitry (see the SDP Clamp Operation section).

If the amplitude of the analog video signal is too high, clipping may occur, resulting in visual artifacts. The analog input range of the ADC, together with the clamp level, determines the maximum supported amplitude of the video signal.

The minimum supported amplitude of the input video is determined by the SDP core's ability to retrieve horizontal and vertical timing and to lock to the color burst (if present).

There are two gain control units, one each for luma and chroma data. Both can operate independently of each other. The chroma unit, however, can also take its gain value from the luma path.

Several AGC modes are possible; Table 64 summarizes them.

It is possible to freeze the automatic gain control loops. This will cause the loops to stop updating and the AGC determined gain at the time of the freeze stays active until the loop is either unfrozen or the gain mode of operation is changed.

The currently active gain from any of the modes can be read back. Please refer to the description of the dual function manual gain registers, LG[11:0] Luma Gain and CG[11:0] Chroma Gain, in the SDP Luma Gain and SDP Chroma Gain sections.

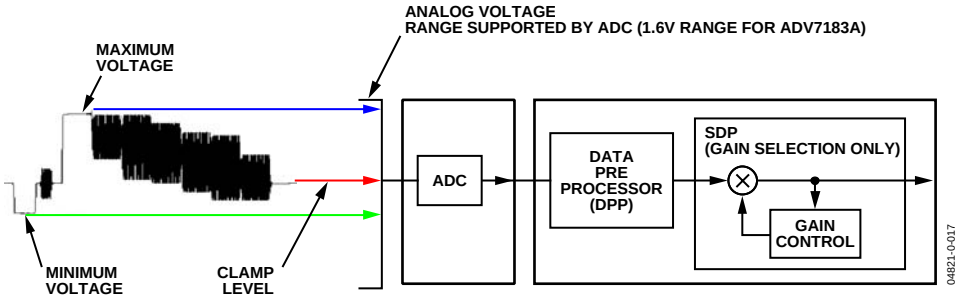

Figure 17. SDP Gain Control Overview

Table 64. SDP AGC Modes

Input Video Type	Luma Gain	Chroma Gain
Any	Manual gain luma.	Manual gain chroma.
CVBS	Dependent on horizontal sync depth.	Dependent on color burst amplitude. Taken from luma path.
	Peak White	Dependent on color burst amplitude. Taken from luma path.
Y/C	Dependent on horizontal sync depth.	Dependent on color burst amplitude. Taken from luma path.
	Peak White.	Dependent on color burst amplitude. Taken from luma path.
YPrPb	Dependent on horizontal sync depth.	Taken from luma path.

SDP Luma Gain

LAGC[2:0] Luma Automatic Gain Control (SDP), Address 0x30, [7:0]

The luma automatic gain control mode bits select the mode of operation for the gain control in the luma path.

There are ADI internal parameters to customize the peak white gain control. Contact ADI for more information.

Table 65. LAGC Function

LAGC[2:0]	Description
000	Manual fixed gain (use LMG[11:0]).
001	AGC (blank level to sync tip). No override through white peak.
010*	AGC (blank level to sync tip). Automatic override through white peak.
011	Reserved.
100	Reserved.
101	Reserved.
110	Reserved.
111	Freeze gain.

*Default value.

LAGT[1:0] Luma Automatic Gain Timing (SDP), Address 0x2F, [7:6]

The luma automatic gain timing register allows the user to influence the tracking speed of the luminance automatic gain control. Please note that this register only has an effect if the LAGC[2:0] register is set to 001, 010, 011, or 100 (automatic gain control modes).

If peak white AGC is enabled and active (see the STATUS_1[7:0] Address 0x10, [7:0] section), the actual gain update speed is dictated by the peak white AGC loop and, as a result, the LAGT settings have no effect. As soon as the part leaves peak white AGC, LAGT becomes relevant again.

The update speed for the peak white algorithm can be customized by the use of internal parameters. Please contact ADI for more information.

Table 66. LAGT Function

LAGT[1:0]	Description
00	Slow (TC = 2 sec)
01	Medium (TC = 1 sec)
10	Fast (TC = 0.2 sec)
11*	Adaptive

*Default value.

LG[11:0] Luma Gain (SDP), Address 0x2F, [3:0]; Address 0x30, [7:0]; LMG[11:0] Luma Manual Gain (SDP), Address 0x2F, [3:0]; Address 0x30, [7:0]

Luma gain [11:0] is a dual function register:

- If written to, a desired manual luma gain can be programmed. This gain becomes active if the LAGC[2:0] mode is switched to manual fixed gain.
- Equation 1 shows how to calculate a desired gain.
- If read back, this register returns the current gain value. Depending on the setting in the ALCM[2:0] bits, this is one of the following values:
    - Luma manual gain value (ALCM[2:0] set to luma manual gain mode)
    - Luma automatic gain value (ALCM[2:0] set to any of the automatic modes)

Table 67. LG/LMG Function

LG[11:0]/LMG[11:0]	Read/Write	Description
LMG[11:0] = X	Write	Manual gain for luma path.
LG[11:0]	Read	Actually used gain.

$$Luma_Gain = \frac{(0 < LG \le 4095)}{2048} = 0...2$$

Equation 1. SDP Luma Gain Formula

Example

Program the ADV7183A into manual fixed gain mode with a desired gain of 0.89:

- Use Equation 1 to convert the gain:
  $0.89 \times 2048 = 1822.72$
- Truncate to integer value:
  $1822.72 = 1822$
- Convert to hexadecimal:
  $1822_d = 0x71E$
- Split into two registers and program:
  Luma Gain Control 1 [3:0] = 0x7
  Luma Gain Control 2 [7:0] = 0x1E
- Enable Manual Fixed Gain Mode:
  Set LAGC[2:0] to 000

BETACAM Enable Betacam Levels (SDP), Address 0x01, [5]

If YPrPb data is routed through the SDP core, the automatic gain control modes can target different video input levels, as outlined in Table 72. Please note that the BETACAM bit is valid only if the input mode is YPrPb (component) and if the data is routed through the SDP core. The BETACAM bit basically sets the target value for AGC operation.

A review of the following sections is useful:

- INSEL[3:0] Input Selection, Address 0x00, [3:0] to find how component video (YPrPb) can be routed through the SDP core.
- Video Standard Selection (SDP) to select the various standards (e.g., with and without pedestal)

The automatic gain control (AGC) algorithms adjust the levels based on the setting of the BETACAM bit(see Table 68.).

Table 68. BETACAM Function

BETACAM	Description
0*	Assuming YPrPb is selected as input format.
	Selecting PAL with pedestal selects MII.
	Selecting PAL without pedestal selects SMPTE.
	Selecting NTSC with pedestal selects MII.
	Selecting NTSC without pedestal selects SMPTE.
1	Assuming YPrPb is selected as input format.
	Selecting PAL with pedestal selects BETACAM.
	Selecting PAL without pedestal selects BETACAM variant.
	Selecting NTSC with pedestal selects BETACAM.
	Selecting NTSC without pedestal selects BETACAM variant.

*Default value.

PW_UPD Peak White Update (SDP), Address 0x2B, [0]

The peak white and average video algorithms determine the gain based on measurements taken from the active video. The PW_UPD bit determines the rate of gain change. Please note that the LAGC[2:0] must be set to the appropriate mode to enable the peak white or average video mode in the first place. For more information, refer to the LAGC[2:0] Luma Automatic Gain Control (SDP), Address 0x30, [7:0] section.

Table 69. PW_UPD Function

PW_UPD	Description
0	Update gain once per video line.
1	Update gain once per field.

*Default value.

SDP Chroma Gain

CAGC[1:0] Chroma Automatic Gain Control (SDP), Address 0x2C, [1:0]

The two bits of Color Automatic Gain Control mode select the basic mode of operation for automatic gain control in the chroma path.

Table 70. CAGC Function

CAGC[1:0]	Description
00	Manual fixed gain (use CMG[11:0]).
01	Use luma gain for chroma.
10*	Automatic gain (based on color burst).
11	Freeze chroma gain.

*Default value.

CAGT[1:0] Chroma Automatic Gain Timing (SDP), Address 0x2D, [7:6]

The Chroma Automatic Gain Timing register allows the user to influence the tracking speed of the chroma automatic gain control. This register only has an effect if the CAGC[1:0] register is set to 10 (automatic gain).

Table 71. CAGT Function

CAGT[1:0]	Description
00	Slow (TC = 2 sec)
01	Medium (TC = 1 sec)
10	Fast (TC = 0.2 sec)
11*	Adaptive

*Default value.

Table 72. Betacam Levels

Name	Betacam (mV)	Betacam Variant (mV)	SMPTE (mV)	MII (mV)
Y Range	0 to 714 (incl. 7.5% pedestal)	0 to 714	0 to 700	0 to 700 (incl. 7.5% pedestal)
Pb and Pr Range	–467 to +467	–505 to +505	–350 to +350	–324 to +324
Sync Depth	286	286	300	300

CG[11:0] Chroma Gain (SDP), Address 0x2D, [3:0]; Address 0x2E, [7:0] CMG[11:0] Chroma Manual Gain (SDP), Address 0x2D, [3:0]; Address 0x2E, [7:0]

Chroma gain [11:0] is a dual function register:

- If written to, a desired manual chroma gain can be programmed. This gain becomes active if the CAGC[1:0] mode is switched to manual fixed gain.
- Refer to Equation 2 for calculating a desired gain.
- If read back, this register returns the current gain value. Depending on the setting in the CAGC[1:0] bits, this will be one of the following values:
    - Chroma manual gain value (CAGC[1:0] set to chroma manual gain mode).
    - Chroma automatic gain value (CAGC[1:0] set to any of the automatic modes).

Table 73. CG/CMG Function

CG[11:0]/CMG[11:0]	Read/Write	Description
CMG[11:0]	Write	Manual gain for chroma path.
CG[11:0]	Read	Currently active gain.

$$Chroma_Gain = \frac{(0 < CG \le 4095)}{1024} = 0...4$$

Equation 2. SDP Chroma Gain Formula

Example

Freezing the automatic gain loop and reading back the CG[11:0] register results in a value of

- Convert the read back value to decimal: $0x47A = 1146_d$
- Apply Equation 2 to convert the readback value: 1146/1024 = 1.12

CKE Color Kill Enable (SDP), Address 0x2B, [6]

The Color Kill Enable bit allows the optional color kill function to be switched on or off.

For QAM based video standards (PAL and NTSC) as well as FM based systems (SECAM), the threshold for the color kill decision is selectable via the CKILLTHR[2:0] bits.

If color kill is enabled, and if the color carrier of the incoming video signal is less than the threshold for 128 consecutive video lines, color processing is switched off (black and white output). To switch the color processing back on, another 128 consecutive lines with a color burst greater than the threshold are required.

The color kill option only works for input signals with a modulated chroma part. For component input (YPrPb), there is no color kill.

Table 74. CKE Function

CKE	Description
0	Color kill disabled.
1*	Color kill enabled.

*Default value.

CKILLTHR[2:0] Color Kill Threshold (SDP), Address 0x3D, [6:4]

The CKILLTHR[2:0] bits allow the user to select a threshold for the color kill function. The threshold only applies to QAM based (NTSC and PAL) or FM modulated (SECAM) video standards.

To enable the color kill function, the CKE bit must be set. For settings 000, 001, 010, and 011, chroma demodulation inside the ADV7183A may not work satisfactorily for poor input video signals.

Table 75. CKILLTHR Function

	Description	
CKILLTHR[2:0]	SECAM	NTSC, PAL
000	No color kill	Kill at < 0.5%
001	Kill at < 5%	Kill at < 1.5%
010	Kill at < 7%	Kill at < 2.5%
011	Kill at < 8%	Kill at < 4.0%
100*	Kill at < 9.5%	Kill at < 8.5%
101	Kill at < 15%	Kill at < 16.0%
110	Kill at < 32%	Kill at < 32.0%
111	Reserved for ADI internal use only. Do not select.	

*Default value.

SDP CHROMA TRANSIENT IMPROVEMENT (CTI)

The signal bandwidth allocated for chroma is typically much smaller than that of luminance. In the past, this was a valid way to fit a color video signal into a given overall bandwidth because the human eye is less sensitive to chrominance than to luminance.

The uneven bandwidth, however, may lead to some visual artifact when it comes to sharp color transitions. At the border of two bars of color, both components (luma and chroma) change at the same time (see Figure 18). Due to the higher bandwidth, the signal transition of the luma component is usually a lot sharper than that of the chroma component. The color edge is not sharp but blurred, in the worst case, over several pixels.

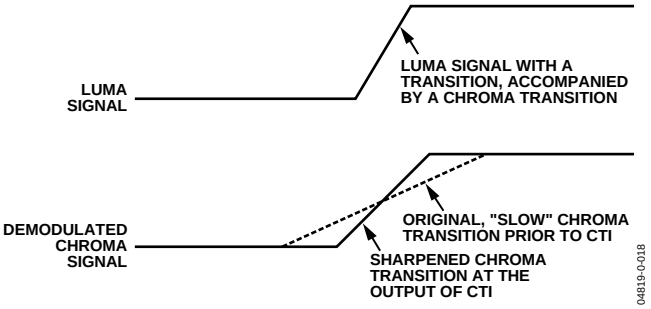

Figure 18. CTI Luma/Chroma Transition

The chroma transient improvement block examines the input video data. It detects transitions of chroma, and can be programmed to "steepen" the chroma edges in an attempt to artificially restore lost color bandwidth. The CTI block, however, only operates on edges above a certain threshold to ensure that noise is not emphasized. Care has also been taken to ensure that edge ringing and undesirable saturation or hue distortion are avoided.

Chroma transient improvements are needed primarily for signals that experienced severe chroma bandwidth limitations. For those types of signals, it is strongly recommended to enable the CTI block via CTI_EN.

CTI_EN Chroma Transient Improvement Enable (SDP), Address 0x4D, [0]

The CTI_EN bit enables the CTI function. If set to 0, the CTI block is inactive and the chroma transients are left untouched.

Table 76. CTI_EN Function

CTI_EN	Description
0*	Disable CTI.
1	Enable CTI block.

*Default value.

CTI_AB_EN Chroma Transient Improvement Alpha Blend Enable (SDP), Address 0x4D, [1]

The CTI_AB_EN bit enables an alpha-blend function within the CTI block. If set to 1, the alpha blender mixes the transient improved chroma with the original signal. The sharpness of the alpha blending can be configured via the CTI_AB[1:0] bits.

For the alpha blender to be active, the CTI block must be enabled via the CTI_EN bit.

Table 77. CTI_AB_EN

CTI_AB_EN	Description
0	Disable CTI alpha blender.
1*	Enable CTI alpha-blend mixing function.

*Default value.

CTI_AB[1:0] Chroma Transient Improvement Alpha Blend (SDP), Address 0x4D, [3:2]

The CTI_AB[1:0] controls the behavior of alpha-blend circuitry that mixes the sharpened chroma signal with the original one. It thereby controls the visual impact of CTI on the output data.

For CTI_AB[1:0] to become effective, the CTI block must be enabled via the CTI_EN bit, and the alpha blender must be switched on via CTI_AB_EN.

Sharp blending maximizes the effect of CTI on the picture, but may also increase the visual impact of small amplitude, high frequency chroma noise.

Table 78. CTI_AB Function

CTI_AB[1:0]	Description
00	Sharpest mixing between sharpened and original chroma signal.
01	Sharp mixing.
10	Smooth mixing.
11*	Smoothest alpha blend function.

*Default value.

CTI_C_TH[7:0] CTI Chroma Threshold (SDP), Address 0x4E, [7:0]

The CTI_C_TH[7:0] value is an unsigned, 8-bit number specifying how big the amplitude step in a chroma transition has to be in order to be steepened by the CTI block. Programming a small value into this register causes even smaller edges to be steepened by the CTI block. Making CTI_C_TH[7:0] a large value causes the block to improve large transitions only.

Table 79. CTI_C_TH Function

CTI_C_TH[7:0]	Description
0x08*	Threshold for chroma edges prior to CTI.

*Default value.

SDP DIGITAL NOISE REDUCTION (DNR)

Digital noise reduction is based on the assumption that high frequency signals with low amplitude are probably noise, and that their removal therefore improves picture quality.

DNR_EN Digital Noise Reduction Enable (SDP), Address 0x4D, [5]

The DNR_EN bit enables the DNR block or bypasses it.

Table 80. DNR_EN Function

DNR_EN	Description
0	Bypass DNR (disable).
1*	Enable digital noise reduction on the luma data.

DNR_TH[7:0] DNR Noise Threshold, Address 0x50, [7:0]

The DNR_TH[7:0] value is an unsigned 8-bit number used to determine the maximum edge that will be interpreted as noise and therefore blanked from the luma data. Programming a large value into DNR_TH[7:0] causes the DNR block to interpret even large transients as noise and remove them. The effect on the video data will therefore be more visible.

Programming a small value causes only small transients to be seen as noise and to be removed.

It should be noted that the recommended DNR_TH[7:0] setting for A/V inputs is 0x04, and the recommended DNR_TH[7:0] setting for tuner inputs is 0x0A.

Table 81. DNR_TH Function

DNR_TH[7:0]	Description
0x08*	Threshold for maximum luma edges to be interpreted as noise.

*Default value.

SDP COMB FILTERS

The comb filters of the ADV7183A have been greatly improved to automatically handle video of all types, standards, and levels of quality. Two user registers are available to customize comb filter operation.

Depending on whichever video standard has been detected (by autodetection) or selected (by manual programming), the NTSC or PAL configuration registers are used. In addition to the bits listed in this section, there are some further ADI internal controls; please contact ADI for more information.

NTSC Comb Filter Settings

Used for NTSC-M/J CVBS inputs.

NSFSEL[1:0] Split Filter Selection NTSC (SDP), Address 0x19, [3:2]

The NSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A narrow split filter selection gives better performance on diagonal lines, but leaves more dot crawl in the final output image. The opposite is true for selecting a wide bandwidth split filter.

Table 82.NSFSEL Function

NSFSEL[1:0]	Description
00*	Narrow
01	Medium
10	Medium
11	Wide

*Default value.

CTAPSN[1:0] Chroma Comb Taps NTSC (SDP), Address 0x38, [7:6]

Table 83. CTAPSN Function

CTAPSN[1:0]	Description
00	Do not use.
01	NTSC chroma comb adapts 3 lines (3 taps) to 2 lines (2 taps).
10*	NTSC chroma comb adapts 5 lines (5 taps) to 3 lines (3 taps).
11	NTSC chroma comb adapts 5 lines (5 taps) to 4 lines (4 taps).

*Default value.

CCMN[2:0] Chroma Comb Mode NTSC (SDP), Address 0x38, [5:3]

Table 84. CCMN Function

CCMN[2:0]	Description	
0xx*	Adaptive comb mode.	Adaptive 3-line chroma comb for CTAPSN = 01. Adaptive 4-line chroma comb for CTAPSN = 10. Adaptive 5-line chroma comb for CTAPSN = 11.
100	Disable chroma comb.	
101	Fixed chroma comb (top lines of line memory).	Fixed 2-line chroma comb for CTAPSN = 01. Fixed 3-line chroma comb for CTAPSN = 10. Fixed 4-line chroma comb for CTAPSN = 11.
110	Fixed chroma comb (all lines of line memory).	Fixed 3-line chroma comb for CTAPSN = 01. Fixed 4-line chroma comb for CTAPSN = 10. Fixed 5-line chroma comb for CTAPSN = 11.
111	Fixed chroma comb (bottom lines of line memory).	Fixed 2-line chroma comb for CTAPSN = 01. Fixed 3-line chroma comb for CTAPSN = 10. Fixed 4-line chroma comb for CTAPSN = 11.

*Default value.

YCMN[2:0] Luma Comb Mode NTSC (SDP), Address 0x38, [2:0]

Table 85.YCMN Function

YCMN[2:0]	Description	
0xx*	Adaptive comb mode.	Adaptive 3-line (3 taps) luma comb.
100	Disable luma comb.	Use low-pass/notch filter; see the Y Shaping Filter section.
101	Fixed luma comb (top lines of line memory).	Fixed 2-line (2 taps) luma comb.
110	Fixed luma comb (all lines of line memory).	Fixed 3-line (3 taps) luma comb.
111	Fixed luma comb (bottom lines of line memory).	Fixed 2-line (2 taps) luma comb.

*Default value.

PAL Comb Filter Settings

Used for PAL-B/G/H/I/D, PAL-M, PAL-Combinational N, PAL-60 and NTSC443 CVBS inputs.

PSFSEL[1:0] Split Filter Selection PAL (SDP), Address 0x19, [1:0]

The NSFSEL[1:0] control selects how much of the overall signal bandwidth is fed to the combs. A wide split filter selection eliminates dot crawl, but shows imperfections on diagonal lines. The opposite is true for selecting a narrow bandwidth split filter.

Table 86. PSFSEL Function

PSFSEL[1:0]	Description
00	Narrow
01*	Medium
10	Wide
11	Widest

*Default value.

CTAPSP[1:0] Chroma Comb Taps PAL (SDP), Address 0x39, [7:6]

Table 87. CTAPSP Function

CTAPSP[1:0]	Description
00	Do not use.
01	PAL chroma comb adapts 5 lines (3 taps) to 3 lines (2 taps); cancels cross luma only.
10	PAL chroma comb adapts 5 lines (5 taps) to 3 lines (3 taps); cancels cross luma and hue error less well.
11*	PAL chroma comb adapts 5 lines (5 taps) to 4 lines (4 taps); cancels cross luma and hue error well.

*Default value.

CCMP[2:0] Chroma Comb Mode PAL (SDP), Address 0x39, [5:3]

Table 88. CCMP Function

CCMP[2:0]	Description	
0xx*	Adaptive comb mode.	Adaptive 3-line chroma comb for CTAPSP = 01. Adaptive 4-line chroma comb for CTAPSP = 10. Adaptive 5-line chroma comb for CTAPSP = 11.
100	Disable chroma comb.	
101	Fixed chroma comb (top lines of line memory).	Fixed 2-line chroma comb for CTAPSP = 01. Fixed 3-line chroma comb for CTAPSP = 10. Fixed 4-line chroma comb for CTAPSP = 11.
110	Fixed chroma comb (all lines of line memory).	Fixed 3-line chroma comb for CTAPSP = 01. Fixed 4-line chroma comb for CTAPSP = 10. Fixed 5-line chroma comb for CTAPSP = 11.
111	Fixed chroma comb (bottom lines of line memory).	Fixed 2-line chroma comb for CTAPSP = 01. Fixed 3-line chroma comb for CTAPSP = 10. Fixed 4-line chroma comb for CTAPSP = 11.

*Default value.

YCMP[2:0] Luma Comb Mode PAL (SDP), Address 0x39, [2:0]

Table 89. YCMP Function

YCMP[2:0]	Description	
0xx*	Adaptive comb mode .	Adaptive 5 lines (3 taps) luma comb.
100	Disable luma comb.	Use low-pass/notch filter; see the Y Shaping Filter section.
101	Fixed luma comb (top lines of line memory).	Fixed 3 lines (2 taps) luma comb.
110	Fixed luma comb (all lines of line memory).	Fixed 5 lines (3 taps) luma comb.
111	Fixed luma comb (bottom lines of line memory).	Fixed 3 lines (2 taps) luma comb.

*Default value.

SDP AV CODE INSERTION AND CONTROLS

This section describes the I²C based controls that affect

- Insertion of AV codes into the data stream
- Data blanking during the vertical blank interval (VBI)
- The range of data values permitted in the output data stream
- The relative delay of luma versus chroma signals

Please note that some of the decoded VBI data is being inserted during the horizontal blanking interval. See the Gemstar Data Recovery section for more information.

BT656-4 ITU Standard BT-R.656-4 Enable (SDP), Address 0x04, [7]

The ITU has changed the position for toggling of the V bit within the SAV EAV codes for NTSC between revisions 3 and 4. The BT656-4 standard bit allows the user to select an output mode that is compliant with either the previous or the new standard. For further information, please review the standard at http://www.itu.int.

Please note that the standard change affects NTSC only and has no bearing on PAL.

Table 90. BT656-4 Function

BT656-4	Description
0*	BT656-3 Spec: V bit goes low at EAV of lines 10 and 273.
1	BT656-4 Spec: V bit goes low at EAV of lines 20 and 283.

*Default value.

SD_DUP_AV SDP Duplicate AV codes (SDP), Address 0x03, [0]

Depending on the output interface width, it may be necessary to duplicate the AV codes from the luma path into the chroma path.

In an 8-bit-wide output interface (Cb/Y/Cr/Y interleaved data), the AV codes are defined as FF/00/00/AV, with AV being the transmitted word that contains information about H/V/F.

In this output interface mode, the following assignment takes place: Cb = FF, Y = 00, Cr = 00, and Y = AV.

In a 16-bit output interface where Y and Cr/Cb are delivered via separate data buses, the AV code is over the whole 16 bits. The SD_DUP_AV bit allows the user to double up the AV codes, so the full sequence can be found on the Y bus as well as (= duplicated) the Cr/Cb bus. See Figure 19.

Table 91. SD_DUP_AV Function

SD_DUP_AV	Description
0	AV codes in single fashion (to suit 8-bit interleaved data output).
1	AV codes duplicated (for 16-bit interfaces).

*Default value.

VBI_EN Vertical Blanking Interval Data Enable (SDP), Address 0x03, [7]

The VBI enable bit allows data such as intercast and closed caption data to be passed through the luma channel of the SDP decoder with only a minimal amount of filtering. All data for lines 1 to 21 is passed through and available at the output port. The ADV7183A does not blank the luma data, and automatically switches all filters along the luma data path into their widest bandwidth. For active video, the filter settings for YSH and YPK are restored.

Refer to the BL_C_VBI Blank Chroma during VBI section for information on the chroma path.

Table 92.

VBI_EN	Description
0*	All video lines are filtered/scaled.
1	Only active video region is filtered/scaled.

*Default value.

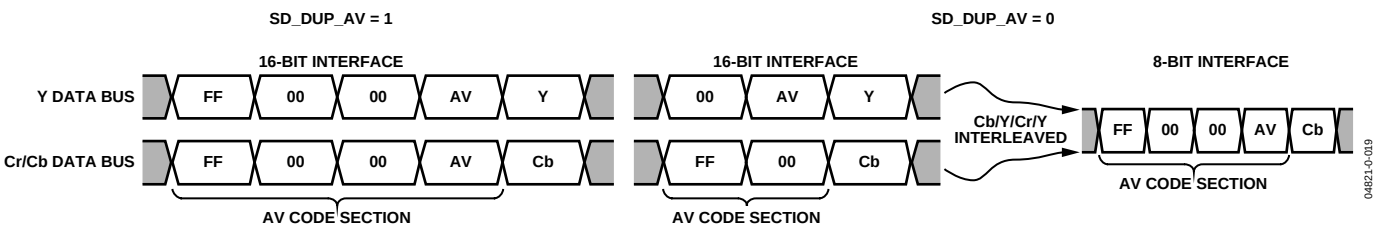

Figure 19. SDP AV Code Duplication Control

BL_C_VBI Blank Chroma during VBI (SDP), Address 0x04, [2]

Setting BL_C_VBI high, the Cr and Cb values of all VBI lines get blanked. This is done so any data that may come during VBI is not decoded as color and output through Cr and Cb. As a result, it should be possible to send VBI lines into the decoder, then output them through an encoder again, undistorted. Without this blanking, any wrongly decoded color gets encoded by the video encoder; therefore, the VBI lines are distorted.

Table 93. BL_C_VBI Function

BL_C_VBI	Description
0	Decode and output color during VBI.
1*	Blank Cr and Cb values during VBI (no color, 0x80).

*Default value.

RANGE Range Selection (SDP), Address 0x04, [0]

AV codes (as per ITU-R BT-656, formerly known as CCIR-656) consist of a fixed header made up of 0xFF and 0x00 values. These two values are reserved and therefore are not to be used for active video. Additionally, the ITU also specifies that the nominal range for video should be restricted to values between 16 and 235 for luma and 16 to 240 for chroma.

The RANGE bit allows the user to limit the range of values output by the ADV7183A to the recommended value range. In any case, it is ensured that the reserved values of 255_d (0xFF) and 00_d (0x00) are not presented on the output pins unless they are part of an AV code header.

Table 94. RANGE Function

RANGE	Description	
0	16 ≤ Y ≤ 235	16 ≤ C/P ≤ 240
1*	1 ≤ Y ≤ 254	1 ≤ C/P ≤ 254

*Default value.

AUTO_PDC_EN Automatic Programmed Delay Control (SDP), Address 0x27, [6]

Enabling the AUTO_PDC_EN function activates a function within the ADV7183A that automatically programs the LTA[1:0] and CTA[2:0] to have the chroma and luma data match delays for all modes of operation. If set, manual registers LTA[1:0] and CTA[2:0] are not used by the SDP. If the automatic mode is disabled (via setting the AUTO_PDC_EN bit to 0), the values programmed into LTA[1:0] and CTA[2:0] registers take effect.

Table 95. AUTO_PDC_EN Function

AUTO_PDC_EN	Description
0	Use LTA[1:0] and CTA[2:0] values for delaying luma and chroma samples. Refer to the LTA[1:0] Luma Timing Adjust (SDP), Address 0x27, [1:0] and CTA[2:0] Chroma Timing Adjust (SDP), Address 0x27, [5:3] sections.
1*	The ADV7183A automatically determines the LTA and CTA values to have luma and chroma aligned at the output.

*Default value.

LTA[1:0] Luma Timing Adjust (SDP), Address 0x27, [1:0]

The Luma Timing Adjust register allows the user to specify a timing difference between chroma and luma samples.

Please note the following:

- There is a certain functionality overlap with the CTA[2:0] register.
- For manual programming, use the following defaults:
  - CVBS input LTA[1:0] = 00.
  - YC input LTA[1:0] = 01.
  - YPrPb input LTA[1:0] =01.

Table 96. LTA Function

LTA[1:0]	Description
00*	No delay.
01	Luma 1 clk (37 ns) delayed.
10	Luma 2clk (74 ns) early.
11	Luma 1 clk (37 ns) early.

*Default value.

CTA[2:0] Chroma Timing Adjust (SDP), Address 0x27, [5:3]

The Chroma Timing Adjust register allows the user to specify a timing difference between chroma and luma samples. This may be used to compensate for external filter group delay differences in the luma versus chroma path, and to allow for a different number of pipeline delays while processing the video downstream. Please review this functionality together with the LTA[1:0] register.

Note that the chroma can only be delayed/advanced in chroma pixel steps. One chroma pixel step is equal to two luma pixels. The programmable delay occurs after demodulation, where one can no longer delay by luma pixel steps.

For manual programming use the following defaults:

- CVBS input CTA[2:0] = 011.
- YC input CTA[2:0] = 101.
- YPrPb input CTA[2:0] =110.

Table 97. CTA Function

CTA[2:0]	Description
000	Not used.
001	Chroma + 2 chroma pixel (early).
010	Chroma + 1 chroma pixel (early).
011*	No delay.
100	Chroma – 1 chroma pixel (late).
101	Chroma – 2 chroma pixel (late).
110	Chroma – 3 chroma pixel (late).
111	Not used.

*Default value.

SDP SYNCHRONIZATION OUTPUT SIGNALS

HS Configuration

The following controls allow the user to configure the behavior of the HS output pin only:

- Beginning of HS signal via HSB[10:0]
- End of HS signal via HSE[10:0]
- Polarity of HS using PHS

HSB[10:0] HS Begin, Address 0x34, [6:4], Address 0x35, [7:0]

The HS Begin and HS End registers allow the user to freely position the HS output (pin) within the video line. The values in HSB[10:0] and HSE[10:0] are measured in pixel units from the falling edge of HS. Using both values, the user can program both the position and length of the HS output signal.

The position of this edge is controlled by placing a binary number into HSB[10:0]. The number applied offsets the edge with respect to an internal counter that is reset to 0 immediately after EAV code FF,00,00,XY (see Figure 20). HSB is set to 00000000010b, which is 2 LLC1 clock cycles from count[0].

Table 98. HSB Function

HSB[10:0]	Description
0x002	The HS pulse starts after the HSB[10:0] pixel after the falling edge of HS.

*Default value.

HSE[10:0] HS End, Address 0x34, [2:0], Address 0x36, [7:0]

The HS Begin and HS End registers allow the user to freely position the HS output (pin) within the video line. The values in HSB[10:0] and HSE[10:0] are measured in pixel units from the falling edge of HS. Using both values, the user can program both the position and length of the HS output signal.

The position of this edge is controlled by placing a binary number into HSE[10:0]. The number applied offsets the edge with respect to an internal counter that is reset to 0 immediately after EAV code FF,00,00,XY (see Figure 20). HSE is set to 00000000000b, which is 0 LLC1 clock cycles from count[0].

Table 99. HSE Function

HSE[9:0]	Description
000*	HS pulse ends after HSE[10:0] pixel after falling edge of HS.

*Default value.

Example

1. To shift the HS towards active video by 20 LLC1s, add 20 LLC1s to both HSB and HSE. i.e., HSB[10:0] = [00000010110], HSE[10:0] = [00000010100]
2. To shift the HS away from active video by 20 LLC1s, add 1696[11] LLC1s to both HSB and HSE (for NTSC).i.e., HSB[10:0] = [11000000100], HSE[10:0] = [11000000110]

To move 20 LLC1s away from active video is equal to subtracting 20 from 1716 and adding the result in binary to both HSB[10:0] and HSE[10:0].

PHS Polarity HS (SDP), Address 0x37, [7]

The polarity of the HS pin as it comes from the SDP block can be inverted using the PHS bit.

Table 100. PHS Function

PHS	Description
0*	HS active high.
1	HS active low.

[11] 1696 is derived from the NTSC total number of pixels = 1716

Table 101. HS Timing Parameters (see Figure 20)

	Characteristic				
Standard	**HS Begin Adjust (HSB[10:0])[1]**	**HS End Adjust (HSE[10:0])[1]**	**HS to Active Video (LLC1 Clock Cycles) (C in Figure 20)[1]**	**Active Video Samples/Line (D in Figure 20)**	**Total LLC1 Clock Cycles (E in Figure 20)**
NTSC	00000000010b	00000000000b	272	720Y + 720C = 1440	1716
NTSC Square Pixel	00000000010b	00000000000b	276	640Y + 640C = 1280	1560
PAL	00000000010b	00000000000b	284	720Y + 720C = 1440	1728

[1]Default.

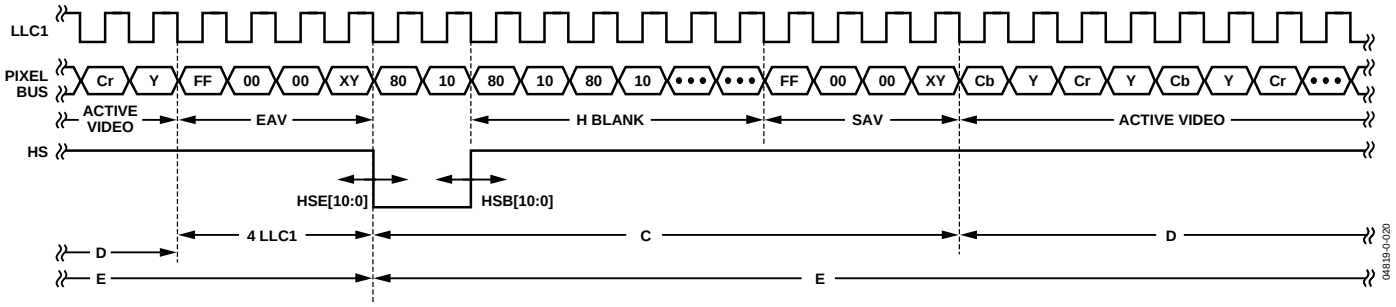

Figure 20. HS Timing (SDP)

VS and FIELD Configuration

The following controls allow the user to configure the behavior of the VS and FIELD output pins, as well as the generation of embedded AV codes:

- ADV encoder compatible signals via NEWAVMODE
- PVS, PF
- HVSTIM
- VSBHO, VSBHE
- VSEHO, VSEHE
- For NTSC control:
  - NVBEGDELO, NVBEGDELE, NVBEGSIGN, NVBEG[4:0]
  - NVENDDELO, NVENDDELE, NVENDSIGN, NVEND[4:0]
  - NFTOGDELO, NFTOGDELE, NFTOGSIGN, NFTOG[4:0]
- For PAL control:
  - PVBEGDELO, PVBEGDELE, PVBEGSIGN, PVBEG[4:0]
  - PVENDDELO, PVENDDELE, PVENDSIGN, PVEND[4:0]
  - PFTOGDELO, PFTOGDELE, PFTOGSIGN, PFTOG[4:0]

NEWAVMODE New AV Mode, Address 0x31, [4]

Table 102. NEWAVMODE Function

NEWAVMODE	Description
0	EAV/SAV codes generated to suit ADI encoders. No adjustments possible.
1*	Enable Manual Position of VSYNC, Field, and AV codes using 0x34 to 0x37 and 0xE5 to 0xEA. Default register settings are CCIR656 compliant; see Figure 21 for NTSC and Figure 26 for PAL. For recommended manual user settings, see Table 110 and Figure 22 for NTSC; see Table 123 and Figure 27 for PAL.

*Default value.

HVSTIM Horizontal VS Timing (SDP), Address 0x31, [3]

The HVSTIM bit allows the user to select where the VS signal is being asserted within a line of video. Some interface circuitry may require VS to go low while HS is low.

Table 103. HVSTIM Function

HVSTIM	Description
0*	Start of line relative to HSE.
1	Start of line relative to HSB.

*Default value.

VSBHO VS Begin Horizontal Position Odd (SDP), Address 0x32, [7]

The VSBHO and VSBHE bits select the position within a line at which the VS pin (not the bit in the AV code) goes active. Some follow-on chips require the VS pin to only change state when HS is high/low.

Table 104. VSBHO Function

VSBHO	Description
0*	VS pin goes high at the middle of a line of video (odd field).
1	VS pin changes state at the start of a line (odd field).

*Default value.

VSBHE VS Begin Horizontal Position Even (SDP), Address 0x32, [6]

The VSBHO and VSBHE bits select the position within a line at which the VS pin (not the bit in the AV code) goes active. Some follow-on chips require the VS pin to only change state when HS is high/low.

Table 105. VSBHE Function

VSBHE	Description
0*	VS pin goes high at the middle of a line of video (even field).
1	VS pin changes state at the start of a line (even field).

*Default value.

VSEHO VS End Horizontal Position Odd (SDP), Address 0x33, [7]

The VSEHO and VSEHE bits select the position within a line at which the VS pin (not the bit in the AV code) goes active. Some follow-on chips require the VS pin to only change state when HS is high/low.

Table 106. VSEHO Function

VSEHO	Description
0*	VS pin goes low (inactive) at the middle of a line of video (odd field).
1	VS pin changes state at the start of a line (odd field).

*Default value.

VSEHE VS End Horizontal Position Even (SDP), Address 0x33, [6]

The VSEHO and VSEHE bits select the position within a line at which the VS pin (not the bit in the AV code) goes active. Some follow-on chips require the VS pin to only change state when HS is high/low.

Table 107. VSEHE Function

VSEHE	Description
0*	VS pin goes low (inactive) at the middle of a line of video (even field).
1	VS pin changes state at the start of a line (even field).

*Default value.

PVS Polarity VS (SDP), Address 0x37, [5]

The polarity of the VS pin as it comes from the SDP block can be inverted using the PVS bit.

Table 108. PVS Function

PVS	Description
0*	VS active high.
1	VS active low.

*Default value.

PF Polarity FIELD (SDP), Address 0x37, [3]

The polarity of the FIELD pin as it comes from the SDP block can be inverted using the PF bit.

Table 109. PF Function

PF	Description
0*	FIELD active high.
1	FIELD active low.

*Default value.

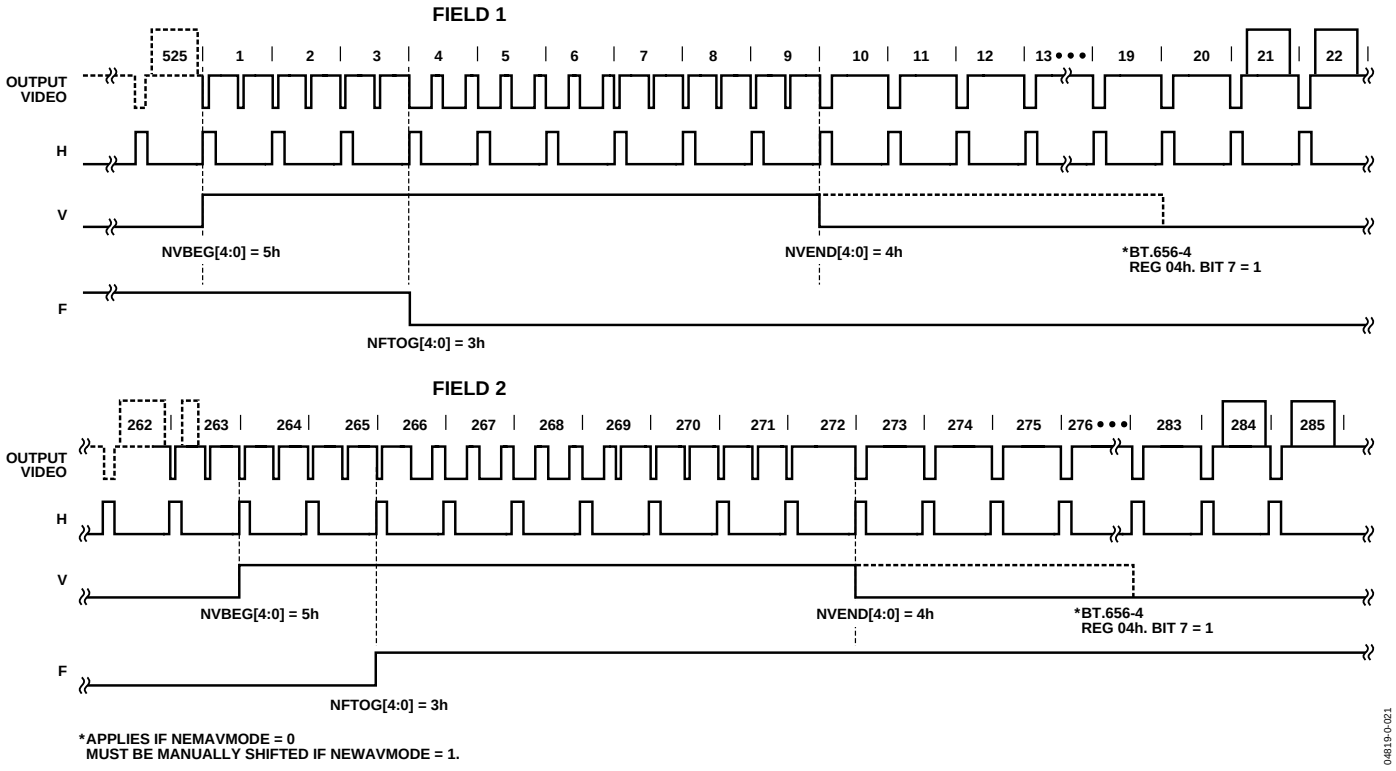

Figure 21. NTSC Default (BT.656). The polarity of H, V, and F is embedded in the data.

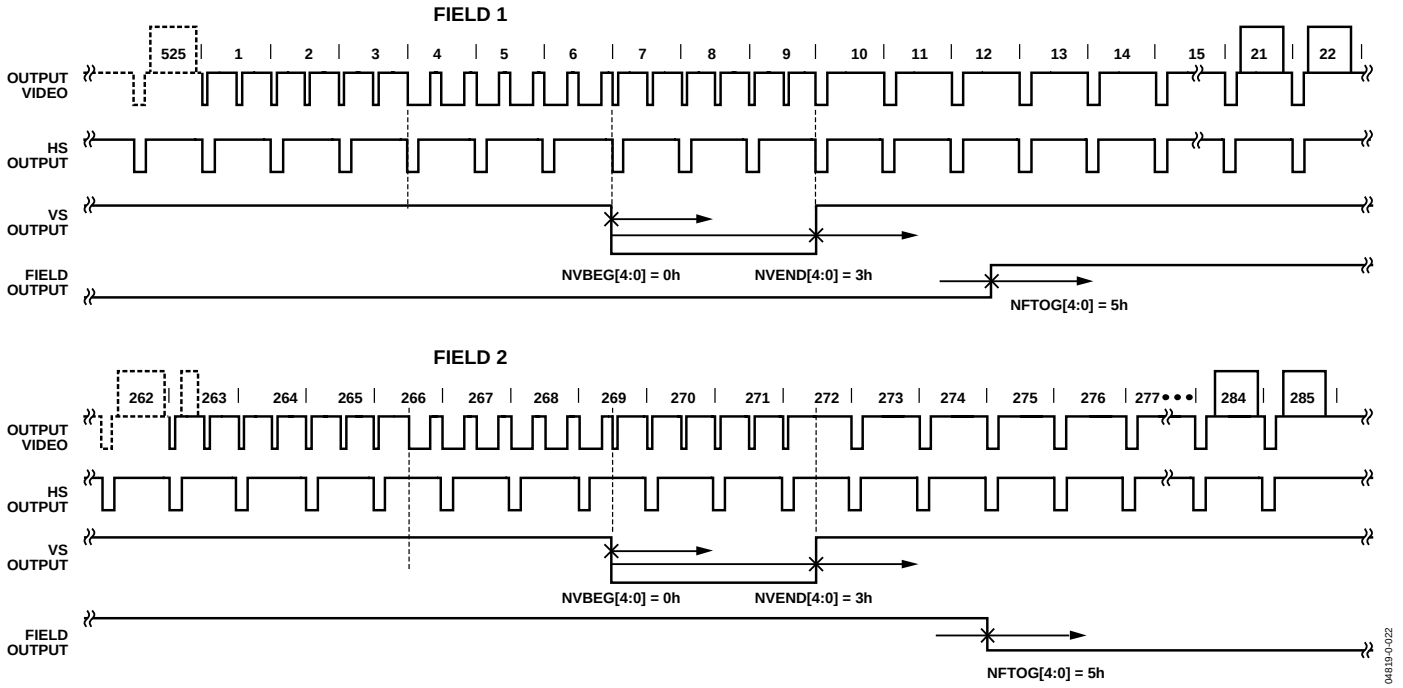

Figure 22. NTSC Typical VSync/Field Positions Using Register Writes in Table 110

Table 110. Recommended User Settings for NTSC (See Figure 22)

Register	Register Name	Write
0x31	VSync Field Control 1	0x12
0x32	VSync Field Control 2	0x81
0x33	VSync Field Control 3	0x84
0x37	Polarity	0x29
0xE5	NTSV_V_Bit_Beg	0x0
0xE6	NTSC_V_Bit_End	0x3
0xE7	NTSC_F_Bit_Tog	0x85

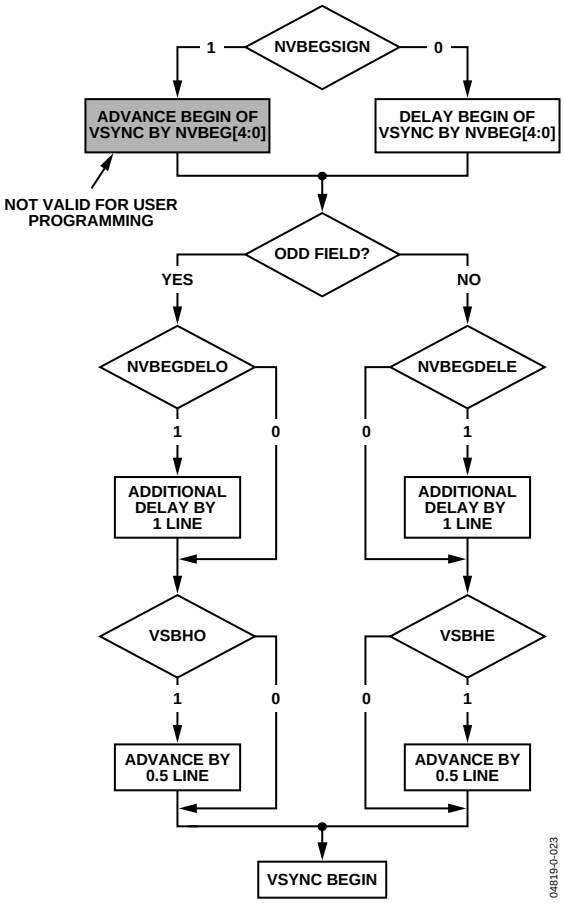

Figure 23. NTSC VSync Begin

NVBEGDELO NTSC VSync Begin Delay on Odd Field, Address 0xE5, [7]

Table 111. NVBEGDELO Function

NVBEGDELO	Description
0*	No Delay.
1	Delay VSync going high on an odd field by a line relative to NVBEG.

*Default value.

NVBEGDELE NTSC Vsync Begin Delay on Even Field, Address 0xE5, [6]

Table 112. NVBEGDELE Function

NVBEGDELE	Description
0*	No Delay.
1	Delay VSync going high on an even field by a line relative to NVBEG.

*Default value.

NVBEGSIGN NTSC VSync Begin Sign, Address 0xE5, [5]

Table 113. NVBEGSIGN Function

NVBEGSIGN	Description
0	Delay start of VSync. Set for user manual programming.
1*	Advance start of VSync. Not recommended for user programming.

*Default value.

NVBEG[4:0] NTSC VSync Begin, Address 0xE5, [4:0]

Table 114. NVBEG Function

NVBEG	Description
00101*	NTSC VSync begin position.

*Default value.

Note: For all NTSC/PAL VSync timing controls, both the V bit in the AV code and the VSync on the VS pin are modified.

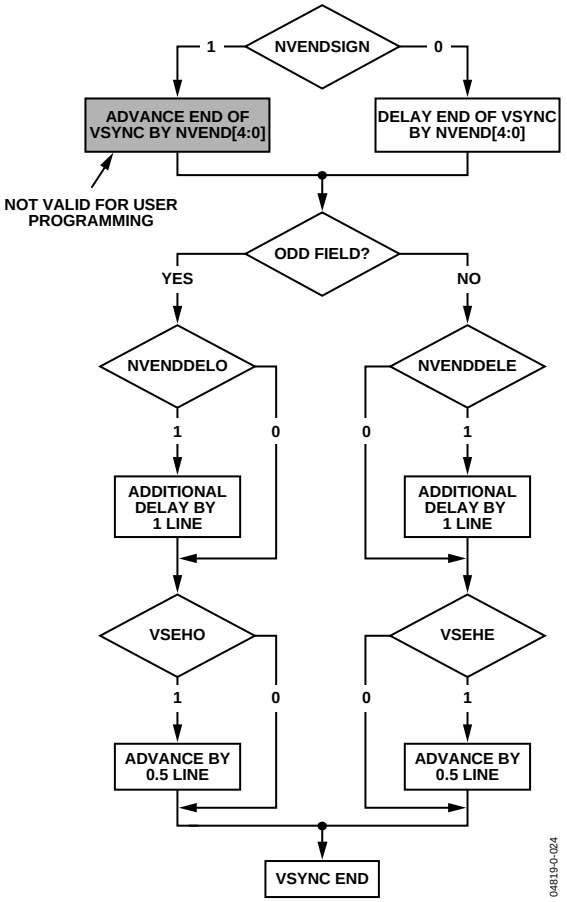

Figure 24. NTSC VSync End

NVENDDELO NTSC VSync End Delay on Odd Field, Address 0xE6, [7]

Table 115. NVENDDELO Function

NVENDDELO	Description
0*	No Delay.
1	Delay VSync going low on an odd field by a line relative to NVEND.

*Default value.

NVENDDELE NTSC VSync End Delay on Even Field, Address 0xE6, [6]

Table 116. NVENDDELE Function

NVENDDELE	Description
0*	No Delay.
1	Delay VSync going low on an even field by a line relative to NVEND

*Default value.

NVENDSIGN NTSC VSync End Sign, Address 0xE6, [5]

Table 117. NVENDSIGN Function

NVENDSIGN	Description
0*	Delay start of VSync. Set for user manual programming.
1	Advance start of VSync. Not recommended for user programming.

*Default value.

NVEND NTSC[4:0] VSync End, Address 0xE6, [4:0]

Table 118. NVEND Function

NVEND	Description
00100*	NTSC VSync end position.

*Default value.

Note: For all NTSC/PAL VSync timing controls, both the V bit in the AV code and the VSync on the VS pin are modified.

NFTOGDELO NTSC Field Toggle Delay on Odd Field, Address 0xE7, [7]

Table 119. NFTOGDELO Function

NFTOGDELO	Description
0*	No delay.
1	Delay Field toggle/transition on an odd field by a line relative to NFTOG.

*Default value.

NFTOGDELE NTSC Field Toggle Delay on Even Field, Address 0xE7, [6]

Table 120. NFTOGDELE Function

NFTOGDELE	Description
0	No Delay
1*	Delay Field toggle/transition on an even field by a line relative to NFTOG.

*Default value.

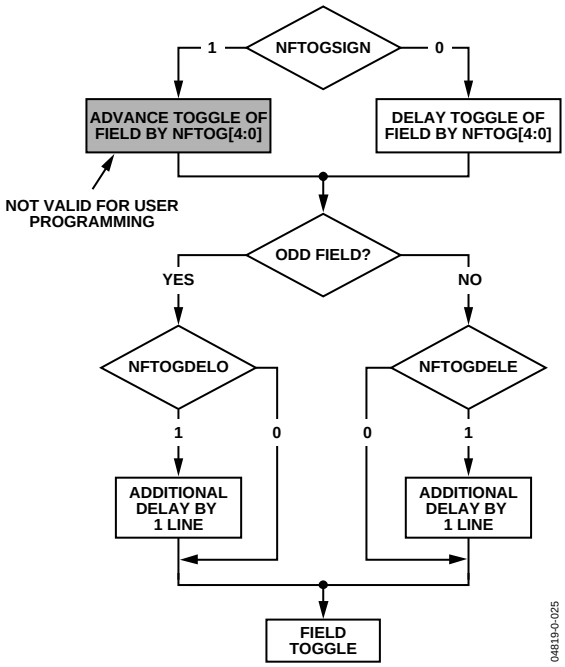

Figure 25. NTSC FIELD Toggle

NFTOGSIGN NTSC Field Toggle Sign, Address 0xE7, [5]

Table 121. NFTOGSIGN Function

NFTOGSIGN	Description
0	Delay field transition. Set for user manual programming.
1*	Advance field transition. Not recommended for user programming.

*Default value.

NFTOG[4:0] NTSC Field Toggle, Address 0xE7, [4:0]

Table 122. NFTOG Function

NFTOG	Description
00011*	NTSC Field toggle position.

*Default value.

Note: For all NTSC/PAL Field timing controls, both the F bit in the AV code and the Field signal on the FIELD/DE pin are modified.

Table 123. Recommended User Settings for PAL (see Figure 27)

Register	Register Name	Write
0x31	VSync Field Control 1	0x12
0x32	VSync Field Control 2	0x81
0x33	VSync Field Control 3	0x84
0x37	Polarity	0x29
0xE8	PAL_V_Bit_Beg	0x1
0xE9	PAL_V_Bit_End	0x4
0xEA	PAL_F_Bit_Tog	0x6

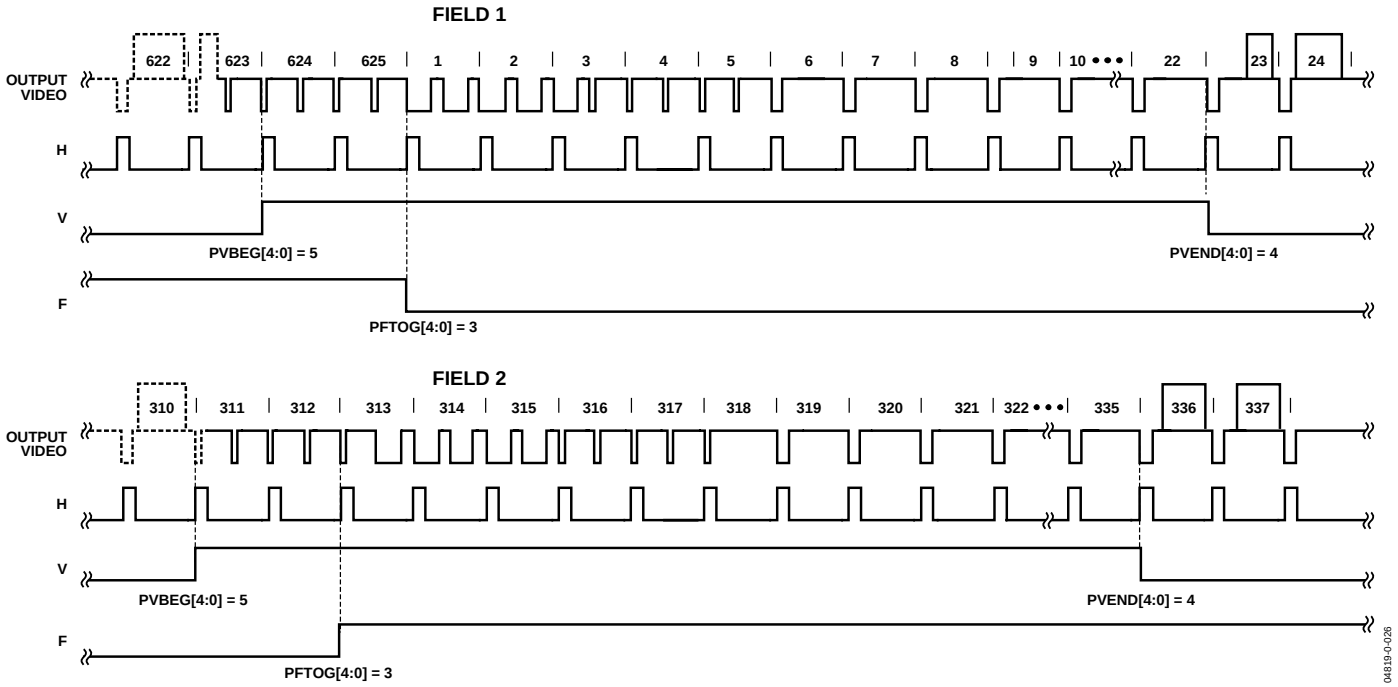

Figure 26. PAL Default (BT.656). The polarity of H, V, and F is embedded in the data.

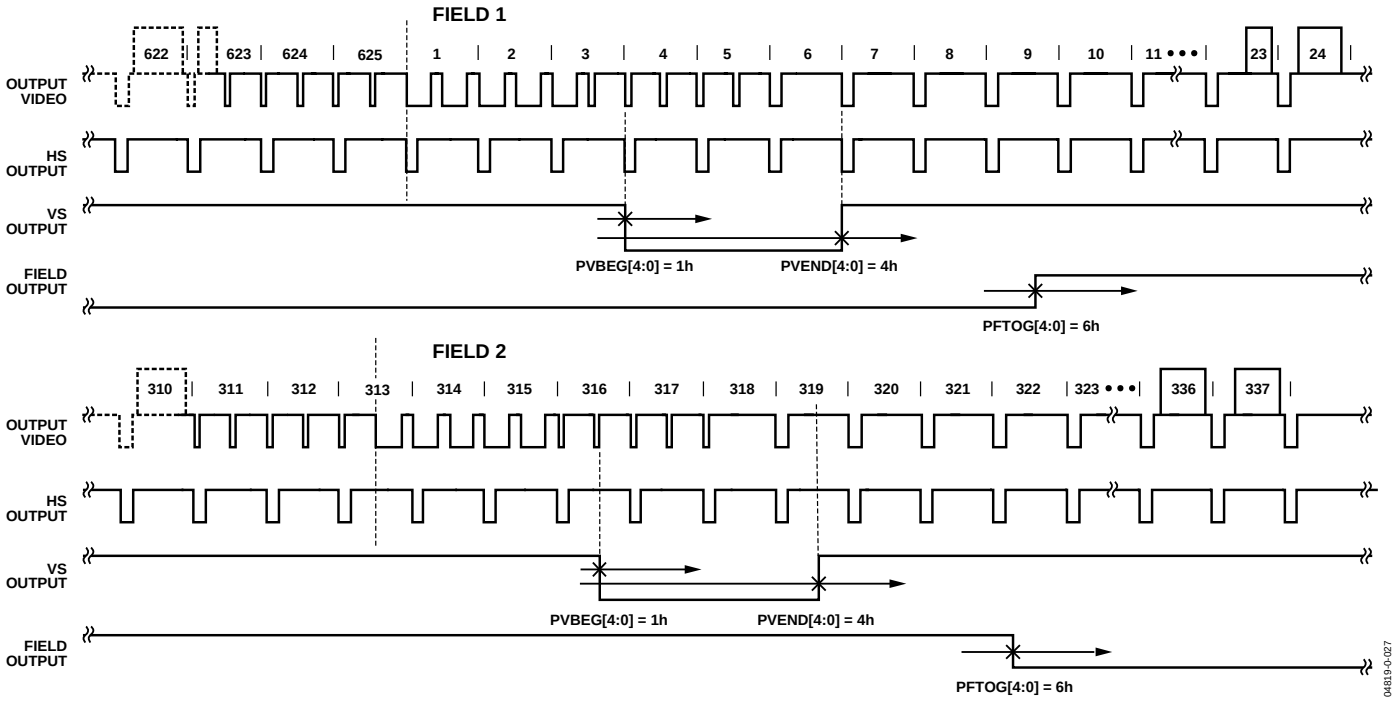

Figure 27. PAL Typical VSync/Field Positions Using Register Writes in Table 123

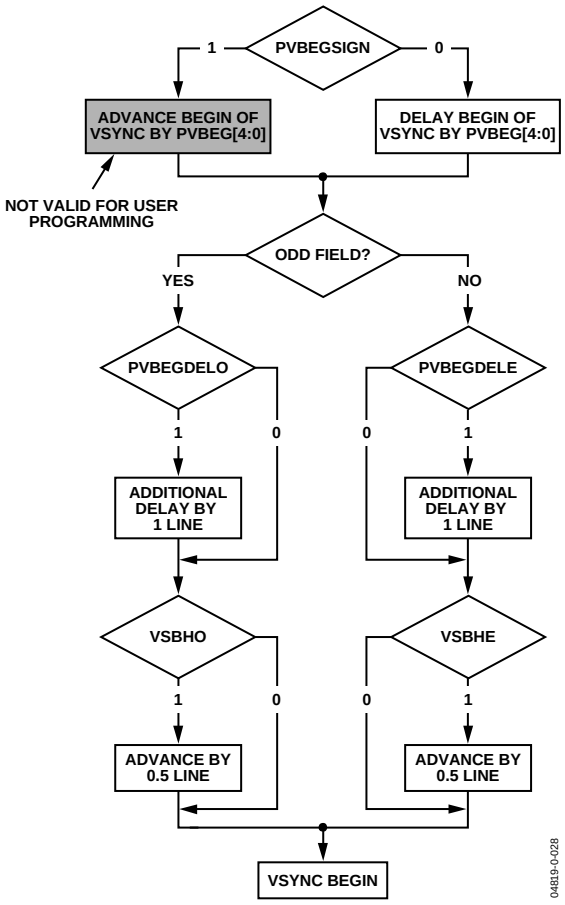

Figure 28. PAL VSync Begin

PVBEGDELO PAL VSync Begin Delay on Odd Field, Address 0xE8, [7]

Table 124. PVBEGDELO Function

PVBEGDELO	Description
0*	No delay.
1	Delay VSync going high on an odd field by a line relative to PVBEG.

*Default value.

PVBEGDELE PAL VSync Begin Delay on Even Field, Address 0xE8, [6]

Table 125. PVBEGDELE Function

PVBEGDELE	Description
0	No delay.
1*	Delay VSync going high on an even field by a line relative to PVBEG.

*Default value.

PVBEGSIGN PAL VSync Begin Sign, Address 0xE8, [5]

Table 126. PVBEGSIGN Function

PVBEGSIGN	Description
0	Delay begin of VSync. Set for user manual programming.
1*	Advance begin of VSync. Not recommended for user programming.

*Default value.

PVBEG[4:0] PAL VSync Begin, Address 0xE8, [4:0]

Table 127. PVBEG Function

PVBEG	Description
00101*	PAL VSync begin position.

*Default value.

For all NTSC/PAL VSync timing controls, both the V bit in the AV code and the VSync on the VS pin are modified.

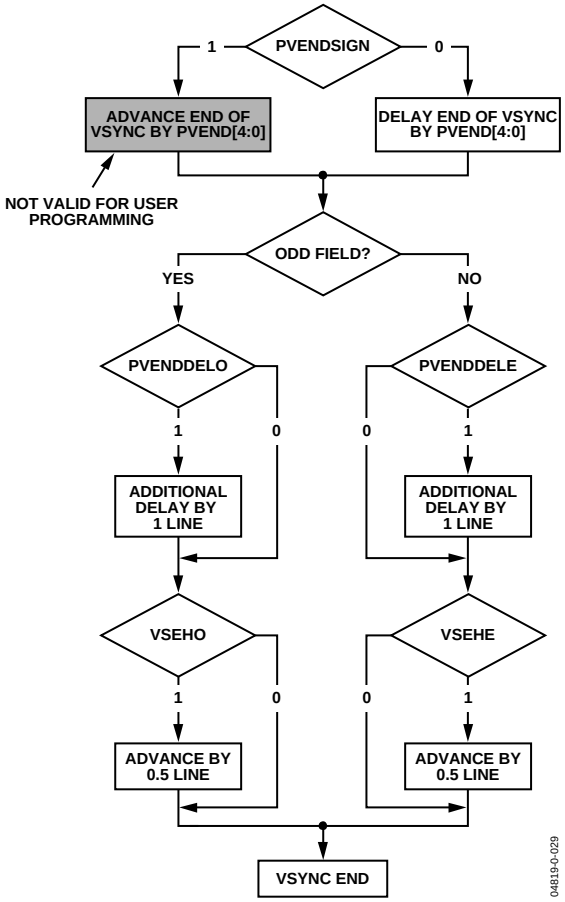

Figure 29. PAL VSync End

PVENDDELO PAL VSync End Delay on Odd Field, Address 0xE9,[7]

Table 128. PVENDDELO Function

PVENDDELO	Description
0*	No delay.
1	Delay VSync going low on an odd field by a line relative to PVEND.

*Default value.

PVENDDELE PAL VSync End Delay on Even Field, Address 0xE9,[6]

Table 129. PVENDDELE Function

PVENDDELE	Description
0*	No delay.
1	Delay VSync going low on an even field by a line relative to PVEND.

*Default value.

PVENDSIGN PAL VSync End Sign, Address 0xE9, [5]

Table 130. PVENDSIGN Function

PVENDSIGN	Description
0*	Delay end of VSync. Set for user manual programming.
1	Advance end of VSync. Not recommended for user programming.

*Default value.

PVEND[4:0] PAL Vsync End, Address 0xE9,[4:0]

Table 131. PVEND Function

PVEND	Description
10100*	PAL VSync end position.

*Default value.

Note: For all NTSC/PAL VSync timing controls, both the V bit in the AV code and the VSync on the VS pin are modified.

PFTOGDELO PAL Field Toggle Delay on Odd Field, Address 0xEA, [7]

Table 132. PFTOGDELO Function

PFTOGDELO	Description
0*	No delay.
1	Delay F toggle/transition on an odd field by a line relative to PFTOG.

*Default value.

PFTOGDELE PAL Field Toggle Delay on Even Field, Address 0xEA [6]

Table 133. PFTOGDELE Function

PFTOGDELE	Description
0	No delay.
1*	Delay F toggle/transition on an even field by a line relative to PFTOG.

*Default value.

PFTOGSIGN PAL Field Toggle Sign, Address 0xEA, [5]

Table 134. PFTOGSIGN Function

PFTOGSIGN	Description
0	Delay Field transition. Set for user manual programming.
1*	Advance Field transition. Not recommended for user programming.

*Default value.

PFTOG PAL Field Toggle, Address 0xEA [4:0]

Table 135. PFTOG Function

PFTOG	Description
00011*	PAL Field toggle position.

*Default value.

For all NTSC/PAL Field timing controls, the F bit in the AV code and the Field signal on the FIELD/DE pin are modified.

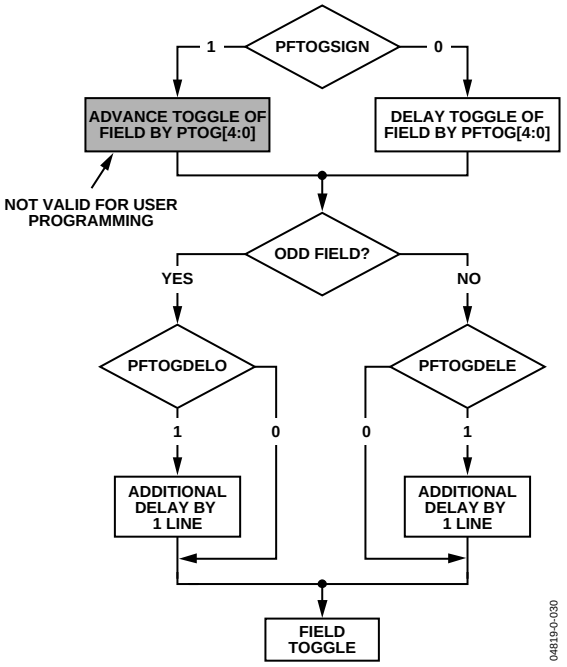

Figure 30. PAL F Toggle

SDP SYNC PROCESSING

The ADV7183A has two additional sync processing blocks that postprocess the raw synchronization information extracted from the digitized input video. If desired, the blocks can be disabled via the following two I²C bits.

ENHSPLL Enable HSync Processor (SDP), Address 0x01, [6]

The HSYNC processor is designed to filter incoming HSyncs that have been corrupted by noise, providing improved performance for video signals with stable time bases but poor SNR.

For CVBS PAL/NTSC, YC PAL/NTSC enable the HSync processor. For SECAM disable the HSync Processor. For YPrPb through SDP, disable HSYNC Processor.

Table 136. ENHSPLL Function

ENHSPLL	Description
0	Disable the HSync processor.
1*	Enable the HSync processor.

*Default value.

ENVSPROC Enable VSync Processor (SDP), Address 0x01, [3]

This block provides extra filtering of the detected VSyncs to give improved vertical lock.

Table 137. ENVSPROC Function

ENVSPROC	Description
0	Disable VSync processor.
1*	Enable VSync processor.

*Default value.

SDP VBI DATA DECODE

The following low data rate VBI signals can be decoded by the ADV7183A:

- Wide screen signaling (WSS)
- Copy generation management systems (CGMS)
- Closed captioning (CCAP)
- EDTV
- Gemstar 1× and 2× compatible data recovery

The presence of any of the above signals is detected and, if applicable, a parity check is performed. The result of this testing is contained in a confidence bit in the VBI Info[7:0] register. Users are encouraged to first examine the VBI Info register before reading the corresponding data registers. All VBI data decode bits are read-only.

All VBI data registers are double-buffered with the field signals. This means that data is extracted from the video lines and appears in the appropriate I²C registers with the next field transition. They are then static until the next field.

The user should start an I²C read sequence with VS by first examining the VBI Info register. Then, depending on what data was detected, the appropriate data registers should be read.

Note that the data registers are filled with decoded VBI data even if their corresponding detection bits are low; it is likely that bits within the decoded data stream are wrong.

Notes

- The closed captioning data (CCAP) is available in the I²C registers, and is also inserted into the output video data stream during horizontal blanking.
- The Gemstar compatible data is not available in the I²C registers, and is inserted into the data stream only during horizontal blanking.

WSSD Wide Screen Signaling Detected (SDP), Address 0x90, [0]

Logic 1 for this bit indicates that the data in the WSS1 and WSS2 registers is valid.

The WSSD bit goes high if the rising edge of the start bit is detected within a time window, and if the polarity of the parity bit matches the data transmitted.

Table 138. WSSD Function

WSSD	Description
0	No WSS detected. Confidence in decoded data is low.
1	WSS detected. Confidence in decoded data is high.

CCAPD Closed Caption Detected (SDP), Address 0x90, [1]

A Logic 1 for this bit indicates that the data in the CCAP1 and CCAP2 registers is valid.

The CCAPD bit goes high if the rising edge of the start bit is detected within a time window, and if the polarity of the parity bit matches the data transmitted.

Table 139. CCAPD Function

CCAPD	Description
0	No CCAP signals detected. Confidence in decoded data is low.
1	CCAP sequence detected. Confidence in decoded data is high.

EDTVD EDTV Sequence Detected (SDP), Address 0x90, [2]

A Logic 1 for this bit indicates that the data in the EDTV1, 2, 3 registers is valid.

The EDTVD bit goes high if the rising edge of the start bit is detected within a time window, and if the polarity of the parity bit matches the data transmitted.

Table 140. EDTVD Function

EDTVD	Description
0	No EDTV sequence detected. Confidence in decoded data is low.
1	EDTV sequence detected. Confidence in decoded data is high.

CGMSD CGMS-A Sequence Detected (SDP), Address 0x90, [3]

Logic 1 for this bit indicates that the data in the CGMS1, 2, 3 registers is valid. The CGMSD bit goes high if a valid CRC checksum has been calculated from a received CGMS packet.

Table 141. CGMSD Function

CGMSD	Description
0	No CGMS transmission detected. Confidence low.
1	CGMS sequence decoded. Confidence high.

CRC_ENABLE CRC CGMS-A Sequence (SDP), Address 0xB2, [2]

For certain video sources, the CRC data bits may have an invalid format. In such circumstances, the CRC checksum validation procedure can be disabled. The CGMSD bit goes high if the rising edge of the start bit is detected within a time window.

Table 142. CRC_ENABLE Function

CRC_ENABLE	Description
0	No CRC check performed. The CGMSD bit goes high if the rising edge of the start bit is detected within a time window.
1*	Use CRC checksum to validate the CGMS-A sequence. The CGMSD bit goes high for a valid checksum. ADI recommended setting.

*Default value.

Wide Screen Signaling Data

WSS1[7:0] (SDP), Address 0x91, [7:0], WSS2[7:0] (SDP), Address 0x92, [7:0]

Figure 31 shows the bit correspondence between the analog video waveform and the WSS1/WSS2 registers. Please note that WSS2[7:6] are undetermined and should be masked out by software.

EDTV Data Registers

EDTV1[7:0] (SDP), Address 0x93, [7:0], EDTV2[7:0] (SDP), Address 0x94, [7:0], EDTV3[7:0] (SDP), Address 0x95, [7:0]

Figure 32 shows the bit correspondence between the analog video waveform and the EDTV1/EDTV2/EDTV3 registers.

Note that EDTV3[7:6] are undetermined and should be masked out by software. EDTV3[5] is reserved for future use and, for now, will contain 0. The three LSBs of the EDTV waveform are currently not supported.

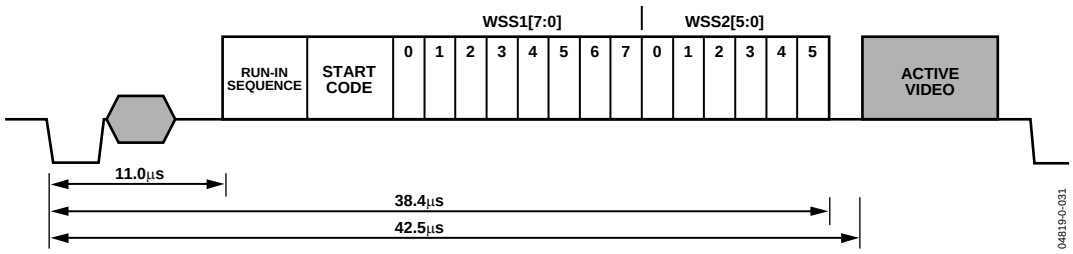

Figure 31. SDP WSS Data Extraction

Table 143. SDP WSS Access Information

Signal Name	Block	Register Location	Address		Register Default Value
WSS1 [7:0]	SDP	WSS 1 [7:0]	145d	91h	Readback Only
WSS2 [5:0]	SDP	WSS 2 [5:0]	146d	92h	Readback Only

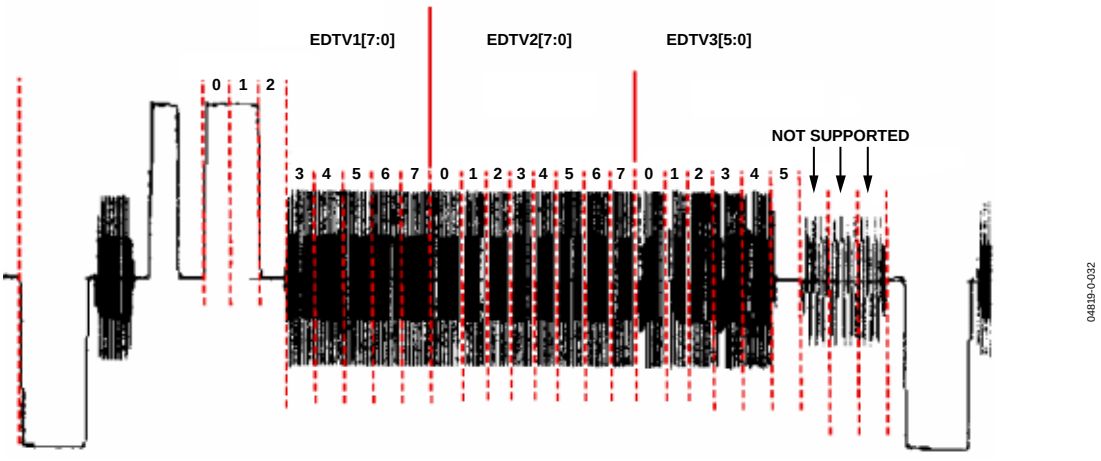

Figure 32. SDP EDTV Data Extraction

Table 144. SDP EDTV Access Information

Signal Name	Block	Register Location	Address		Register Default Value
EDTV1[7:0]	SDP	EDTV 1 [7:0]	147d	93h	Readback Only
EDTV2[7:0]	SDP	EDTV 2 [7:0]	148d	94h	Readback Only
EDTV3[7:0]	SDP	EDTV 3 [7:0]	149d	95h	Readback Only

CGMS Data Registers

CGMS1[7:0] (SDP), Address 0x96, [7:0], CGMS2[7:0] (SDP), Address 0x97, [7:0], CGMS3[7:0] (SDP), Address 0x98, [7:0]

Figure 33 shows the bit correspondence between the analog video waveform and the CGMS1/CGMS2/CGMS3 registers. CGMS3[7:4] are undetermined and should be masked out by software.

Closed Caption Data Registers

CCAP1[7:0] (SDP), Address 0x99, [7:0], CCAP2[7:0] (SDP), Address 0x9A, [7:0]

Figure 34 shows the bit correspondence between the analog video waveform and the CCAP1/CCAP2 registers.

Notes

- CCAP1[7] contains the parity bit from the first word. CCAP2[7] contains the parity bit from the second word.
- Refer to the GDECAD Gemstar Decode Ancillary Data Format (SDP), Address 0x4C, [0] section.

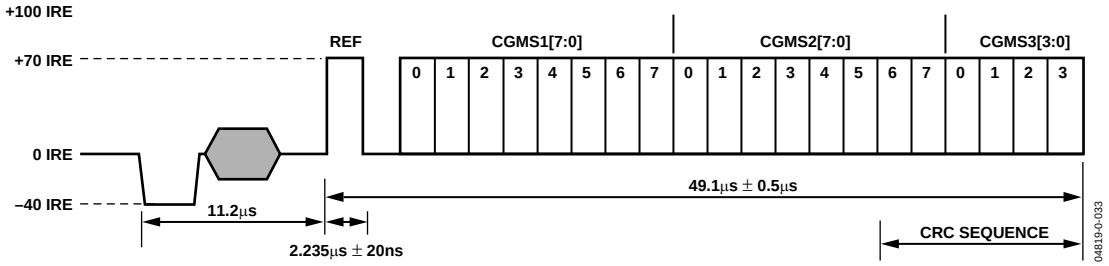

Figure 33. SDP CGMS Data Extraction

Table 145. SDP CGMS Access Information

Signal Name	Block	Register Location	Address		Register Default Value
CGMS1[7:0]	SDP	CGMS 1 [7:0]	150d	96h	Readback Only
CGMS2[7:0]	SDP	CGMS 2 [7:0]	151d	97h	Readback Only
CGMS3[3:0]	SDP	CGMS 3 [3:0]	152d	98h	Readback Only

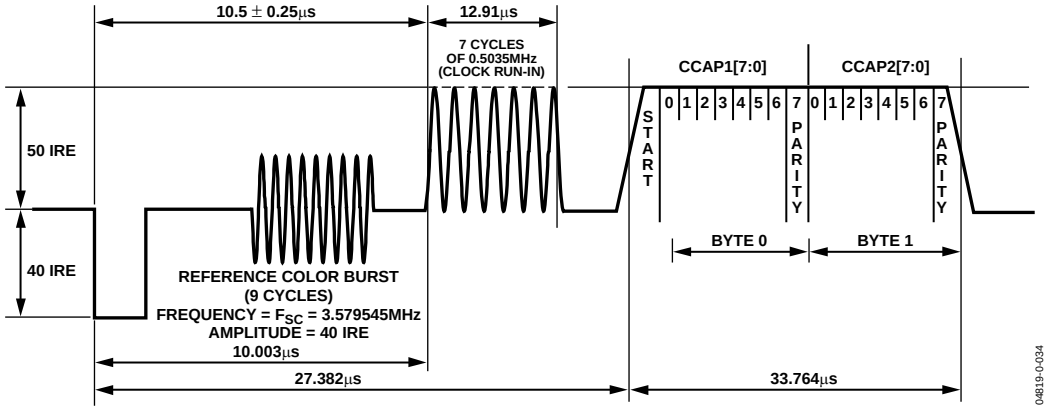

Figure 34. SDP Closed Caption Data Extraction

Table 146. SDP CCAP Access Information

Signal Name	Block	Register Location	Address		Register Default Value
CCAP1[7:0]	SDP	CCAP 1 [7:0]	153d	99h	Readback Only
CCAP2[7:0]	SDP	CCAP 2 [7:0]	154d	9Ah	Readback Only

Letterbox Detection

Incoming video signals may conform to different aspect ratios (16:9 wide screen of 4:3 standard). For certain transmissions in the wide screen format, a digital sequence (WSS) is transmitted with the video signal. If a WSS sequence is provided, the aspect ratio of the video can be derived from the digitally decoded bits WSS contains.

In the absence of a WSS sequence, letterbox detection may be used to find wide screen signals. The detection algorithm examines the active video content of lines at the start and end of a field. If black lines are detected, this may serve as an indication that the currently shown picture is in wide screen format.

The active video content (luminance magnitude) over a line of video is summed together. At the end of a line, this accumulated value is compared with a threshold, and a decision is made as to whether or not a particular line is black. The threshold value needed may depend on the type of input signal; some control is provided via LB_TH[4:0].

Detection at the Start of a Field

The ADV7183A expects a section of at least six consecutive black lines of video at the top of a field. Once those lines have been detected, Register LB_LCT[7:0] reports back the number of black lines that were actually found. By default, the ADV7183A starts looking for those black lines in sync with the beginning of active video (e.g., straight after the last VBI video line). LB_SL[3:0] allows the user to set the start of letterbox detection from the beginning of a frame on a line-by-line basis. The detection window closes in the middle of the field.

Detection at the End of a Field

The ADV7183A expects at least six continuous lines of black video at the bottom of a field before reporting back the number of lines actually found via the LB_LCB[7:0] value. The activity window for letterbox detection (end of field) starts in the middle of an active field. Its end is programmable via LB_EL[3:0].

Detection at the Midrange

Some transmissions of wide screen video include subtitles within the lower black box. If the ADV7183A finds at least two black lines followed by some more nonblack video (e.g.,. the subtitle) and finally followed by the remainder of the bottom black block, it reports back a midcount via LB_LCM[7:0]. In cases where no subtitles are found, LB_LCM[7:0] reports the same number as LB_LCB[7:0].

Notes

- There is a 2-field delay in the reporting of any line count parameters.
- There is no "letterbox detected" bit. The user is asked to read the LB_LCT[7:0] and LB_LCB[7:0] register values and to come to a conclusion about the presence of letterbox type video in software.

LB_LCT[7:0] Letterbox Line Count Top (SDP), Address 0x9B, [7:0]; LB_LCM[7:0] Letterbox Line Count Mid (SDP), Address 0x9C, [7:0]; LB_LCB[7:0] Letterbox Line Count Bottom (SDP), Address 0x9D, [7:0]

Table 147. LB_LCx Access Information

Signal Name	Block	Address	Register Default Value
LB_LCT[7:0]	SDP	0x9B	Readback only
LB_LCM[7:0]	SDP	0x9C	Readback only
LB_LCB[7:0]	SDP	0x9D	Readback only

LB_TH[4:0] Letterbox Threshold Control (SDP), Address 0xDC, [4:0]

Table 148.LB_TH Function

LB_TH[4:0]	Description

Table 206. Registers 0xE5 to 0xE7

Subaddress	Register	Bit Description	Bit 7	6	5	4	3	2	1	0	Comments
0xE5	NTSC V Bit Begin	**NVBEG[4:0]**. How many lines after I_{COUNT} rollover to set V high.									
						0	0	1	0	1	NTSC Default(BT.656)
		NVBEGSIGN									
					0						Set to low when manual programming
					1						Not suitable for user programming
		NVBEGDELE. Delay V bit going high by one line relative to NVBEG (even field).									
				0							No delay
				1							Additional delay by 1 line
		NVBEGDELO. Delay V bit going high by one line relative to NVBEG (odd field).									
			0								No delay
			1								Additional delay by 1 line
0xE6	NTSC V Bit End	**NVEND[4:0]**. How many lines after I_{COUNT} rollover to set V low.									
						0	0	1	0	0	NTSC Default (BT.656)
		NVENDSIGN									
					0						Set to low when manual programming
					1						Not suitable for user programming
		NVENDDELE. Delay V bit going low by one line relative to NVEND (even field).									
				0							No delay
				1							Additional delay by 1 line
		NVENDDELO. Delay V bit going low by one line relative to NVEND (odd field).									
			0								No delay
			1								Additional delay by 1 line
0xE7	NTSC F Bit Toggle	**NFTOG[4:0]**. How many lines after I_{COUNT} rollover to toggle F signal.									
						0	0	0	1	1	NTSC Default
		NFTOGSIGN									
					0						Set to low when manual programming
					1						Not suitable for user programming
		NFTOGDELE. Delay F transition by one line relative to NFTOG (even field).									
				0							No delay
				1							Additional delay by 1 line
		NFTOGDELO. Delay F transition by one line relative to NFTOG (odd field).									
			0								No delay
			1								Additional delay by 1 line

Table 207. Registers 0xE8 to 0xEA

Subaddress	Register	Bit Description	Bit 7	6	5	4	3	2	1	0	Comments
0xE8	PAL V Bit Begin	**PVBEG[4:0]**. How many lines after I_{COUNT} rollover to set V high.									
						0	0	1	0	1	PAL Default (BT.656)
		PVBEGSIGN									
					0						Set to low when manual programming
					1						Not suitable for user programming
		PVBEGDELE. Delay V bit going high by one line relative to PVBEG (even field).									
				0							No delay
				1							Additional delay by 1 line
		PVBEGDELO. Delay V bit going high by one line relative to PVBEG (odd field).									
			0								No delay
			1								Additional delay by 1 line
0xE9	PAL V Bit End	**PVEND[4:0]**. How many lines after I_{COUNT} rollover to set V low.									
						1	0	1	0	0	PAL Default (BT.656)
		PVENDSIGN									
					0						Set to low when manual programming
					1						Not suitable for user programming
		PVENDDELE. Delay V bit going low by one line relative to PVEND (even field).									
				0							No delay
				1							Additional delay by 1 line
		PVENDDELO. Delay V bit going low by one line relative to PVEND (odd field).									
			0								No delay
			1								Additional delay by 1 line
0xEA	PAL F Bit Toggle	**PFTOG[4:0]**. How many lines after I_{COUNT} rollover to toggle F signal.									
						0	0	0	1	1	PAL Default (BT.656)
		PFTOGSIGN.									
					0						Set to low when manual programming
					1						Not suitable for user programming
		PFTOGDELE. Delay F transition by one line relative to PFTOG (even field).									
				0							No delay
				1							Additional delay by 1 line
		PFTOGDELO. Delay F transition by one line relative to PFTOG (odd field).									
			0								No delay
			1								Additional delay by 1 line

APPENDIX A

I²C PROGRAMMING EXAMPLES

Mode 1 CVBS Input (Composite Video on AIN5)

All standards are supported through autodetect, 8-bit, 4:2:2, ITU-R BT.656 output on P15–P8.

Table 208. Mode 1 CVBS Input

Register Address	Register Value	Notes
0x00	0x04	CVBS input on AIN5.
0x01	0x88	Turn off HSYNC processor (SECAM only[13]).
0x17	0x41	Set CSFM to SH1.
0x2B	0xE2	AGC tweak
0x3A	0x16	Power down ADC 1 and ADC 2.
0x51	0x24	Turn off FSC detect for IN LOCK status.
0xD2	0x01	AGC tweak.
0xD3	0x01	AGC tweak.
0xDB	0x9B	AGC tweak.
0x0E	0x85	ADI recommended programming sequence. This sequence must be followed exactly when setting up the decoder.
0x89	0x0D	Recommended setting.
0x8D	0x9B	Recommended setting.
0x8F	0x48	Recommended setting.
0xB5	0x8B	Recommended setting.
0xD4	0xFB	Recommended setting.
0xD6	0x6D	Recommended setting.
0xE2	0xAF	Recommended setting.
0xE3	0x00	Recommended setting.
0xE4	0xB5	Recommended setting.
0xE8	0xF3	Recommended setting.
0x0E	0x05	Recommended setting.

[13] For all SECAM modes of operation, HSYNC PROCESSOR must be turned off.

Mode 2 S-Video Input (Y on AIN1 and C on AIN4)

All standards are supported through autodetect, 8-bit, ITU-R BT.656 output on P15–P8.

Table 209. Mode 2 S-Video Input

Register Address	Register Value	Notes
0x00	0x06	Y1 = AIN1, C1 = AIN4.
0x01	0x88	Turn off HSYNC processor (SECAM only).
0x2B	0xE2	AGC tweak.
0x3A	0x12	Power down ADC 2.
0x51	0x24	Turn off FSC detect for IN LOCK status.
0xD2	0x01	AGC tweak.
0xD3	0x01	AGC tweak.
0xDB	0x9B	AGC tweak.
0x0E	0x85	ADI recommended programming sequence. This sequence must be followed exactly when setting up the decoder.
0xB5	0x8B	Recommended setting.
0xD4	0xFB	Recommended setting.
0xD6	0x6D	Recommended setting.
0xE2	0xAF	Recommended setting.
0xE3	0x00	Recommended setting.
0xE4	0xB5	Recommended setting.
0xE8	0xF3	Recommended setting.
0x0E	0x05	Recommended setting.

Mode 3 525i/625i YPrPb Input (Y on AIN2, Pr on AIN3, and Pb on AIN6)

All standards are supported through autodetect, 8-bit, ITU-R BT.656 output on P15–P8.

Table 210. Mode 3 YPrPb Input 525i/625i

Register Address	Register Value	Notes
0x00	0x0A	Y2 = AIN2, Pr2 = AIN3, Pb2 = AIN6.
0x01	0x88	Disable HSync PLL.
0x2B	0xE2	AGC tweak.
0x3A	0x10	Set latch clock.
0x51	0x24	Turn off FSC detect for IN LOCK status.
0xD2	0x01	AGC tweak.
0xD3	0x01	AGC tweak.
0xDB	0x9B	AGC tweak.
0x0E	0x85	ADI recommended programming sequence. This sequence must be followed exactly when setting up the decoder.
0xD6	0x6D	Recommended setting.
0xE8	0xF3	Recommended setting.
0x0E	0x05	Recommended setting.

Mode 4 CVBS Tuner Input PAL Only on AIN4

8-bit, ITU-R BT.656 output on P15–P8.

Table 211. Mode 4 Tuner Input CVBS PAL Only

Register Address	Register Value	Notes
0x00	0x83	CVBS AIN4 Force PAL only mode.
0x07	0x01	Enable PAL autodetection only.
0x17	0x41	Set CSFM to SH1.
0x19	0xFA	Stronger dot crawl reduction.
0x2B	0xE2	AGC tweak.
0x3A	0x16	Power down ADC 1 and ADC 2.
0x50	0x0A	Set higher DNR threshold.
0x51	0x24	Turn off FSC detect for IN LOCK status.
0xD2	0x01	AGC tweak.
0xD3	0x01	AGC tweak.
0xDB	0x9B	AGC tweak.
0x0E	0x85	ADI recommended programming sequence. This sequence must be followed exactly when setting up the decoder.
0x89	0x0D	Recommended setting.
0x8D	0x9B	Recommended setting.
0x8F	0x48	Recommended setting.
0xB5	0x8B	Recommended setting.
0xD4	0xFB	Recommended setting.
0xD6	0x6D	Recommended setting.
0xE2	0xAF	Recommended setting.
0xE3	0x00	Recommended setting.
0xE4	0xB5	Recommended setting.
0xE8	0xF3	Recommended setting.
0x0E	0x05	Recommended setting.

APPENDIX B

PCB LAYOUT RECOMMENDATIONS

The ADV7183A is a high precision, high speed mixed-signal device. To achieve the maximum performance from the part, it is important to have a well laid-out PCB board. The following is a guide for designing a board using the ADV7183A.

Analog Interface Inputs

The inputs should receive care when being routed on the PCB. Track lengths should be kept to a minimum, and 75 Ω trace impedances should be used when possible. Trace impedances other than 75 Ω also increase the chance of reflections.

Power Supply Decoupling

It is recommended to decouple each power supply pin with 0.1 µF and 10 nF capacitors. The fundamental idea is to have a decoupling capacitor within about 0.5 cm of each power pin. Also, avoid placing the capacitor on the opposite side of the PC board from the ADV7183A, as doing so interposes resistive vias in the path. The decoupling capacitors should be located between the power plane and the power pin. Current should flow from the power plane to the capacitor to the power pin. Do not make the power connection between the capacitor and the power pin. Placing a via underneath the 100 nF capacitor pads, down to the power plane, is generally the best approach (see Figure 38).

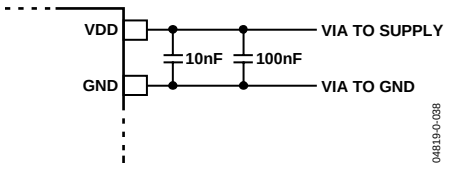

Figure 38. Recommend Power Supply Decoupling

It is particularly important to maintain low noise and good stability of PVDD. Careful attention must be paid to regulation, filtering, and decoupling. It is highly desirable to provide separate regulated supplies for each of the analog circuitry groups (AVDD, DVDD, DVDDIO, and PVDD).

Some graphic controllers use substantially different levels of power when active (during active picture time) and when idle (during horizontal and vertical sync periods). This can result in a measurable change in the voltage supplied to the analog supply regulator, which can, in turn, produce changes in the regulated analog supply voltage. This can be mitigated by regulating the analog supply, or at least PVDD, from a different, cleaner, power source (for example, from a 12 V supply).

It is also recommend to use a single ground plane for the entire board. This ground plane should have a spacing gap between the analog and digital sections of the PCB (see Figure 39).

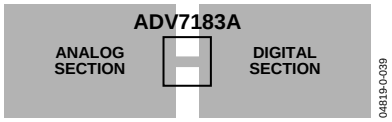

Figure 39. PCB Ground Layout

Experience has repeatedly shown that the noise performance is the same or better with a single ground plane. Using multiple ground planes can be detrimental because each separate ground plane is smaller, and long ground loops can result.

In some cases, using separate ground planes is unavoidable. For those cases, it is recommended to at least place a single ground plane under the ADV7183A. The location of the split should be under the ADV7183A. For this case, it is even more important to place components wisely because the current loops will be much longer (current takes the path of least resistance). An example of a current loop: power plane to ADV7183A to digital output trace to digital data receiver to digital ground plane to analog ground plane.

PLL

Place the PLL loop filter components as close to the ELPF pin as possible. Do not place any digital or other high frequency traces near these components. Use the values suggested in the data sheet with tolerances of 10% or less.

Digital Outputs (Both Data and Clocks)

Try to minimize the trace length that the digital outputs have to drive. Longer traces have higher capacitance, which requires more current, which causes more internal digital noise. Shorter traces reduce the possibility of reflections.

Adding a series resistor of a value between 30 Ω and 50 Ω can suppress reflections, reduce EMI, and reduce the current spikes inside the ADV7183A. If series resistors are used, place them as close to the ADV7183A pins as possible. However, try not to add vias or extra length to the output trace to get the resistors closer.

If possible, limit the capacitance that each of the digital outputs drives to less than 15 pF. This can easily be accomplished by keeping traces short and by connecting the outputs to only one device. Loading the outputs with excessive capacitance increases the current transients inside the ADV7183A, creating more digital noise on its power supplies.

Digital Inputs

The digital inputs on the ADV7183A were designed to work with 3.3 V signals, and are not tolerant of 5 V signals. Extra components are needed if 5 V logic signals are required to be applied to the decoder.

Antialiasing Filters

For inputs from some video sources that are not bandwidth limited, signals outside the video band can alias back into the video band during A/D conversion and appear as noise on the output video. The ADV7183A oversamples the analog inputs by a factor of 4. This 54 MHz sampling frequency reduces the requirement for an input filter; for optimal performance it is recommended that an antialiasing filter be employed. The recommended low cost circuit for implementing this buffer and filter circuit for all analog input signals is shown in Figure 41.

The buffer is a simple emitter-follower using a single npn transistor. The antialiasing filter is implemented using passive components. The passive filter is a third-order Butterworth filter with a -3dB point of 9MHz. The frequency response of the passive filter is shown in Figure 40. The flat pass band up to 6 MHz is essential. The attenuation of the signal at the output of the filter due to the voltage divider of R24 and R63 is compensated for in the ADV7183A part using the automatic gain control. The ac coupling capacitor at the input to the buffer creates a high-pass filter with the biasing resistors for the transistor. This filter has a cut-off of

$$\{2 \times \pi \times (R39||R89) \times C93\}^{-1} = 0.62 \text{ Hz}$$

It is essential that the cutoff of this filter be less than 1 Hz to ensure correct operation of the internal clamps within the part. These clamps ensure that the video stays within the 5 V range of the op amp used.

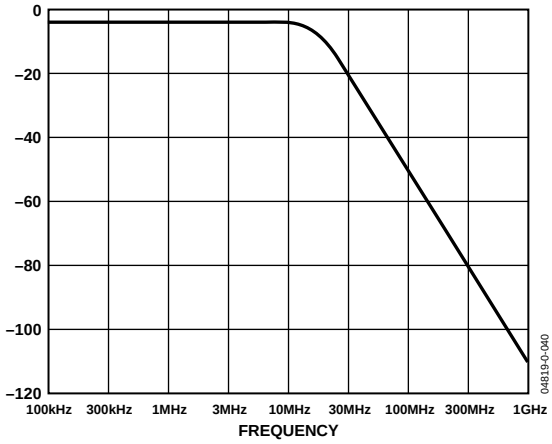

Figure 40. Third-Order Butterworth Filter Response

APPENDIX C

TYPICAL CIRCUIT CONNECTION

Examples of how to connect the ADV7183A video decoder are shown in Figure 41 and Figure 42.

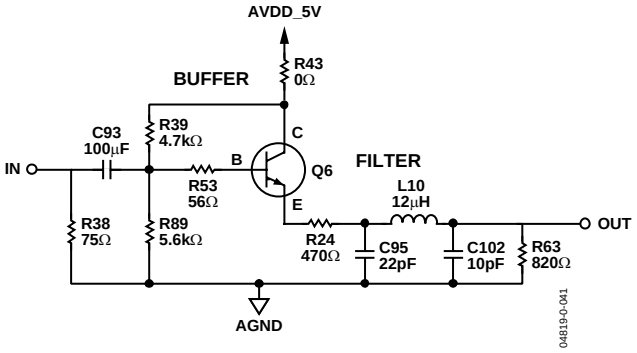

Figure 41. ADI Recommended Antialiasing Circuit for All Input Channels

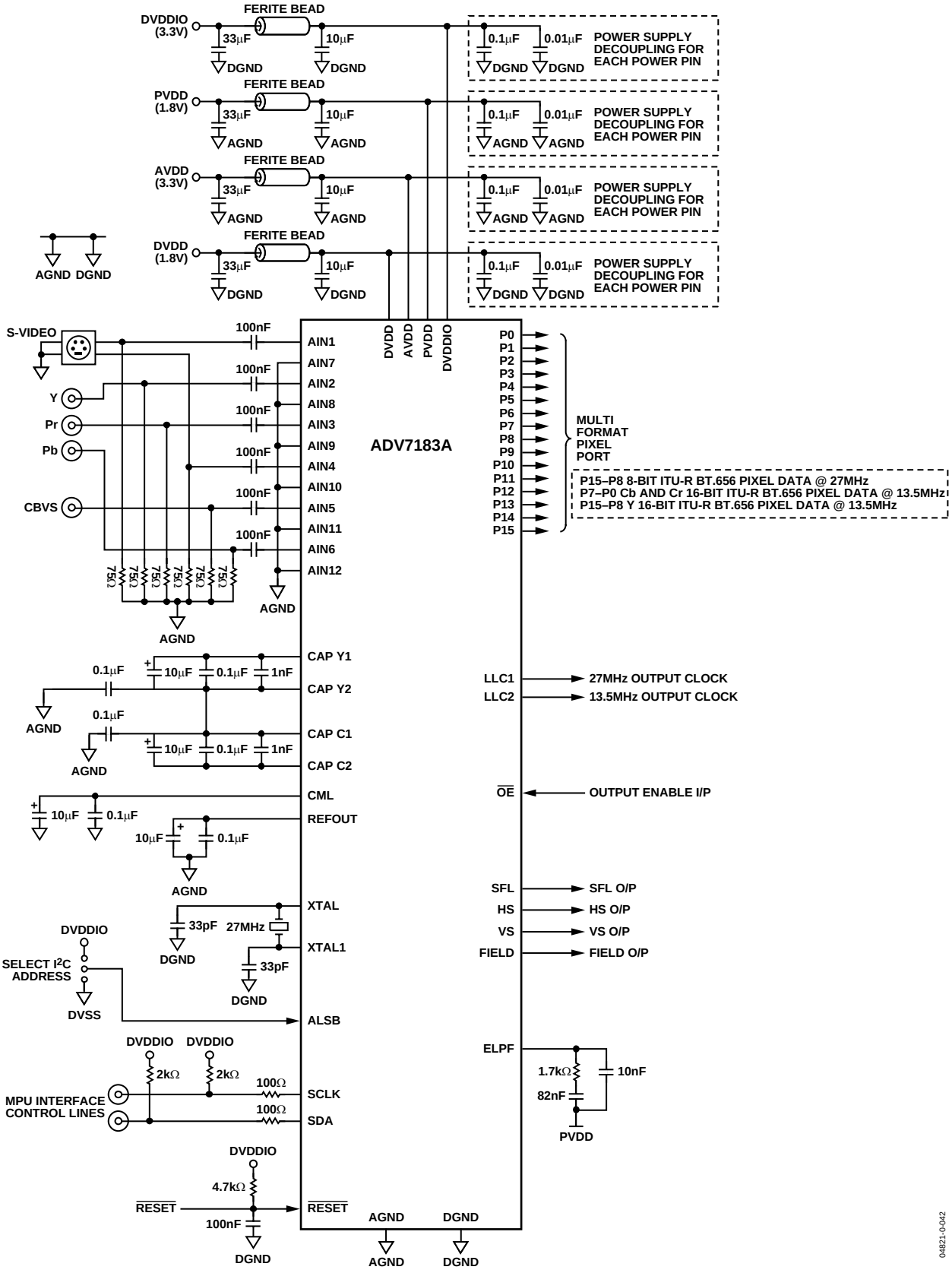

Figure 42. Typical Connection Diagram

OUTLINE DIMENSIONS

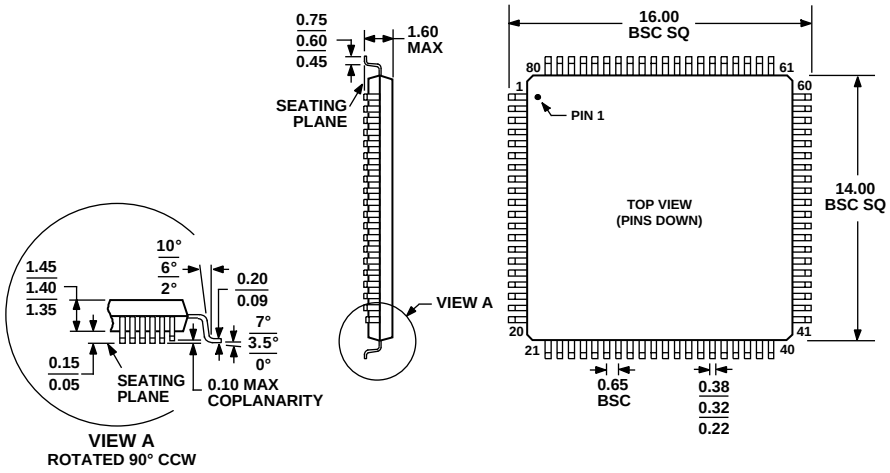

Figure 43. 80-Lead Low Profile Quad Flat Package [LQFP]
(ST-80-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADV7183AKST	–25°C to +70°C	Low Profile Quad Flat Package (LQFP)	ST-80-2
ADV7183ABST	–40°C to +85°C	Low Profile Quad Flat Package (LQFP)	ST-80-2
EVAL-ADV7183AEBM		Evaluation Board	

Note: The ADV7183A is a Pb-free environmentally friendly product. It is manufactured using the most up-to-date materials and processes. The coating on the leads of each device is 100% pure Sn electroplate. The device is suitable for Pb-free applications, and can withstand surface-mount soldering at up to 255°C (±5°C).

In addition, it is backward-compatible with conventional SnPb soldering processes. This means the electroplated Sn coating can be soldered with Sn/Pb solder pastes at conventional reflow temperatures of 220°C to 235°C.

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