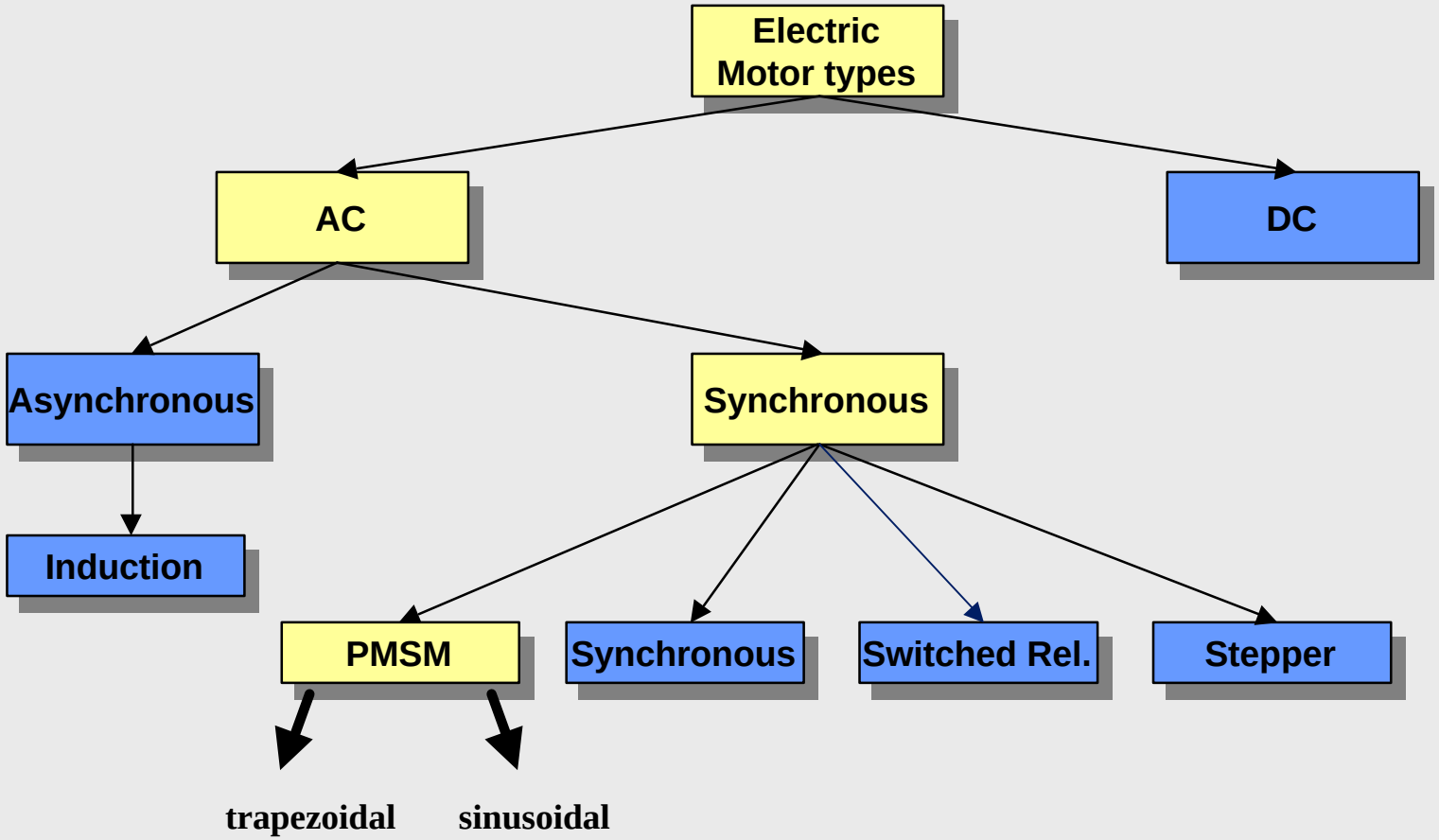
3 Phase Motor Drive

Implementation of Space Vector Modulation
based on XC164CS / XC167CI

Overview


Electric
Motor types
AC
DC
Asynchronous
Synchronous
Induction
PMSM
Synchronous
Switched Rel.
Stepper
trapezoidal
sinusoidal

Why Space Vector Modulation ?

Block Commutation:

- Enough performance to control low dynamic motors (BLDC Motor)
- Less Systemcosts
  - Sensorless control (BEMF-detection)
  - Less CPU resources due to defined commutation points (least 6 points)

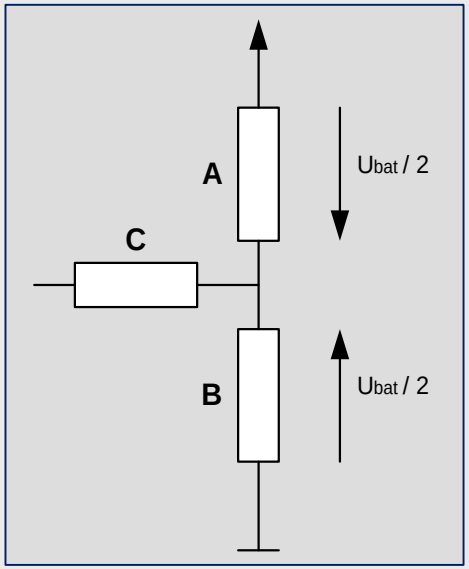
Space Vector Modulation:

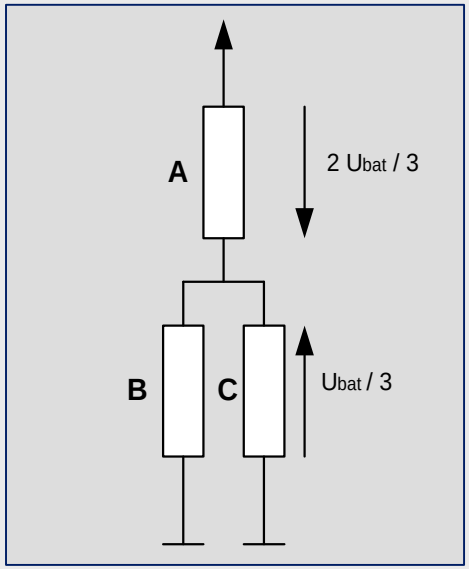
- Higher performance to control mid / high dynamic motors
- Higher efficiency (86 %), sinusoidally weighted PWM (75%)
- Improved torque management
  - better startup performance, low speed with constant torque
  - constant torque, less torque ripple
  - improved dynamical reaction

Block commutation (2 phase / 3 phase active)

2 phase active:
- no dead time generation
- BEMF detection (sensorless)
- less torque

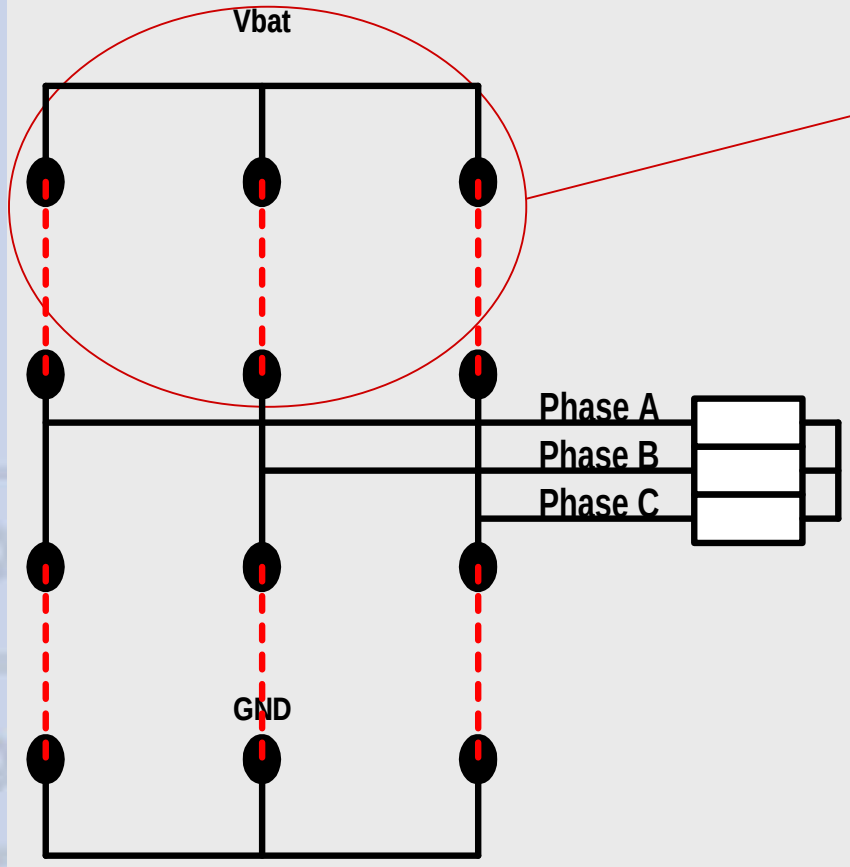
3 phase active:
- dead time generation
- higher torque
- higher system costs





Space Vector Modulation

Generation of a rotating field



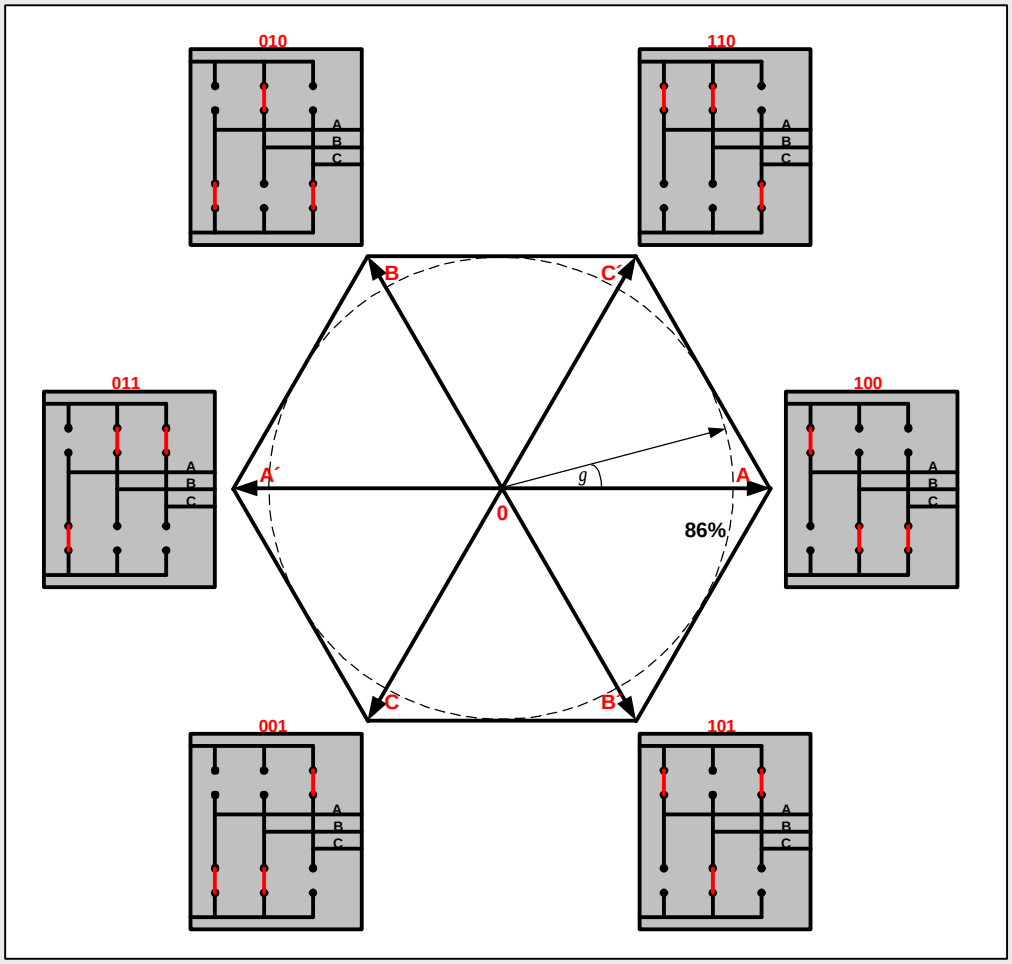
B6 Bridge:

8 different states are possible for high side switches

0	0	0	Vector zero
0	0	1	Phase C pos.
0	1	0	Phase B pos.
0	1	1	Phase A neg.
1	0	0	Phase A pos.
1	0	1	Phase B neg.
1	1	0	Phase C neg.
1	1	1	Vector zero

low side switches builds the complement

Generation of a rotating field



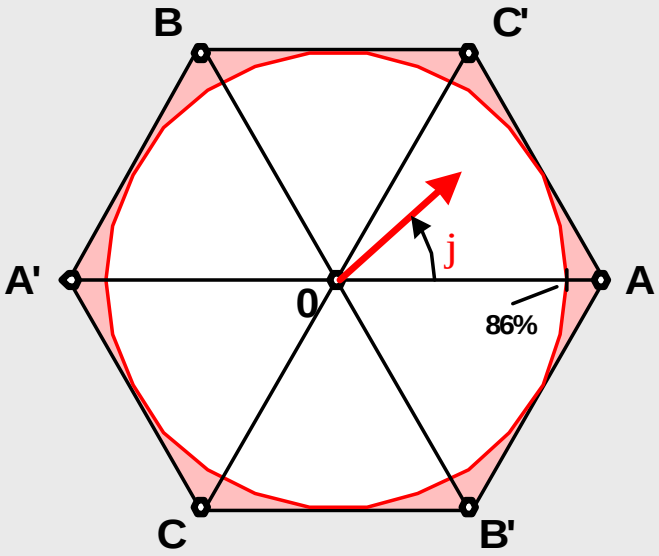
The eight possible switching patterns lead to six possible field orientations (plus two 0-vectors).

The points located inside the hexagon (operating area of the inverter) can be reached by the field vector.

The points outside can't be reached.

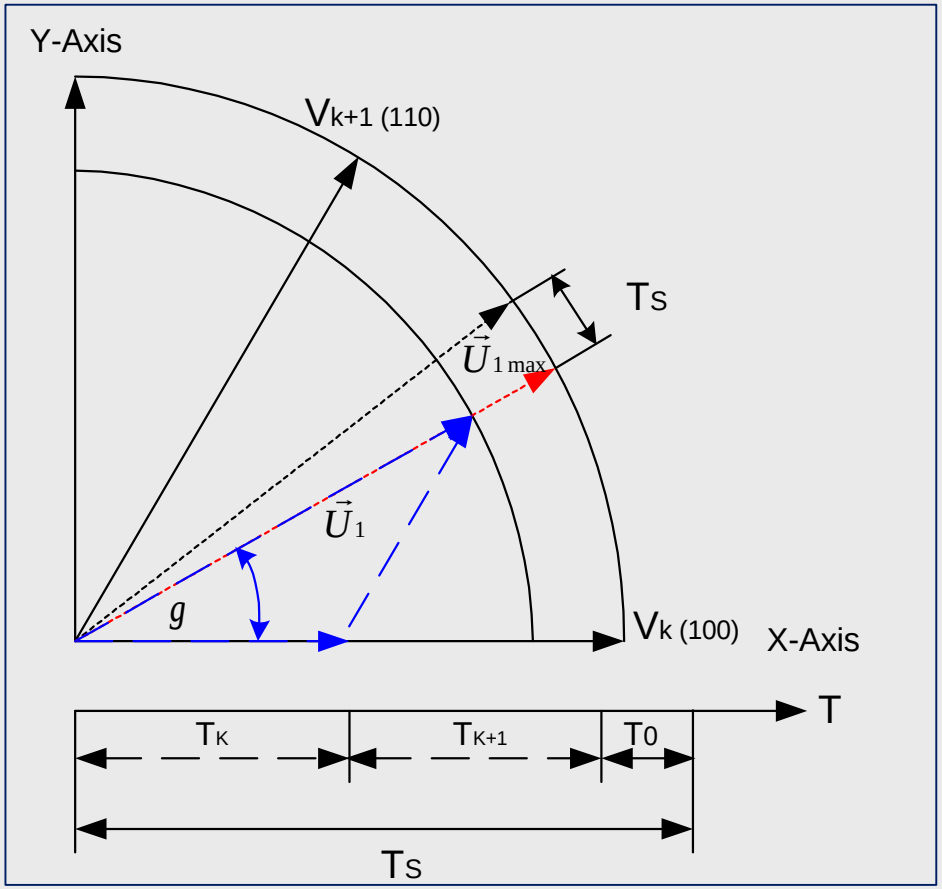
Space Vector Modulation

A PWM generation based on the combination of the seven resulting switching vectors (0, A, B, C, A', B', C') is called Space Vector Modulation. The amplitude and the orientation of the desired field are the inputs for the PWM generation.



The inner circle in the hexagon limits the maximum amplitude for a field with few harmonics.
The area between the inner circle and the hexagon is called "overmodulation area" and adds harmonics.

Space Vector Modulation (Sector 1)



Ts:	Sampling Time, e.g. $PWM_{Freq.}$ = 20 KHz
V_{K+1}:	Vector (60 degree)
V_K:	Vector (0 degree)
T_{K+1}:	f(V_{K+1})
T_K:	f(V_K)
$\vec{U}_1$:	Phase voltage vector for angle g
$\vec{U}_{1\max}$ vector	: Max. phase voltage for angle
T_0:	Time for vector zero
Ubat:	DC link voltage

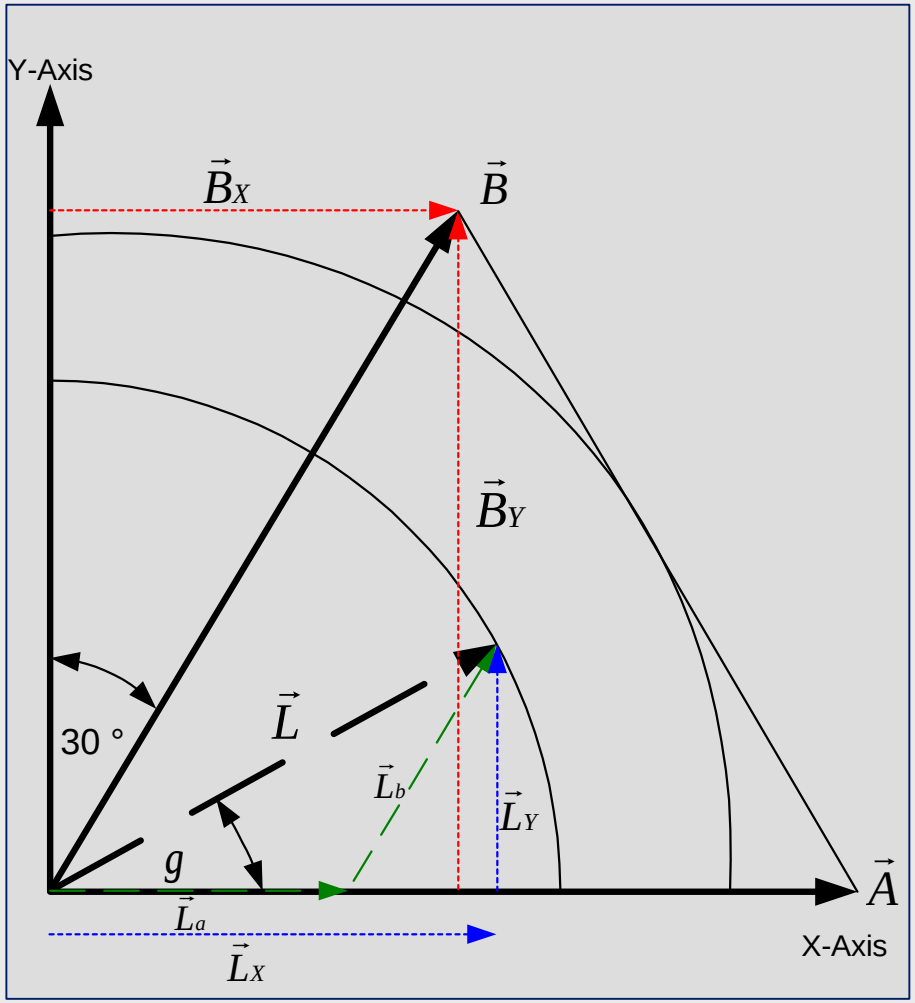
$$\vec{U}1 = \frac{1}{T_S} \times \left(T_{K+1} \times V_{K+1} + T_k \times V_K\right)$$

$$T_K = T_S \times \frac{|\vec{U}1|}{U_{bat}} \times \sqrt{3} \times \sin\left(\frac{p}{3} - g\right)$$

$$T_{K+1} = T_S \times \frac{|\vec{U}1|}{U_{bat}} \times \sqrt{3} \times \sin(g)$$

$$T_0 = T_S\left(1 - T_{K+1} - T_K\right)$$

Space Vector Modulation (Graphical Approach)



$$\vec{L} = \vec{L}_a + \vec{L}_b = a \times \vec{A} + b \times \vec{B}$$

$$\vec{L}_Y = \vec{L} \times \sin g$$
$$\vec{L}_X = \vec{L} \times \cos g$$

$$\vec{B}_Y = \vec{B} \times \cos 30°$$
$$\vec{B}_X = \vec{B} \times \sin 30°$$

$$\vec{L}_X = b \times \vec{B}_X + a \times \vec{A}_X$$
$$\vec{L}_Y = b \times \vec{B}_Y + a \times \vec{A}_Y; \vec{A}_Y = 0; \Rightarrow \vec{L}_Y = b \times \vec{B}_Y$$

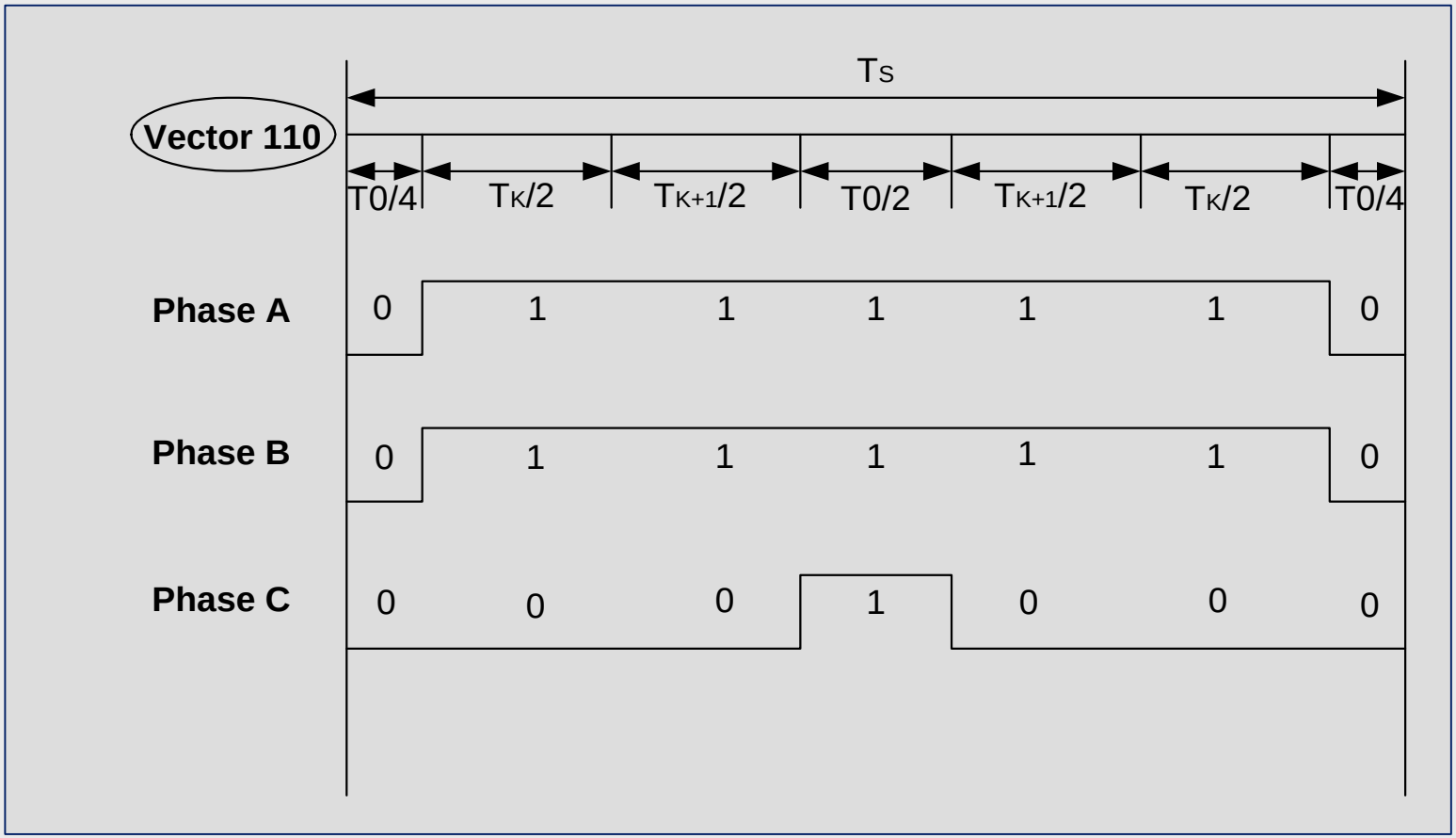
$$b = \frac{\vec{L}_Y}{\vec{B}_Y} = \frac{|\vec{L}|}{|\vec{B}| \times \cos 30°} \times \sin g$$

$$a = \frac{\vec{L}_X - b \times \vec{B}_X}{\vec{A}_X} = \frac{|\vec{L}| \times \cos g - b \times |\vec{B}| \times \sin 30°}{|\vec{A}|}$$

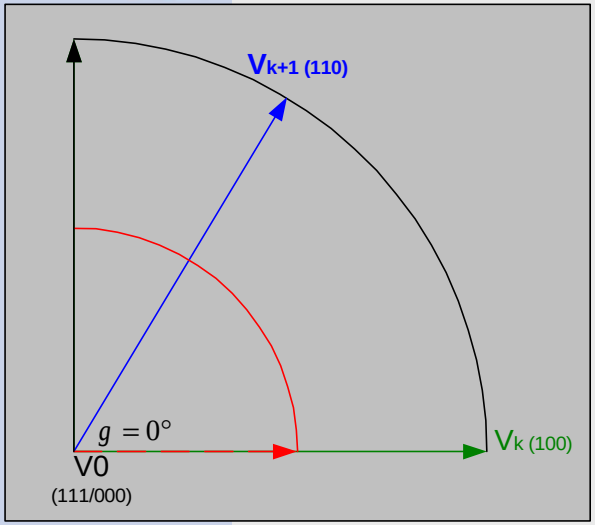
$\Rightarrow a, b = f(g)$ **Lookup Table**

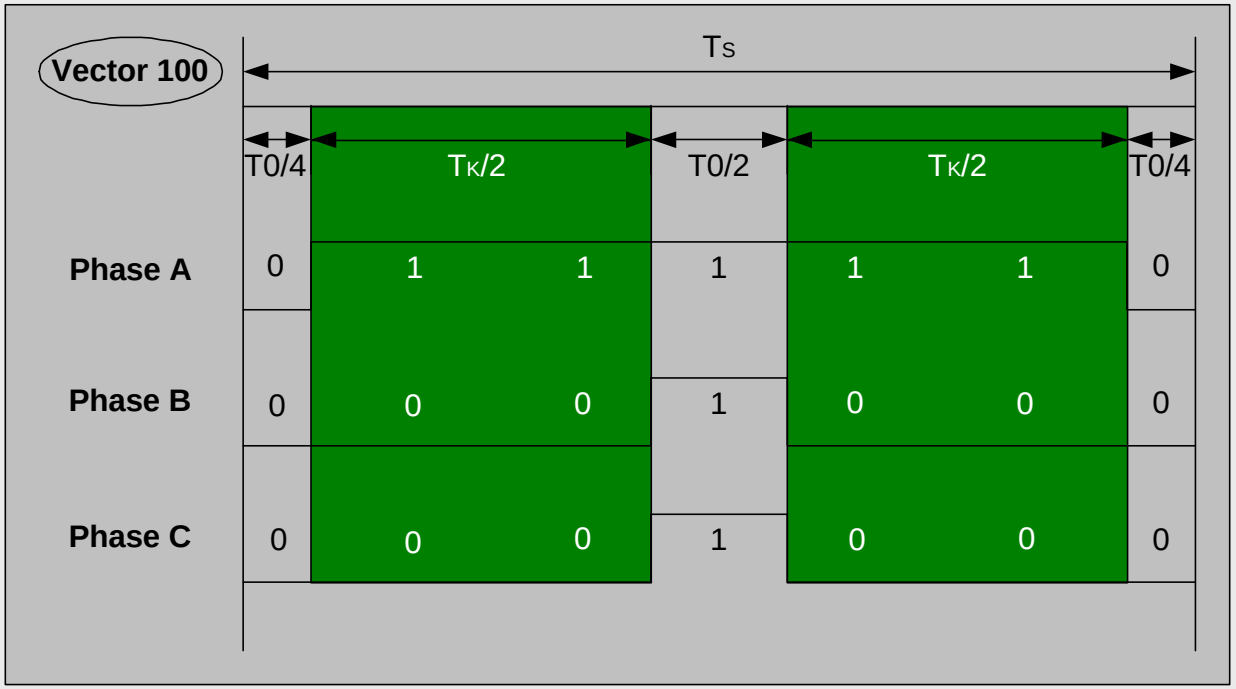
$\Rightarrow T_K = f(a)$
$\Rightarrow T_{K+1} = f(b)$

PWM output patterns (Principle)



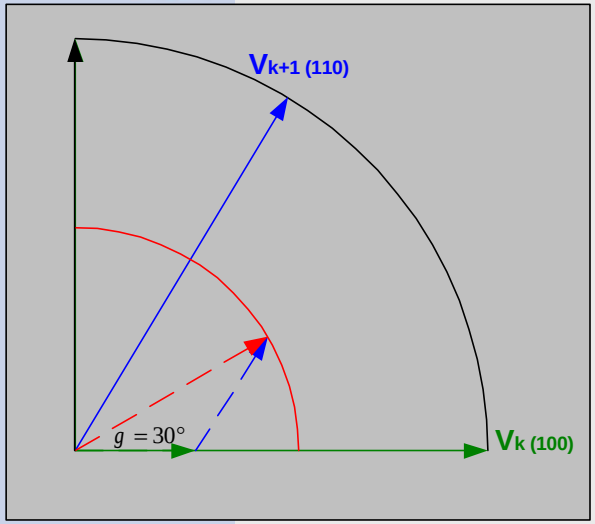
PWM output patterns (vector 100) in sector 1

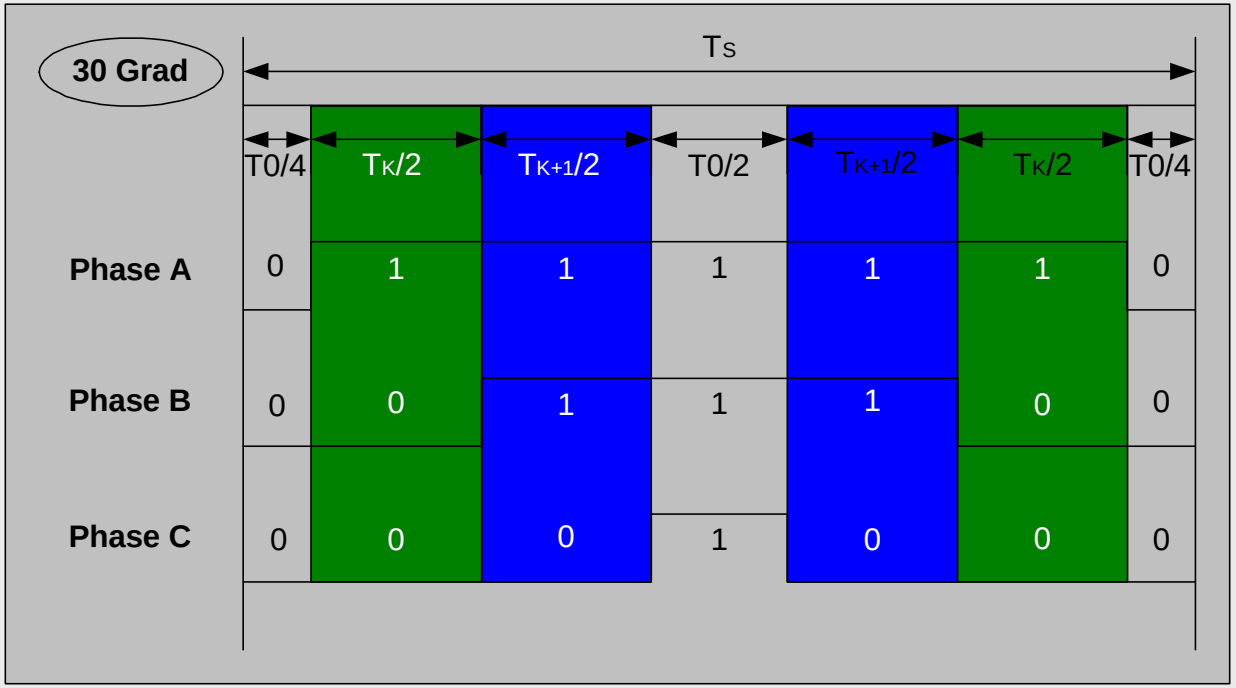




Space Vector Modulation

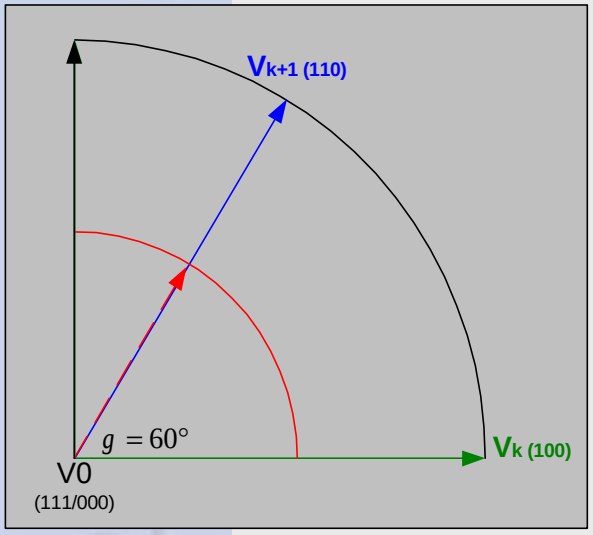
PWM output patterns (30 degree) in sector 1

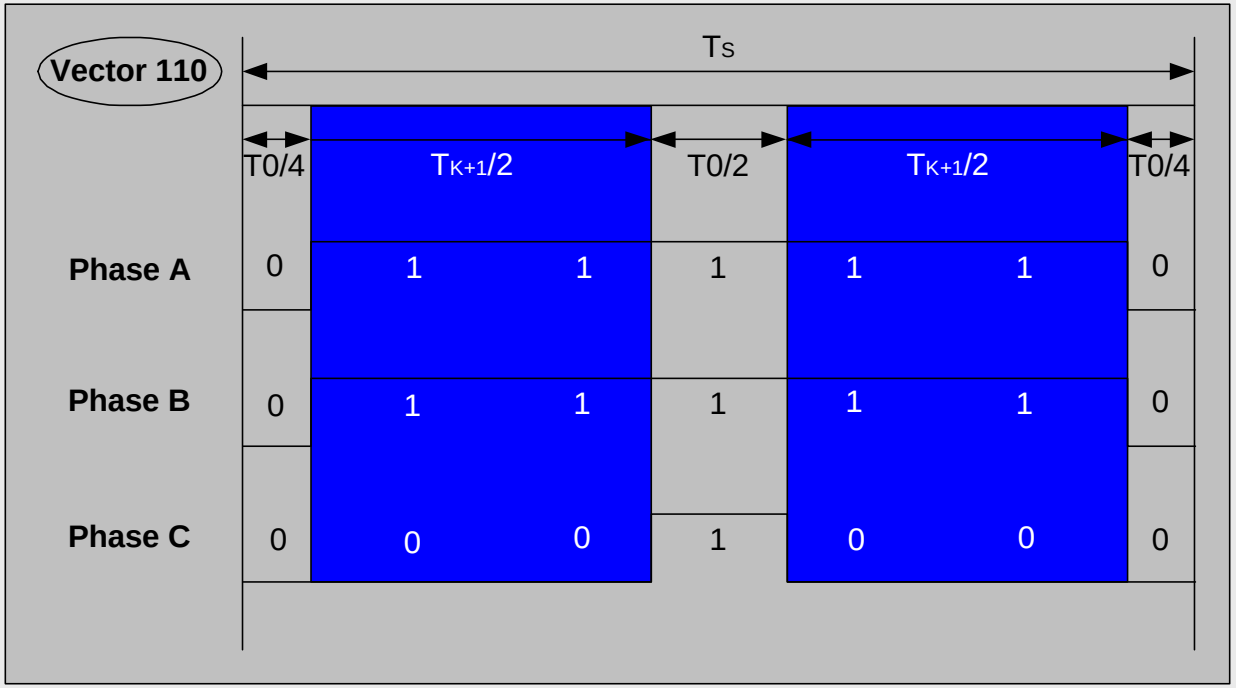




Space Vector Modulation

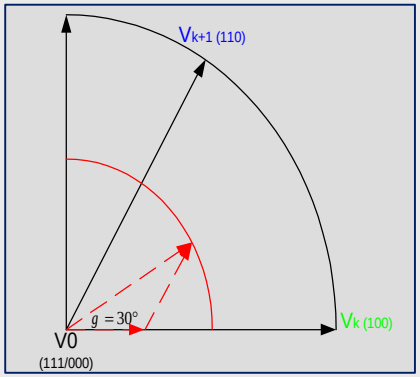
PWM output patterns (vector 110) in sector 1

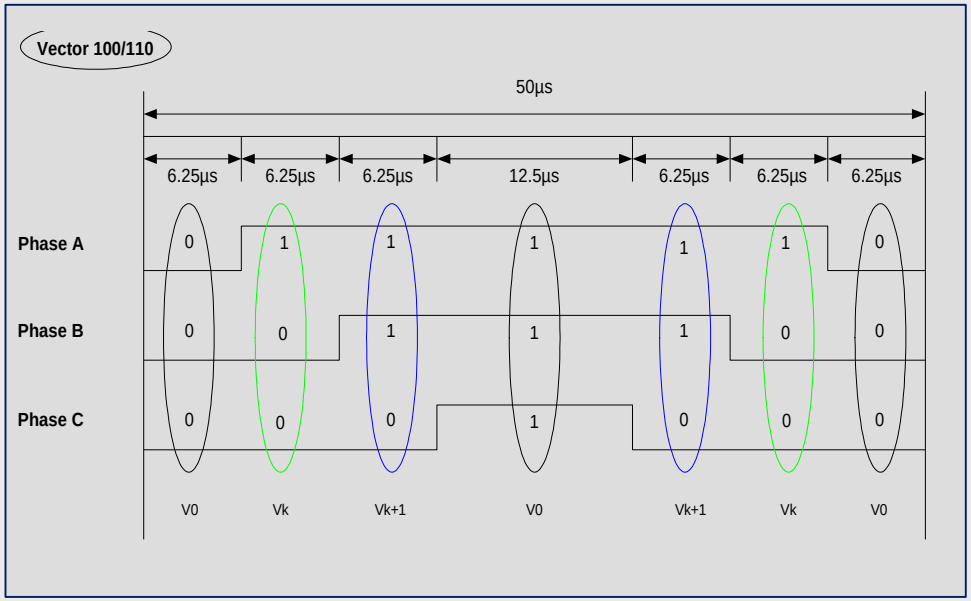




Space Vector Modulation

PWM output patterns (Example for 50 % duty cycle)





Example:

$|\vec{U}_1| = 0.5 \times |\vec{U}_{1Max}|$

$g = 30°$

$T_S = 50\mu s$

$$T_K = T_S \times \frac{|\vec{U}_1|}{U_{bat}} \times \sqrt{3} \times \sin\left(\frac{p}{3} - g\right)$$

$T_K = 50\mu s \times 0.5 \times 0.5$

$T_{K(30°)} = 12.5\mu s$

$$T_{K+1} = T_S \times \frac{|\vec{U}_1|}{U_{bat}} \times \sqrt{3} \times \sin(g)$$

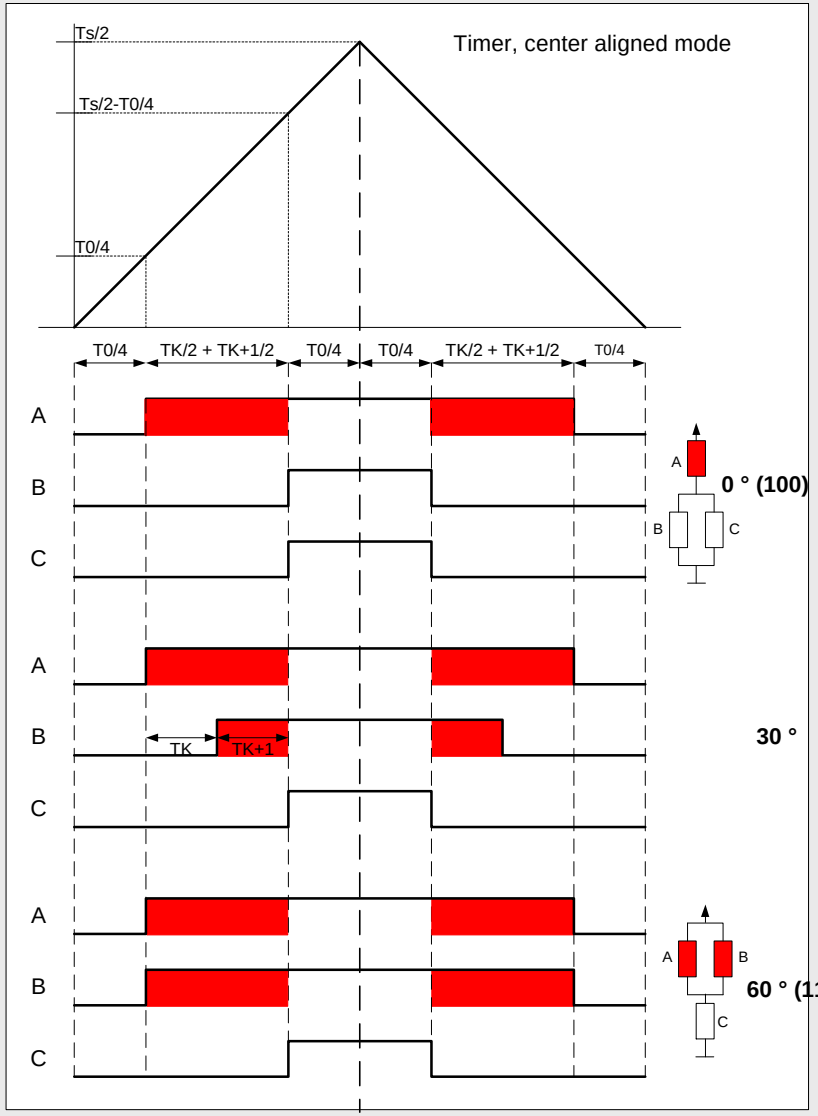
$T_{K+1(30°)} = 12.5\mu s$

$T_0 = T_S(1 - T_K - T_{K-1})$

$T_{0(30°)} = 25\mu s$

Space Vector Modulation

PWM Generation



Equations for Capture/Compare Unit 6:

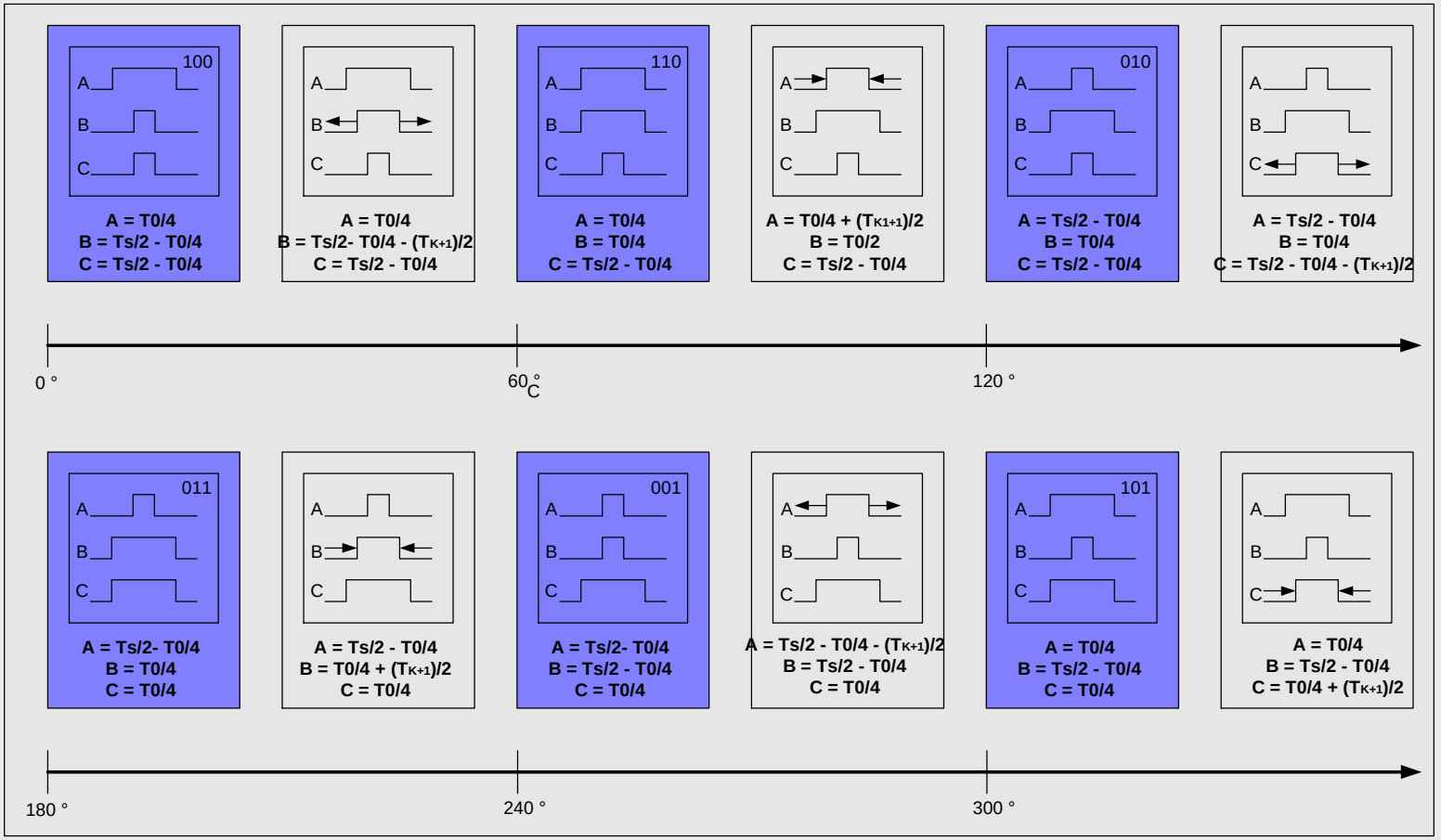
CCU6_CC60SR = T0/4
CCU6_CC61SR = Ts/2-T0/4
CCU6_CC62SR = Ts/2-T0/4

CCU6_CC60SR = T0/4
CCU6_CC61SR = Ts/2-T0/4-TK+1/2
CCU6_CC62SR = T-T0/2

CCU6_CC60SR = T0/4
CCU6_CC61SR = T0/4
CCU6_CC62SR = Ts/2-T0/4

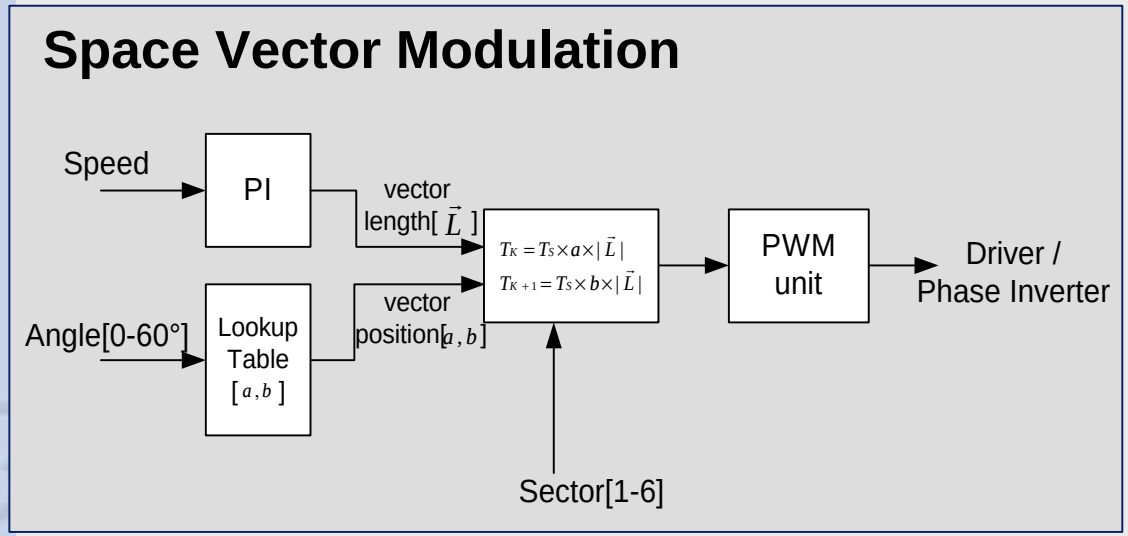
Space Vector Modulation

PWM Generation cont.



Generation of PWM output patterns with Lookup Table

Space Vector Modulation



PI-Controller:

Dependent of the measured speed the length of the vector is calculated.

Lookup Table:

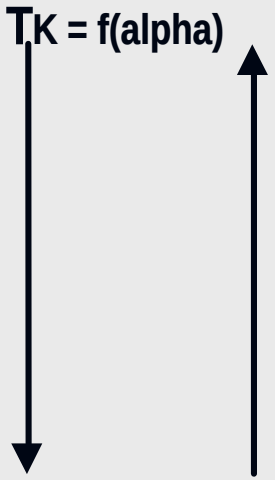
It contains for an range of 60 degree values for alpha and beta. With the length of the vector and alpha and beta Tk and Tk+1 may be calculated.

PWM unit:

These values and the information of the sector can be used to update the PWM unit and generate the output pattern for the driver.

Lookup Table

Array[240]	Degree (°)	alpha
0	0	0.866
1	0.25	
....		
119	30	0.5
.....		
238	59.75	
239	60.00	0



$$T_K = T_S \times a \times |\vec{L}|$$

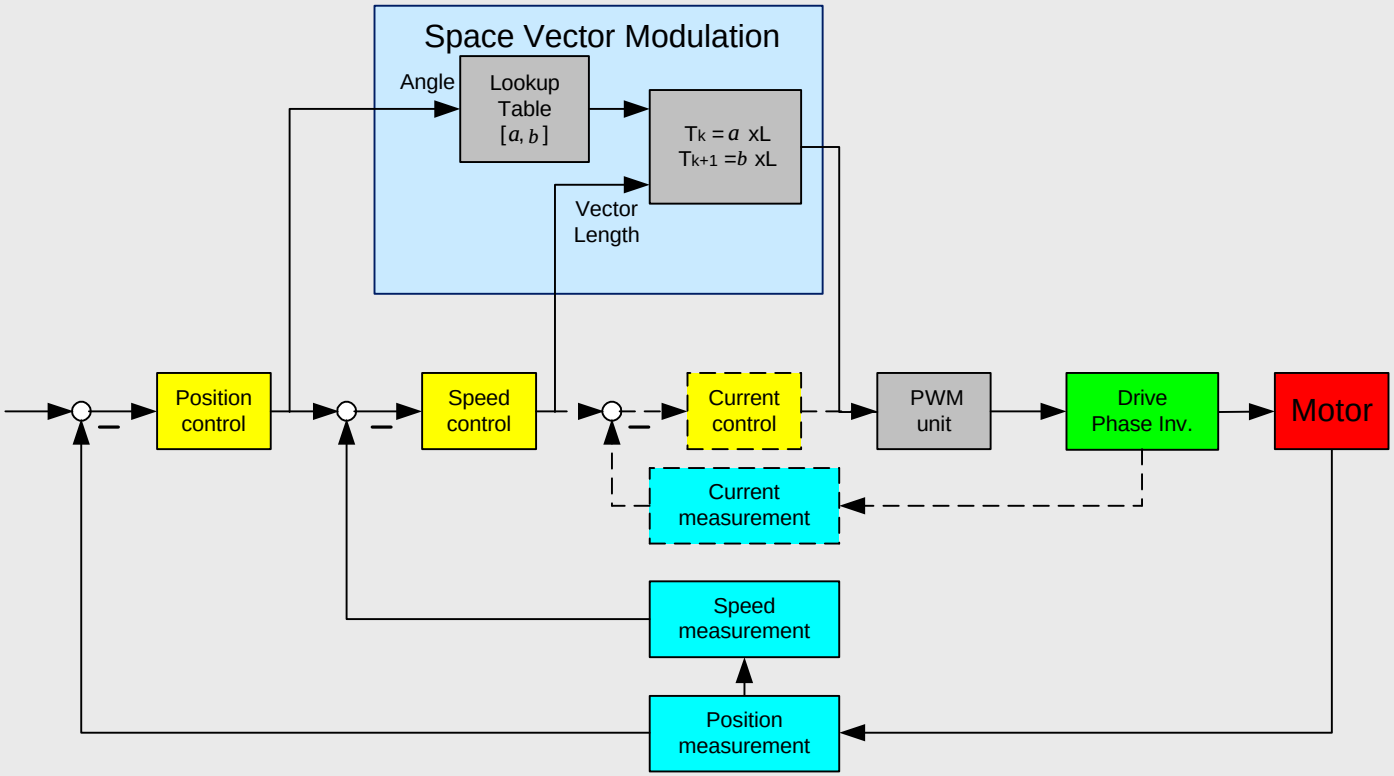
$$T_{K+1} = T_S \times (0.866 - a) \times |\vec{L}|$$

PWM output patterns (Example for 50/100 duty cycle)

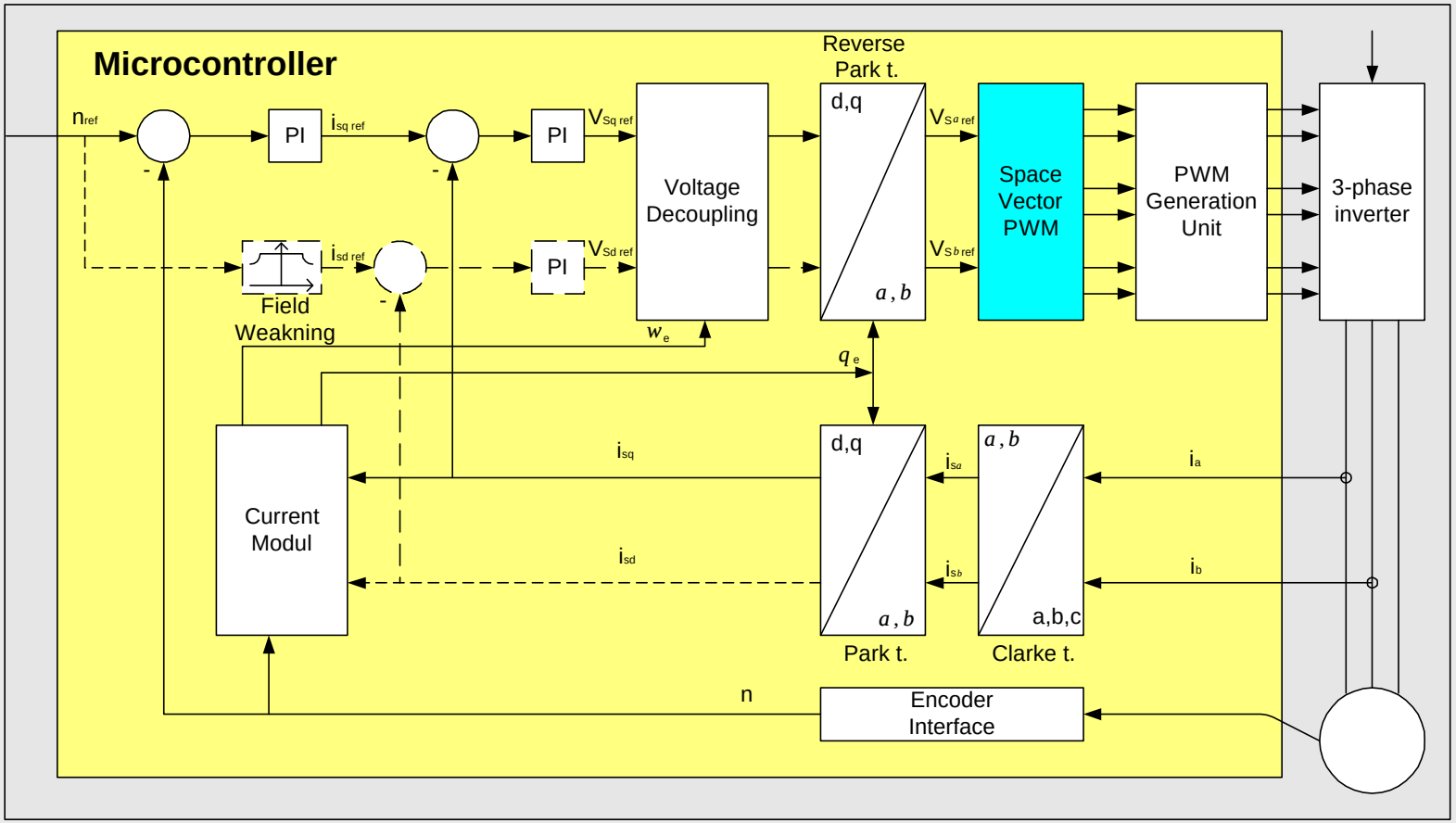
Degree(°)	TS(µs)	TK(µs)	TK+1(µs)	T0(µs)	PWM(%)	Alpha	Beta
0	50	43.30	0	6.69	100	0.866	0
10	50	38.30	8.68	3.02	100	0.766	0.174
20	50	32.14	17.10	0.76	100	0.643	0.342
30	50	25.00	25.00	0	100	0.5	0.5
40	50	17.10	32.14	0.76	100	0.342	0.643
50	50	8.68	38.30	3.02	100	0.174	0.766
60	50	0	43.30	6.69	100	0	0.866

Degree(°)	TS(µs)	TK(µs)	TK+1(µs)	T0(µs)	PWM(%)	Alpha	Beta
0	50	21.65	0	28.35	50	0.866	0
10	50	19.15	4.34	26.5	50	0.766	0.174
20	50	16.07	8.55	25.38	50	0.643	0.342
30	50	12.5	12.5	25.0	50	0.5	0.5
40	50	8.55	16.07	25.38	50	0.342	0.643
50	50	4.34	19.15	26.5	50	0.174	0.766
60	50	0	21.65	28.35	50	0	0.866

Cascaded control loop for BLDC application (Space Vector Modulation)



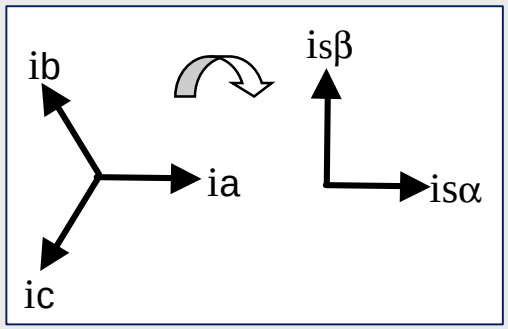
Field oriented control for synchronous 3 phase drives



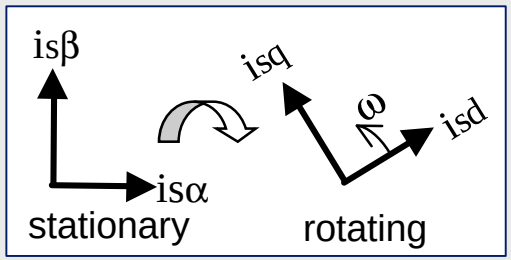
Space Vector Modulation

FOC (Field Oriented Control)

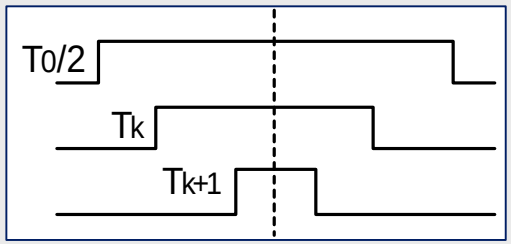
- **Clarke Transformation**



- **Park Transformation**



- **Space Vector Modulation**



→ **Higher demand on performance**

(XC16x architecture, MAC unit, single cycle CPU)

Space Vector Modulation

FOC Benchmark

- The following figures do not cover the complete control algorithms for induction drives. It should give the customer only a roughly idea about the effectiveness of the MAC unit. The values are in 16 bit integer format.
  - Clark transform: 13 cycle (325ns@40MHz)
  - Inverse Clarke transform: 16 cycle (400ns@40MHz)
  - Park transform: 37 cycle (925ns@40MHz)
  - Inverse Park transform: 31 cycle (775ns@40MHz)

→ **less than 100 cycle (2.5µs@ 40 MHz) for one transformation**

C166S-V2 CPU Architecture Overview (1)

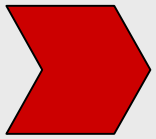
- High Performance 16-bit CPU
  - Op-code fully upward compatible with C166 family
  - 5-stage execution pipeline
  - 2-stage instruction fetch pipeline with FIFO for instruction pre-fetching
  - Single clock cycle instruction execution
  - 25 ns instruction time at 40 MHz CPU clock
  - 40 MIPS at 40 MHz CPU clock
  - Pipeline with forwarding that controls data dependencies in hardware
  - Multiple high bandwith internal busses for code and data

C166S-V2 CPU Architecture Overview (2)

- High Performance 16-bit CPU
  - Fast multiplication (16 x 16 bit), (1 cycle, 25ns @ 40MHz)
  - Fast background division (32/16-bit), (up to 21 cycle, 525ns @ 40MHz)
  - High performance branch, call and loop processing
    - Branch detection and branch prediction (JMPA, CALLA..)
    - Zero cycle jump execution
  - Built-in advanced MAC unit
    - Single cycle multiply and accumulate instruction (MAC) execution (25ns @ 40MHz)
    - DSP instruction set (CoXXX arithmetic instructions)
  - Enhanced boolean bit manipulation facilities
  - Additional Instructions to support HLL and operating systems

C166S-V2 CPU Architecture Overview (3)

- High Performance 16-bit CPU
  - Register-based design with multiple variable register banks
  - 2 additional fast register banks
    - Single-cycle context switching support
  - 16 MByte total linear address space for code and data



Approximately 1.7 to 2.x times more performance than the C166 CPU