# Intel® StrongARM* SA-1110 Microprocessor

## Specification Update

***December 2001***

**Notice:** The SA-1110 may contain design defects or errors known as errata. Characterized errata that may cause the SA-1110's behavior to deviate from published specifications are documented in this specification update.

Order Number: 278259-023

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# Revision History

| Date | Version | Description |
|---|---|---|
| 11/16/01 | 023 | Modified item 29, “USB Controller Endpoint 2 (IN) Transmits Incorrect Data” (page 31)<br>New Errata, added item 30, “SA-1110 UDC Registers can be corrupted when writing to OS Timer Match Registers (OSMR0,1,2).” (page 31), item 31, “During USB Bulk OUT transfers, DMA reads of the SA-1110 UDC Endpoint 1 input FIFO can result in the FIFO not advancing its qued data to the next positions.” (page 32), item 32, “After a USB Control read or write of the SA1110 UDC Endpoint 0 FIFO, the FIFO does not always advance its qued data to the next positions.” (page 32), item 33, “The TCP bit in SA1110 UDC Endpoint 2 (IN) Control Status Register (UDCCS2) must be cleared by software after every Bulk IN packet has been transmitted.” (page 32), item 34, “LCD Controller does not generate an interrupt when its input FIFO under-runs.” (page 32), item 35, “LCD Controller input and output FIFOs retain their respective error states even if the respective status bits are cleared in the LCD Status Register (LCSR).” (page 33), item 36, “Serial Port 2 loopback mode does not work when operating the port as IrDA-SIR or UART. IrDA-HSSP loopback mode does work.” (page 33), item 37, “Audio Transmit Data in Serial Port 4: MCP Mode can be corrupted when writing to OS Timer Count Register (OSCR) or OS Timer Match Register 0 (OSMR0).” (page 33).<br>Under Documentation Changes, removed documentation changes 1-30, 32-36, 38, 39, 41-55, 57-71, 74-88, 90-94, 96, 97, 99-103, 105-110, 112-118 (having been incorporated into revision -003 of the developer’s manual) respective to Specification Update Revisions 017 through 022.<br>Under Documentation Changes, added item 4, “Memory and PC-Card Control Module: Section 10” (page 38). |
| 4/3/01 | 022 | Under Specification Change, modified item 5, “Power Supply Voltages and Currents: Section 12.3” (page 34) to include the B5 stepping.<br>Under Documentation Changes, added item 11, “Memory Map: Section 2.4” (page 41), item 25, “Data Aborts: Section 7.3” (page 44), item 26, “GPIO Pin Output Set Register (GPSR) and Pin Output Clear Register (GPCR): Section 9.1.1.3” (page 44), item 29, “Interrupt Controller Pending Register (ICPR): Section 9.2.1.1” (page 46), item 31, “Interrupt Controller IRQ Pending Register (ICIP) and FIQ Pending Register (ICFP): Section 9.2.1.2” (page 37), item 33, “Real-Time Clock: Section 9.3” (page 48), item 35, “RTC Alarm Register (RTAR): Section 9.3.2” (page 48), item 39, “RTC Status Register (RTSR): Section 9.3.3” (page 49), item 42, “Transaction Summary: Section 10.1.5” (page 50), item 44, “MDCAS Registers with SDRAM and SMROM: Section 10.2.3.2” (page 50), item 45, “Static Memory Control Registers (MSC2 – 0): Section 10.2.4” (page 50), item 51, “DMA Device Address Register (DDARn): Section 11.6.1.1” (page 52), item 54, “DMA Control/ Status Register (DCSRn): Section 11.6.1.2” (page 54), item 56, “DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4” (page 38), item 58, “DMA Buffer B Transfer Count Register (DBTBn): Section 11.6.1.6” (page 55), item 60, “Frame Buffer: Section 11.7.1.2” (page 56), item 61, “LCD Enable (LEN): Section 11.7.3.1” (page 57), item 72, “LCD Disable Done Flag: Section 11.7.11.1” (page 38), item 73, “Base Address Update Flag: Section 11.7.11.2” (page 38), item 75, “Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12” (page 60), item 80, “Serial Port 0 – USB Device Controller: Section 11.8” (page 63), item 81, “USB Operation: Section 11.8.1” (page 64), item 82, “UDC Endpoint 2 Control/Status Register: Section 11.8.9” (page 64), item 87, “4PPM Modulation: Section 11.10.2.1” (page 65), item 88, “CPU and DMA Register Access Sizes: Secti9on 11.10.2.11” (page 65), item 90, “Low-Power Mode (LPM): Section 11.10.4.2” (page 65), item 91, “IrDA Transmission Rate (ITR): Section 11.10.6.1” (page 66), item 92, “Loopback Mode (LBM): Section 11.10.6.2” (page 66), item 93, “Transmit Enable (TXE): Section 11.10.6.4” (page 66), item 94, “Receive Pin Polarity Select (RXP): Section 11.10.8.2” (page 66), item 95, “End/Error in FIFO Status (EIF) (read-only, nonmaskable interrupt): Section 11.10.10.1” (page 38), item 96, “Framing Error Status (FRE) (read/write, nonmaskable interrupt): Section 11.10.10.6” (page 67), item 97, “CRC Error Status (CRE) (read-only, noninterruptible): Section 11.10.11.6” (page 67), 98, “Receiver Overrun Status (ROR) (read-only, noninterruptible): Section 11.10.11.7” (page 38), item 101, “UART Data Register: Section 11.11.6” (page 68), item 112, “Power Supply Voltages and Currents: Section 12.3” (page 71), item 113, “Timing Parameters: Section 13.6” (page 72), item 115, “Package and Pinout: Section 14” (page 73), and item 116, “Intel® StrongARM SA-1110 Device Identification (ID) Code Register: Section 16.6.2” (page 74). |

| Date | Version | Description |
|---|---|---|
| 2/26/01 | 021 | New Errata item 29, “USB Controller Endpoint 2 (IN) Transmits Incorrect Data” (page 31) has been added.<br>Modified the workaround for 27, “Incorrect Values Are Read from RTTR and RCNR Registers Immediately After They Are Written” (page 27).<br>Under Specification Change, added item 4, “DC Operating Conditions: Section 12.2” (page 34), and item 5, “Power Supply Voltages and Currents: Section 12.3” (page 34).<br>Under Documentation Changes, added item 10, “Data Cache: Section 1.4.5” (page 41), item 12, “Coprocessors: Section 3.3” (page 42), item 13, “Internal Coprocessor Instructions: Section 5.1” (page 42), item 14, “Register 7 – Cache Control Operations: Section 5.2.8” (page 42), item 15, “Register 9 – Read-Buffer Operations: Section 5.2.10” (page 42), item 24, “Read Buffer: Section 6.4” (page 44), item 28, “Interrupt Controller: Section 9.2” (page 45), item 30, “Interrupt Controller FIQ Pending Register (ICFP): Section 9.2.1.2” (page 46), item 32, “Interrupt Controller Control Register (ICCR): Section 9.2.1.5” (page 47), item 34, “RTC Counter Register (RCNR): Section 9.3.1” (page 48), item 36, “RTC Status Register (RTSR): Section 9.3.3” (page 49), item 36, “RTC Status Register (RTSR): Section 9.3.3” (page 46), item 37, “RTC Trim Register (RTTR): Section 9.3.4” (page 46), item 47, “SDRAM Commands: Section 10.4.4” (page 51), item 59, “Frame Buffer: Section 11.7.1.2” (page 55), item 64, “Double-Pixel Data (DPD) Pin Mode: Section 11.7.3.9” (page 58), item 77, “LCD Controller Pin Timing Diagrams: Section 11.7.13” (page 60), item 78, “LCD Controller Pin Timing Diagrams: Section 11.7.13” (page 61), item 79, “LCD Controller Pin Timing Diagrams: Section 11.7.13” (page 62), item 85, “Sample Clock Direction (SCD): Section 11.9.2.3” (page 65), item 86, “Transmit Enable (TXE): Section 11.9.3.1” (page 65), item 103, “SSP Transmit and Receive FIFOs: Section 11.12.7.3” (page 68), item 107, “PPC Pin State Register: Section 11.13.4” (page 70), item 109, “PPC Sleep Mode Pin Direction Register: Section 11.13.6” (page 70), item 110, “PPC Pin Flag Register: Section 11.13.7” (page 70), item 111, “DC Operating Conditions: Section 12.2” (page 70), item 112, “Power Supply Voltages and Currents: Section 12.3” (page 71), and item 115, “Package and Pinout: Section 14” (page 73) |
| 12/08/00 | 020 | New Errata item 28, “Incorrect Address Decode in USB Controller” (page 28) has been added.<br>Under Documentation Changes, added item 33, “Real-Time Clock: Section 9.3” (page 48), item 38, “RTC Status Register (RTSR): Section 9.3.3” (page 49), item 43, “DRAM Refresh Control Register (MDREFR): Section 10.2.2” (page 50), item 46, “SMROM Configuration Register (SMCNFG): Section 10.3” (page 51), item 49, “DMA Device Address Register (DDARn): Section 11.6.1.1” (page 51), item 50, “DMA Device Address Register (DDARn): Section 11.6.1.1” (page 52), item 52, “DMA Control/Status Register (DCSRn): Section 11.6.1.2” (page 53), item 53, “DMA Control/Status Register (DCSRn): Section 11.6.1.2” (page 53), item 55, “DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4” (page 54), item 57, “DMA Buffer B Transfer Count Register (DBTBn): Section 11.6.1.6” (page 55), item 66, “Palette DMA Request Delay (PDD): Section 11.7.3.10” (page 58), item 76, “LCD Controller Register Locations: Section 11.7.12” (page 60), item 83, “UDC Endpoint Data Register: Section 11.8.10” (page 64), item 84, “UDC Data Register: Section 11.8.12” (page 64), item 100, “UART Data Register: Section 11.11.6” (page 68), item 102, “SSP Transmit and Receive FIFOs: Section 11.12.7.3” (page 68), item 104, “SSP Data Register: Section 11.12.11” (page 68), item 105, “PPC Pin Direction Register: Section 11.13.3” (page 69), item 106, “PPC Pin State Register: Section 11.13.4” (page 69), and item 108, “PPC Pin Assignment Register: Section 11.13.5.2” (page 70). |
| 10/20/00 | 019 | New Errata item 27, “Incorrect Values Are Read from RTTR and RCNR Registers Immediately After They Are Written” (page 27) has been added.<br>New Specification Change item 3, “Modifications in SDRAM/SMROM Data Input Hold Time” (page 34) has been added.<br>Under Documentation Changes, added item 23, “Read Buffer: Section 6.4” (page 43), item 43, “DRAM Refresh Control Register (MDREFR): Section 10.2.2” (page 50), item 46, “SMROM Configuration Register (SMCNFG): Section 10.3” (page 51), item 59, “Frame Buffer: Section 11.7.1.2” (page 55), item 69, “Output Enable Polarity (OEP): Section 11.7.6.7” (page 59), item 74, “Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12” (page 60), item 76, “LCD Controller Register Locations: Section 11.7.12” (page 60), item 99, “Sample Clock GPIO: Section 11.11.3.5” (page 67), item 111, “DC Operating Conditions: Section 12.2” (page 67), item 113, “Timing Parameters: Section 13.6” (page 72), and item 118, “Boundary Scan Interface Signals: Section 16.7” (page 74). |

| Date | Version | Description |
|---|---|---|
| 9/12/00 | 018 | Under Errata item 21, “Failure of Synchronous Serial Port (SSP) Receiver Overrun Status Bit to Generate Interrupt Request” (page 26) -- the workaround instructions have been modified. In Item 24, “Software Sleep Status Bit (PSSR:SSS) May Be Improperly Set After Sleep Wakeup” (page 27) the “affected steppings” have been modified (affects all steppings). New items 25, “Improper Operation of LCD Controller LCCR2 Register EFW (End of Frame Line Clock Wait Count)” (page 27) and 26, “Between Two Successive PCMCIA Accesses, Bus Arbiter Might Not Recognize Pending, Highest-Priority, Bus Access Request From LCD Controller” (page 27) have been added.<br><br>Under Documentation Changes, removed documentation changes 1-6, 8-11, 13-20, 23-28, 30, 32, 34-36, 39-97 (having been incorporated into revision -003 of the developer’s manual) respective to Specification Update Revision 017.<br><br>Under Documentation Changes, modified documentation change 21 (respective to revision 017) by removing the description for changing ‘9 bits’ to ‘9 bytes’ as this part of the modification was already implemented in revision -003 of the developer’s manual. Modified documentation change 22 (respective to revision 017) by removing the description for changing bits 24 and 25 as this part of the modification is no longer required. The new descriptions of these changes are now documentation changes 3 and 4.<br><br>Under Documentation Changes, added item 16, “Register 14 – Debug Support (Breakpoints): Section 5.2.13” (page 42) item 17, “Data Caches (Dcaches): Section 6.2” (page 42), item 18, “Writes to a Bufferable and Noncacheable Location (B=1,C=0): Section 6.3.2.2” (page 43), item 19, “Unbufferable and Noncacheable Writes (B=0, C=0): Section 6.3.2.3” (page 43), item 20, “Writes to a Non-Bufferable and Cacheable Location (B=0, C=1): Section 6.3.2.4” (page 43), item 21, “Read Buffer (RB): Section 6.4” (page 43), item 22, “Read Buffer: Section 6.4” (page 43), item 41, “Sleep Mode: Section 9.5.3” (page 49), item 48, “8-, 16-, and 32-Bit Data Bus Operation: Section 10.6.1” (page 51), item 50, “DMA Device Address Register (DDARn): Section 11.6.1.1” (page 52), item 59, “Frame Buffer: Section 11.7.1.2” (page 55), item 62, “Passive/Active Display Select (PAS): Section 11.7.3.7” (page 57), item 63, “Passive/Active Display Select (PAS): Section 11.7.3.7” (page 57), item 65, “Palette DMA Request Delay (PDD): Section 11.7.3.10” (page 58)item 67, “Beginning-of-Frame Line Clock Wait Count (BFW): Section 11.7.5.4” (page 58), item 70, “DMA Channel 1 Current Address Register: Section 11.7.9” (page 59), item 71, “Output FIFO Underrun Lower Panel Status (OUL) (read only, maskable interrupt): Section 11.7.10” (page 59), item 74, “Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12” (page 60), item 74, “Output FIFO Underrun Upper Panel Status (OUU) (read/write, maskable interrupt): Section 11.7.11.12” (page 60), item 76, “LCD Controller Register Locations: Section 11.7.12” (page 60), item 111, “DC Operating Conditions: Section 12.2” (page 70), item 112, “Power Supply Voltages and Currents: Section 12.3” (page 71), item 113, “Timing Parameters: Section 13.6” (page 72), item 114, “Timing Parameters: Section 13.6” (page 73), item 116, “Intel® StrongARM SA-1110 Device Identification (ID) Code Register: Section 16.6.2” (page 74), and item 117, “Boundary-Scan Interface Signals: Section 16.7” (page 74). |

| Date | Version | Description |
|---|---|---|
| 6/22/00 | 017 | Under Errata, changed the No Fix setting to Fix in the Status fields of Errata 13 — 16 and 18, established errata 17 as a No Fix, as well as adding the B4 step designator to the Affected Steppings fields for all forementioned. Also added two new errata (19 and 20) describing a failure to Reset UDC IN/OUT Data Packet Toggle Generation to DATA0/1 on Endpoints 1/2. And added errata describing the failure of the SSP bit to generate an interrupt request (21), describing the failure of the LCD Controller to operate correctly following reconfiguration events (22), and describing how a misaligned word access with a 16-bit data bus can generate incorrect data (23).<br>Under Documentation Changes, added to documentation change 2 two tables to Section 13.1 describing output derating parameters for slow and fast output buffers, removed documentation changes 3—63 (having been incorporated into the revision 003 developer's manual) respective to Specification Update Revision 016. Also added updated information for the Reset Interrupt Mask, Receive Packet Error bit, Force Stall bit, and the UDC Control Register. Added information describing: Software Control of the UDC; a new section entitled "GPCLK Control Register 1"; changed section formally named "GPCLK Control Registers 1 and 2"; updated the table in the "GPCLK Register Locations" section. Made sentence corrections to the following sections: Serial Port 3 – UART; Baud Rate Divisor (BRD); Baud Rate Generation. Made general format corrections. Corrected bit assignment values to registers in Chapter 11. Rewrote sections 11.8.3, 11.8.3.4, 11.8.3.5, 11.8.3.6, 11.8.3.7, 11.8.3.3, 11.8.13.2, 11.8.13.13, 11.8.13.4, 11.8.13.5, 11.9, 9.3.4. Restructured Section 10.4.1. Added a note as appropriate in Chapters 9 and 11 to identify the use of a question mark as a value designator in register Reset fields. Added new section for GPCLK Register 1. Added new section describing software control of the UDC register. Rewrote Section 9.5.2.2, "exit Idle Mode." Added new data for the Force Stall bit.Added new output derating tables to Chapter 13. Updated GPCLK register locations table. Changed "899.78 MHz" to "900 Hz" as needed in Section 11.9. Updated section for GPCLK registers 1 and 2. Corrected baud rate divisor descriptions. Restructured Section 13.6. Corrected Figure 10-1. See Documentation Changes 41 through 97 for details. |
| 4/6/00 | 016 | Under Documentation Changes, added notes describing use definition of register reset value, listed in documentation changes 66–95. Corrected Transaction Formats figure (30) and corrected text and figure for Packet Formats (31). Added table footnote for GPIO functions and corrected USB web site listing. Corrected Figure 11-17 figure title and text located in paragraph above Figure 11-17. Corrected bit definitions for the MCCR0 register table. Corrected text in sections 11.8.3.8 and 11.8.12. Updated Table 12-3.<br>Under Errata, added 5 errata documenting register reads/writes following SDRAM/SDROM reads and sleep requests and SDRAM refresh issues. |
| 1/25/00 | 015 | Under Documentation Changes, removed documentation changes #63 — #99 (referencing the 014 specification update) from the specification update and applied them to the developer's manual; added two changes documenting a change in the exit idle mode process (Chapter 9) and a change in the register summary table (Appendix A).<br>Under Specification Changes, added one line to Specification Changes table. |
| 1/11/00 | 014 | Under Documentation Changes, added 38 documentation changes removing all references to SDLC, substituting SDLC information with GPCLK information. Made four changes substituting RDN+1 with RDF+1. Changed one line in the parameters definition list in section 10.5.8 and added one footnote for Figure 10-18. Also added GPCLKR0 register to Section 11.9.3.6.<br>Under Errata, added one errata documenting UDC work-around procedure. |
| 12/07/99 | 013 | Under Errata, added nine errata; under Documentation Changes, changed output signals listed in Table 13-2; changes made to Section 10.1.7, Section 10.2.1, Section 10.2.2, Section 10.2.3, Section 10.2.4, Section 10.2.5, Section 10.3, Section 10.4.6, Section 10.5.1, Section 10.5.11, Section 10.7, Section 10.7.1, and Section 10.7.2; changed Section 13.6.SDLC feature changed from an errata to a specification change. |
| 11/18/99 | 012 | Under Documentation Changes, changed ID code and added stepping information in section 5.2.1. |
| 11/15/99 | 011 | Under Errata, added two errata; under Documentation Changes, changed title of section 13.2. |
| 11/05/99 | 010 | Under Documentation Changes, added sentence to end of first paragraph in section 9.5.2.2. |
| 11/03/99 | 009 | Under Documentation Changes, changed signal description of GPIO pin 25 in table in section 9.1.2; added note to end of section 11.11.6; deleted note to bit 3 of the RCSR register in section 9.6.1.2; revised bit 0 description of USB Device Controller (UDC) CR register in section 11.8.3.8; replaced section 11.10.2.3; corrected typo in table 9-3 title; changed sentence in section 10.8. |

| Date | Version | Description |
|---|---|---|
| 10/08/99 | 008 | Under Errata, added one errata; under Documentation Changes, added paragraph to section 16.6.3; added boundary-scan signals and pins table 16-2. |
| 09/15/99 | 007 | Under Documentation Changes, added footnote to GPIO Alternate Functions Table in Section 9.1.2. |
| 08/19/99 | 006 | Under Documentation Changes, changed settings for serial port 2 and serial port 4 in Table 11-6. |
| 07/22/99 | 005 | Under Documentation Changes, changed code example for section 6.2.3; changed last sentence of section 9.5.3; added output signals to table 13-2. |
| 06/28/99 | 004 | Under Documentation Changes, removed section 16.8; changed Test Unit Control Register's description of bit 10; added change to Section 9.5.7.7; changed Figure 10-6; added change to section 10.5.1; added change to section 10.1; added change to section 10.2.2.and description of MDREFR:EAPD and MDREFR:KAPD bits; added step #8 to section 10.7.1; removed the SA-1110 Tool Chains and Operating Systems Table from the brief datasheet and the developer's manual; added change to section 9.5.6; added change to section 11.13.1; added change to section 11.13.6; added change to section 10.5.5. |
| 05/18/99 | 003 | Under Documentation Changes, added changes to the PPSR and PSDR register drawing graphics; added changes to the OS Timer Interrupt Enable register; added change to the Big and Little Endian DMA Transfers graphic; corrected peripheral pin assignments; changed 15 timing diagrams; changed bit 31 description in the DRAM Refresh Control Register; added changes to section 10.4.7; added changes to section 10.7.1; added changes to section 10.8. |
| 04/19/99 | 002 | Under Document Changes, added changes to section 1.1; section 9.1.2.1; section 3.1; section 10.2.4; and section 10.6. |
| 03/26/99 | 001 | This is the new specification update document. It contains all identified errata published prior to this date. |

# *Preface*

This document is an update to the specifications contained in the Affected Documents/Related Documents table below. This document is a compilation of device and documentation errata, specification clarifications and changes. It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools.

Information types defined in Nomenclature are consolidated into the specification update and are no longer published in other documents.

This document may also contain information that was not previously published.

## Affected Documents/Related Documents

| Title | Order |
|---|---|
| Intel® StrongARM* SA-1110 Microprocessor Developer's Manual | 278240-004 |

## Nomenclature

**Errata** are design defects or errors. These may cause the published (component, board, system) behavior to deviate from published specifications. Hardware and software designed to be used with any component, board, and system must consider all errata documented.

**Specification Changes** are modifications to the current published specifications. These changes will be incorporated in any new release of the specification.

**Specification Clarifications** describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in any new release of the specification.

**Documentation Changes** include typos, errors, or omissions from the current published specifications. These will be incorporated in any new release of the specification.

***Note:*** Errata remain in the specification update throughout the product's lifecycle, or until a particular stepping is no longer commercially available. Under these circumstances, errata removed from the specification update are archived and available upon request. Specification changes, specification clarifications and documentation changes are removed from the specification update when the appropriate changes are made to the appropriate product specification or user documentation (datasheets, manuals, etc.).

# *Summary Table of Changes*

The following table indicates the errata, specification changes, specification clarifications, or documentation changes which apply to the SA-1110 microprocessor. Intel may fix some of the errata in a future stepping of the component, and account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

## Codes Used in Summary Table

### Stepping

| | |
|---|---|
| X: | Errata exists in the stepping indicated. Specification Change or Clarification that applies to this stepping. |
| (No mark) or (Blank box): | This erratum is fixed in listed stepping or specification change does not apply to listed stepping. |

### Page

| | |
|---|---|
| (Page): | Page location of item in this document. |

### Status

| | |
|---|---|
| Doc: | Document change or update will be implemented. |
| Fix: | This erratum s intended to be fixed in a future step of the component. |
| Fixed: | This erratum has been previously fixed. |
| No Fix: | There are no plans to fix this erratum. |
| Eval: | Plans to fix this erratum are under evaluation. |

### Row

| | |
|---|---|
| **\|** | Change bar to left of table row indicates this erratum is either new or modified from the previous version of the document. |

# Errata (Sheet 1 of 3)

| No. | Steppings | | | | | | Page | Status | ERRATA |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | B1 | B2 | B4 | B5 | | | |
| 1 | X | X | X | X | X | X | 19 | No Fix | Incorrect Sign-Extended Value in Register After a Read Buffer Allocate |
| 2 | X | X | X | X | X | X | 19 | No Fix | LCD Ghost Lines |
| 3 | X | | | | | | 19 | Fixed | High Current on VDDX During Reset |
| 4 | X | | | | | | 19 | Fixed | High Current on VDDX During Sleep |
| 5 | X | | | | | | 19 | Fixed | LCD State Machine Throughput Fails Using SDRAM at Full-Memory Clock Frequency |
| 6 | X | | | | | | 20 | Fixed | USB Stalls When More Than One USB Client Is Present |
| 7 | X | | | | | | 20 | Fixed | SDRAM Auto-Power-Up Failure |
| 8 | X | | | | | | 20 | Fixed | SDRAM RAS Precharge Counter May Not Work in the Presence of SMROM |
| 9 | X | X | | | | | 20 | Fixed | DRAM Refresh Corrupting ROM/Flash Burst of 4/8 Timing |
| 10 | X | X | X | | | | 21 | Fixed | Data Contention Caused by Hardware, Software, or Watchdog Reset During SDRAM/SMROM Reads |
| 11 | X | X | X | | | | 22 | Fixed | Erroneous SMROM Precharge All (PALL) Command with Mode Register Set (MRS) Command After Hardware, Software, Watchdog, or Sleep Reset |
| 12 | X | X | X | | | | 22 | Fixed | UDC Not Responding to IN Packet After Receiving an SOF Packet |
| 13 | X | X | X | | | | 22 | Fixed | Corruption of Internal Register Reads/Writes Following SDRAM/SDROM Reads |
| 14 | X | X | X | X | | | 23 | Fixed | Failure on Sleep Request During Variable Latency I/O to Perform SDRAM Self-Refresh and Enter Sleep |
| 15 | X | X | X | X | | | 23 | Fixed | Failure on Sleep Request During CBR Refreshes to Perform SDRAM Self-Refresh Prior to Entering Sleep |
| 16 | | | | X | | | 24 | Fixed | Erroneous SDRAM Power-Down-Exit and Power-Down Following Self-Refresh and Sleep Entry |
| 17 | X | X | X | X | X | X | 25 | No Fix | Corruption of Internal Register Reads/Writes Following Reads from SDRAM on 16-bit Data Busses at Full Memory Clock Frequency |
| 18 | X | X | X | X | | | 25 | Fixed | Failure on Sleep Request During SDRAM Read/Write Bursts to Precharge SDRAM Row Prior to Performing SDRAM Self-Refresh and Entering Sleep |
| 19 | X | X | X | X | | | 25 | Fixed | Failure to Reset UDC OUT Data Packet Toggle Checking to DATA0 on Endpoint 1 After a Sequence of Setting/Clearing Force Stall Bit (UDCCS1:FST) and Clearing Sent Stall Bit (UDCCS1:SST) |

# Errata (Sheet 1 of 3)

| No. | Steppings | | | | | | Page | Status | ERRATA |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | B1 | B2 | B4 | B5 | | | |
| 1 | X | X | X | X | X | X | 19 | No Fix | Incorrect Sign-Extended Value in Register After a Read Buffer Allocate |
| 2 | X | X | X | X | X | X | 19 | No Fix | LCD Ghost Lines |
| 3 | X | | | | | | 19 | Fixed | High Current on VDDX During Reset |
| 4 | X | | | | | | 19 | Fixed | High Current on VDDX During Sleep |
| 5 | X | | | | | | 19 | Fixed | LCD State Machine Throughput Fails Using SDRAM at Full-Memory Clock Frequency |
| 6 | X | | | | | | 20 | Fixed | USB Stalls When More Than One USB Client Is Present |
| 7 | X | | | | | | 20 | Fixed | SDRAM Auto-Power-Up Failure |
| 8 | X | | | | | | 20 | Fixed | SDRAM RAS Precharge Counter May Not Work in the Presence of SMROM |
| 9 | X | X | | | | | 20 | Fixed | DRAM Refresh Corrupting ROM/Flash Burst of 4/8 Timing |
| 10 | X | X | X | | | | 21 | Fixed | Data Contention Caused by Hardware, Software, or Watchdog Reset During SDRAM/SMROM Reads |
| 11 | X | X | X | | | | 22 | Fixed | Erroneous SMROM Precharge All (PALL) Command with Mode Register Set (MRS) Command After Hardware, Software, Watchdog, or Sleep Reset |
| 12 | X | X | X | | | | 22 | Fixed | UDC Not Responding to IN Packet After Receiving an SOF Packet |
| 13 | X | X | X | | | | 22 | Fixed | Corruption of Internal Register Reads/Writes Following SDRAM/SDROM Reads |
| 14 | X | X | X | X | | | 23 | Fixed | Failure on Sleep Request During Variable Latency I/O to Perform SDRAM Self-Refresh and Enter Sleep |
| 15 | X | X | X | X | | | 23 | Fixed | Failure on Sleep Request During CBR Refreshes to Perform SDRAM Self-Refresh Prior to Entering Sleep |
| 16 | | | | X | | | 24 | Fixed | Erroneous SDRAM Power-Down-Exit and Power-Down Following Self-Refresh and Sleep Entry |
| 17 | X | X | X | X | X | X | 25 | No Fix | Corruption of Internal Register Reads/Writes Following Reads from SDRAM on 16-bit Data Busses at Full Memory Clock Frequency |
| 18 | X | X | X | X | | | 25 | Fixed | Failure on Sleep Request During SDRAM Read/Write Bursts to Precharge SDRAM Row Prior to Performing SDRAM Self-Refresh and Entering Sleep |
| 19 | X | X | X | X | | | 25 | Fixed | Failure to Reset UDC OUT Data Packet Toggle Checking to DATA0 on Endpoint 1 After a Sequence of Setting/Clearing Force Stall Bit (UDCCS1:FST) and Clearing Sent Stall Bit (UDCCS1:SST) |

# Errata (Sheet 2 of 3)

| No. | Steppings | | | | | | Page | Status | ERRATA |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | B1 | B2 | B4 | B5 | | | |
| 20 | X | X | X | X | | | 26 | Fixed | Failure to Reset UDC IN Data Packet Toggle Generation to DATA0 on Endpoint 2 After a Sequence of Setting/Clearing Force Stall Bit (UDCCS2:FST) and Clearing Sent Stall Bit (UDCCS2:SST) |
| 21 | X | X | X | X | X | X | 26 | Eval | Failure of Synchronous Serial Port (SSP) Receiver Overrun Status Bit to Generate Interrupt Request |
| 22 | X | X | X | X | X | X | 26 | No Fix | LCD Controller Fails to Operate Correctly Following Reconfiguration |
| 23 | X | X | X | X | X | X | 26 | No Fix | Misaligned Word Accesses with 16-Bit Data Bus May Produce Incorrect Data |
| 24 | X | X | X | X | X | X | 27 | No Fix | Software Sleep Status Bit (PSSR:SSS) May Be Improperly Set After Sleep Wakeup |
| 25 | X | X | X | X | X | X | 27 | No Fix | Improper Operation of LCD Controller LCCR2 Register EFW (End of Frame Line Clock Wait Count) |
| 26 | X | X | X | X | X | X | 27 | No Fix | Between Two Successive PCMCIA Accesses, Bus Arbiter Might Not Recognize Pending, Highest-Priority, Bus Access Request From LCD Controller |
| 27 | X | X | X | X | X | X | 27 | No Fix | Incorrect Values Are Read from RTTR and RCNR Registers Immediately After They Are Written |
| 28 | X | X | X | X | X | | 28 | Fixed | Incorrect Address Decode in USB Controller |
| 29 | X | X | X | X | X | | 31 | Fixed | USB Controller Endpoint 2 (IN) Transmits Incorrect Data |
| 30 | X | X | X | X | X | X | 31 | No Fix | SA-1110 UDC Registers can be corrupted when writing to OS Timer Match Registers (OSMR0,1,2). |
| 31 | X | X | X | X | X | X | 32 | No Fix | During USB Bulk OUT transfers, DMA reads of the SA-1110 UDC Endpoint 1 input FIFO can result in the FIFO not advancing its qued data to the next positions. |
| 32 | X | X | X | X | X | X | 32 | No Fix | After a USB Control read or write of the SA1110 UDC Endpoint 0 FIFO, the FIFO does not always advance its qued data to the next positions. |
| 33 | X | X | X | X | X | X | 32 | No Fix | The TCP bit in SA1110 UDC Endpoint 2 (IN) Control Status Register (UDCCS2) must be cleared by software after every Bulk IN packet has been transmitted. |
| 34 | X | X | X | X | X | X | 31 | No Fix | LCD Controller does not generate an interrupt when its input FIFO under-runs. |

## Errata (Sheet 3 of 3)

| No. | Steppings | | | | | | Page | Status | ERRATA |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | B1 | B2 | B4 | B5 | | | |
| 35 | X | X | X | X | X | X | 31 | No Fix | LCD Controller input and output FIFOs retain their respective error states even if the respective status bits are cleared in the LCD Status Register (LCSR). |
| 36 | X | X | X | X | X | X | 31 | No Fix | Serial Port 2 loopback mode does not work when operating the port as IrDA-SIR or UART. IrDA-HSSP loopback mode does work. |
| 37 | X | X | X | X | X | X | 31 | No Fix | Audio Transmit Data in Serial Port 4: MCP Mode can be corrupted when writing to OS Timer Count Register (OSCR) or OS Timer Match Register 0 (OSMR0). |

## Specification Changes

| No. | Steppings | | | | | | Page | Status | Specification Changes |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | B1 | B2 | B4 | B5 | | | |
| 1 | X | X | X | X | X | X | 34 | Eval | SDLC Feature |
| 2 | X | X | X | X | X | X | 34 | No Fix | SDLC Feature Not Supported |
| 3 | X | X | X | X | X | X | 34 | No Fix | Modifications in SDRAM/SMROM Data Input Hold Time |
| 4 | X | X | X | X | X | X | 34 | No Fix | DC Operating Conditions: Section 12.2 |
| 5 | X | X | X | X | X | X | 34 | No Fix | Power Supply Voltages and Currents: Section 12.3 |

## Specification Clarifications

| No. | Steppings | | | | | | Page | Status | Specification Clarifications |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | B1 | B2 | B4 | B5 | | | |
| | | | | | | | | | None for this revision of this specification update. |

## Documentation Changes (Sheet 1 of 2)

| No. | Document Revision | Page | Status | Documentation Changes |
|---|---|---|---|---|
| 1 | 278240-004 | 37 | Doc | Interrupt Controller IRQ Pending Register (ICIP) and FIQ Pending Register (ICFP): Section 9.2.1.2 |
| 2 | 278240-004 | 37 | Doc | RTC Status Register (RTSR): Section 9.3.3 |
| 3 | 278240-004 | 37 | Doc | RTC Trim Register (RTTR): Section 9.3.4 |
| 4 | 278240-004 | 38 | Doc | Memory and PC-Card Control Module: Section 10 |
| 5 | 278240-004 | 39 | Doc | DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4 |

# Documentation Changes (Sheet 2 of 2)

| No. | Document Revision | Page | Status | Documentation Changes |
|---|---|---|---|---|
| 6 | 278240-004 | 39 | Doc | LCD Disable Done Flag: Section 11.7.11.1 |
| 7 | 278240-004 | 39 | Doc | Base Address Update Flag: Section 11.7.11.2 |
| 8 | 278240-004 | 39 | Doc | HP-SIR * Enable (HSE): Section 11.10.4.1 |
| 9 | 278240-004 | 39 | Doc | End/Error in FIFO Status (EIF) (read-only, nonmaskable interrupt): Section 11.10.10.1 |
| 10 | 278240-004 | 39 | Doc | Receiver Overrun Status (ROR) (read-only, noninterruptible): Section 11.10.11.7 |
| 11 | 278240-004 | 39 | Doc | SSP Data Register: Section 11.12.11 |
| 12 | 278240-004 | 40 | Doc | DC Operating Conditions: Section 12.2 |

# *Identification Information*

## Markings

| Package Markings | Voltage (V) | Package Type | Speed (MHz) | Stepping[2] |
|---|---|---|---|---|
| SL3Z4 (MM#827856)[1] | 1.55 | 256PBGA | 133 | B1 |
| SL3Z5 (MM#827859)[1] | 1.75 | 256PBGA | 206 | B1 |
| GDS1110AB[1] | 1.55 | 256PBGA | 133 | B2 |
| GDS1110BB[1] | 1.75 | 256PBGA | 206 | B2 |
| GDS1110AC | 1.55 | 256PBGA | 133 | B4 |
| GDS1110BC | 1.75 | 256PBGA | 206 | B4 |
| GDS1110AD | 1.55 | 256PBGA | 133 | B5 |
| GDS1110BD | 1.75 | 256PBGA | 206 | B5 |

**NOTES:**
1. This device can no longer be ordered.
2. This value may be read from the ID register Register 0

# Errata

## 1. Incorrect Sign-Extended Value in Register After a Read Buffer Allocate

**Problem:** After a read buffer allocate, a Load Register Signed Halfword (LDRSH) or a Load Register Signed Byte (LDRSB) will not return the correct value in the register, due to long propagation delays in the sign extend logic.

**Affected Step:** A0, B0, B1, B2, B4, and B5

**Workaround:** Execute the command twice and the data is guaranteed to be correctly sign-extended for the second read.

**Status:** No Fix

## 2. LCD Ghost Lines

**Problem:** The SA-1110 LCD when driving a color passive display has diagonal ghost lines and flicker. These ghost lines are image dependent and are more evident with intensities 3 and 11.

**Affected Step:** A0, B0, B1, B2, B4, and B5

**Workaround:** None. There is a marked improvement by setting bits 11:10 in LCD Control Register 0 (Address 0h B010 0000) to 0x8. The actual setting of bits 11:10 should be experimented with to determine the best LCD performance.

**Status:** No Fix

## 3. High Current on VDDX During Reset

**Problem:** The SA-1110 exhibits high VDDX current under the scenario of power-on reset and hardware reset with subsequent VDD failure.

**Affected Step:** A0

**Workaround:** Use external logic to ensure that VDD powers up with VDDX and cannot be held low when hardware reset is asserted. In a typical application, this would require that VDD be enabled if either PWR_EN = 1 or nRESET = 0.

**Status:** Fixed

## 4. High Current on VDDX During Sleep

**Problem:** The SA-1110 exhibits high VDDX current (2.5 mA) during sleep.

**Affected Step:** A0

**Workaround:** None identified.

**Status:** Fixed

## 5. LCD State Machine Throughput Fails Using SDRAM at Full-Memory Clock Frequency

**Problem:** The LCD controller fails when the frame buffer is read from SDRAM that does burst transfers at the full-memory clock frequency (one-half CPU frequency). When using other memory types, which cannot burst at full-memory clock frequency, or using SDRAM at half-memory clock frequency (one-fourth CPU frequency), the LCD controller works correctly.

**Affected Step:** A0

**Workaround:** Set up SDRAM used for the LCD frame buffer to run at half-memory clock frequency.

**Status:** Fixed

### 6. USB Stalls When More Than One USB Client Is Present

**Problem:** When multiple USB clients are present, the USB stalls after the master completes a transmission to another device. The USB does not respond when the master addresses it.

**Affected Step:** A0

**Workaround:** Do not allow multiple clients on the USB bus.

**Status:** Fixed

### 7. SDRAM Auto-Power-Up Failure

**Problem:** If the memory controller is configured to allow SDRAM auto-power-down of minimum possible duration (SDCKE 1 low for exactly one and one-half memory clocks), the subsequent auto-power-up (SDCKE 1 goes high and appropriate SDCLK 2:1 starts running) may not work correctly.

**Affected Step:** A0

**Workaround:** For SDRAM transfers, increase RAS precharge time (MDCNFG:TRP2 or MDCNFG:TRP0) to be greater than or equal to 5. This forces the first SDRAM transfer following auto-power-up to be delayed, such that SDCKE 1 can be sampled high upon a rising edge of SDCLK 2:1 prior to sampling the next ACT command.

**Status:** Fixed

### 8. SDRAM RAS Precharge Counter May Not Work in the Presence of SMROM

**Problem:** Because SMROM does not require the use of the SA-1110's counter for minimum SDRAM RAS precharge time, this counter is overridden during SMROM transfers. The override logic does not consistently use upper address bits to distinguish between SDRAM and SMROM. Therefore, when like-numbered SMROM and SDRAM chip selects (for example, nCS 0 and nRAS/nSDCS 0) are enabled, the RAS precharge counter may not work for those SDRAM chip selects.

**Affected Step:** A0

**Workaround:** Avoid enabling like-numbered chip selects for SMROM and SDRAM. For example, enable SMROM only on nCS 1:0 and SDRAM only on nRAS/nSDCS 3:2.

**Status:** Fixed

### 9. DRAM Refresh Corrupting ROM/Flash Burst of 4/8 Timing

**Problem:** Asynchronous DRAM and SDRAM refreshes are allowed to interrupt burst transfers to any static, asynchronous memory type (ROM, SRAM, VLIO, or Flash) between 32-bit transfers. This works properly when any of those memory types are configured for non-burst timings (MCSx:RTx = 0 or 1). But when ROM/Flash is configured for burst timings (MSCx:RTx = 2 or 3), burst-of-4/8 aligned addresses may erroneously use the burst access time (MCSx:RDNx) rather than the intended non-burst access time (MSCx:RDFx). This happens when the refresh request (internally generated) occurs just prior to a burst-of-4/8 unaligned address. The problem affects burst-of-4 timings on either 16-bit or 32-bit data busses, or burst-of-8 timings on 16-bit busses.

**Affected Step:** A0 and B0

**Workaround:** Use non-burst timing (MSCx:RTx = 0) for ROM/Flash.

**Status:** Fixed

## 10. Data Contention Caused by Hardware, Software, or Watchdog Reset During SDRAM/SMROM Reads

**Problem:** If a SA-1110 hardware, software, or watchdog reset occurs while SDRAM/SMROM is executing a read command, the SA-1110 de-asserts all control pins: SDCKE 1:0, SDCLK 2:0, nCS 3:0, nRAS/ nSDCS 3:0, nSDRAS, nSDCAS, nWE, nOE, and nCAS/DQM 3:0. This correctly prevents new commands from being started. But, because SDCKE 1:0 and SDCLK 2:0 are de-asserted within a few cycles of the last read command, that read may not complete. Instead, SDRAM/SMROM may continue to drive D 31:0 during reset assertion and after reset de-assertion: until a few cycles after SDCKE 1:0 and SDCLK 2:0 are asserted again and the final read data is driven. This continuous D 31:0 drive by SDRAM/SMROM may contend with read data from other memory devices or write data from the SA-1110 itself.

**Affected Step:** A0, B0, and B1

**Workarounds (2) for Hardware Reset:** Use the following workarounds for a hardware reset:

1. Do not use hardware reset after the initial power-on hardware reset.
2. During each assertion of the SA-1110's hardware reset pin (nRESET=0), temporarily remove power from SDRAM/SMROM VDD and VDDQ pins.

**Workaround for Software Reset:** Prior to executing a software reset, all outstanding SDRAM and SMROM transfers must be allowed to complete and the banks must be disabled via writes to the MDCNFG and SMCNFG registers.

1. If burst reads from SMROM are not already enabled, enable them without changing the number of row address bits, CAS latency, or RAS latency.
   a. Write MDCAS00, MDCAS01, and MDCAS02 with their present number of leads 1's, but filled through the 96th bit with the 2-bit repeating pattern of 0 followed by 1 (see Section 10.2.3.2 for explanation).
   b. Force a mode register set (MRS) command by writing SMCNFG with its present value. The MRS configures the SMROMs' internal mode registers for a burst length of eight.
2. If the instruction cache is not already enabled, enable it by setting bit 12 of the coprocessor 15 control register (see Chapter 5 and Chapter 6). This causes subsequent fetches to be performed as 8-word bursts.
3. Align the store instruction which alters SMCNFG to an 8-word address boundary. Locate the store instructions that alter MDCNFG and RSRR at the subsequent two addresses. Aligning these three instructions to the start of a cache line ensures that they are fetched together and executed prior to any other SMROM read.

**Workaround for Watchdog Reset:** Do not use watchdog reset. The combination of watchdog interrupt and software reset may be used instead of watchdog reset.

**Status:** Fixed

### 11. Erroneous SMROM Precharge All (PALL) Command with Mode Register Set (MRS) Command After Hardware, Software, Watchdog, or Sleep Reset

**Problem:** After any type of reset (hardware, software, watchdog, or sleep), an SMROM mode register set (MRS) command may be followed in less than three SDCLK cycles by an unnecessary SMROM precharge all (PALL) command. According to SMROM specifications, a minimum of three cycles is required between issue of MRS and any subsequent command. Issue of the unnecessary PALL command is dependent upon the precise timing of reset within the SDCLK cycle, and upon use of MDREFR:K0DB2=1.

**Affected Step:** A0, B0, and B1

**Workaround:** Confirm that SMROM are insensitive to the issue of unnecessary PALL commands that follow MRS commands by less than three SDCLK cycles.

**Status:** Fixed

### 12. UDC Not Responding to IN Packet After Receiving an SOF Packet

**Problem:** The host requests data from the UDC by sending an IN packet to Endpoint 2. The UDC must respond with a NAK signal if it does not currently have any data stored in the FIFO. Sporadically, the UDC does not respond with a NAK signal after an SOF packet is received.

**Affected Step:** A0, B0, and B1

**Workaround:** Connect a USB hub between the UDC and the host system.

**Status:** Fixed

### 13. Corruption of Internal Register Reads/Writes Following SDRAM/SDROM Reads

**Problem:** Reads and writes, from and to internal registers other than memory controller registers, can be corrupted if they immediately follow reads from SDRAM or SMROM, shown as follows:

1. Register reads immediately following reads from SDRAM on 16-bit data busses (MDCNFG:DWIDn=1), with SDCLK running at full memory clock frequency (MDREFR:KnDB2=0), and using delayed data latching.
2. Register reads/writes immediately following reads from SDRAM or SMROM on 32-bit data busses (MDCNFG:DWIDn=0), with SDCLK running at full memory clock frequency (MDREFR:KnDB2=0), and using non-delayed data latching*.

***Note:*** See Section 10.2.3.2 of SA-1110 Developer's Manual for a description of delayed and non-delayed data latching. Delayed data latching must be used at high core clock frequencies (e.g.- 206MHz) and non-delayed data latching must be used at low core clock frequencies (e.g.- 100MHz).

**Affected Step:** A0, B0, and B1

**Workaround:** The following workaround applies:

1. For SDRAM on 16-bit data busses, use SDCLK running at half memory clock frequency (MDREFR:KnDB2=1)
2. For SDRAM or SMROM on 32-bit data busses, use either:
   - — a higher core clock frequency and delayed data latching, or;
   - — set the SDCLK to run at half memory clock frequency (MDREFR:KnDB2=1).

**Status:** Fixed

## 14. Failure on Sleep Request During Variable Latency I/O to Perform SDRAM Self-Refresh and Enter Sleep

**Problem:** If the memory controller receives a request to enter sleep mode during a variable latency I/O (VLIO) transfer, the SA-1110 may fail to put SDRAM into self-refresh (with SLFRSH command) and fail to enter sleep mode. In this case the corresponding VLIO chip select (nCS[3, 4, or 5]) and byte enables (nCAS/DQM[3:0]) may remain asserted indefinitely. This problem applies to sleep entry requests initiated by either software or a power supply fault.

**Affected Step:** A0, B0, B1, B2, Fixed on B4

**Workaround:** Initiate SDRAM self-refresh and sleep mode only by software, not BATT_FAULT=1 or VDD_FAULT=1 power supply fault. Prior to entering sleep disable CBR refresh, force all SDRAM into self-refresh, disable all SDRAM banks, clear self-refresh, and clear SDRAM clock enable. The following software sequence must be fully contained in the instruction cache before execution. Also, all sources of interrupt and DMA activity must be stopped before execution of the software sequence. After step 5 of this sequence is complete, BATT_FAULT=1 or VDD_FAULT=1 may be used to enter sleep (instead of step 6) and/or subsequently to maintain sleep mode.

1. Write Static Memory Control Register(s) to clear the RT field(s) (MSCx:RT = 0) for any bank(s) that were configured for VLIO.
2. Write the DRAM Refresh Control Register to clear the DRI field (MDREFR[15:4]=0), while maintaining all other bits at their current values.
3. Write the DRAM Refresh Control Register to set the SLFRSH bit (MDREFR[31] = 1), while maintaining all other bits at their current values.
4. Write the DRAM Configuration Register to clear the DE bits (MDCNFG[17,16,1,0] = 0): any or all other MDCNFG bits may also be cleared.
5. Write the DRAM Refresh Control Register to clear the SLFRSH bit (MDREFR[31] = 0), and clear the E1PIN bit (MDREFR[20] = 0), while maintaining all other bits at their current values
6. Write the Power Manager Control Register to set the SF bit (PMCR[0]=1).

**Status:** Fixed

## 15. Failure on Sleep Request During CBR Refreshes to Perform SDRAM Self-Refresh Prior to Entering Sleep

**Problem:** When the memory controller receives a request to enter sleep mode during a SDRAM/DRAM CBR refresh, the SA-1110 may fail to put SDRAM into self-refresh (with SLFRSH command) prior to entering sleep mode. Sleep mode is entered. This problem applies to sleep entry requests initiated by either software or a power supply fault.

**Affected Step:** A0, B0, B1, B2, Fixed on B4

**Workaround:** Initiate SDRAM self-refresh and sleep mode only by software, not BATT_FAULT=1 or VDD_FAULT=1 power supply fault. Prior to entering sleep disable CBR refresh, force all SDRAM into self-refresh, disable all SDRAM banks, clear self-refresh, and clear SDRAM clock enable. The following software sequence must be fully contained in the instruction cache before execution. Also, all sources of interrupt and DMA activity must be stopped before execution of the software sequence. After step 5 of this sequence is complete, BATT_FAULT=1 or VDD_FAULT=1 may be used to enter sleep (instead of step 6) and/or subsequently to maintain sleep mode.

1. Write Static Memory Control Register(s) to clear the RT field(s) (MSCx:RT = 0) for any bank(s) that were configured for VLIO.

2. Write the DRAM Refresh Control Register to clear the DRI field (MDREFR[15:4]=0), while maintaining all other bits at their current values.
3. Write the DRAM Refresh Control Register to set the SLFRSH bit (MDREFR[31] = 1), while maintaining all other bits at their current values.
4. Write the DRAM Configuration Register to clear the DE bits (MDCNFG[17,16,1,0] = 0): any or all other MDCNFG bits may also be cleared.
5. Write the DRAM Refresh Control Register to clear the SLFRSH bit (MDREFR[31] = 0), and clear the E1PIN bit (MDREFR[20] = 0), while maintaining all other bits at their current values
6. Write the Power Manager Control Register to set the SF bit (PMCR[0]=1).

**Status:** Fixed

## 16. Erroneous SDRAM Power-Down-Exit and Power-Down Following Self-Refresh and Sleep Entry

**Problem:** If the memory controller receives a request to enter sleep mode while any SDRAM banks are enabled, and SDRAM are properly put into self-refresh (with SLFRSH command), and sleep mode is properly entered, the SA-1110 may subsequently perform erroneous SDRAM Power-Down-Exit (PWRDNX) and Power-Down (PWRDN) commands. The PWRDNX command erroneously takes SDRAM out of self-refresh. The PWRDN command returns SDRAM to a low power state, but leaves it without CBR or self-refresh throughout sleep. This problem applies to sleep entry requests initiated by either software or a power supply fault.

**Affected Step:** B2, Fixed on B4

**Workaround:** Initiate SDRAM self-refresh and sleep mode only by software, not BATT_FAULT=1 or VDD_FAULT=1 power supply fault. Prior to entering sleep disable CBR refresh, force all SDRAM into self-refresh, disable all SDRAM banks, clear self-refresh, and clear SDRAM clock enable. The following software sequence must be fully contained in the instruction cache before execution. Also, all sources of interrupt and DMA activity must be stopped before execution of the software sequence. After step 5 of this sequence is complete, BATT_FAULT=1 or VDD_FAULT=1 may be used to enter sleep (instead of step 6) and/or subsequently to maintain sleep mode.

1. Write Static Memory Control Register(s) to clear the RT field(s) (MSCx:RT = 0) for any bank(s) that were configured for VLIO.
2. Write the DRAM Refresh Control Register to clear the DRI field (MDREFR[15:4]=0), while maintaining all other bits at their current values.
3. Write the DRAM Refresh Control Register to set the SLFRSH bit (MDREFR[31] = 1), while maintaining all other bits at their current values.
4. Write the DRAM Configuration Register to clear the DE bits (MDCNFG[17,16,1,0] = 0): any or all other MDCNFG bits may also be cleared.
5. Write the DRAM Refresh Control Register to clear the SLFRSH bit (MDREFR[31] = 0), and clear the E1PIN bit (MDREFR[20] = 0), while maintaining all other bits at their current values.
6. Write the Power Manager Control Register to set the SF bit (PMCR[0]=1).

**Status:** Fixed

### 17. Corruption of Internal Register Reads/Writes Following Reads from SDRAM on 16-bit Data Busses at Full Memory Clock Frequency

**Problem:** If a read from SDRAM on a 16-bit data bus (MDCNFG:DWID0=1 or MDCNFG:DWID2=1) running at full memory clock frequency (MDREFR:K1DB2=0 or MDREFR:K2DB2=0, respectively) is immediately followed by a core read/write from/to an internal register other than memory controller registers, the register read/write data may be corrupted.

**Affected Step:** A0, B0, B1, B2, B4, and B5

**Workaround:** Configure all SDRAM for 32-bit data busses (MDCNFG:DWID0=MDCNFG:DWID2=0) or configure all SDRAM to run at half-memory clock frequency (MDREFR:K1DB2=MDREFR:K2DB2=1).

**Status:** No Fix

### 18. Failure on Sleep Request During SDRAM Read/Write Bursts to Precharge SDRAM Row Prior to Performing SDRAM Self-Refresh and Entering Sleep

**Problem:** When the memory controller receives a request to enter sleep mode during a burst read or write with SDRAM, the SA-1110 may fail to precharge the currently active SDRAM row prior to putting SDRAM into self-refresh (with SLFRSH command) and entering sleep mode. Because it is an illegal SDRAM operation to attempt self-refresh while a row is active, the resulting SDRAM behavior is indeterminate. However, the SA-1110 enters sleep mode. This problem applies to sleep entry requests initiated by either software or a power supply fault.

**Affected Step:** A0, B0, B1, B2, Fixed on B4

**Workaround:** Initiate SDRAM self-refresh and sleep mode only by software, not BATT_FAULT=1 or VDD_FAULT=1 power supply fault. Prior to entering sleep disable CBR refresh, force all SDRAM into self-refresh, disable all SDRAM banks, clear self-refresh, and clear SDRAM clock enable. The following software sequence must be fully contained in the instruction cache before execution. Also, all sources of interrupt and DMA activity must be stopped before execution of the software sequence. After step 5 of this sequence is complete, BATT_FAULT=1 or VDD_FAULT=1 may be used to enter sleep (instead of step 6) and/or subsequently to maintain sleep mode.

1. Write Static Memory Control Register(s) to clear the RT field(s) (MSCx:RT = 0) for any bank(s) that were configured for VLIO.
2. Write the DRAM Refresh Control Register to clear the DRI field (MDREFR[15:4]=0), while maintaining all other bits at their current values.
3. Write the DRAM Refresh Control Register to set the SLFRSH bit (MDREFR[31] = 1), while maintaining all other bits at their current values.
4. Write the DRAM Configuration Register to clear the DE bits (MDCNFG[17,16,1,0] = 0): any or all other MDCNFG bits may also be cleared.
5. Write the DRAM Refresh Control Register to clear the SLFRSH bit (MDREFR[31] = 0), and clear the E1PIN bit (MDREFR[20] = 0), while maintaining all other bits at their current values
6. Write the Power Manager Control Register to set the SF bit (PMCR[0]=1).

**Status:** Fixed

### 19. Failure to Reset UDC OUT Data Packet Toggle Checking to DATA0 on Endpoint 1 After a Sequence of Setting/Clearing Force Stall Bit (UDCCS1:FST) and Clearing Sent Stall Bit (UDCCS1:SST)

**Problem:** When the UDC receives a command from the host (for example the ClearFeature(HALT) command) which requires the endpoint to reset its data packet toggle flag to DATA0 so that when

the host sends the next data packet to Endpoint 1, the UDC should expect the data packet to be of type DATA0. The UDC fails to reset its data packet toggle flag to DATA0 (and actually leaves it in its current state) after executing the proper sequence of setting the Force Stall Bit (UDCCS1:FST), clearing the Force Stall Bit, and then clearing the Sent Stall Bit (UDCCS1:SST).

**Affected Step:** A0, B0, B1, B2, Fixed on B4

**Workaround:** None.

**Status:** Fixed

### 20. Failure to Reset UDC IN Data Packet Toggle Generation to DATA0 on Endpoint 2 After a Sequence of Setting/Clearing Force Stall Bit (UDCCS2:FST) and Clearing Sent Stall Bit (UDCCS2:SST)

**Problem:** When the UDC receives a command from the host (for example the ClearFeature(HALT) command), it requires the endpoint to reset its data packet toggle flag to DATA0. Therefore, the next data packet sent from Endpoint 2 to the host, must be of type DATA0. The UDC fails to reset its data packet toggle flag to DATA0 (and actually sets it to DATA1) after executing the proper sequence of setting the Force Stall Bit (UDCCS2:FST), clearing the Force Stall Bit, and then clearing the Sent Stall Bit (UDCCS2:SST).

**Affected Step:** A0, B0, B1, Fixed on B4

**Workaround:** None.

**Status:** Fixed

### 21. Failure of Synchronous Serial Port (SSP) Receiver Overrun Status Bit to Generate Interrupt Request

**Problem:** Non-maskable interrupt is not generated when the Receiver Overrun (ROR) status bit is set in the SSP status register. In addition, the ROR bit is set when data is placed in the ninth entry of the 12-entry receive FIFO.

**Affected Step:** A0, B0, B1, B2, B4, and B5

**Workaround:** The SSP Status Register ROR bit can be polled to determine if a receiver overrun has occurred. Software must detect if there was missing data due to an overrun. This can be accomplished by methods such as counting data packets, or adding a CRC packet, or implementing a checksum algorithm.

**Status:** Eval

### 22. LCD Controller Fails to Operate Correctly Following Reconfiguration

**Problem:** If the LCD Controller is configured and enabled following a reset event, and is subsequently disabled and reconfigured for different display characteristics, unpredictable behavior may result when the LCD controller is re-enabled.

**Affected Step:** A0, B0, B1, B2, B4, and B5

**Workaround:** Configure and enable the LCD Controller only one time after a reset event.

**Status:** No Fix

### 23. Misaligned Word Accesses with 16-Bit Data Bus May Produce Incorrect Data

**Problem:** If a misaligned word (32-bit) access is attempted with the data bus configured for 16-bit operation, address bus bit 1 does not toggle as required to support the access. Additionally, the data bytes being transferred may be erroneously swapped.

**Affected Step:** A0, B0, B1, B2, B4, and B5

**Workaround:** Do not configure SA-1110 for operation with 16-bit data bus.

**Status:** No Fix

### 24. Software Sleep Status Bit (PSSR:SSS) May Be Improperly Set After Sleep Wakeup

**Problem:** The software sleep status bit (PSSR:SSS) may inadvertently be set after sleep wakeup, even though the part was not put into sleep mode by setting the force sleep (PMCR:SF) bit.

**Affected Step:** A0, B0, B1, B2, B4, and B5

**Workaround:** Use a bit in the PWER registers as a substitute for the PSSR:SSS bit. You must choose a bit in PWER that corresponds to a bit set as an output in the GPDR in the application system. For example, if you use bit 5 of PWER as a flag to indicate whether the part went to sleep via software or hardware, then define PWER[5]=1 to mean that the part went to sleep via software. If you boot from a hard reset (RCSR:HWR = 1), ignore PWER[5]. When you are going to sleep via software, then the last thing to do before setting PMCR:SF bit, is to set PWER[5]=1. When the part wakes up, if RCSR:SMR bit is set (sleep mode reset), then read the PWER[5] bit to see if it was in sleep due to software (= 1) or not (= 0). This bit in the PWER register is now a substitute for the PSSR:SSS bit.

**Status:** No Fix

### 25. Improper Operation of LCD Controller LCCR2 Register EFW (End of Frame Line Clock Wait Count)

**Problem:** When the SA-1110's LCCR2: EFW (End of Frame Line Clock Wait Count) is **not** zero, LCCR1: ELW (End of Line Pixel Clock Wait Count) is mistakenly loaded into the End of Frame Wait Counter.

**Affected Step:** A0, B0, B1, B2, B4, and B5

**Workaround:** Always program LCCR2: EFW to zero. Use LCCR2: BFW (Beginning of Frame Line Clock Wait Count) to delay the next frame.

**Status:** Eval

### 26. Between Two Successive PCMCIA Accesses, Bus Arbiter Might Not Recognize Pending, Highest-Priority, Bus Access Request From LCD Controller

**Problem:** Between two successive accesses to the SA-1110's PCMCIA Interface, the Bus Arbiter might not recognize a pending, highest-priority request from the LCD Controller and, therefore, the LCD Controller is not granted bus access as it should be.

**Affected Step:** A0, B0, B1, B2, B4, and B5

**Workaround:** To unlock the Bus Arbiter, follow the PCMCIA access with a “dummy” store-to or load-from uncached/unbuffered memory space.

**Status:** Eval

### 27. Incorrect Values Are Read from RTTR and RCNR Registers Immediately After They Are Written

**Problem:** A read back of the RTTR or RCNR register immediately after a load of the RTTR or RCNR register does not read back the loaded value. This is caused by a long propagation delay through the read back logic.

**Affected Step:** A0, B0, B1, B2, B4, and B5

**Workaround:** At least a 32 µsec delay is needed for the values to propagate through the RTC logic before the stored value can be read back correctly. You may generate this delay by performing multiple reads, but only using the result of the last read.

**Status:** No fix.

## 28. Incorrect Address Decode in USB Controller

**Problem:** Generally, SA-1110 USB functionality is limited to a USB bus with a maximum of two USB devices, this bus would include the SA-1110 USB device. Alternately, there may be three or more USB devices on the bus if the SA-1110 USB device is assigned address 0x4. The following paragraphs explain in detail this environment.

The SA-1110 USB controller may incorrectly decode an address on the bus causing one of these problems:

1. USB Port responds to the wrong address
2. USB Port accepts data to the wrong address
3. Port may freeze because of various address and endpoint combinations on the bus

**SA-1110 USB Port Responds to the Wrong Address**

There are two conditions where the SA-1110 USB Port responds to an incorrect address:

1. Three or more devices and hubs in a system when the SA-1110 device is assigned to address 0x4
2. Three or more devices in a system when the SA-1110 device is assigned to an address other than 0x4

The SA-1110 USB functions properly when it is the only device in a system or with only one other device. In this case the SA-1110 USB device did not fail in laboratory tests. The following paragraphs explain what happens when an SA-1110 USB device is in a system with two or more other USB devices.

If an SA-1110 device is assigned to address 0x4, the error was not duplicated in the lab. However, if these conditions occur:

- An installed SA-1110 USB device is disconnected from your system,
- Another USB device is connected, and
- The SA-1110 USB device is re-connected,

Then the SA-1110 USB device will fail because it is no longer assigned to address 0x4.

After the SA-1110 USB device is disconnected, the host frees-up address 0x4 and it is assigned to the next device plugged into the system. If the SA-1110 device is simply disconnected and re-connected without disconnecting or connecting any other USB devices, the host again assigns address 0x4 to the SA-1110 device and the error does not occur.

If the SA-1110 USB device is not assigned to address 0x4, an error will occur. If the SA-1110 USB device is connected after address 0x4 has been assigned to another USB device, the failure occurs immediately. If the SA-1110 USB device is connected before address 0x4 has been assigned, no failure occurs unless the SA-1110 USB device is disconnected and re-connected. Hence, the major problem is when another device is assigned to address 0x4 in a system before the SA-1110 device is assigned an address.

Other address and endpoint combinations cause the SA-1110 USB device to incorrectly respond, thereby causing contention on the USB Bus. The table below shows some of the more likely combinations that cause an incorrect response. If the SA-1110 USB device is assigned to the address in the SA-1110 Device column and there is an access to the address and endpoint combination shown in the Other Devices column, the SA-1110 USB device incorrectly responds.

## Other SA-1110 Erroneous Response Cases

| Other Devices | | | SA-1110 Device | |
|---|---|---|---|---|
| **Address** | **Endpoint** | **crc** | **address** | **endpoint** |
| 0x0F | 0x0 | 0x03 | 0x00 | 0x1 |
| 0x04 | 0x0 | 0x05 | 0x00 | 0x2 |
| 0x0B | 0x0 | 0x04 | 0x00 | 0x2 |
| 0x02 | 0x1 | 0x03 | 0x08 | 0x1 |
| 0x0D | 0x1 | 0x02 | 0x08 | 0x1 |
| 0x06 | 0x1 | 0x04 | 0x08 | 0x2 |
| 0x09 | 0x1 | 0x05 | 0x08 | 0x2 |

**USB Port Accepts Data to the Wrong Address**

A few cases exist where the SA-1110 USB device incorrectly decodes an address and incorrectly accepts data that was intended for another USB device. This error only occurs during an OUT transaction, and could cause data corruption to the SA-1110 USB device. All of these cases occur when a particular address, endpoint, and CRC combination is incorrectly compared (by the SA-1110 USB) to the address assigned to the SA-1110 USB device and endpoint 0x1. The table below shows some of the address, endpoint, and CRC combinations that cause this error.

## Some Addresses that cause the SA-1110 to Accept Bad Data

| Other Devices | | | SA-1110 Device | |
|---|---|---|---|---|
| **Address** | **Endpoint** | **crc** | **address** | **endpoint** |
| 0x02 | 0x1 | 0x03 | 0x08 | 0x1 |
| 0x0D | 0x1 | 0x02 | 0x08 | 0x1 |
| 0x0F | 0x0 | 0x03 | 0x00 | 0x1 |

The first two rows in the table above occur only with 16 or fewer devices in a system and where the SA-1110 USB device is assigned to address 0x8 and an OUT transaction occurs to address 0x2 or address 0xD at endpoint 0x1. The third row in the table above occurs only if 15 or more devices and hubs are in a system and where an OUT transaction occurs to address 0xF at endpoint 0 while the SA-1110 USB device has just been reset and does not yet have an address assigned. While these cases are rare and depend on the number of devices in the system as well as the type of transaction and the address being accessed, the error occurs if these conditions are met.

**The SA-1110 USB Controller Freezes and Recovers**

As with condition 1 and 2, condition 2 occurs when the SA-1110 USB device incorrectly decodes an address. In this case, however, the decode does not include an endpoint for the SA-1110 USB device. When this happens the SA-1110 USB device does not try to respond, rather it freezes while

waiting for more data to decode for a valid endpoint. This error, while frequently occurring, recovers as soon as a valid address, endpoint, and CRC combination are seen on the bus. The table below shows all of the combinations that cause the SA-1110 USB device to freeze when as many as 16 USB devices are in a system.

## Addresses That Cause the SA-1110 USB Controller to Freeze

| Other Devices | | | SA-1110 Device |
|---|---|---|---|
| **address** | **endpoint** | **crc** | **address** |
| 0x04 | 0x2 | 0x00 | 0x00 |
| 0x09 | 0x3 | 0x00 | 0x00 |
| 0x03 | 0x4 | 0x00 | 0x01 |
| 0x0E | 0x5 | 0x00 | 0x01 |
| 0x00 | 0x9 | 0x00 | 0x02 |
| 0x0D | 0x8 | 0x00 | 0x02 |
| 0x07 | 0xF | 0x00 | 0x03 |
| 0x0A | 0xE | 0x00 | 0x03 |
| 0x06 | 0x3 | 0x01 | 0x04 |
| 0x0B | 0x2 | 0x01 | 0x04 |
| 0x01 | 0x5 | 0x01 | 0x05 |
| 0x0C | 0x4 | 0x01 | 0x05 |
| 0x02 | 0x8 | 0x01 | 0x06 |
| 0x0F | 0x9 | 0x01 | 0x06 |
| 0x05 | 0xE | 0x01 | 0x07 |
| 0x08 | 0xF | 0x01 | 0x07 |
| 0x00 | 0x0 | 0x02 | 0x08 |
| 0x0D | 0x1 | 0x02 | 0x08 |
| 0x07 | 0x6 | 0x02 | 0x09 |
| 0x0A | 0x7 | 0x02 | 0x09 |
| 0x04 | 0xB | 0x02 | 0x0A |
| 0x09 | 0xA | 0x02 | 0x0A |
| 0x03 | 0xD | 0x02 | 0x0B |
| 0x0E | 0xC | 0x02 | 0x0B |
| 0x02 | 0x1 | 0x03 | 0x0C |
| 0x0F | 0x0 | 0x03 | 0x0C |
| 0x05 | 0x7 | 0x03 | 0x0D |
| 0x08 | 0x6 | 0x03 | 0x0D |
| 0x06 | 0xA | 0x03 | 0x0E |
| 0x0B | 0xB | 0x03 | 0x0E |
| 0x01 | 0xC | 0x03 | 0x0F |
| 0x0C | 0xD | 0x03 | 0x0F |

While laboratory tests have shown this error will recover, it has not been fully characterized. It is suspected that either an SOF or EOP for another USB device causes the SA-1110 USB device to recover. However, in some cases an ACK to another address also helped the SA-1110 USB device recover. Since a wide variety of circumstances caused the SA-1110 USB device to easily recover, thorough testing was not done to find all recovery cases.

**Affected Step:** A0, B0, B1, B2, and B4

**Workaround:** None

**Status:** Fixed in B5

### 29. USB Controller Endpoint 2 (IN) Transmits Incorrect Data

**Problem:** If the SA-1110 system uses so much memory bandwidth that the USB transmit FIFO can underrun, the USB controller may transmit incorrect data to the host with no indication an error occurred. During normal operation, the USB controller requests data be put into the Endpoint 2 FIFO. This data is then transmitted to the host after the host sends an IN command. Between the core or DMA putting a data byte into the transmit FIFO and the serial shifter beginning a byte transmission, the SA-1110 can transmit an old byte. There is no indication an underrun or CRC error occurred during this transfer. This condition causes the host to use corrupt data without the USB controller or the host reporting an error. Using a checksum on the entire data transfer is only software recovery from this condition.

**Affected Step:** A0, B0, B1, B2, and B4

**Workaround:** To prevent the FIFO from being starved for data, allow enough bandwidth in the system for the core or DMA to service the USB endpoint 2 FIFO.

Alternatively, a software checksum can be used for the entire data transfer to indicate any incorrect data that may have been transferred.

**Status:** Fixed in B5 - To activate the fix, you must set UDCCR bit 7 to one by writing a one to it. The UDC must be connected to a USB Host in order to successfully access UDCCR. This fix must be activated each time the UDC is enabled.

***Note:*** UDCCR Bit-7 is "reserved" in A0, B0, B1, B2, B4.

### 30. SA-1110 UDC Registers can be corrupted when writing to OS Timer Match Registers (OSMR0,1,2).

**Problem:** When the SA1110 UDC is enabled:

1. Writing to OST Match Register 0 can result in corruption of the UDC Control Register (UDCCR)
2. Writing to OST Match Register 1 can result in corruption of the UDC Address Register (UDCAR)
3. Writing to OST Match Register 2 can result in corruption of the UDC OUT Max Packet Register (UDCOMP)

**Affected Step:** A0, B0, B1, B2, B4, B5

**Workaround:** Avoid writing to OST Match Registers when the SA-1110 UDC is enabled.

**Status:** No fix.

### 31. During USB Bulk OUT transfers, DMA reads of the SA-1110 UDC Endpoint 1 input FIFO can result in the FIFO not advancing its qued data to the next positions.

**Problem:** The Endpoint 1 input FIFO does not have a counter that shows how much data is in the FIFO. So, during a DMA read, there is no way to determine if the FIFO properly advanced its qued data to the next positions or erroneously did not advance its qued data to the next positions.

**Affected Step:** A0, B0, B1, B2, B4, B5

**Workaround:** Use CPU reads of the Endpoint 1 input FIFO rather than using DMA.

**Status:** No fix.

### 32. After a USB Control read or write of the SA1110 UDC Endpoint 0 FIFO, the FIFO does not always advance its qued data to the next positions.

**Problem:** 1. When reading data from the UDC Endpoint 0 FIFO, the FIFO does not always advance its qued data to the next positions. This can result in erroneously reading the same data entry multiple times.

2. When writing data to the UDC Endpoint 0 FIFO, the FIFO does not always advance its qued data to the next positions. This can result in lost data when a data write operation overwrites data already in the FIFO.

**Affected Step:** A0, B0, B1, B2, B4, B5

**Workaround:** 1. Software must read the UDC Endpoint 0 Write Count Register (UDCWC) before and after reading the FIFO to determine if the FIFO has advanced its qued data to the next positions. If UDCWC has not decremented, software must re-read the FIFO until UDCWC does decrement.

2. Software must read the UDC Endpoint 0 Write Count Register (UDCWC) before and after writing to the FIFO to determine if the FIFO has advanced its qued data to the next positions. If UDCWC has not incremented, software must re-write the FIFO until UDCWC does increment.

**Status:** No fix.

### 33. The TCP bit in SA1110 UDC Endpoint 2 (IN) Control Status Register (UDCCS2) must be cleared by software after every Bulk IN packet has been transmitted.

**Problem:** The Transmit Packet Complete (TPC) bit in UDCCS2 is automatically set after transmission of a Bulk IN packet to the host. If software does not clear TCP before the Host requests the next Bulk IN packet, a NAK will be sent to the host rather than the next Bulk IN packet.

**Affected Step:** A0, B0, B1, B2, B4, B5

**Workaround:** Software must clear the TCP bit in UDCCS2 before the host requests the next Bulk IN packet to be sent by the SA1110 UDC.

**Status:** No fix.

### 34. LCD Controller does not generate an interrupt when its input FIFO under-runs.

**Problem:** If the LCD Controller's dedicated DMA engine does not supply frame buffer data to the LCD Controller's input FIFO fast enough, the input FIFO could under-run. This under-run condition does not generate an interrupt as it should, and incorrect data is supplied to the LCD pannel.

**Affected Step:** A0, B0, B1, B2, B4, B5

**Workaround:** To prevent the input FIFO from under-running, allow enough bandwidth for the DMA engine to fill the input FIFO before it becomes empty. See Bandwidth Calculations for SA-1110 Processor LCD Displays application note found at:

http://developer.intel.com/design/strong/applnots/index.htm?iid=strongarm+leftnav&

**Status:** No fix.

### 35. LCD Controller input and output FIFOs retain their respective error states even if the respective status bits are cleared in the LCD Status Register (LCSR).

**Problem:** One or more LCSR bits 11:4 are automatically set when an error occurs in either (or both) the input or output FIFOs. Software writing a 1 to clear a status bit clears the bit temporarily, but does not clear the condition that caused the status bit to be set. So, the status bit is cleared for one clock period, but gets automatically set again on the next clock.

**Affected Step:** A0, B0, B1, B2, B4, B5

**Workaround:** After one or more LCSR bits are set, software must disable and re-enable the LCD Controller in order to clear the FIFO error conditions. Then software must clear the status bits by writing ones to them.

**Status:** No fix.

### 36. Serial Port 2 loopback mode does not work when operating the port as IrDA-SIR or UART. IrDA-HSSP loopback mode does work.

**Problem:** A gate is missing from the multiplexer that provides the loopback pathway, preventing loopback operation.

**Affected Step:** A0, B0, B1, B2, B4, B5

**Workaround:** Do not set bit 5 (LBM) to 1 in UTCR3 (0h8003 000C). Do not use Serial Port 2 loopback mode when operating as IrDA-SIR or UART.

IrDA-HSSP has a separate loopback multiplexer. IrDA-HSSP loopback mode works and is selected by setting bit 1 of HSCR0 to 1.

**Status:** No fix.

### 37. Audio Transmit Data in Serial Port 4: MCP Mode can be corrupted when writing to OS Timer Count Register (OSCR) or OS Timer Match Register 0 (OSMR0).

**Problem:** When Serial Port 4: MCP Mode is enabled and no data is in the Audio Transmit Data FIFO, writing data to OSCR or OSMR0 can result in:

- The data being erroneously copied into the Audio Transmit Data field of the MCP transmit frame
- The Audio Valid (AV) bit of the MCP transmit frame is erroneously set

**Affected Step:** A0, B0, B1, B2, B4, B5

**Workaround:** Avoid writing to OSCR or OSMR0 when Serial Port 4: MCP Mode is enabled.

**Status:** No fix.

# Specification Changes

## 1. SDLC Feature

The SDLC feature is not available in this release of the product.

## 2. SDLC Feature Not Supported

Effective January 2000, the SDLC feature is not supported by the SA-1110 device.

## 3. Modifications in SDRAM/SMROM Data Input Hold Time

Table 13-3 of the *Intel StrongARM SA-1110 Microprocessor Developer's Manual* and its underlying Note 1 have been changed. Specifically, the Tsdih guidelines for 133 MHz SA-1110 microprocessors using SDRAM or SMROM at 66 MHz have changed. Also, the Tsdih guidelines for 206 MHz SA-1110 microprocessors using SDRAM or SMROM at frequencies less than 103 MHz have also been changed.

Most significantly, for 133 MHz SA-1110 microprocessors with a 66 MHz SDRAM/SMROM clock, the specified read data latching mode has changed from delayed to non-delayed. The MDCASxx registers need to be programmed accordingly. Also, the Table 13-3 Note 2 technique of serpentine SDCLK routing delay must not be used with 133 MHz SA-1110 microprocessors.

For 206 MHz SA-1110 microprocessors using an SDRAM/SMROM clock frequency of less than 103 MHz, there are four options:

- Confirm that the system design satisfies the new Tsdih guidelines (see Table 13-3).
- Carefully use the Table 13-3 Note 2 technique to adjust the system design so that it satisfies the new Tsdih guidelines.
- Set MDREFR:KnDB2=1 to divide the SDRAM/SMROM clock frequency by two and automatically use non-delayed read data latching.
- Change the CPU frequency such that the new Tsdih guidelines are satisfied at the non-divided SDRAM/SMROM clock frequency.

## 4. DC Operating Conditions: Section 12.2

The new parameters for Table 12-2:

- Changed the Minimum for Vihc from 0.8 X VDDX to 2.4
- Removed 1 from ESD Nominal
- Added 1000 V to ESD Maximum

## 5. Power Supply Voltages and Currents: Section 12.3

The new parameters for the AC and AD version of the device are:

- Maximum Run Mode Power changed from TBD to 500 mW
- Typical Run Mode Power changed from 240 mW to 200 mW
- Maximum Idle Mode Power changed from TBD to 100 mW

- Maximum Sleep Mode Current changed from 65 to 75 uA

The new parameters for the BC and BD version of the device are:

- Maximum Run Mode Power changed from TBD to 1000 mW
- Typical Run Mode Power changed from 400 mW to 350 mW
- Maximum Idle Mode Power changed from TBD to 200 mW
- Vddi Max changed from 1.93 V to 2.10 V
- Vddi Min changed from 1.58 V to 1.65 V

# *Specification Clarifications*

None for this revision of this specification update.

# Documentation Changes

## 1. Interrupt Controller IRQ Pending Register (ICIP) and FIQ Pending Register (ICFP): Section 9.2.1.2

Changed the reset values for the Interrupt Controller IRQ and FIQ Pending Registers (ICIP and ICFP) from undefined to 0. Added the word Reset to the left column in the row that indicates the reset value.

**0h 9005 0000** **ICIP** **Read-Only**

| | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | IP31 | IP30 | IP29 | IP28 | IP27 | IP26 | IP25 | IP24 | IP23 | IP22 | IP21 | IP20 | IP19 | IP18 | IP17 | IP16 | IP15 | IP14 | IP13 | IP12 | IP11 | IP10 | IP9 | IP8 | IP7 | IP6 | IP5 | IP4 | IP3 | IP2 | IP1 | IP0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 31..0 | — | These flags reflect the OR of the reset state of the individual interrupt status bits at the source unit. |

**0h 9005 0010** **ICFP** **Read-Only**

| | 31 | 30 | 29 | 28 | 27 | 26 | 25 | 24 | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | FP31 | FP30 | FP29 | FP28 | FP27 | FP26 | FP25 | FP24 | FP23 | FP22 | FP21 | FP20 | FP19 | FP18 | FP17 | FP16 | FP15 | FP14 | FP13 | FP12 | FP11 | FP10 | FP9 | FP8 | FP7 | FP6 | FP5 | FP4 | FP3 | FP2 | FP1 | FP0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

| Bits | Name | Description |
|---|---|---|
| 31..0 | — | These flags reflect the OR of the reset state of the individual interrupt status bits at the source unit. |

## 2. RTC Status Register (RTSR): Section 9.3.3

Changed the second sentence to read:

The HZE interrupt enable bit must be set by software to allow the RTC assertion of the HZ bit and the 1-Hz interrupt.

## 3. RTC Trim Register (RTTR): Section 9.3.4

Added this note at the end of section 9.3.4.

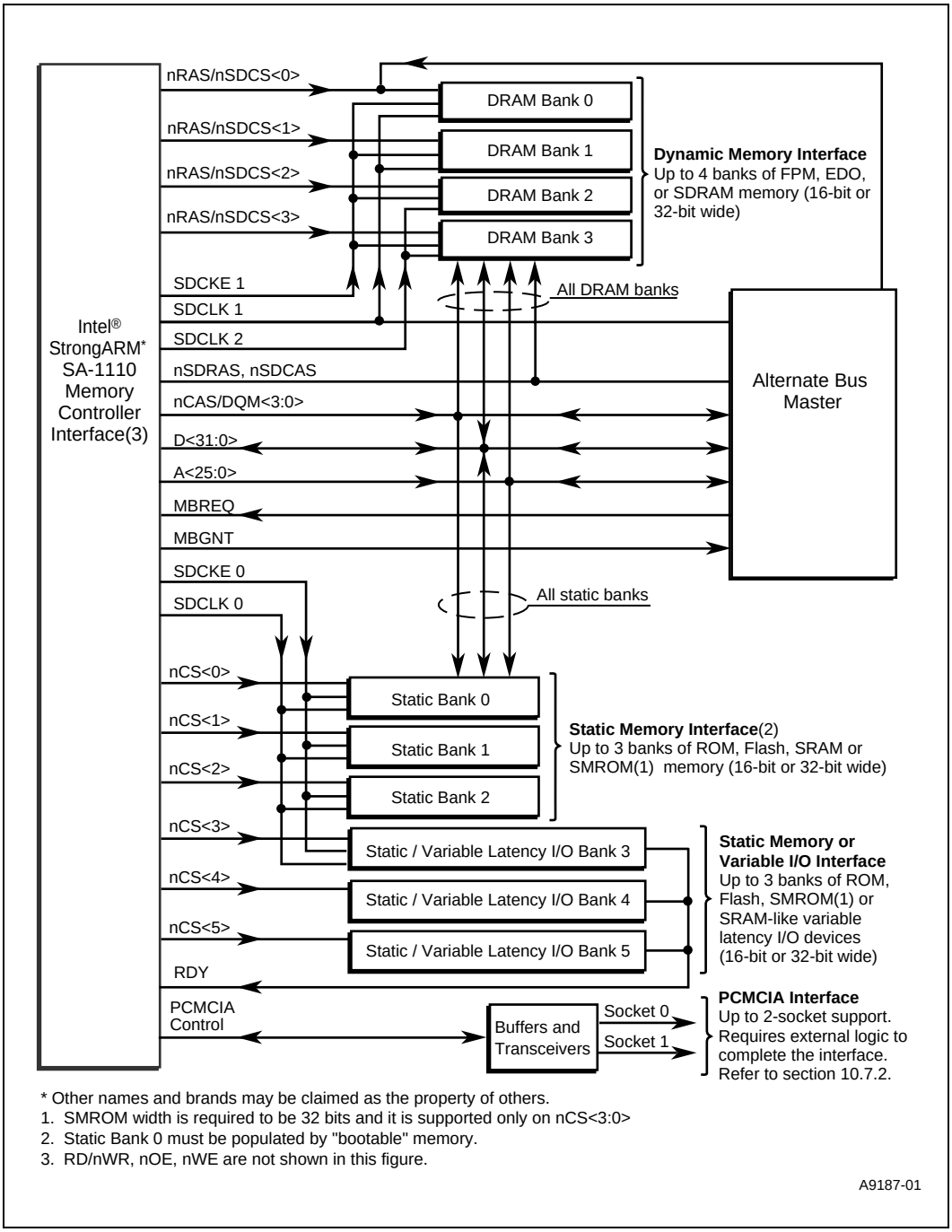
***Note:*** When a value is written to the RTC registers RTTR or RCNR, the value is stored correctly, but doing a read immediately after the write will read an incorrect value. At least a 32 µsec delay is needed for the values to propagate through the RTC logic before the stored value can be read back

correctly. You may generate this delay by performing multiple reads, but only using the result of the last read.

## 4. Memory and PC-Card Control Module: Section 10

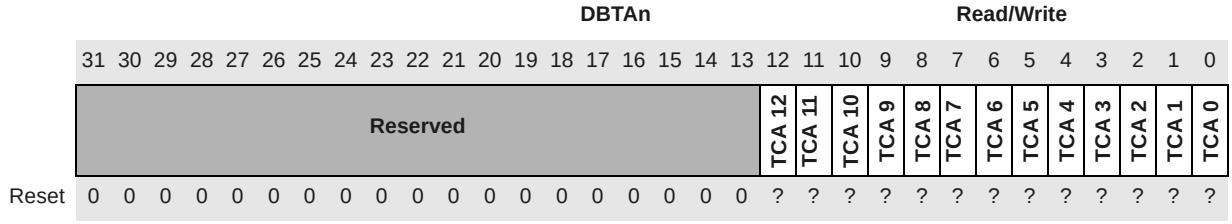
Changed Figure 10-1:

**Figure 10-1. General Memory Interface Configuration**



## 5. DMA Buffer A Transfer Count Register (DBTAn): Section 11.6.1.4

Changed DMA Buffer A Transfer Count register reset values for the Reserved bits to 0.




## 6. LCD Disable Done Flag: Section 11.7.11.1

Changed the paragraph title to:

**11.7.11.1 LCD Disable Done Status (LDD) (read/write, maskable interrupt)**

## 7. Base Address Update Flag: Section 11.7.11.2

Changed the paragraph title to:

**11.7.11.2 Base Address Update Status (BAU) (read-only, maskable interrupt)**

## 8. HP-SIR * Enable (HSE): Section 11.10.4.1

The second sentence has been changed and now appears as follows:

When HSE=0, HP-SIR * modulation is disabled, and if UART operation is enabled (ITR=0), it is used for normal serial transmission rather than IrDA communication.

## 9. End/Error in FIFO Status (EIF) (read-only, nonmaskable interrupt): Section 11.10.10.1

Changed the paragraph title to:

**11.10.10.1 End/Error in FIFO Flag (EIF) (read-only, nonmaskable interrupt)**

## 10. Receiver Overrun Status (ROR) (read-only, noninterruptible): Section 11.10.11.7

Changed the paragraph title to:

**11.10.11.7 Receiver Overrun Flag (ROR) (read-only, noninterruptible)**

## 11. SSP Data Register: Section 11.12.11

Changed the Top of Receive FIFO to the Top of Transmit FIFO and changed the reset values of Bottom of Receive FIFO and Top of Transmit FIFO from zero to ?.

**0h 8007 006C** **SSP Data Register: SSDR** **Read/Write**

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Bottom of Receive FIFO** | | | | | | | | | | | | | | | |
| Reset | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? |
| | **Read Access** | | | | | | | | | | | | | | | |

| | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | **Top of Transmit FIFO** | | | | | | | | | | | | | | | |
| Reset | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? | ? |
| | **Write Access** | | | | | | | | | | | | | | | |

## 12. DC Operating Conditions: Section 12.2

These changes have been made in Table 12-2 (new table shown below):

- Rows Ioh and Iol have been removed
- Row ESD has had information added and 1 was removed from the Nominal column
- Changed the Minimum for Vihc from 0.8 X VDDX to 2.4
- Replaced note 5

### Table 12-2. SA-1110 DC Operating Conditions

| Symbol | Parameter | Minimum | Nominal | Maximum | Units | Notes |
|---|---|---|---|---|---|---|
| Vihc | IC input high voltage | 2.4 | — | VDDX | V | 1, 2, 5 |
| Vilc | IC input low voltage | 0.0 | — | 0.2 × VDDX | V | 1, 2 |
| Vohc | OCZ output high voltage | 0.8 × VDDX | — | VDDX | V | 1, 3 |
| Volc | OCZ output low voltage | 0.0 | — | 0.2 × VDDX | V | 1, 3 |
| Iohc | High-level output current | — | — | – 2 | mA | — |
| Iolc | Low-level output current | — | — | 2 | mA | — |
| Ta | Ambient operating temperature | 0 | — | 70 | °C | — |
| Iin | IC input leakage current | — | 10 | — | µA | — |
| Cin | Input capacitance | — | 5 | — | pF | 4 |
| ESD | HBM model ESD | — | — | **1000** | V | |

**NOTES:**
1. Voltages measured with respect to VSS.
2. IC – CMOS-level inputs (includes IC and ICOCZ pin types).
3. OCZ – Output, CMOS levels, three state.
4. Parameter guaranteed by design.
5. Minimum not tested at this time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