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SFF Committee

SFF-8472 Specification for

Diagnostic Monitoring Interface for Optical Xcvrs

Rev 9.3 August 1, 2002

Secretariat: SFF Committee

Abstract: This specification defines an enhanced digital diagnostic monitoring interface for optical transceivers which allows real time access to device operating parameters.

This document provides a common specification for systems manufacturers, system integrators, and suppliers. This is an internal working document of the SFF Committee, an industry ad hoc group.

This specification is made available for public review, and written comments are solicited from readers. Comments received by the members will be considered for inclusion in future revisions of this document.

Support: This document is supported by the identified member companies of the SFF Committee.

POINTS OF CONTACT:

Dan Kane
Technical Editor
Finisar
1308 Moffett Park Dr
Sunnyvale CA 94089

408-542-4137
408-514-6139Fx
d_kane@finisar.com

I. Dal Allan
Chairman SFF Committee
14426 Black Walnut Court
Saratoga
CA 95070

408-867-6630
408-867-2115Fx
endlcom@acm.org

EXPRESSION OF SUPPORT BY MANUFACTURERS

The following member companies of the SFF Committee voted in favor of this industry specification.

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PRINCIPLES OF THE SFF COMMITTEE

The SFF Committee is an ad hoc group formed to address storage industry needs in a prompt manner. When formed in 1990, the original goals were limited to defining de facto mechanical envelopes within which disk drives can be developed to fit compact computer and other small products.

Adopting a common industry size simplifies the integration of small drives (2 1/2" or less) into such systems. Board-board connectors carrying power and signals, and their position relative to the envelope are critical parameters in a product that has no cables to provide packaging leeway for the integrator.

In November 1992, the SFF Committee objectives were broadened to encompass other areas which needed similar attention, such as pinouts for interface applications, and form factor issues on larger disk drives. SFF is a forum for resolving industry issues that are either not addressed by the standards process or need an immediate solution.

Documents created by the SFF Committee are expected to be submitted to bodies such as EIA (Electronic Industries Association) or an ASC (Accredited Standards Committee). They may be accepted for separate standards, or incorporated into other standards activities.

The principles of operation for the SFF Committee are not unlike those of an accredited standards committee. There are 3 levels of participation:

- Attending the meetings is open to all, but taking part in discussions is limited to member companies, or those invited by member companies
- The minutes and copies of material which are discussed during meetings are distributed only to those who sign up to receive documentation.
- The individuals who represent member companies of the SFF Committee receive documentation and vote on issues that arise. Votes are not taken during meetings, only guidance on directions. All voting is by letter ballot, which ensures all members an equal opportunity to be heard.

Material presented at SFF Committee meetings becomes public domain. There are no restrictions on the open mailing of material presented at committee meetings. In order to reduce disagreements and misunderstandings, copies must be provided for all agenda items that are discussed. Copies of the material presented, or revisions if completed in time, are included in the documentation mailings.

The sites for SFF Committee meetings rotate based on which member companies volunteer to host the meetings. Meetings have typically been held during the ASC T10 weeks.

The funds received from the annual membership fees are placed in escrow, and are used to reimburse ENDL for the services to manage the SFF Committee.

If you are not receiving the documentation of SFF Committee activities or are interested in becoming a member, the following signup information is reprinted here for your information.

Annual SFF Committee Membership Fee	$ 1,800.00
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SFF Committee
14426 Black Walnut Ct
Saratoga CA 95070

408-867-6630
408-867-2115Fx
250-1752@mcimail.com

SFF Committee --

Diagnostic Monitoring Interface for Optical Xcvrs

1. Scope

This specification defines an enhanced digital diagnostic monitoring interface for optical which allows real time access to device operating parameters. It also adds new options to the previously defined serial ID memory map that accommodates new transceiver types which were not considered in the INF-8074 SFP MSA or SFF-8053 GBIC specifications.

1.1 Description of Clauses

Clause 1 contains the Scope and Purpose.

Clause 2 contains Referenced and Related Standards and SFF Specifications.

Clause 3 contains the General Description

Clause 4 contains the Definitions and Conventions

Clause 5 contains the Interface Description

2. References

The SFF Committee activities support the requirements of the storage industry, and it is involved with several standards.

2.1 Industry Documents

The following documents are relevant to this Specification.

- SFF-8053 GBIC (Gigabit Interface Converter)
- INF-8074i SFP (Small Formfactor Pluggable) Transceiver

2.2 SFF Specifications

There are several projects active within the SFF Committee. At the date of printing document numbers had been assigned to the following projects. The status of Specifications is dependent on committee activities.

F = Forwarded	The document has been approved by the members for forwarding to a formal standards body.
P = Published	The document has been balloted by members and is available as a published SFF Specification.
A = Approved	The document has been approved by ballot of the members and is in preparation as an SFF Specification.
C = Canceled	The project was canceled, and no Specification was Published.
D = Development	The document is under development at SFF.
E = Expired	The document has been published as an SFF Specification, and the members voted against re-publishing it when it came up for annual review.
e = electronic	Used as a suffix to indicate an SFF Specification which has Expired but is still available in electronic form from SFF e.g. a specification has been incorporated into a draft or published standard which is only available in hard copy.
i = Information	The document has no SFF project activity in progress, but it defines features in developing industry standards. The document was provided by a company,

editor of an accredited standard in development, or an individual. It is provided for broad review (comments to the author are encouraged).

s = submitted — The document is a proposal to the members for consideration to become an SFF Specification.

Spec #	Rev	List of Specifications as of August 1, 2002
SFF-8000		SFF Committee Information
INF-8001i	E	44-pin ATA (AT Attachment) Pinouts for SFF Drives
INF-8002i	E	68-pin ATA (AT Attachment) for SFF Drives
SFF-8003	E	SCSI Pinouts for SFF Drives
SFF-8004	E	Small Form Factor 2.5" Drives
SFF-8005	E	Small Form Factor 1.8" Drives
SFF-8006	E	Small Form Factor 1.3" Drives
SFF-8007	E	2mm Connector Alternatives
SFF-8008	E	68-pin Embedded Interface for SFF Drives
SFF-8009	4.1	Unitized Connector for Cabled Drives
SFF-8010	E	Small Form Factor 15mm 1.8" Drives
INF-8011i	E	ATA Timing Extensions for Local Bus
SFF-8012	3.0	4-Pin Power Connector Dimensions
SFF-8013	E	ATA Download Microcode Command
SFF-8014	C	Unitized Connector for Rack Mounted Drives
SFF-8015	E	SCA Connector for Rack Mounted SFF SCSI Drives
SFF-8016	C	Small Form Factor 10mm 2.5" Drives
SFF-8017	E	SCSI Wiring Rules for Mixed Cable Plants
SFF-8018	E	ATA Low Power Modes
SFF-8019	E	Identify Drive Data for ATA Disks up to 8 GB
INF-8020i	E	ATA Packet Interface for CD-ROMs
INF-8028i	E	- Errata to SFF-8020 Rev 2.5
SFF-8029	E	- Errata to SFF-8020 Rev 1.2
SFF-8030	1.8	SFF Committee Charter
SFF-8031		Named Representatives of SFF Committee Members
SFF-8032	1.5	SFF Committee Principles of Operation
INF-8033i	E	Improved ATA Timing Extensions to 16.6 MBs
INF-8034i	E	High Speed Local Bus ATA Line Termination Issues
INF-8035i	E	Self-Monitoring, Analysis and Reporting Technology
INF-8036i	E	ATA Signal Integrity Issues
INF-8037i	E	Intel Small PCI SIG
INF-8038i	E	Intel Bus Master IDE ATA Specification
INF-8039i	E	Phoenix EDD (Enhanced Disk Drive) Specification
SFF-8040	1.2	25-pin Asynchronous SCSI Pinout
SFF-8041	C	SCA-2 Connector Backend Configurations
SFF-8042	C	VHDCI Connector Backend Configurations
SFF-8043	E	40-pin MicroSCSI Pinout
SFF-8045	4.5	40-pin SCA-2 Connector w/Parallel Selection
SFF-8046	E	80-pin SCA-2 Connector for SCSI Disk Drives
SFF-8047	C	40-pin SCA-2 Connector w/Serial Selection
SFF-8048	C	80-pin SCA-2 Connector w/Parallel ESI
SFF-8049	E	80-conductor ATA Cable Assembly
INF-8050i	1.0	Bootable CD-ROM
INF-8051i	E	Small Form Factor 3" Drives
INF-8052i	E	ATA Interface for 3" Removable Devices
SFF-8053	5.5	GBIC (Gigabit Interface Converter)
INF-8055i	E	SMART Application Guide for ATA Interface
SFF-8056	C	50-pin 2mm Connector
SFF-8057	E	Unitized ATA 2-plus Connector
SFF-8058	E	Unitized ATA 3-in-1 Connector

SFF-8059	E	40-pin ATA Connector
SFF-8060	1.1	SFF Committee Patent Policy
SFF-8061	1.1	Emailing drawings over the SFF Reflector
SFF-8062		Rolling Calendar of SSWGs and Plenaries
SFF-8065	C	40-pin SCA-2 Connector w/High Voltage
SFF-8066	C	80-pin SCA-2 Connector w/High Voltage
SFF-8067	3.0	40-pin SCA-2 Connector w/Bidirectional ESI
INF-8068i	1.0	Guidelines to Import Drawings into SFF Specs
SFF-8069	E	Fax-Access Instructions
INF-8070i	1.3	ATAPI for Rewritable Removable Media
SFF-8072	1.2	80-pin SCA-2 for Fibre Channel Tape Applications
SFF-8073	-	20-pin SCA-2 for GBIC Applications
INF-8074i	1.0	SFP (Small Formfactor Pluggable) Transceiver
SFF-8075	1.0	PCI Card Version of SFP Cage
SFF-8080	E	ATAPI for CD-Recordable Media
INF-8090i	5.4	ATAPI for DVD (Digital Video Data)
SFF-8101		3 Gbs and 4 Gbs Signal Characteristics
SFF-8110	C	5V Parallel 1.8" drive form factor
SFF-8111	1.2	1.8" drive form factor (60x70mm)
SFF-8120	2.6	1.8" drive form factor (78x54mm)
SFF-8200e	1.1	2 1/2" drive form factors (all of 82xx family)
SFF-8201e	1.3	2 1/2" drive form factor dimensions
SFF-8212e	1.2	2 1/2" drive w/SFF-8001 44-pin ATA Connector
SFF-8221	1.3	Pre-Aligned 2.5" Drive >10mm Form Factor
SFF-8222	1.1	2.5" Drive w/SCA-2 Connector
SFF-8223		2.5" Drive w/Serial Attachment Connector
SFF-8300e	1.2	3 1/2" drive form factors (all of 83xx family)
SFF-8301	1.4	3 1/2" drive form factor dimensions
SFF-8302e	1.1	3 1/2" Cabled Connector locations
SFF-8323		3 1/2" drive w/Serial Attachment Connector
SFF-8332e	1.2	3 1/2" drive w/80-pin SFF-8015 SCA Connector
SFF-8337e	1.2	3 1/2" drive w/SCA-2 Connector
SFF-8342e	1.3	3 1/2" drive w/Serial Unitized Connector
INF-8350i	6.1	3 1/2" Packaged Drives
SFF-8400	C	VHDCI (Very High Density Cable Interconnect)
SFF-8410	16.1	High Speed Serial Testing for Copper Links
SFF-8411		High Speed Serial Testing for Backplanes
SFF-8412	8.1	HSOI (High Speed Optical Interconnect) Testing
SFF-8415	3.1	HPEI (High Performance Electrical Interconnect) Testing
SFF-8416	0.1	HPEI Measurement of Bulk Cable
SFF-8420	11.1	HSSDC-1 Shielded Connections
SFF-8421	2.4	HSSDC-2 Shielded Connections
SFF-8422	C	FCI Shielded Connections
SFF-8423	C	Molex Shielded Connections
SFF-8424		Dual Row HSSDC-2 Shielded Connections
SFF-8430	4.1	MT-RJ Duplex Optical Connections
SFF-8441	14.1	VHDCI Shielded Configurations
SFF-8451	10.1	SCA-2 Unshielded Connections
SFF-8452	3.1	Glitch Free Mating Connections for Multidrop Aps
SFF-8453		Shielded High Speed Serial connectors
SFF-8460	1.2	HSS Backplane Design Guidelines
SFF-8470	2.1	Multi Lane Copper Connector
SFF-8471	C	ZFP Multi Lane Copper Connector
SFF-8472	9.3	Diagnostic Monitoring Interface for Optical Xcvrs

INF-8475i		tba (Jay Neer)
SFF-8480	2.1	HSS (High Speed Serial) DB9 Connections
SFF-8482	0.0	Internal Serial Attachment Connector
SFF-8483		External Serial Attachment Connector
SFF-8500e	1.1	5 1/4" drive form factors (all of 85xx family)
SFF-8501e	1.1	5 1/4" drive form factor dimensions
SFF-8508e	1.1	5 1/4" ATAPI CD-ROM w/audio connectors
SFF-8523		5 1/4" drive w/Serial Attachment Connector
SFF-8551	3.2	5 1/4" CD Drives form factor
SFF-8572	-	5 1/4" Tape form factor
SFF-8610	C	SDX (Storage Device Architecture)

2.3 Sources

Copies of SFF Specifications are available by joining the SFF Committee as an Observer or Member.

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The increasing size of SFF Specifications has made FaxAccess impractical to obtain large documents. Document subscribers and members are automatically updated every two months with the latest specifications. Specifications are available by FTP at ftp://ftp.seagate.com/sff

Electronic copies of documents are also made available via CD_Access, a service which provides copies of all the specifications plus SFF reflector traffic. CDs are mailed every 2 months as part of the document service, and provide the letter ballot and paper copies of what was distributed at the meeting as well as the meeting minutes.

3. General Description

The purpose of this specification is to enhance the digital diagnostic monitoring interface for optical transceivers to allow real time access to device operating parameters.

It also adds new options to the previously defined serial ID memory map to accommodate new transceiver types that were not considered in the SFF-8053 GBIC or INF-8074i SFP MSA specifications.

The interface is an extension of the serial ID interface defined in SFF-8053 as well as INF-8074i. Both specifications define a 256 byte memory map in EEPROM which is accessible over a 2 wire serial interface at the 8 bit address 1010000X (A0h). The digital diagnostic monitoring interface makes use of the 8 bit address 1010001X (A2h), so the originally defined serial ID memory map remains unchanged. The interface is backward compatible with both the SFF-8053 GBIC and INF-8074i SFP MSA specifications.

4. Definitions and Conventions

4.1 Definitions

For the purpose of SFF Specifications, the following definitions apply:

4.1.1 Optional: This term describes features which are not required by the SFF Specification. However, if any feature defined by the SFF Specification is implemented, it shall be done in the same way as defined by the Specification.

4.1.2 Reserved: Where this term is used for bits, bytes, fields and code values; the bits, bytes, fields and code values are set aside for future standardization. The default value shall be zero. The originator is required to define a Reserved field or bit as zero, but the receiver should not check Reserved fields or bits for zero.

4.1.3 VU (Vendor Unique): This term is used to describe bits, bytes, fields, pins, signals, code values and features which are not described in this SFF Specification, and may be used in a way that varies between vendors.

4.1.4 VU Mode: A mode of execution by the drive in which its use is not defined by this SFF Specification. The means by which a vendor invokes vendor unique operations within a drive is defined by this SFF Specification.

4.2 Conventions

Certain terms used herein are the proper names of signals. These are printed in uppercase to avoid possible confusion with other uses of the same words; e.g., ATTENTION. Any lower-case uses of these words have the normal American-English meaning.

A number of conditions, commands, sequence parameters, events, English text, states or similar terms are printed with the first letter of each word in uppercase and the rest lower-case; e.g., In, Out, Request Status. Any lower-case uses of these words have the normal American-English meaning.

The American convention of numbering is used i.e., the thousands and higher multiples are separated by a comma and a period is used as the decimal point. This is equivalent to the ISO convention of a space and comma.

American:	ISO:
0.6	0,6
1,000	1 000
1,323,462.9	1 323 462,9

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SFF document number: SFF-8472, revision 9.3

Dated: 08/01/02

Digital Diagnostic Monitoring Interface for Optical Transceivers

Revision 9.3

Technical Editors:

Lew Aronson
Dan Kane
Steve Hosking
Finisar Corporation
1308 Moffett Park Drive
Sunnyvale, CA 94089

Technical Contributors:

Randy Clark, Agilent Technologies
Pete Mahowald, Agilent Technologies
Leland Day, JDS Uniphase
Jim Judkins, Micrel Semiconductor
Gus Carroll, Pine Photonics
Tom Lindsay, Stratos Lightwave
Luis Torres, Stratos Lightwave

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4.0	Draft Fourth Revision, Preliminary	10/8/01
5.0	Draft Fifth Revision	11/5/01
6.0	Draft Sixth Revision	11/19/01
7.0	Draft Revision 7.0	01/09/02
8.0	Draft Revision 8.0	02/01/02
9.0	Draft Revision 9.0	03/28/02
9.0	Revision 9.0 Approved for Technical Content	5/02
9.2	Revision 9.2 Submitted for Publication	5/30/02
9.3	Editorial Modifications to rev. 9.2. 9.3 Submitted for Publication	8/01/02

1. Scope and Overview

This document defines an enhanced digital diagnostic monitoring interface for optical transceivers that allows real time access to device operating parameters. It also adds new options to the previously defined serial ID memory map that accommodate new transceiver types that were not considered in the SFP MSA or GBIC documents.

The interface is an extension of the serial ID interface defined in the GBIC specification as well as the SFP MSA. Both specifications define a 256 byte memory map in EEPROM which is accessible over a 2 wire serial interface at the 8 bit address 1010000X (A0h). The digital diagnostic monitoring interface makes use of the 8 bit address 1010001X (A2h), so the originally defined serial ID memory map remains unchanged. The interface is backward compatible with both the GBIC specification and the SFP MSA.

2. Applicable Documents

Gigabit Interface Converter (GBIC). SFF document number: SFF-0053, rev. 5.5, September 27, 2000.

Small Form Factor Pluggable (SFP) Transceiver MultiSource Agreement (MSA), September 14, 2000.

3. Enhanced Digital Diagnostic Interface Definition

Overview

The enhanced digital diagnostic interface is a superset of the MOD_DEF interface defined in the SFP MSA document dated September 14, 2000. The 2 wire interface pin definitions, hardware, and timing are clearly defined there.

This document describes an extension to the memory map defined in the SFP MSA (See Figure 3.1). The enhanced interface uses the two wire serial bus address 1010001X (A2h) to provide diagnostic information about the module's present operating conditions. The transceiver generates this diagnostic data by digitization of internal analog signals. Calibration and alarm/warning threshold data is written during device manufacture.

Figure 3.1: Digital Diagnostic Memory Map
Specific Data Field Descriptions

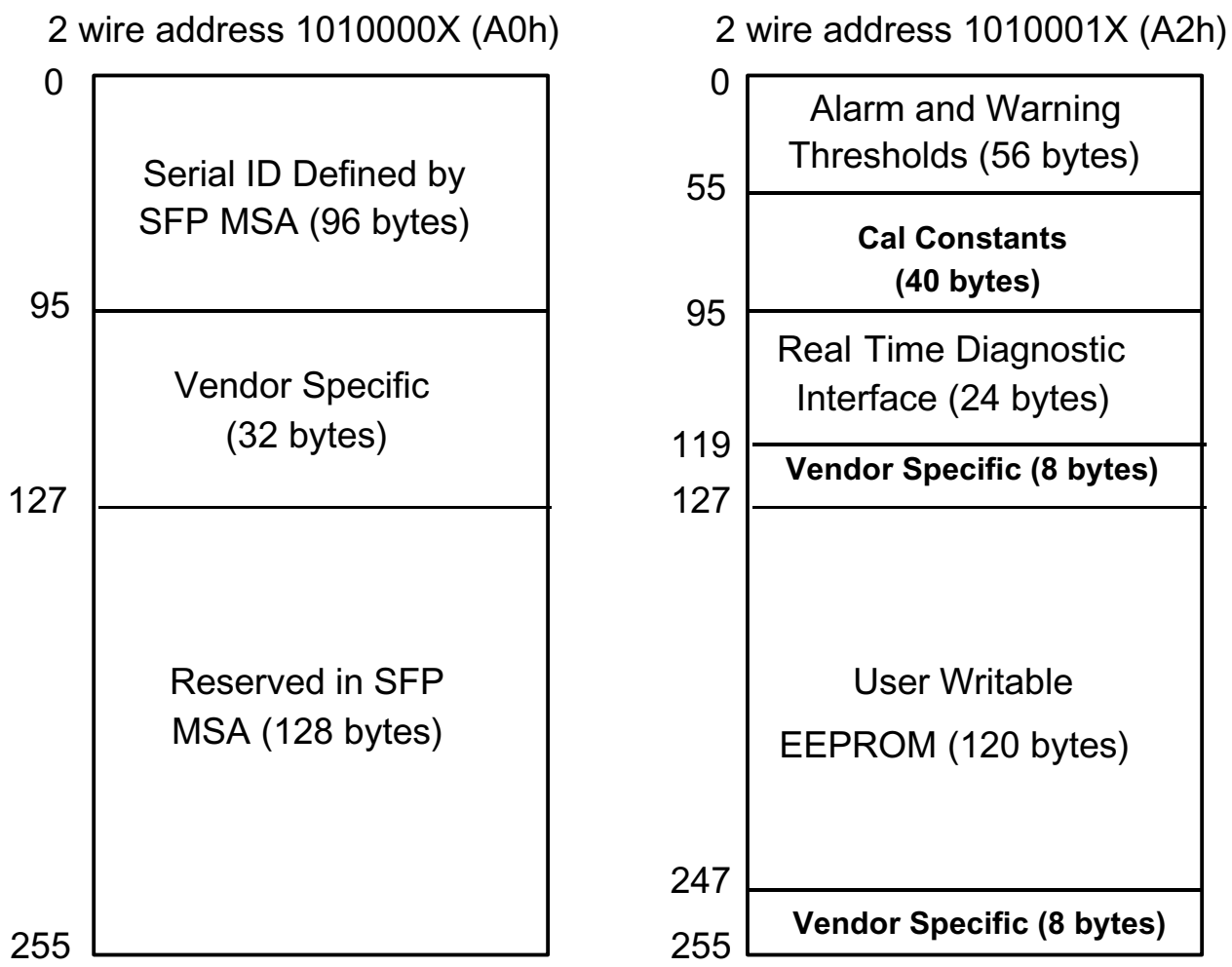

Table 3.1 Serial ID: Data Fields – Address A0

Data Address	Size (Bytes)	Name of Field	Description of Field
BASE ID FIELDS			
0	1	Identifier	Type of serial transceiver (see table 3.2)
1	1	Ext. Identifier	Extended identifier of type of serial transceiver (see table 3.3)
2	1	Connector	Code for connector type (see table 3.4)
3-10	8	Transceiver	Code for electronic compatibility or optical compatibility (see table 3.5)
11	1	Encoding	Code for serial encoding algorithm (see table 3.6)
12	1	BR, Nominal	Nominal bit rate, units of 100 MBits/sec.
13	1	Reserved	
14	1	Length(9µm) - km	Link length supported for 9/125 µm fiber, units of km
15	1	Length (9µm)	Link length supported for 9/125 µm fiber, units of 100 m
16	1	Length (50µm)	Link length supported for 50/125 µm fiber, units of 10 m
17	1	Length (62.5µm)	Link length supported for 62.5/125 µm fiber, units of 10 m
18	1	Length (Copper)	Link length supported for copper, units of meters
19	1	Reserved	
20-35	16	Vendor name	SFP vendor name (ASCII)
36	1	Reserved	
37-39	3	Vendor OUI	SFP vendor IEEE company ID
40-55	16	Vendor PN	Part number provided by SFP vendor (ASCII)
56-59	4	Vendor rev	Revision level for part number provided by vendor (ASCII)
60-61	2	Wavelength	Laser wavelength
62	1	Reserved	
63	1	CC_BASE	Check code for Base ID Fields (addresses 0 to 62)
EXTENDED ID FIELDS			
64-65	2	Options	Indicates which optional transceiver signals are implemented (see table 3.7)
66	1	BR, max	Upper bit rate margin, units of %
67	1	BR, min	Lower bit rate margin, units of %
68-83	16	Vendor SN	Serial number provided by vendor (ASCII)
84-91	8	Date code	Vendor's manufacturing date code (see table 3.8)
92	1	Diagnostic Monitoring Type	Indicates which type of diagnostic monitoring is implemented (if any) in the transceiver (see Table 3.9)
93	1	Enhanced Options	Indicates which optional enhanced features are implemented (if any) in the transceiver (see Table 3.10)
94	1	SFF-8472 Compliance	Indicates which revision of SFF-8472 the transceiver complies with. (see table 3.12)
95	1	CC_EXT	Check code for the Extended ID Fields (addresses 64 to 94)
VENDOR SPECIFIC ID FIELDS			
96-127	32	Vendor Specific	Vendor Specific EEPROM
128-255	128	Reserved	Reserved for future use.

Identifier

The identifier value specifies the physical device described by the serial information. This value shall be included in the serial data. The defined identifier values are shown in table 3.2.

TABLE 3.2: Identifier values

Value	Description of physical device
00h	Unknown or unspecified
01h	GBIC
02h	Module/connector soldered to motherboard
03h	SFP
04-7Fh	Reserved
80-FFh	Vendor specific

Extended Identifier

The extended identifier value provides additional information about the transceiver.

The field should be set to 04h for all SFP modules indicating serial ID module definition.

In many cases, a GBIC elects to use MOD_DEF 4 to make additional information about the GBIC available, even though the GBIC is actually compliant with one of the 6 other MOD_DEF values defined for GBICs. The extended identifier allows the GBIC to explicitly specify such compliance without requiring the MOD_DEF value to be inferred from the other information provided. The defined extended identifier values are shown in table 3.3.

TABLE 3.3: Extended identifier values

Value	Description of connector
00h	GBIC definition is not specified or the GBIC definition is not compliant with a defined MOD_DEF. See product specification for details.
01h	GBIC is compliant with MOD_DEF 1
02h	GBIC is compliant with MOD_DEF 2
03h	GBIC is compliant with MOD_DEF 3
04h	GBIC/SFP function is defined by serial ID only
05h	GBIC is compliant with MOD_DEF 5
06h	GBIC is compliant with MOD_DEF 6
07h	GBIC is compliant with MOD_DEF 7
08-FFh	Reserved

Connector

The Connector value indicates the external connector provided on the interface. This value shall be included in the serial data. The defined connector values are shown in table 3.4. Note that 01h – 05h are not SFP compatible, and are included for compatibility with GBIC standards

TABLE 3.4: Connector values

Value	Description of connector
00h	Unknown or unspecified
01h	SC
02h	Fibre Channel Style 1 copper connector
03h	Fibre Channel Style 2 copper connector
04h	BNC/TNC
05h	Fibre Channel coaxial headers
06h	FiberJack
07h	LC
08h	MT-RJ
09h	MU
0Ah	SG
0Bh	Optical pigtail
0C-1Fh	Reserved
20h	HSSDC II
21h	Copper Pigtail
22h-7Fh	Reserved
80-FFh	Vendor specific

Transceiver

The following bit significant indicators define the electronic or optical interfaces that are supported by the transceiver. At least one bit shall be set in this field. For Fibre Channel transceivers, the Fibre Channel speed, transmission media, transmitter technology, and distance capability shall all be indicated. SONET compliance codes are described in more detail in table 3.5a.

Table 3.5: Transceiver codes

Data Addr	Bit[1]	Description of transceiver	Data Addr	Bit[1]	Description of transceiver
Infiniband Compliance Codes			Fibre Channel link length		
3	4-7	Reserved	7	7	very long distance (V)
3	3	1X SX	7	6	short distance (S)
3	2	1X LX	7	5	intermediate distance (I)
3	1	1X Copper Active	7	4	long distance (L)
3	0	1X Copper Passive	Fibre Channel transmitter technology		
			7	3-2	Reserved
SONET Compliance Codes			7	1	Longwave laser (LC)
4	5-7	Reserved	7	0	Electrical inter-enclosure (EL)
4	4	SONET reach specifier bit 1	8	7	Electrical intra-enclosure (EL)
4	3	SONET reach specifier bit 2	8	6	Shortwave laser w/o OFC (SN)
4	2	OC 48, long reach	8	5	Shortwave laser w/ OFC (SL)
4	1	OC 48, intermediate reach	8	4	Longwave laser (LL)
4	0	OC 48 short reach	8	0-3	Reserved
5	7	Reserved			
5	6	OC 12, single mode long reach	Fibre Channel transmission media		
5	5	OC 12, single mode inter. reach	9	7	Twin Axial Pair (TW)
5	4	OC 12 multi-mode short reach	9	6	Shielded Twisted Pair (TP)
5	3	Reserved	9	5	Miniature Coax (MI)
5	2	OC 3, single mode long reach	9	4	Video Coax (TV)
5	1	OC 3, single mode inter. reach	9	3	Multi-mode, 62.5m (M6)
5	0	OC 3, multi-mode short reach	9	2	Multi-mode, 50 m (M5)
			9	1	Reserved
Gigabit Ethernet Compliance Codes			9	0	Single Mode (SM)
6	7-4	Reserved			
6	3	1000BASE-T	Fibre Channel speed		
6	2	1000BASE-CX	10	7-5	Reserved
6	1	1000BASE-LX	10	4	400 MBytes/Sec
6	0	1000BASE-SX	10	3	Reserved
			10	2	200 MBytes./Sec
			10	1	Reserved
			10	0	100 MBytes/Sec

[1]Bit 7 is the high order bit and is transmitted first in each byte.

The SONET compliance code bits allow the host to determine with which specifications a SONET transceiver complies. For each bit rate defined in Table 3.5 (OC-3, OC-12, OC-48), SONET specifies short reach (SR), intermediate reach (IR), and long reach (LR) requirements. For each of the three bit rates, a single short reach (SR) specification is defined. Two variations of intermediate reach (IR-1, IR-2) and three variations of long reach (LR-1, LR-2, and LR-3) are also defined for each bit rate. Byte 4, bits 0-2, and byte 5, bits 0-7 allow the user to determine which of the three reaches has been implemented – short, intermediate, or long. Two additional bits (byte 4, bits 3-4) are necessary to discriminate between different intermediate or long reach variations. These codes are defined in Table 3.5a.

Table 3.5a: SONET Compliance Specifiers

Speed	Reach	Specifier bit 1	Specifier bit 2	Description
OC-3/OC-12/OC-48	Short	0	0	SONET SR compliant
OC-3/OC-12/OC-48	Intermediate	1	0	SONET IR-1 compliant
OC-3/OC-12/OC-48	Intermediate	0	1	SONET IR-2 compliant
OC-3/OC-12/OC-48	Long	1	0	SONET LR-1 compliant
OC-3/OC-12/OC-48	Long	0	1	SONET LR-2 compliant
OC-3/OC-12/OC-48	Long	1	1	SONET LR-3 compliant

Encoding

The encoding value indicates the serial encoding mechanism that is the nominal design target of the particular transceiver. The value shall be contained in the serial data. The defined encoding values are shown in table 3.6.

Table 3.6: Encoding codes

code	Description of encoding mechanism
00h	Unspecified
01h	8B10B
02h	4B5B
03h	NRZ
04h	Manchester
05h	SONET Scrambled
06h -FFh	Reserved

BR, nominal

The nominal bit rate (BR, nominal) is specified in units of 100 Megabits per second, rounded off to the nearest 100 Megabits per second. The bit rate includes those bits necessary to encode and delimit the signal as well as those bits carrying data information. A value of 0 indicates that the bit rate is not specified and must be

determined from the transceiver technology. The actual information transfer rate will depend on the encoding of the data, as defined by the encoding value.

Length (9m)-km

Addition to EEPROM data from original GBIC definition. This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using single mode fiber. The value is in units of kilometers. A value of 255 means that the transceiver supports a link length greater than 254 km. A value of zero means that the transceiver does not support single mode fiber or that the length information must be determined from the transceiver technology.

Length (9m)

This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using single mode fiber. The value is in units of 100 meters. A value of 255 means that the transceiver supports a link length greater than 25.4 km. A value of zero means that the transceiver does not support single mode fiber or that the length information must be determined from the transceiver technology.

Length (50m)

This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using 50 micron multi-mode fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver does not support 50 micron multi-mode fiber or that the length information must be determined from the transceiver technology.

Length (62.5m)

This value specifies the link length that is supported by the transceiver while operating in compliance with the applicable standards using 62.5 micron multi-mode fiber. The value is in units of 10 meters. A value of 255 means that the transceiver supports a link length greater than 2.54 km. A value of zero means that the transceiver does not 62.5 micron multi-mode fiber or that the length information must determined from the transceiver technology. It is common for the transceiver to support both 50 micron and 62.5 micron fiber.

Length (Copper)

This value specifies the minimum link length that is supported by the transceiver while operating in compliance with the applicable standards using copper cable. The value is in units of 1 meter. A value of 255 means that the transceiver supports a link length greater than 254 meters. A value of zero means that the transceiver does not support copper cables or that the length information must be determined from the transceiver technology. Further information about the cable design, equalization, and connectors is usually required to guarantee meeting a particular length requirement.

Vendor name

The vendor name is a 16 character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h). The vendor name shall be the full name of the corporation, a commonly accepted abbreviation of the name of the corporation, the SCSI company code for the corporation, or the stock exchange code for the corporation. At least one of the vendor name or the vendor OUI fields shall contain valid serial data.

Vendor OUI

The vendor organizationally unique identifier field (vendor OUI) is a 3-byte field that contains the IEEE Company Identifier for the vendor. A value of all zero in the 3-byte field indicates that the Vendor OUI is unspecified.

Vendor PN

The vendor part number (vendor PN) is a 16-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor part number or product name. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified.

Vendor Rev

The vendor revision number (vendor rev) is a 4-byte field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's product revision number. A value of all zero in the 4-byte field indicates that the vendor PN is unspecified.

Laser Wavelength

Nominal transmitter output wavelength at room temperature. 16 bit value with byte 60 as high order byte and byte 61 as low order byte. The laser wavelength is equal to the the 16 bit integer value in nm. This field allows the user to read the laser wavelength directly, so it is not necessary to infer it from the transceiver "Code for Electronic Compatibility" (bytes 3 – 10). This also allows specification of wavelengths not covered in bytes 3 – 10, such as those used in coarse WDM systems.

CC_BASE

The check code is a one byte code that can be used to verify that the first 64 bytes of serial information in the SFP is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 0 to byte 62, inclusive.

Options

The bits in the option field shall specify the options implemented in the transceiver as described in table 3.7.

Table 3.7: Option values

data address	bit	Description of option
64	7-0	Reserved
65	7-6	Reserved
65	5	RATE_SELECT is implemented NOTE: Lack of implemention does not indicate lack of simultaneous compliance with multiple standard rates. Compliance with particular standards should be determined from Transceiver Code Section (Table 3.5)
65	4	TX_DISABLE is implemented and disables the serial output.
65	3	TX_FAULT signal implemented. (See SFP MSA)
65	2	Loss of Signal implemented, signal inverted from standard definition in SFP MSA. NOTE: This is not standard SFP/GBIC behavior and should be avoided, since non-interoperable behavior results.
65	1	Loss of Signal implemented, signal as defined in SFP MSA
65	0	Reserved

BR, max

The upper bit rate limit at which the transceiver will still meet its specifications (BR, max) is specified in units of 1% above the nominal bit rate. A value of zero indicates that this field is not specified.

BR, min

The lower bit rate limit at which the transceiver will still meet its specifications (BR, min) is specified in units of 1% below the nominal bit rate. A value of zero indicates that this field is not specified.

Vendor SN

The vendor serial number (vendor SN) is a 16 character field that contains ASCII characters, left-aligned and padded on the right with ASCII spaces (20h), defining the vendor's serial number for the transceiver. A value of all zero in the 16-byte field indicates that the vendor PN is unspecified.

Date Code

The date code is an 8-byte field that contains the vendor's date code in ASCII characters. The date code is mandatory. The date code shall be in the format specified by table 3.8.

Table 3.8: Date Code

Data Address	Description of field
84-85	ASCII code, two low order digits of year. (00 = 2000).
86-87	ASCII code, digits of month (01 = Jan through 12 = Dec)
88-89	ASCII code, day of month (01 - 31)
90-91	ASCII code, vendor specific lot code, may be blank

Diagnostic Monitoring Type

"Diagnostic Monitoring Type" is a 1 byte field with 8 single bit indicators describing how diagnostic monitoring is implemented in the particular transceiver.

Note that if bit 6, address 92 is set indicating that digital diagnostic monitoring has been implemented, received power monitoring, transmitted power monitoring, bias current monitoring, supply voltage monitoring and temperature monitoring must all be implemented. Additionally, alarm and warning thresholds must be written as specified in this document at locations 00 – 55 on 2 wire serial address 1010001X (A2h) (see Table 3.9).

Two calibration options are possible if bit 6 has been set indicating that digital diagnostic monitoring has been implemented. If bit 5, "Internally calibrated", is set, the transceiver directly reports calibrated values in units of current, power etc. If bit 4, "Externally calibrated", is set, the reported values are A/D counts which must be converted to real world units using calibration values read using 2 wire serial address 1010001X (A2h) from bytes 55 - 95. See "Diagnostics" section for details.

Bit 3 indicates whether the received power measurement represents average input optical power or OMA. If the bit is set, average power is monitored. If it is not, OMA is monitored.

Addressing Modes

Bit 2 indicates whether or not it is necessary for the host to perform an address change sequence before accessing information at 2-wire serial address A2h. If this bit is not set, the host may simply read from either address, A0h or A2h, by using that value in the address byte during the 2-wire communication sequence. If the bit is set, the following sequence must be executed prior to accessing information at address A2h. Once A2h has been accessed, it will be necessary to execute the address change sequence again prior to reading from A0h. The address change sequence is defined as the following steps on the 2 wire serial interface:

1) Host controller performs a Start condition, followed by a slave address of 0b00000000.
-- Note that the R/W bit of this address indicates transfer from host to device (‘0’b).
2) Device responds with Ack
3) Host controller transfers 0b00000100 (04h) as the next 8 bits of data
-- This value indicates that the device is to change its address
4) Device responds with Ack
5) Host controller transfers one of the following values as the next 8 bits of data:
--0bXXXXXX00 – specifies Serial ID memory page
--0bXXXXXX10 – specifies Digital Diagnostic memory page
6) Device responds with Ack
7) Host controller performs a Stop condition
8) Device changes address that it responds to, based on the Step 5 byte value above:
--0bXXXXXX00 – address becomes 0b1010000X (A0h)
--0bXXXXXX10 – address becomes 0b1010001X (A2h)

Table 3.9: Diagnostic Monitoring Type

Data Address	Bits	Description
92	7	Reserved for legacy diagnostic implementations. Must be ‘0’ for compilance with this document.
92	6	Digital diagnostic monitoring implemented (described in this document). Must be ‘1’ for compliance with this document.
92	5	Internally Calibrated
92	4	Externally Calibrated
92	3	Received power measurement type 0 = OMA, 1 = Average Power
92	2	Address change required see section above, “addressing modes”
92	1-0	Reserved

Enhanced Options

“Enhanced Options” is a 1 byte field with 8 single bit indicators which describe the optional digital diagnostic features implemented in the transceiver. Since transceivers will not necessarily implement all optional features described in this document, the “Enhanced Options” bit field allows the host system to determine which functions are available over the 2 wire serial bus. A ‘1’ indicates that the particular function is implemented in the transceiver. Bits 3 and 6 of byte 110 (see Table 3.17) allow the

user to control the Rate_Select and TX_Disable functions. If these functions are not implemented, the bits remain readable and writable, but the transceiver ignores them.

Note that the "soft" control functions - TX_DISABLE, TX_FAULT, RX_LOS, and RATE_SELECT do not meet the timing requirements specified in the SFP MSA section B3 "Timing Requirements of Control and Status I/O" and the GBIC Specification, revision 5.5, (SFF-8053), section 5.3.1, for their corresponding pins. The soft functions allow a host to poll or set these values over the serial bus as an alternative to monitoring/setting pin values. Timing is vendor specific, but must meet the requirements specified in Table 3.11 below.

Table 3.10: Enhanced Options

Data Address	Bits	Description
93	7	Optional Alarm/warning flags implemented for all monitored quantities (see Table 3.18)
93	6	Optional Soft TX_DISABLE control and monitoring implemented
93	5	Optional Soft TX_FAULT monitoring implemented
93	4	Optional Soft RX_LOS monitoring implemented
93	3	Optional Soft RATE_SELECT control and monitoring implemented
93	2-0	Reserved

Table 3.11: I/O Timing for Soft Control & Status Functions

Parameter	Symbol	Min	Max	Units	Conditions
TX_DISABLE assert time	t_off		100	ms	Time from TX_DISABLE bit set[1] until optical output falls below 10% of nominal
TX_DISABLE deassert time	t_on		100	ms	Time from TX_DISABLE bit cleared[1] until optical output rises above 90% of nominal
Time to initialize, including reset of TX_FAULT	t_init		300	ms	Time from power on or negation of TX_FAULT using TX_DISABLE until transmitter output is stable[2].
TX_FAULT assert time	t_fault		100	ms	Time from fault to TX_FAULT bit set.
LOS assert time	t_loss_on		100	ms	Time from LOS state to RX_LOS bit set
LOS deassert time	t_loss_off		100	ms	Time from non-LOS state to RX_LOS bit cleared
Rate select change time	T_rate_sel		100	ms	Time from change of state of Rate Select bit[1] until receiver bandwidth is in conformance with appropriate specification
Serial ID clock rate	f_serial_clock		100	kHz	n/a
Analog parameter data ready	t_data		1000	ms	From power on to data ready, bit 0 of byte 110 set
Serial bus hardware ready	t_serial		300	ms	Time from power on until module is ready for data transmission over the serial bus.

[1] measured from falling clock edge after stop bit of write transaction.
[2] See Gigabit Interface Converter (GBIC). SFF-0053, rev. 5.5, September 27, 2000

SFF-8472 Compliance

Byte 94 contains an unsigned integer that indicates which feature set(s) are implemented in the transceiver.

Table 3.12: SFF-8472 Compliance

Data Address	Value	Interpretation
94	0	Digital diagnostic functionality not included or undefined.
94	1	Includes functionality described in Rev 9.3 SFF-8472.
94	2	TBD
94	3	TBD

CC_EXT

The check code is a one byte code that can be used to verify that the first 32 bytes of extended serial information in the SFP is valid. The check code shall be the low order 8 bits of the sum of the contents of all the bytes from byte 64 to byte 94, inclusive.

Diagnostics

2 wire serial bus address 1010001X (A2h) is used to access measurements of transceiver temperature, internally measured supply voltage, TX bias current, TX output power, received optical power, and two additional quantities to be defined in the future.

The values are interpreted differently depending upon the option bits set at address 92. If bit 5 “internally calibrated” is set, the values are calibrated absolute measurements, which should be interpreted according to the section “Internal Calibration” below. If bit 4 “externally calibrated” is set, the values are A/D counts, which are converted into real units per the subsequent section titled “External Calibration”.

Measured parameters are reported in 16 bit data fields, i.e., two concatenated bytes. The 16 bit data fields allow for wide dynamic range. This is not intended to imply that a 16 bit A/D system is recommended or required in order to achieve the accuracy goals stated below. The width of the data field should not be taken to imply a given level of precision. It is conceivable that the accuracy goals herein can be achieved by a system having less than 16 bits of resolution. It is recommended that any low-order data bits beyond the system’s specified accuracy be fixed at zero. Overall system accuracy and precision will be vendor dependent.

To guarantee coherency of the diagnostic monitoring data, the host is required to retrieve any multi-byte fields from the diagnostic monitoring data structure (IE: Rx Power MSB - byte 104 in A2h, Rx Power LSB - byte 105 in A2h) by the use of a single two-byte read sequence across the serial interface.

The transceiver is required to insure that any multi-byte fields which are updated with diagnostic monitoring data (e.g. Rx Power MSB - byte 104 in A2h, Rx Power LSB - byte 105 in A2h) must have this update done in a fashion which guarantees coherency and consistency of the data. In other words, the update of a multi-byte field by the transceiver must not occur such that a partially updated multi-byte field can be transferred to the host. Also, the transceiver shall not update a multi-byte field within the structure during the transfer of that multi-byte field to the host, such that partially updated data would be transferred to the host.

Accuracy requirements specified below shall apply to the operating signal range specified in the relevant standard. The manufacturer’s specification should be consulted for more detail on the conditions under which the accuracy requirements are met.

Internal Calibration

Measurements are calibrated over vendor specified operating temperature and voltage and should be interpreted as defined below. Alarm and warning threshold values should be interpreted in the same manner as real time 16 bit data.

1) Internally measured transceiver temperature. Represented as a 16 bit signed twos complement value in increments of 1/256 degrees Celsius, yielding a total range of –128C to +128C. Temperature accuracy is vendor specific but must be better than ±3 degrees Celsius over specified operating temperature and voltage. Please see vendor specification for details on location of temperature sensor. The temperature in degrees Celsius is given by the signed twos complement value with LSB equal to 1/256 C. See Tables 3.13 and 3.14 below for examples of temperature format.

2) Internally measured transceiver supply voltage. Represented as a 16 bit unsigned integer with the voltage defined as the full 16 bit value (0 – 65535) with LSB equal to 100 µVolt, yielding a total range of 0 to +6.55 Volts. Practical considerations to be defined by transceiver manufacturer will tend to limit the actual bounds of the supply voltage measurement. Accuracy is vendor specific but must be better than ±3% of the manufacturer's nominal value over specified operating temperature and voltage. Note that in some transceivers, transmitter supply voltage and receiver supply voltage are isolated. In that case, only one supply is monitored. Refer to the device specification for more detail.

3) Measured TX bias current in µA. Represented as a 16 bit unsigned integer with the current defined as the full 16 bit value (0 – 65535) with LSB equal to 2 µA, yielding a total range of 0 to 131 mA. Accuracy is vendor specific but must be better than ±10% of the manufacturer's nominal value over specified operating temperature and voltage.

4) Measured TX output power in mW. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 – 65535) with LSB equal to 0.1 µW, yielding a total range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). Data is assumed to be based on measurement of laser monitor photodiode current. It is factory calibrated to absolute units using the most representative fiber output type. Accuracy is vendor specific but must be better than ±3dB over specified temperature and voltage. Data is not valid when the transmitter is disabled.

5) Measured RX received optical power in mW. Value can represent either average received power or OMA depending upon how bit 3 of byte 92 (A0h) is set. Represented as a 16 bit unsigned integer with the power defined as the full 16 bit value (0 – 65535) with LSB equal to 0.1 µW, yielding a total range of 0 to 6.5535 mW (~ -40 to +8.2 dBm). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than ±3dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss)

per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is vendor specific.

Tables 3.13 and 3.14 below illustrate the 16 bit signed twos complement format used for temperature reporting. The most significant bit (D7) represents the sign, which is zero for positive temperatures and one for negative temperatures.

Table 3.13: Bit weights (°C) for temperature reporting registers

Most Significant Byte (byte 96)								Least Significant Byte (byte 97)							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
SIGN	64	32	16	8	4	2	1	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256

Table 3.14: Digital temperature format

Temperature		BINARY		HEXADECIMAL	
DECIMAL	FRACTION	HIGH BYTE	LOW BYTE	HIGH BYTE	LOW BYTE
+127.996	+127 255/256	01111111	11111111	7F	FF
+125.000	+125	01111101	00000000	7D	00
+25.000	+25	00011001	00000000	19	00
+1.004	+1 1/256	00000001	00000001	01	01
+1.000	+1	00000001	00000000	01	00
+0.996	+255/256	00000000	11111111	00	FF
+0.004	+1/256	00000000	00000001	00	01
0.000	0	00000000	00000000	00	00
-0.004	-1/256	11111111	11111111	FF	FF
-1.000	-1	11111111	00000000	FF	00
-25.000	-25	11100111	00000000	E7	00
-40.000	-40	11011000	00000000	D8	00
-127.996	-127 255/256	10000000	00000001	80	01
-128.000	-128	10000000	00000000	80	00

External Calibration

Measurements are raw A/D values and must be converted to real world units using calibration constants stored in EEPROM locations 56 – 95 at 2 wire serial bus address A2h. Calibration is valid over vendor specified operating temperature and voltage. Alarm and warning threshold values should be interpreted in the same manner as real time 16 bit data.

After calibration per the equations given below for each variable, the results are consistent with the accuracy and resolution goals for internally calibrated devices.

1) Internally measured transceiver temperature. Module temperature, T, is given by the following equation: $T(C) = T_{slope} * T_{AD}$ (16 bit signed twos complement value) + T_{offset}. The result is in units of 1/256C, yielding a total range of –128C to +128C. See Table 3.16 for locations of T_{SLOPE} and T_{OFFSET}. Temperature accuracy is vendor specific but must be better than ±3 degrees Celsius over specified operating temperature and voltage. Please see vendor specification sheet for details on location of temperature sensor. Tables 3.13 and 3.14 above give examples of the 16 bit signed twos complement temperature format.

2) Internally measured supply voltage. Module internal supply voltage, V, is given in microvolts by the following equation: $V(\mu V) = V_{SLOPE} * V_{AD}$ (16 bit unsigned integer) + V_{OFFSET}. The result is in units of 100μV, yielding a total range of 0 – 6.55V. See Table 3.16 for locations of V_{SLOPE} and V_{OFFSET}. Accuracy is vendor specific but must be better than ±3% of the manufacturer's nominal value over specified operating temperature and voltage. Note that in some transceivers, transmitter supply voltage and receiver supply voltage are isolated. In that case, only one supply is monitored. Refer to the manufacturer's specification for more detail.

3) Measured transmitter laser bias current. Module laser bias current, I, is given in microamps by the following equation: $I(\mu A) = I_{SLOPE} * I_{AD}$ (16 bit unsigned integer) + I_{OFFSET}. This result is in units of 2 μA, yielding a total range of 0 to 131 mA. See Table 3.16 for locations of I_{SLOPE} and I_{OFFSET}. Accuracy is vendor specific but must be better than ±10% of the manufacturer's nominal value over specified operating temperature and voltage.

4) Measured coupled TX output power. Module transmitter coupled output power, TX_PWR, is given in μW by the following equation: $TX\_PWR\ (\mu W) = TX\_PWR_{SLOPE} * TX\_PWR_{AD}$ (16 bit unsigned integer) + TX_PWR_{OFFSET}. This result is in units of 0.1μW yielding a total range of 0 – 6.5mW. See Table 3.16 for locations of TX_PWR_{SLOPE} and TX_PWR_{OFFSET}. Accuracy is vendor specific but must be better than ±3dB over specified operating temperature and voltage. Data is assumed to be based on measurement of a laser monitor photodiode current. It is factory calibrated to absolute units using the most representative fiber output type. Data is not valid when the transmitter is disabled.

5) Measured received optical power. Received power, RX_PWR, is given in µW by the following equation:

Rx_PWR (µW) = Rx_PWR(4) * $Rx\_PWR_{AD}^4$ (16 bit unsigned integer) + Rx_PWR(3)*$Rx\_PWR_{AD}^3$(16 bit unsigned integer) + Rx_PWR(2)*$Rx\_PWR_{AD}^2$(16 bit unsigned integer) + Rx_PWR(1) *Rx_PWR_{AD} (16 bit unsigned integer) + Rx_PWR(0)

The result is in units of 0.1µW yielding a total range of 0 – 6.5mW. See Table 3.16 for locations of Rx_PWR(4-0). Absolute accuracy is dependent upon the exact optical wavelength. For the vendor specified wavelength, accuracy shall be better than ±3dB over specified temperature and voltage. This accuracy shall be maintained for input power levels up to the lesser of maximum transmitted or maximum received optical power per the appropriate standard. It shall be maintained down to the minimum transmitted power minus cable plant loss (insertion loss or passive loss) per the appropriate standard. Absolute accuracy beyond this minimum required received input optical power range is vendor specific.

Alarm and Warning Thresholds

Each A/D quantity has a corresponding high alarm, low alarm, high warning and low warning threshold. These factory preset values allow the user to determine when a particular value is outside of “normal” limits as determined by the transceiver manufacturer. It is assumed that these values will vary with different technologies and different implementations. When external calibration is used, data may be compared to alarm and warning threshold values before or after calibration by the host. Comparison can be done directly before calibration. If comparison is to be done after calibration, calibration must first be applied to both data and threshold values.

The values reported in the alarm and warning thresholds area (see below) may be temperature compensated or otherwise adjusted when setting warning and/or alarm flags. Any threshold compensation or adjustment is vendor specific and optional. See vendor’s data sheet for use of alarm and warning thresholds.

Table 3.15: Alarm and Warning Thresholds (2-Wire Address A2h)

Address	# Bytes	Name	Description
00-01	2	Temp High Alarm	MSB at low address
02-03	2	Temp Low Alarm	MSB at low address
04-05	2	Temp High Warning	MSB at low address
06-07	2	Temp Low Warning	MSB at low address
08-09	2	Voltage High Alarm	MSB at low address
10-11	2	Voltage Low Alarm	MSB at low address
12-13	2	Voltage High Warning	MSB at low address
14-15	2	Voltage Low Warning	MSB at low address
16-17	2	Bias High Alarm	MSB at low address
18-19	2	Bias Low Alarm	MSB at low address
20-21	2	Bias High Warning	MSB at low address
22-23	2	Bias Low Warning	MSB at low address
24-25	2	TX Power High Alarm	MSB at low address
26-27	2	TX Power Low Alarm	MSB at low address
28-29	2	TX Power High Warning	MSB at low address
30-31	2	TX Power Low Warning	MSB at low address
32-33	2	RX Power High Alarm	MSB at low address
34-35	2	RX Power Low Alarm	MSB at low address
36-37	2	RX Power High Warning	MSB at low address
38-39	2	RX Power Low Warning	MSB at low address
40-55	16	Reserved	Reserved for future monitored quantities

Calibration Constants

TABLE 3.16: Calibration constants for External Calibration Option (2 Wire Address A2h)

Address	# Bytes	Name	Description
56-59	4	Rx_PWR(4)	Single precision floating point calibration data - Rx optical power. Bit 7 of byte 56 is MSB. Bit 0 of byte 59 is LSB. Rx_PWR(4) should be set to zero for “internally calibrated” devices.
60-63	4	Rx_PWR(3)	Single precision floating point calibration data - Rx optical power. Bit 7 of byte 60 is MSB. Bit 0 of byte 63 is LSB. Rx_PWR(3) should be set to zero for “internally calibrated” devices.
64-67	4	Rx_PWR(2)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 64 is MSB, bit 0 of byte 67 is LSB. Rx_PWR(2) should be set to zero for “internally calibrated” devices.
68-71	4	Rx_PWR(1)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 68 is MSB, bit 0 of byte 71 is LSB. Rx_PWR(1) should be set to 1 for “internally calibrated” devices.
72-75	4	Rx_PWR(0)	Single precision floating point calibration data, Rx optical power. Bit 7 of byte 72 is MSB, bit 0 of byte 75 is LSB. Rx_PWR(0) should be set to zero for “internally calibrated” devices.
76-77	2	Tx_I(Slope)	Fixed decimal (unsigned) calibration data, laser bias current. Bit 7 of byte 76 is MSB, bit 0 of byte 77 is LSB. Tx_I(Slope) should be set to 1 for “internally calibrated” devices.
78-79	2	Tx_I(Offset)	Fixed decimal (signed two’s complement) calibration data, laser bias current. Bit 7 of byte 78 is MSB, bit 0 of byte 79 is LSB. Tx_I(Offset) should be set to zero for “internally calibrated” devices.
80-81	2	Tx_PWR(Slope)	Fixed decimal (unsigned) calibration data, transmitter coupled output power. Bit 7 of byte 80 is MSB, bit 0 of byte 81 is LSB. Tx_PWR(Slope) should be set to 1 for “internally calibrated” devices.
82-83	2	Tx_PWR(Offset)	Fixed decimal (signed two’s complement) calibration data, transmitter coupled output power. Bit 7 of byte 82 is MSB, bit 0 of byte 83 is LSB. Tx_PWR(Offset) should be set to zero for “internally calibrated” devices.
84-85	2	T (Slope)	Fixed decimal (unsigned) calibration data, internal module temperature. Bit 7 of byte 84 is MSB, bit 0 of byte 85 is LSB. T(Slope) should be set to 1 for “internally calibrated” devices.
86-87	2	T (Offset)	Fixed decimal (signed two’s complement) calibration data, internal module temperature. Bit 7 of byte 86 is MSB, bit 0 of byte 87 is LSB. T(Offset) should be set to zero for “internally calibrated” devices.
88-89	2	V (Slope)	Fixed decimal (unsigned) calibration data, internal module supply voltage. Bit 7 of byte 88 is MSB, bit 0 of byte 89 is LSB. V(Slope) should be set to 1 for “internally calibrated” devices.
90-91	2	V (Offset)	Fixed decimal (signed two’s complement) calibration data, internal module supply voltage. Bit 7 of byte 90 is MSB. Bit 0 of byte 91 is LSB. V(Offset) should be set to zero for “internally calibrated” devices.
92-4	3	Reserved	Reserved
95	1	Checksum	Byte 95 contains the low order 8 bits of the sum of bytes 0 – 94.

The slope constants at addresses 76, 80,84, and 88, are unsigned fixed-point binary numbers. The slope will therefore always be positive. The binary point is in between the upper and lower bytes, i.e., between the eight and ninth most significant bits. The most significant byte is the integer portion in the range 0 to +255. The least significant byte represents the fractional portion in the range of 0.00391 (1/256) to 0.9961 (255/256). The smallest real number that can be represented by this format is 0.00391 (1/256); the largest real number that can be represented using this format is 255.9961 (255 + 255/256). Slopes are defined, and conversion formulas found, in the "External Calibration" section. Examples of this format are illustrated below:

Table 3.16a: Unsigned fixed-point binary format for slopes

Decimal Value	Binary Value		Hexadecimal Value	
	MSB	LSB	High Byte	Low Byte
0.0000	00000000	00000000	00	00
0.0039	00000000	00000001	00	01
1.0000	00000001	00000000	01	00
1.0313	00000001	00001000	01	08
1.9961	00000001	11111111	01	FF
2.0000	00000010	00000000	02	00
255.9921	11111111	11111110	FF	FE
255.9961	11111111	11111111	FF	FF

The calibration offsets are 16-bit signed twos complement binary numbers. The offsets are defined by the formulas in the "External Calibration" section. The least significant bit represents the same units as described above under "Internal Calibration" for the corresponding analog parameter, e.g., 2μA for bias current, 0.1μW for optical power, etc. The range of possible integer values is from +32767 to -32768. Examples of this format are shown below.

Table 3.16b: Format for offsets

Decimal Value	Binary Value		Hexadecimal Value	
	High Byte	Low Byte	High Byte	Low Byte
+32767	01111111	1111111	7F	FF
+3	00000000	00000011	00	03
+2	00000000	00000010	00	02
+1	00000000	00000001	00	01
0	00000000	00000000	00	00
-1	11111111	11111111	FF	FF
-2	11111111	11111110	FF	FE
-3	11111111	11111101	FF	FD
-32768	10000000	00000000	80	00

External calibration of received optical power makes use of single-precision floating-point numbers as defined by *IEEE Standard for Binary Floating-Point Arithmetic*, IEEE Std 754-1985. Briefly, this format utilizes four bytes (32 bits) to represent real numbers. The first and most significant bit is the sign bit; the next eight bits indicate an exponent in the range of +126 to –127; the remaining 23 bits represent the mantissa. The 32 bits are therefore arranged as in Table 3.16c below.

Table 3.16c: IEEE-754 Single-Precision Floating Point Number Format

FUNCTION	SIGN	EXPONENT	MANTISSA		
BIT	31	30……23	22……0		
BYTE	3		2	1	0
← Most Significant					Least Significant →

Rx_PWR(4), as an example, is stored as in Table 3.16d.

Table 3.16d: Example of Floating Point Representation

BYTE ADDRESS	CONTENTS	SIGNIFICANCE
56	SEEEEEEE	Most
57	EMMMMMMM	2nd Most
58	MMMMMMMM	2nd Least
59	MMMMMMMM	Least

where S = sign bit; E = exponent bit; M = mantissa bit.

Special cases of the various bit values are reserved to represent indeterminate values such as positive and negative infinity; zero; and “NaN”or not a number. NaN indicates an invalid result. As of this writing, explanations of the IEEE single precision floating point format were posted on the worldwide web at

http://www.psc.edu/general/software/packages/ieee/ieee.html

and

http://research.microsoft.com/~hollasch/cgindex/coding/ieeefloat.html.

The actual IEEE standard is available at www.IEEE.org.

Real Time Diagnostic Registers

TABLE 3.17: A/D Values and Status Bits (2 Wire Address A2h)

Byte	Bit	Name	Description
Converted analog values. Calibrated 16 bit data.			
96	All	Temperature MSB	Internally measured module temperature.
97	All	Temperature LSB	
98	All	Vcc MSB	Internally measured supply voltage in transceiver.
99	All	Vcc LSB	
100	All	TX Bias MSB	Internally measured TX Bias Current.
101	All	TX Bias LSB	
102	All	TX Power MSB	Measured TX output power.
103	All	TX Power LSB	
104	All	RX Power MSB	Measured RX input power.
105	All	RX Power LSB	
106	All	Reserved MSB	Reserved for 1st future definition of digitized analog input
107	All	Reserved LSB	Reserved for 1st future definition of digitized analog input
108	All	Reserved MSB	Reserved for 2nd future definition of digitized analog input
109	All	Reserved LSB	Reserved for 2nd future definition of digitized analog input
Optional Status/Control Bits			
110	7	TX Disable State	Digital state of the TX Disable Input Pin. Updated within 100msec of change on pin.
110	6	Soft TX Disable	Read/write bit that allows software disable of laser. Writing '1' disables laser. Turn on/off time is 100 msec max from acknowledgement of serial byte transmission. This bit is "OR"d with the hard TX_DISABLE pin value. Note, per SFP MSA TX_DISABLE pin is default enabled unless pulled low by hardware. If Soft TX Disable is not implemented, the transceiver ignores the value of this bit. Default power up value is 0.
110	5	Reserved	
110	4	RX Rate Select State	Digital state of the SFP RX Rate Select Input Pin. Updated within 100msec of change on pin.
110	3	Soft RX Rate Select	Read/write bit that allows software RX rate select. Writing '1' selects full bandwidth operation. This bit is "OR'd with the hard RX RATE_SELECT pin value. Enable/disable time is 100msec max from acknowledgement of serial byte transmission. Soft RX rate select does not meet the autonegotiation requirements specified in FC-FS. Default at power up is zero. If Soft RX Rate Select is not implemented, the transceiver ignores the value of this bit.
110	2	TX Fault	Digital state of the TX Fault Output Pin. Updated within 100msec of change on pin.
110	1	LOS	Digital state of the LOS Output Pin. Updated within 100msec of change on pin.
110	0	Data_Ready_Bar	Indicates transceiver has achieved power up and data is ready. Bit remains high until data is ready to be read at which time the device sets the bit low.
111	7-0	Reserved	Reserved.

The data_ready_bar bit is high during module power up and prior to the first valid A/D reading. Once the first valid A/D reading occurs, the bit is set low until the device is powered down. The bit must be set low within 1 second of power up.

Bytes 112 – 119 contain an optional set of alarm and warning flags. The flags may be latched or non-latched. Implementation is vendor specific, and the vendor's specification sheet should be consulted for details. It is recommended that in either case, detection of an asserted flag bit should be verified by a second read of the flag at least 100msec later. For users who do not wish to set their own threshold values or read the values in locations 0 - 55, the flags alone can be monitored. Two flag types are defined.

1) Alarm flags associated with transceiver temperature, supply voltage, TX bias current, TX output power and received optical power as well as reserved locations for future flags. Alarm flags indicate conditions likely to be associated with an in-operational link and cause for immediate action.

2) Warning flags associated with transceiver temperature, supply voltage, TX bias current, TX output power and received optical power as well as reserved locations for future flags. Warning flags indicate conditions outside the normally guaranteed bounds but not necessarily causes of immediate link failures. Certain warning flags may also be defined by the manufacturer as end-of-life indicators (such as for higher than expected bias currents in a constant power control loop).

Alarm and Warning Flags

Table 3.18: Alarm and Warning Flag Bits (2-Wire Address A2h)

Reserved Optional Alarm and Warning Flag Bits (See Notes 3-6)			
112	7	Temp High Alarm	Set when internal temperature exceeds high alarm level.
112	6	Temp Low Alarm	Set when internal temperature is below low alarm level.
112	5	Vcc High Alarm	Set when internal supply voltage exceeds high alarm level.
112	4	Vcc Low Alarm	Set when internal supply voltage is below low alarm level.
112	3	TX Bias High Alarm	Set when TX Bias current exceeds high alarm level.
112	2	TX Bias Low Alarm	Set when TX Bias current is below low alarm level.
112	1	TX Power High Alarm	Set when TX output power exceeds high alarm level.
112	0	TX Power Low Alarm	Set when TX output power is below low alarm level.
113	7	RX Power High Alarm	Set when Received Power exceeds high alarm level.
113	6	RX Power Low Alarm	Set when Received Power is below low alarm level.
113	5	Reserved Alarm	
113	4	Reserved Alarm	
113	3	Reserved Alarm	
113	2	Reserved Alarm	
113	1	Reserved Alarm	
113	0	Reserved Alarm	
114	All	Reserved	
115	All	Reserved	
116	7	Temp High Warning	Set when internal temperature exceeds high warning level.
116	6	Temp Low Warning	Set when internal temperature is below low warning level.
116	5	Vcc High Warning	Set when internal supply voltage exceeds high warning level.
116	4	Vcc Low Warning	Set when internal supply voltage is below low warning level.
116	3	TX Bias High Warning	Set when TX Bias current exceeds high warning level.
116	2	TX Bias Low Warning	Set when TX Bias current is below low warning level.
116	1	TX Power High Warning	Set when TX output power exceeds high warning level.
116	0	TX Power Low Warning	Set when TX output power is below low warning level.
117	7	RX Power High Warning	Set when Received Power exceeds high warning level.
117	6	RX Power Low Warning	Set when Received Power is below low warning level.
117	5	Reserved Warning	
117	4	Reserved Warning	
117	3	Reserved Warning	
117	2	Reserved Warning	
117	1	Reserved Warning	
117	0	Reserved Warning	
118	All	Reserved	
119	All	Reserved	

Vendor Specific Locations

Bytes 120 – 127 are defined for vendor specific functions.

Table 3.19: Vendor Specific Memory Addresses (2-Wire Address A2h)

Byte	Bit	Name	Description
120-127	All	Vendor Specific	Vendor Specific

User Accessible EEPROM

Table 3.20: User EEPROM (2-Wire Address A2h)

Address	# Bytes	Name	Description
128-247	120	User EEPROM	User writable EEPROM
248-255	8	Vendor Specific	Vendor specific control functions