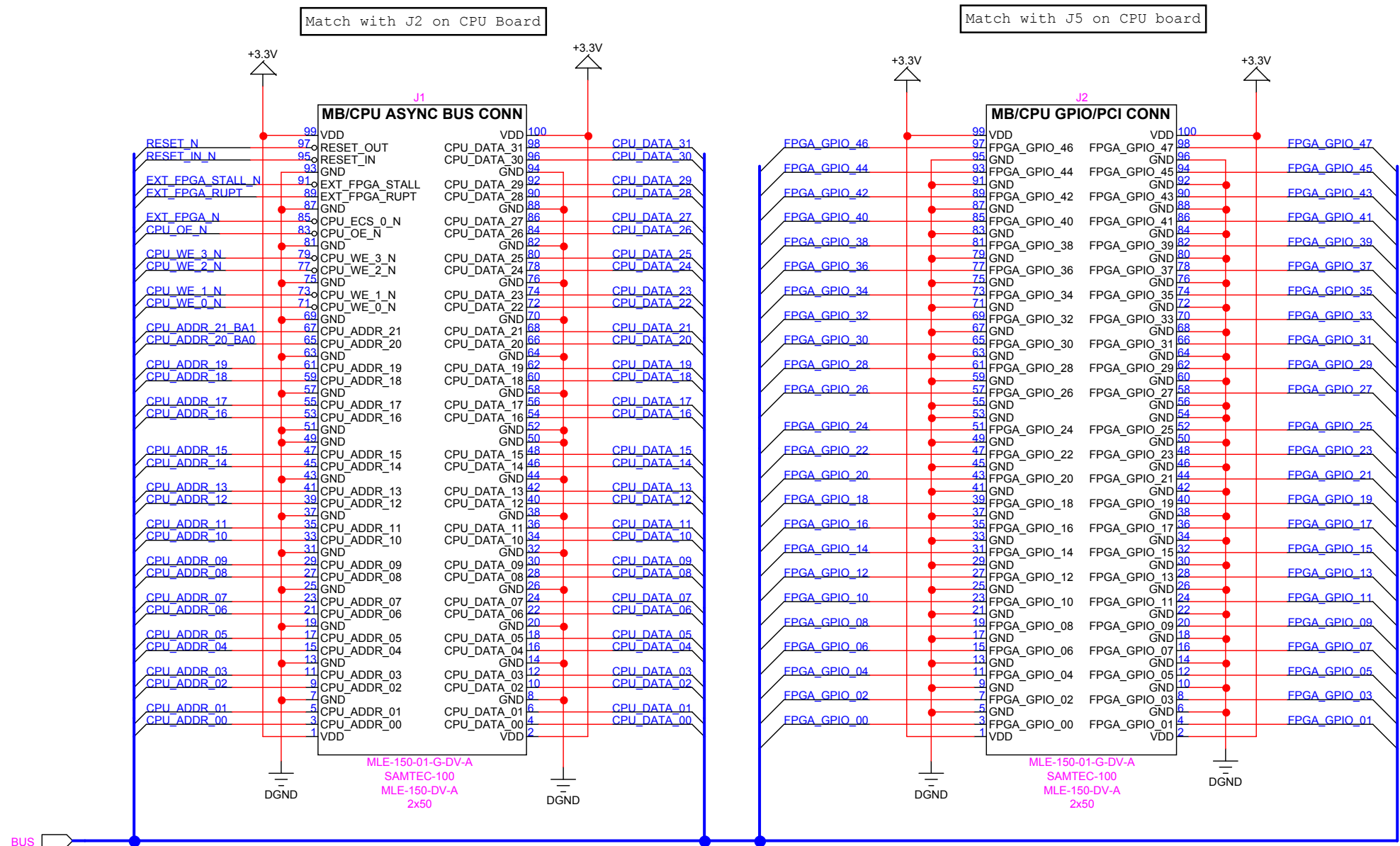


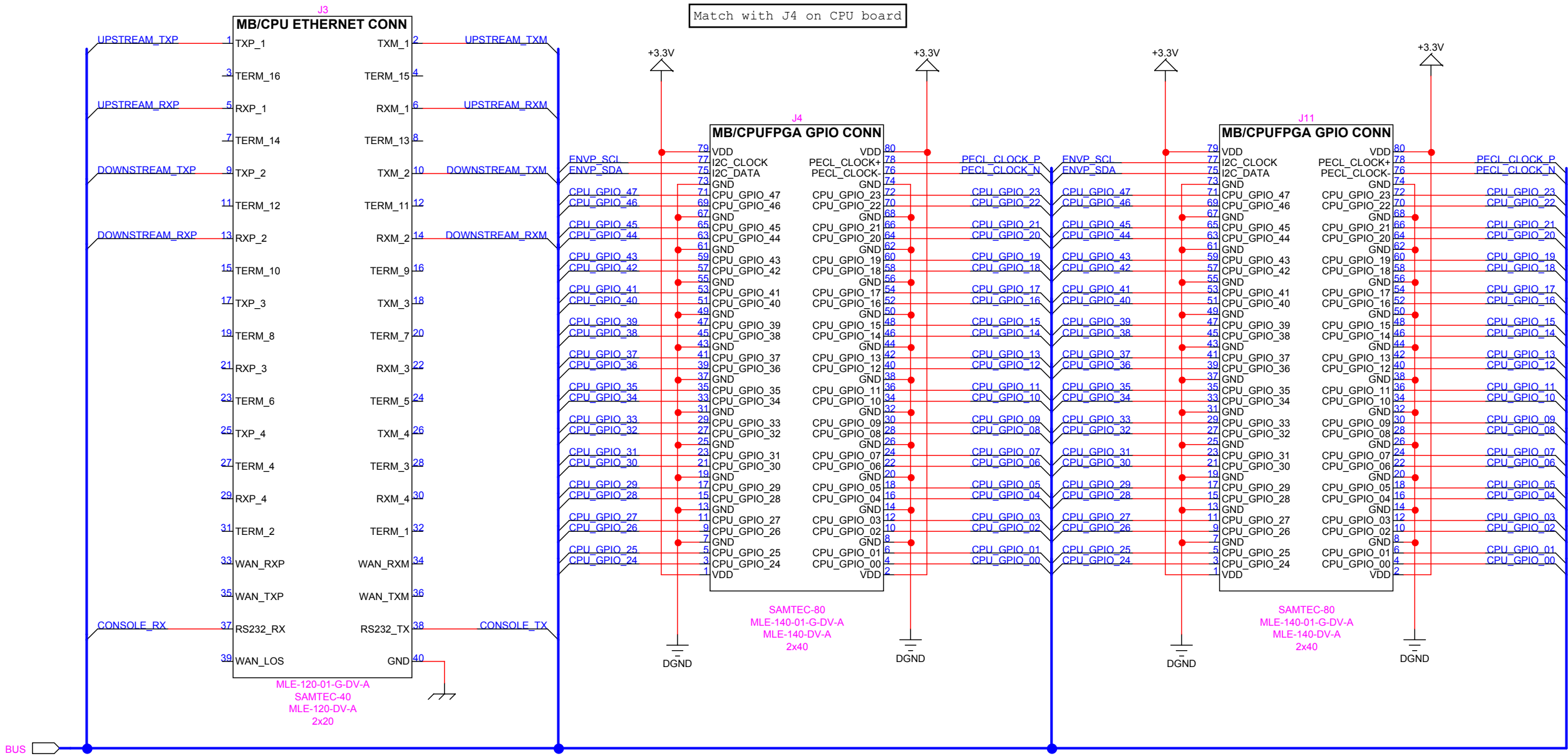
# CPU BOARD INTERFACE



# CPU ETHERNET AND GPIO

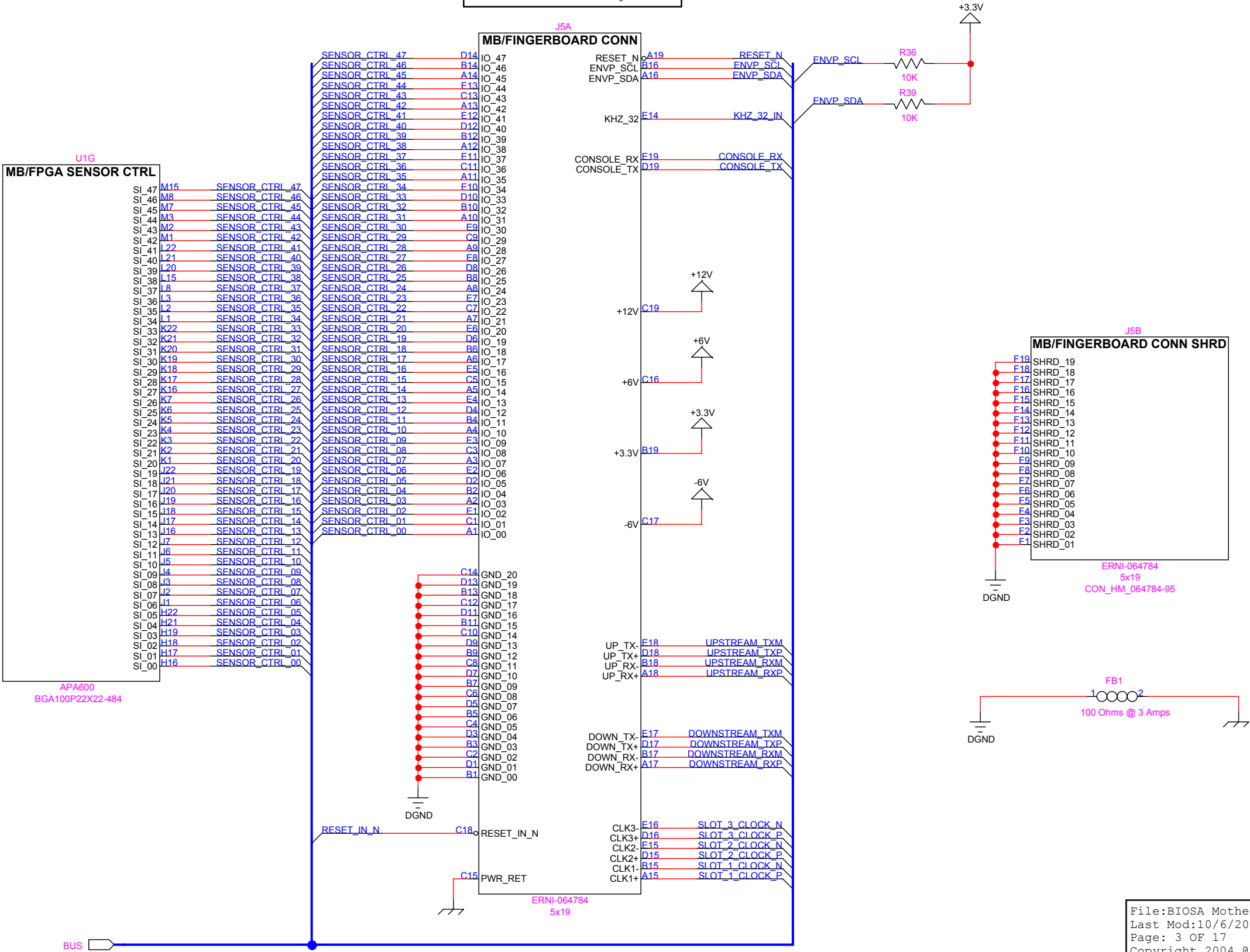
4 RJ45 Compatible ports  
Match with J6 on CPU board

Match with J4 on CPU board

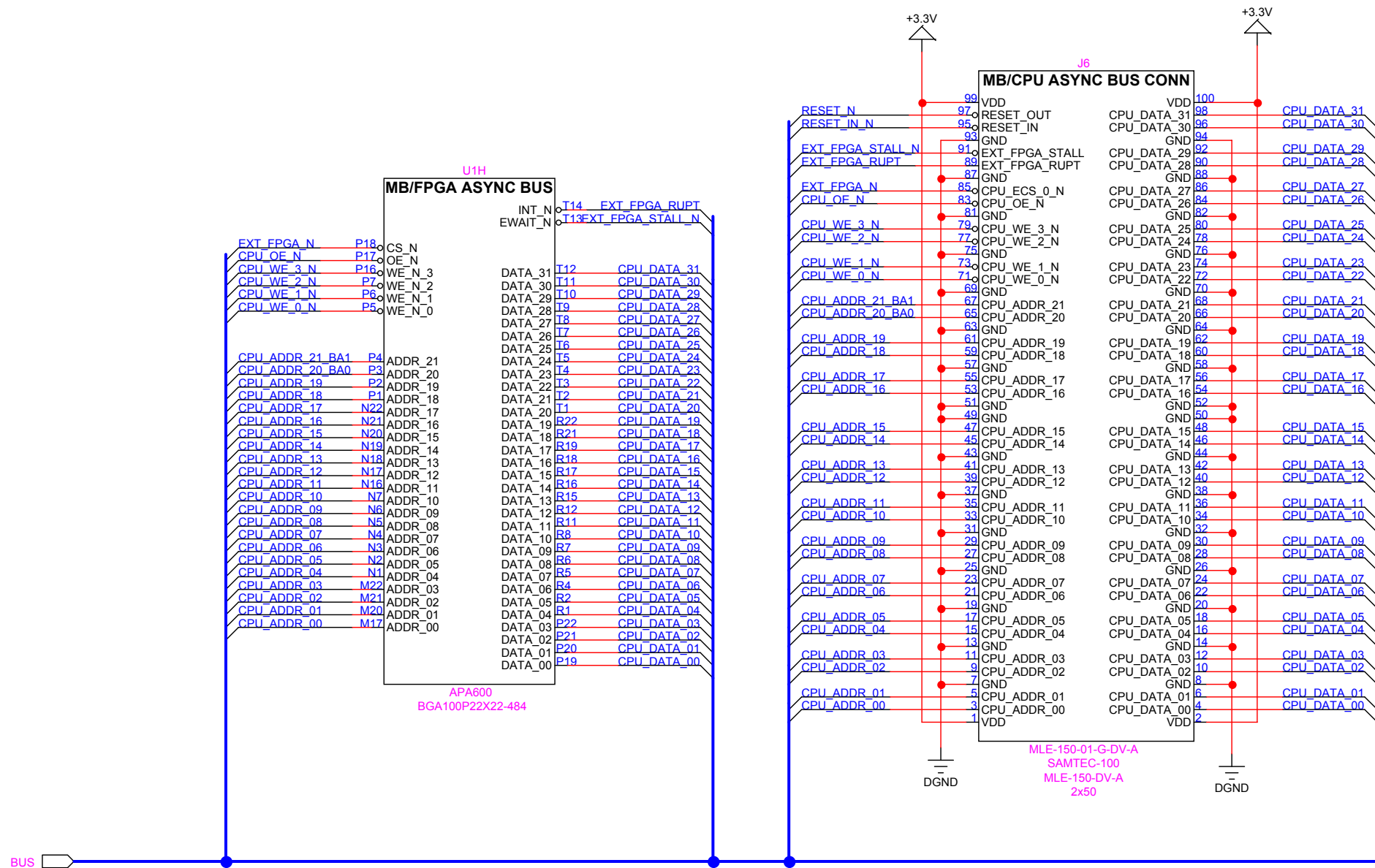


# FINGERBOARD INTERFACE

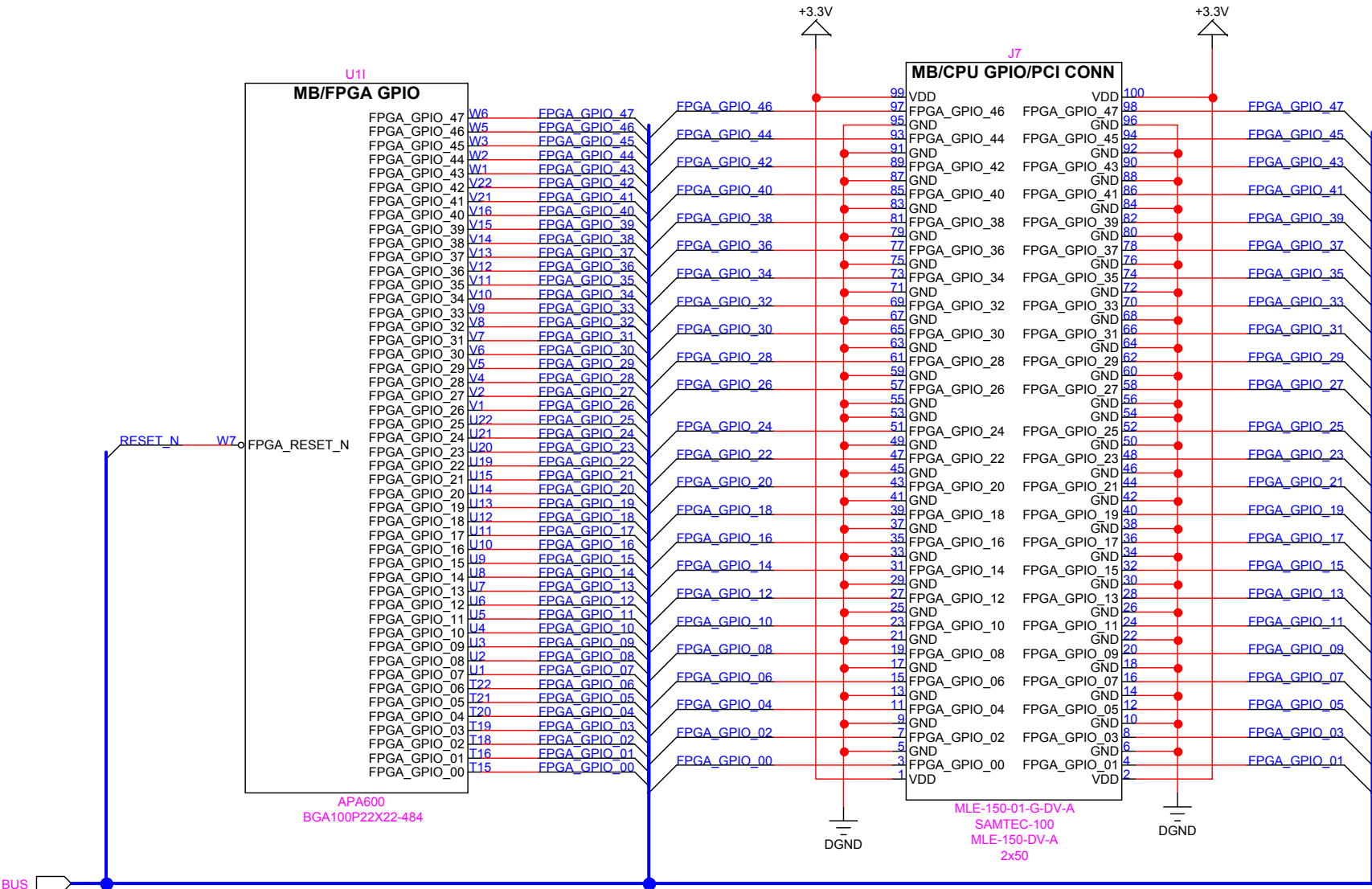
Match with J1 on Fingerboard



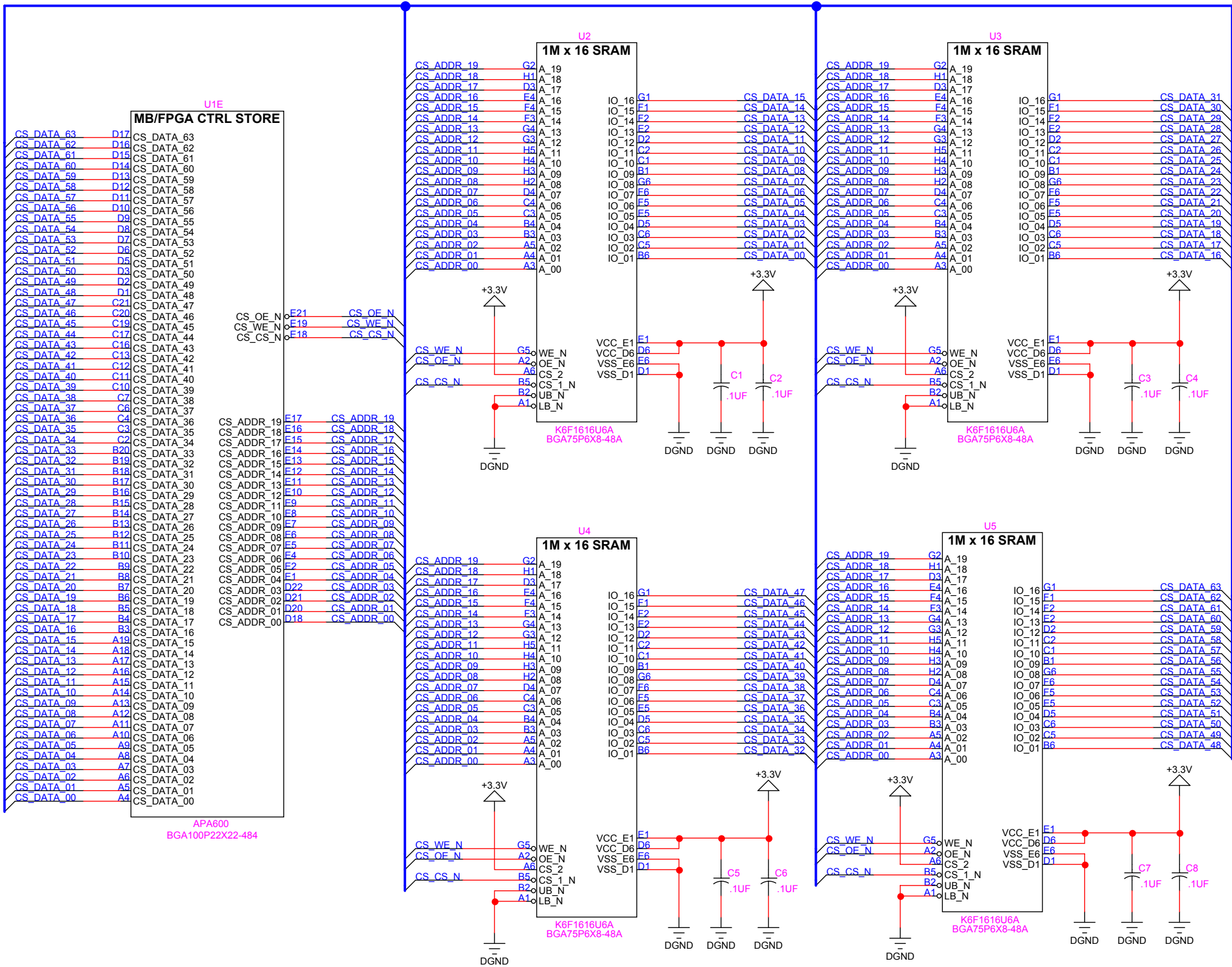
# FPGA ASYNC INTERFACE



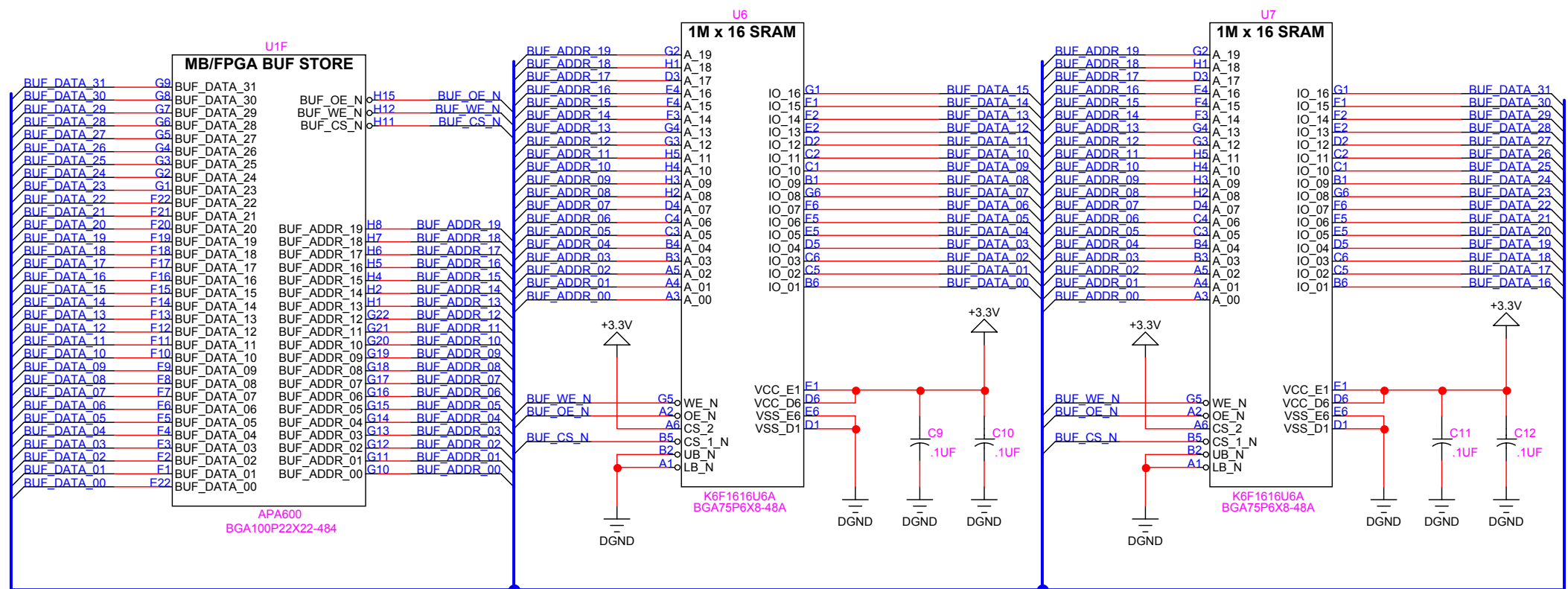
# FPGA GPIO INTERFACE



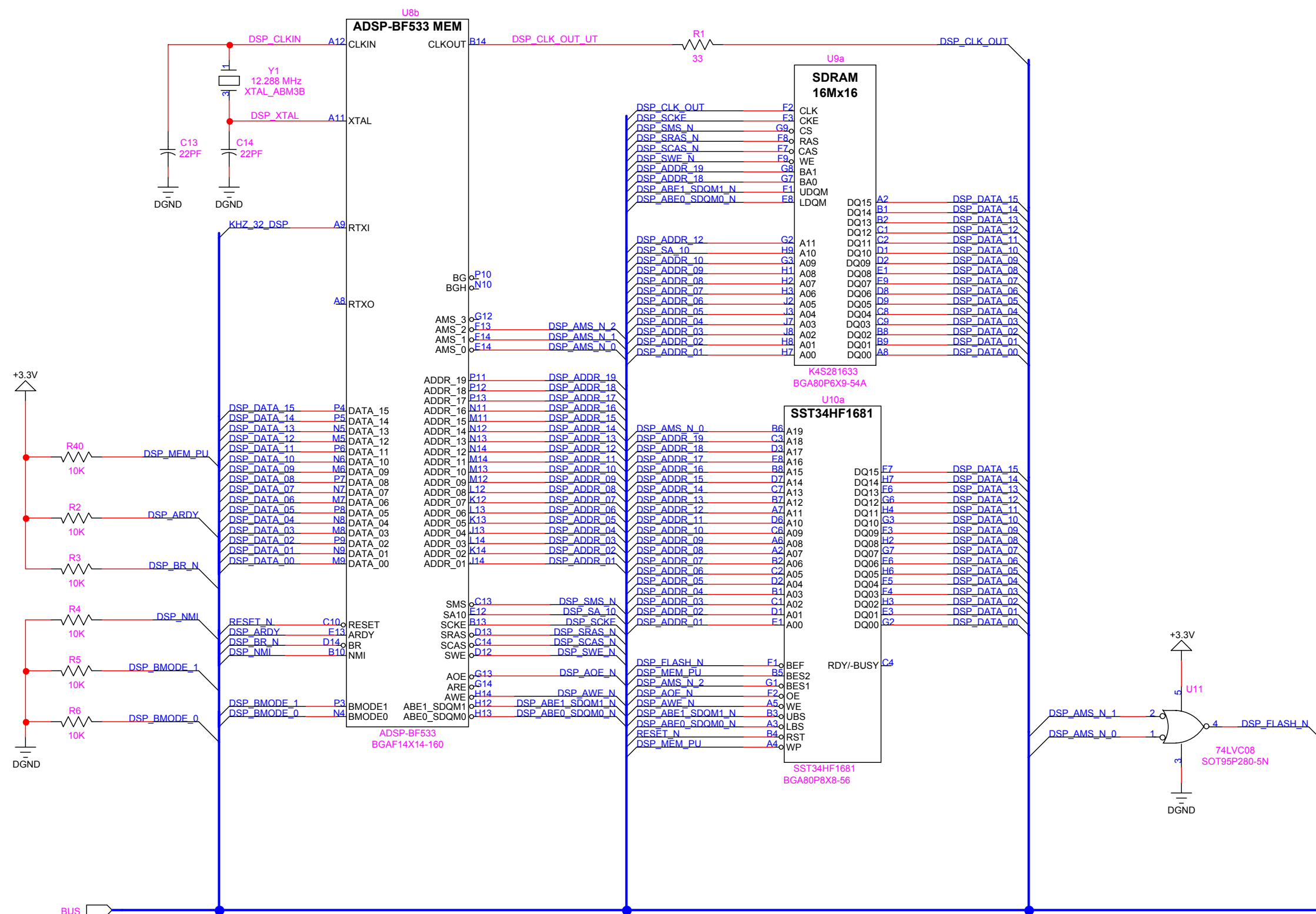
# CONTROL STORE



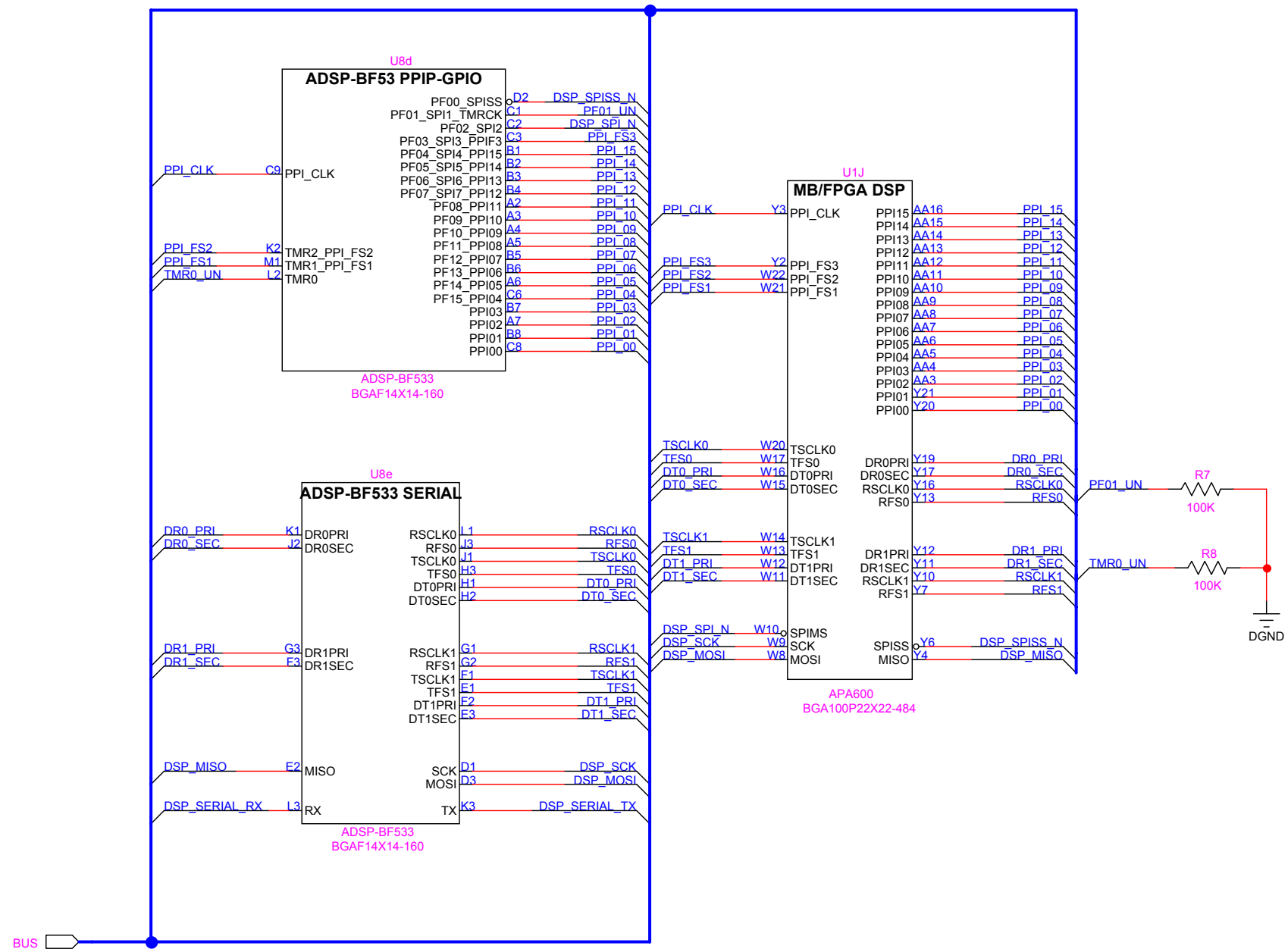
# BUFFER MEMORY



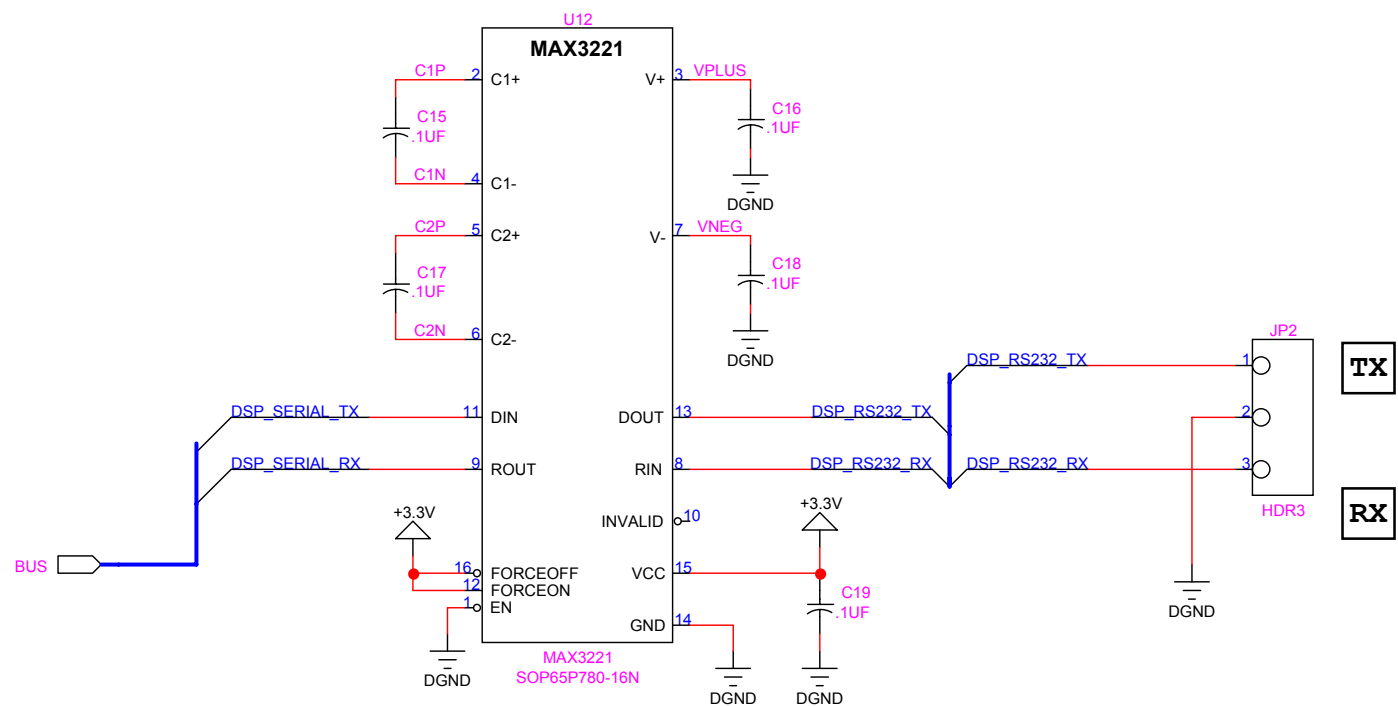
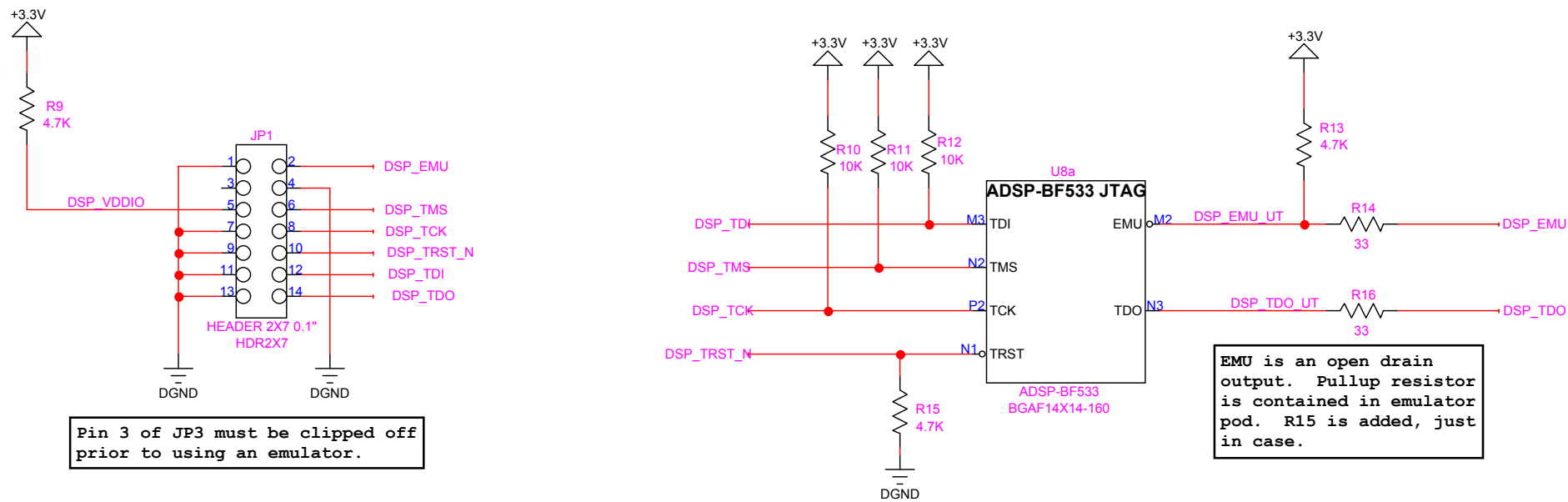
# DSP AND STORAGE



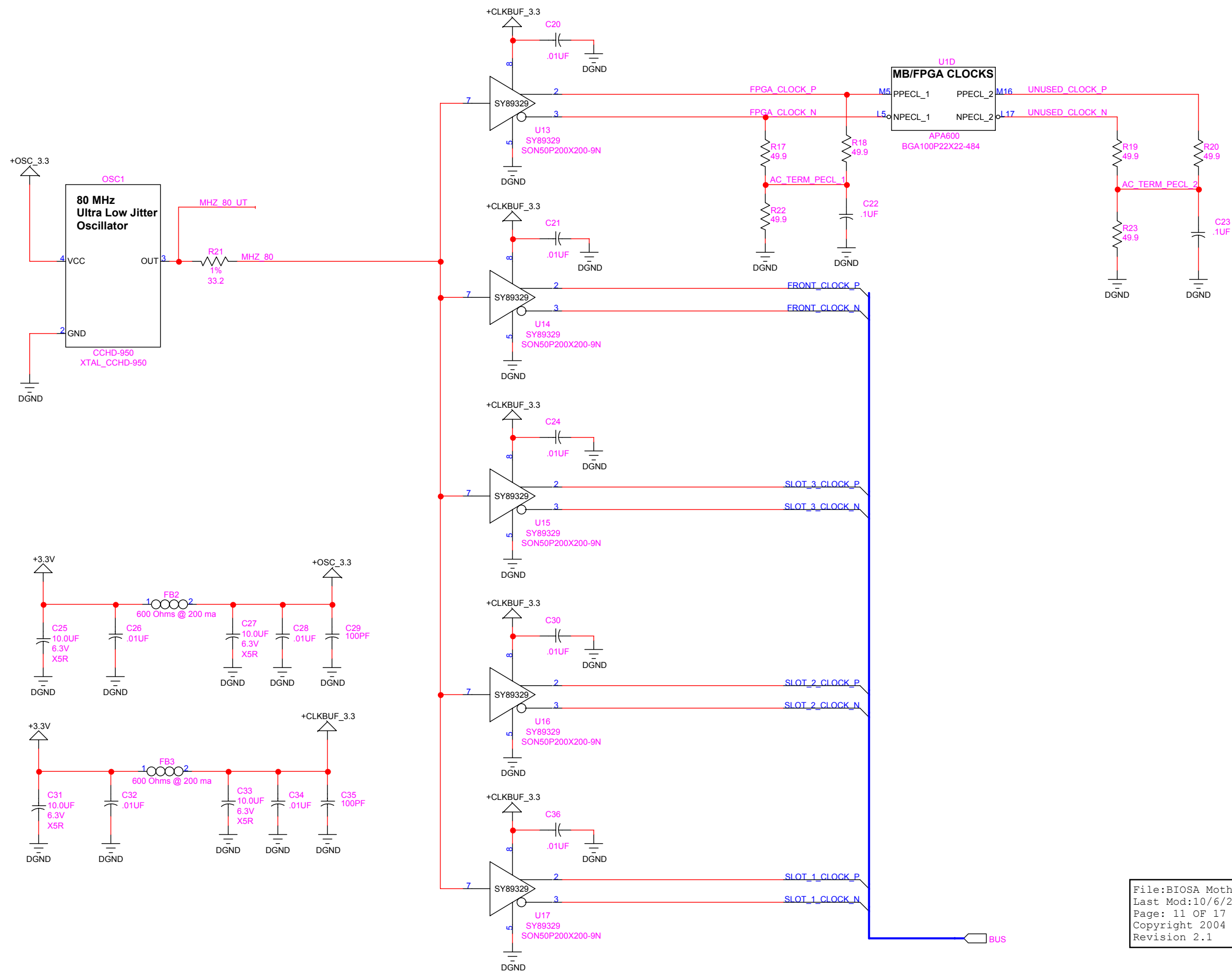
# DSP TO FPGA INTERFACE



# DSP JTAG DEBUG

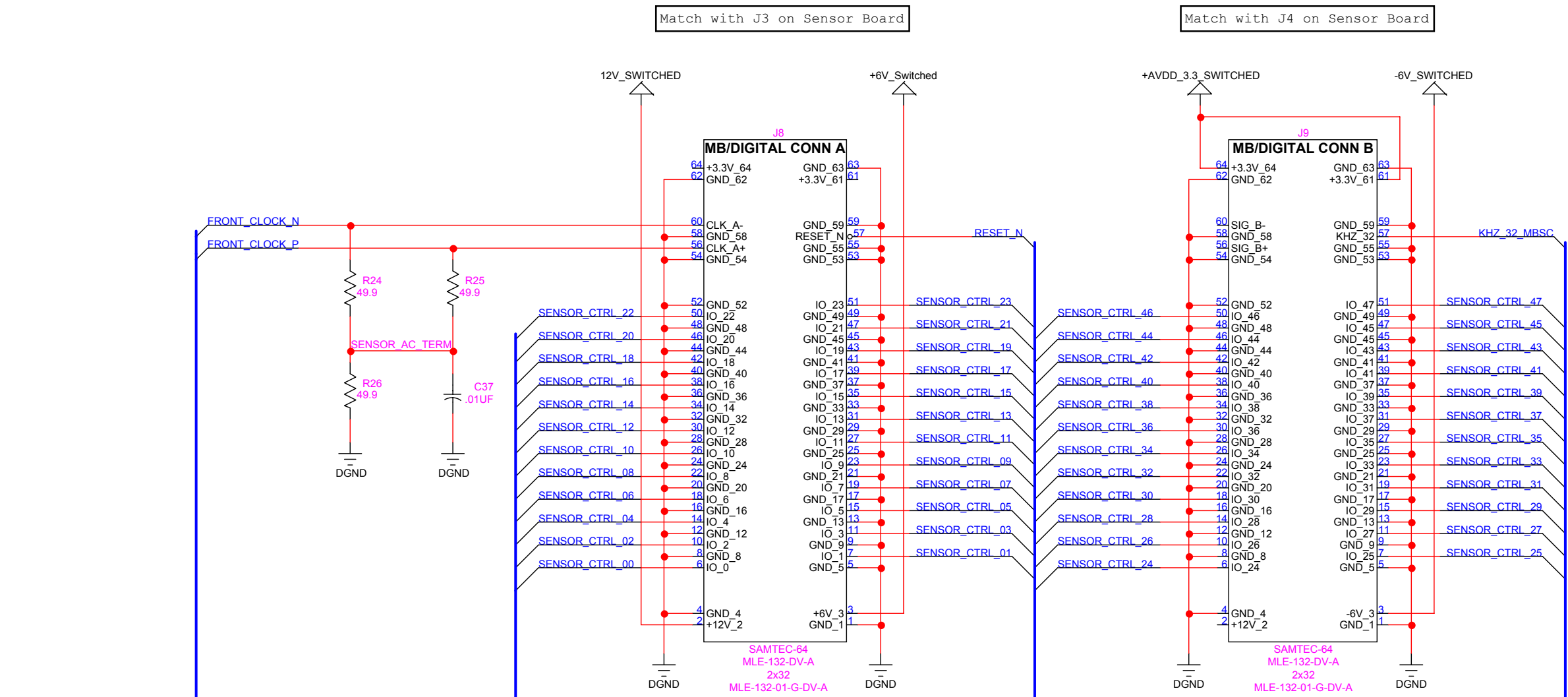


# FINGERBOARD CLOCK GENERATOR



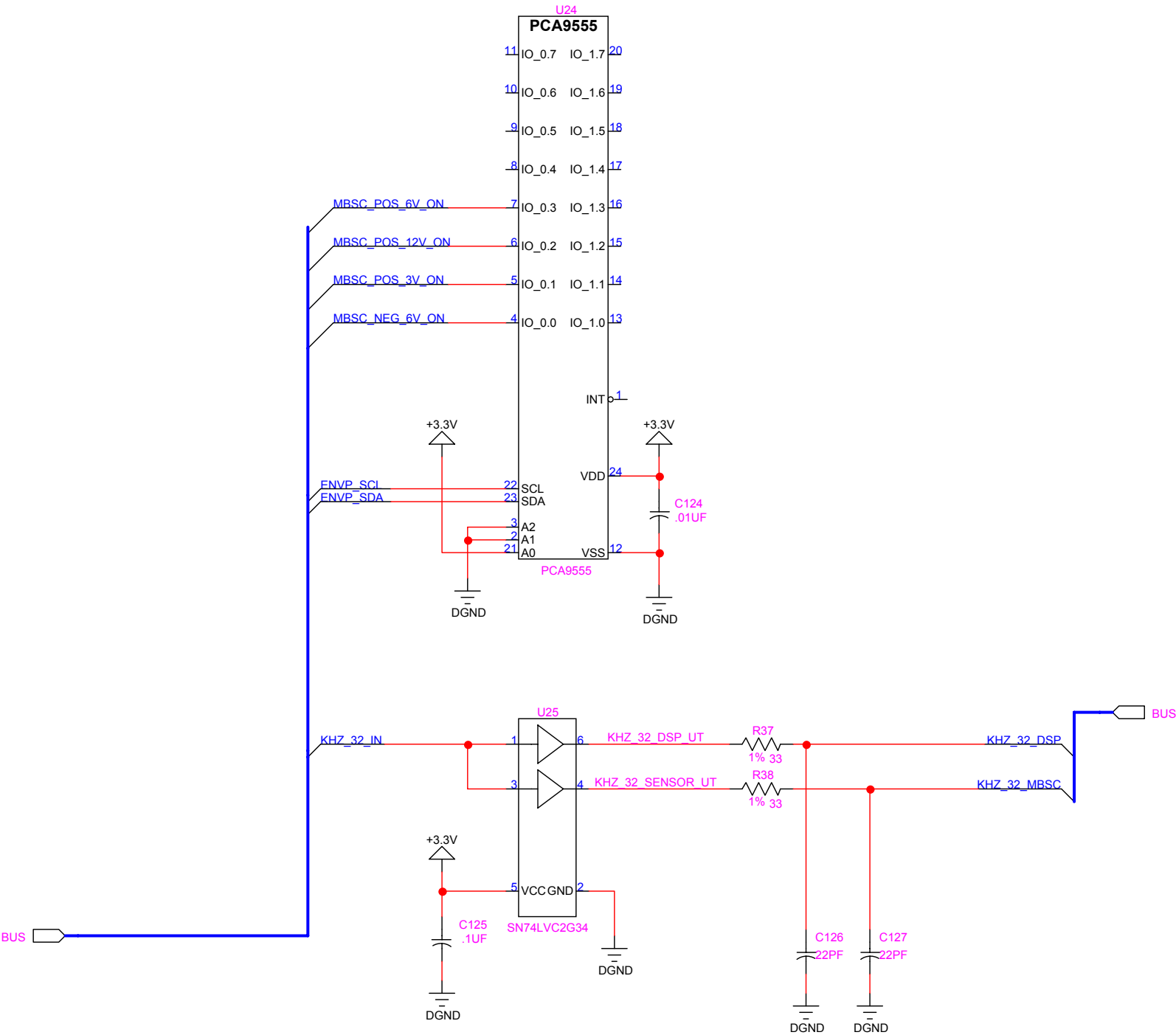
File:BIOSA Motherboard\_2P1.cct  
Last Mod:10/6/2005  
Page: 11 OF 17  
Copyright 2004 @ MBARI  
Revision 2.1

# SENSOR CONTROL CONNECTOR

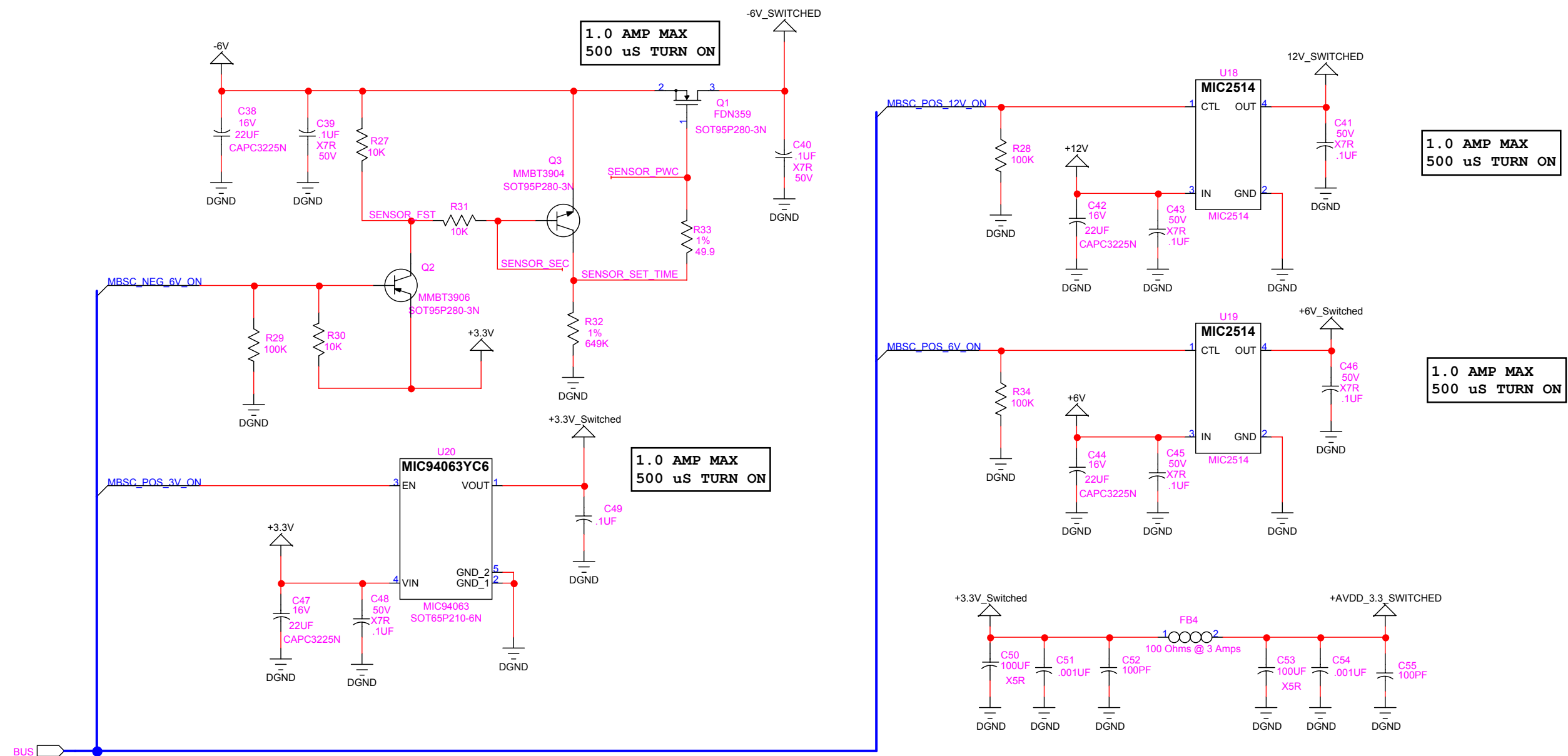


# I2C POWER CONTROL AND 32KHZ DISTRIBUTION

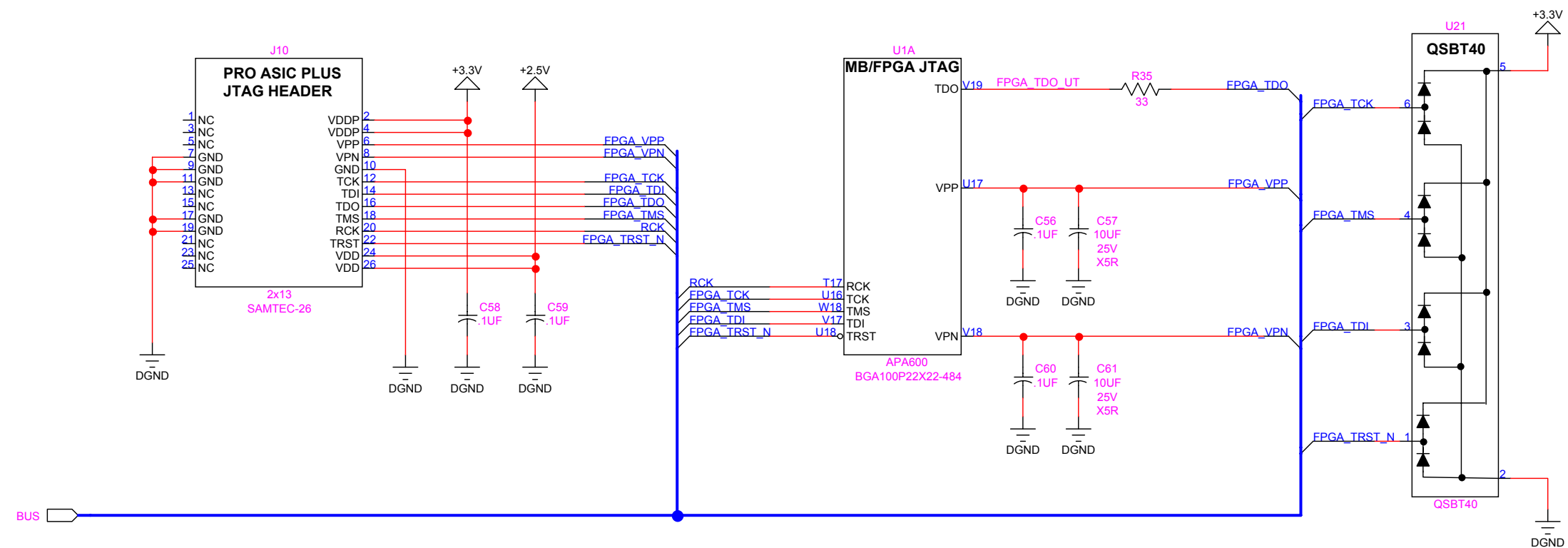
I2C Address = "0100001R"



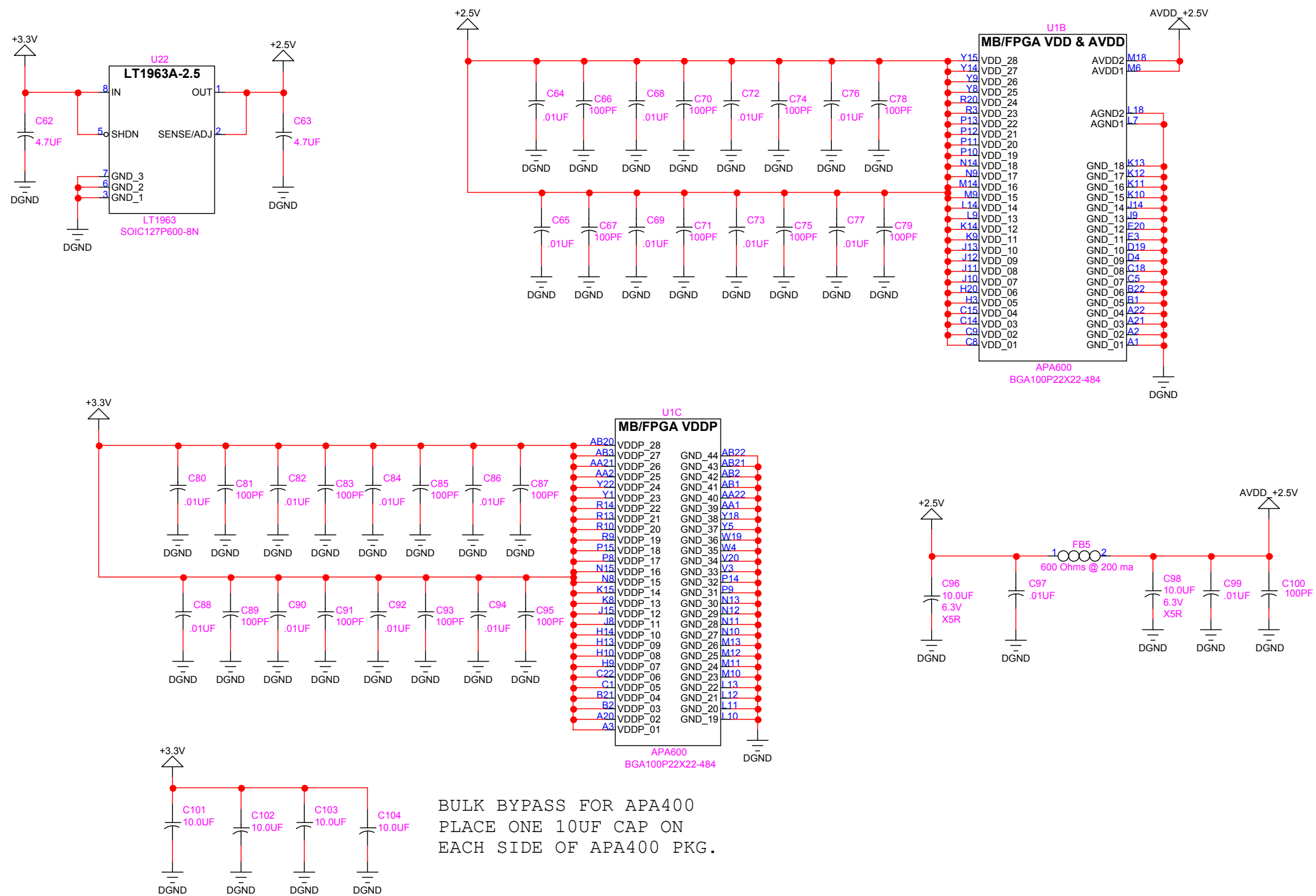
# INSTRUMENT POWER CONTROL



# FPGA PROGRAMMING INTERFACE



# FPGA POWER DISTRIBUTION



# DSP POWER DISTRIBUTION

