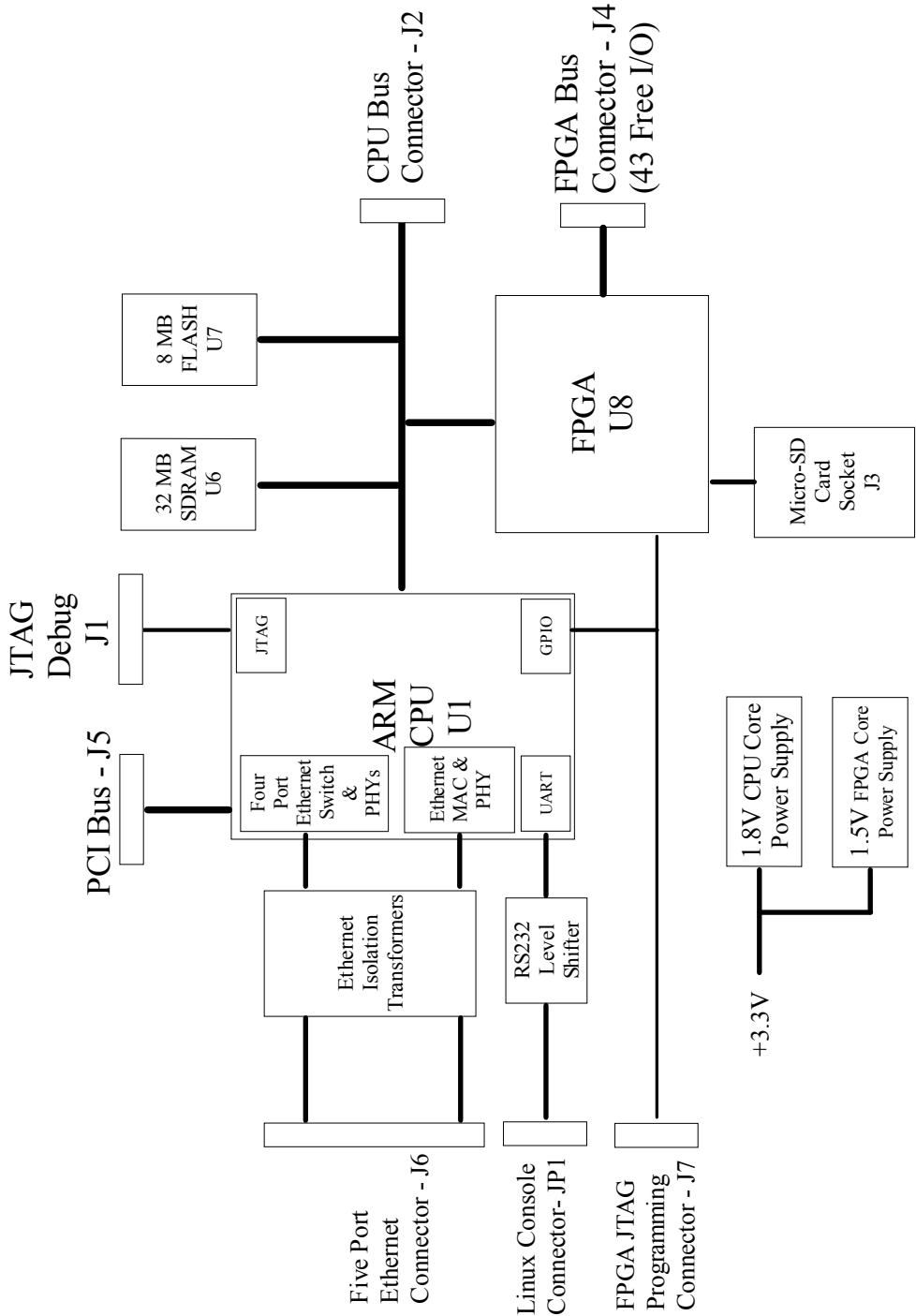
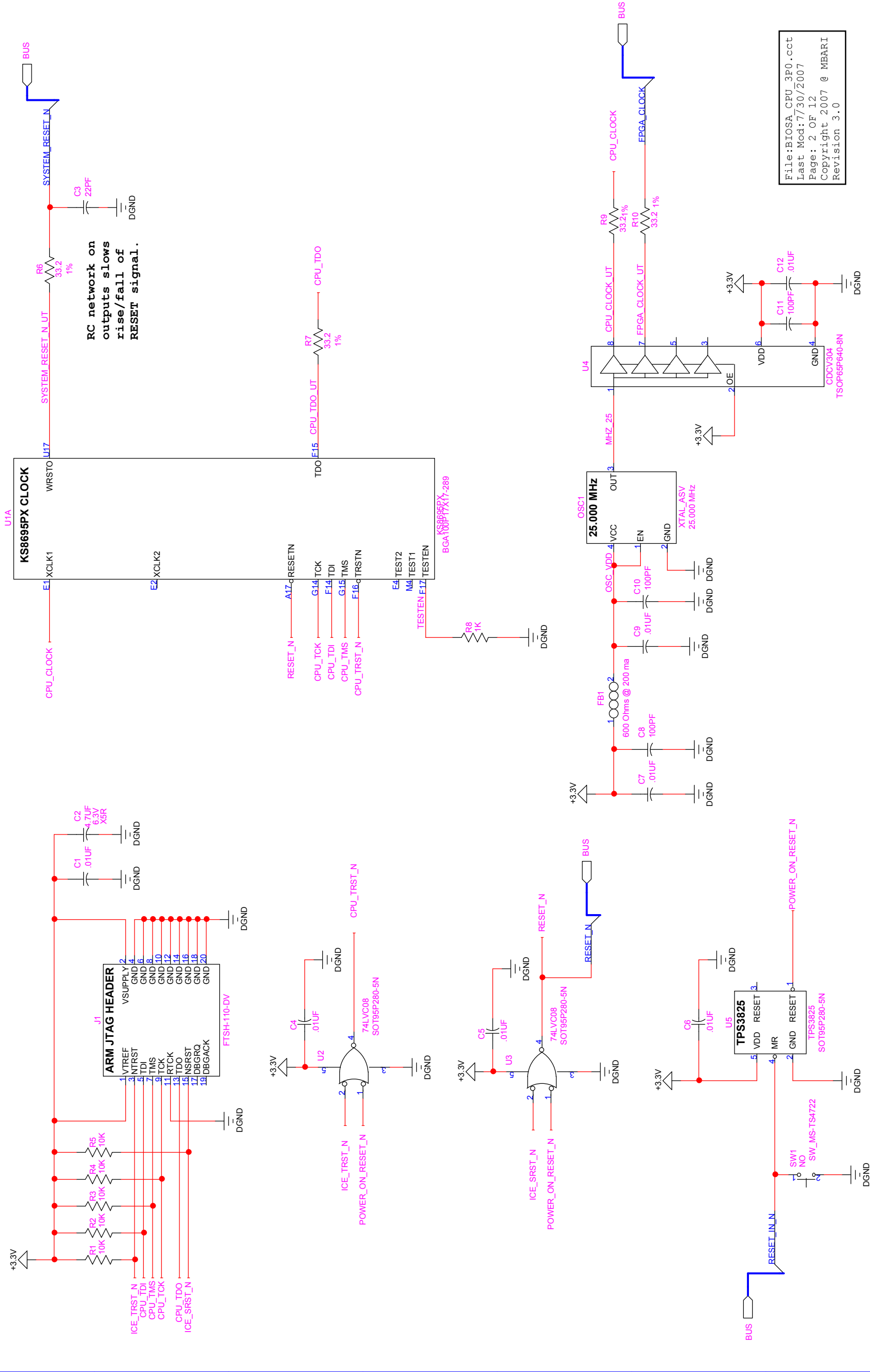


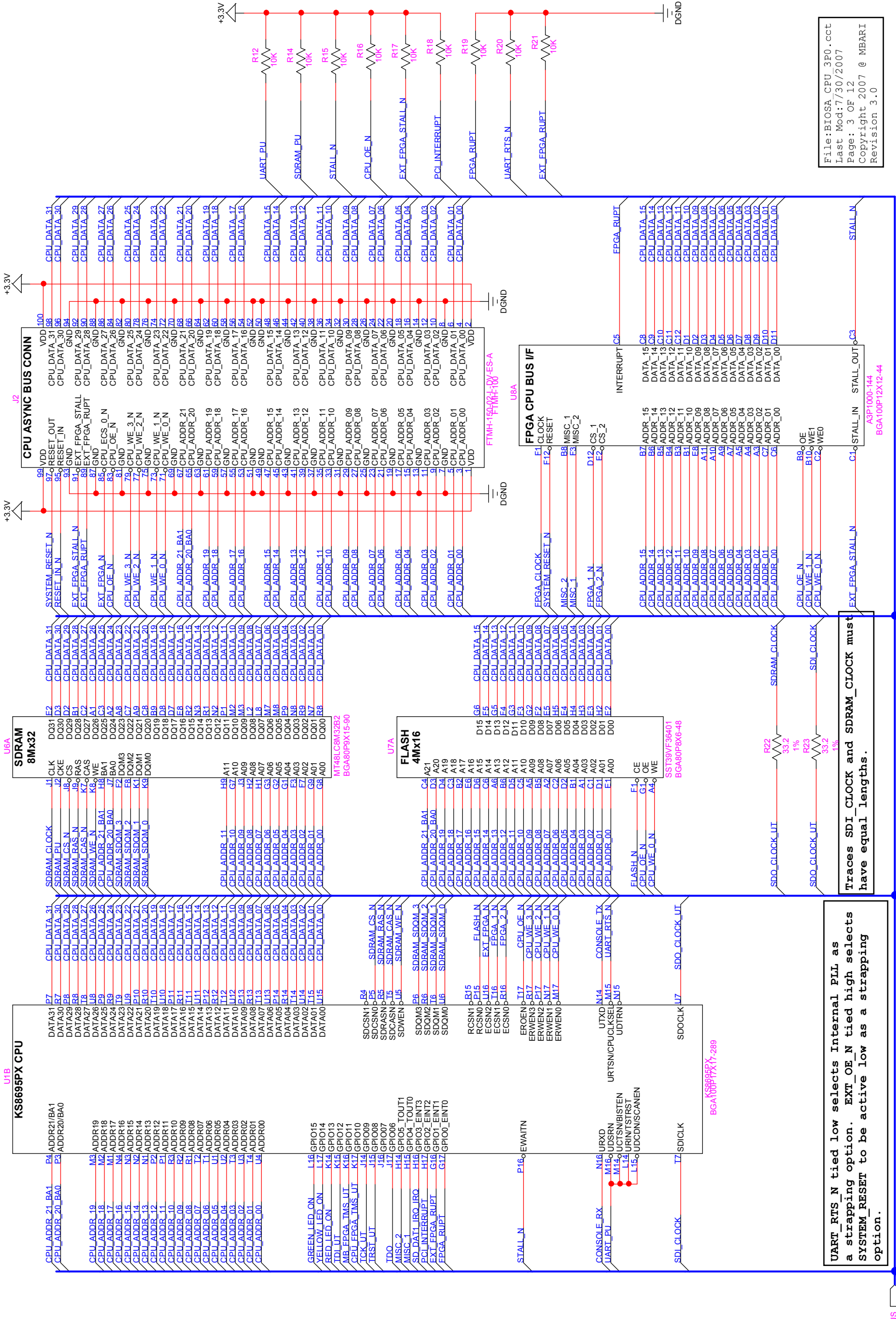
BLOCK DIAGRAM



CPU CLOCK & JTAG



CPU , MEMORY , CONSOLE & ASYNC BUS

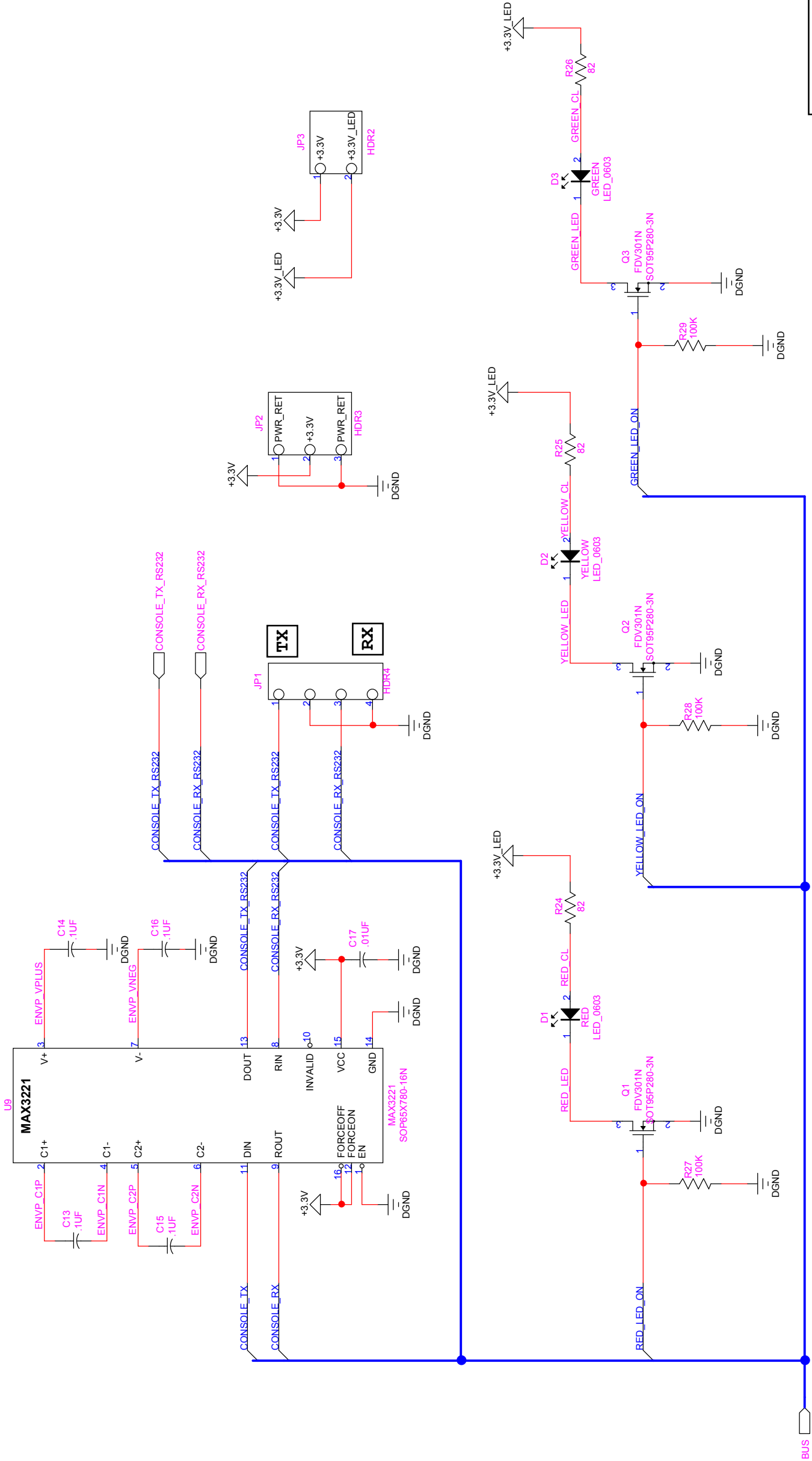


File: BIOSA_CPU_3P0.cct
Last Mod: 7/30/2007
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Revision 3.0

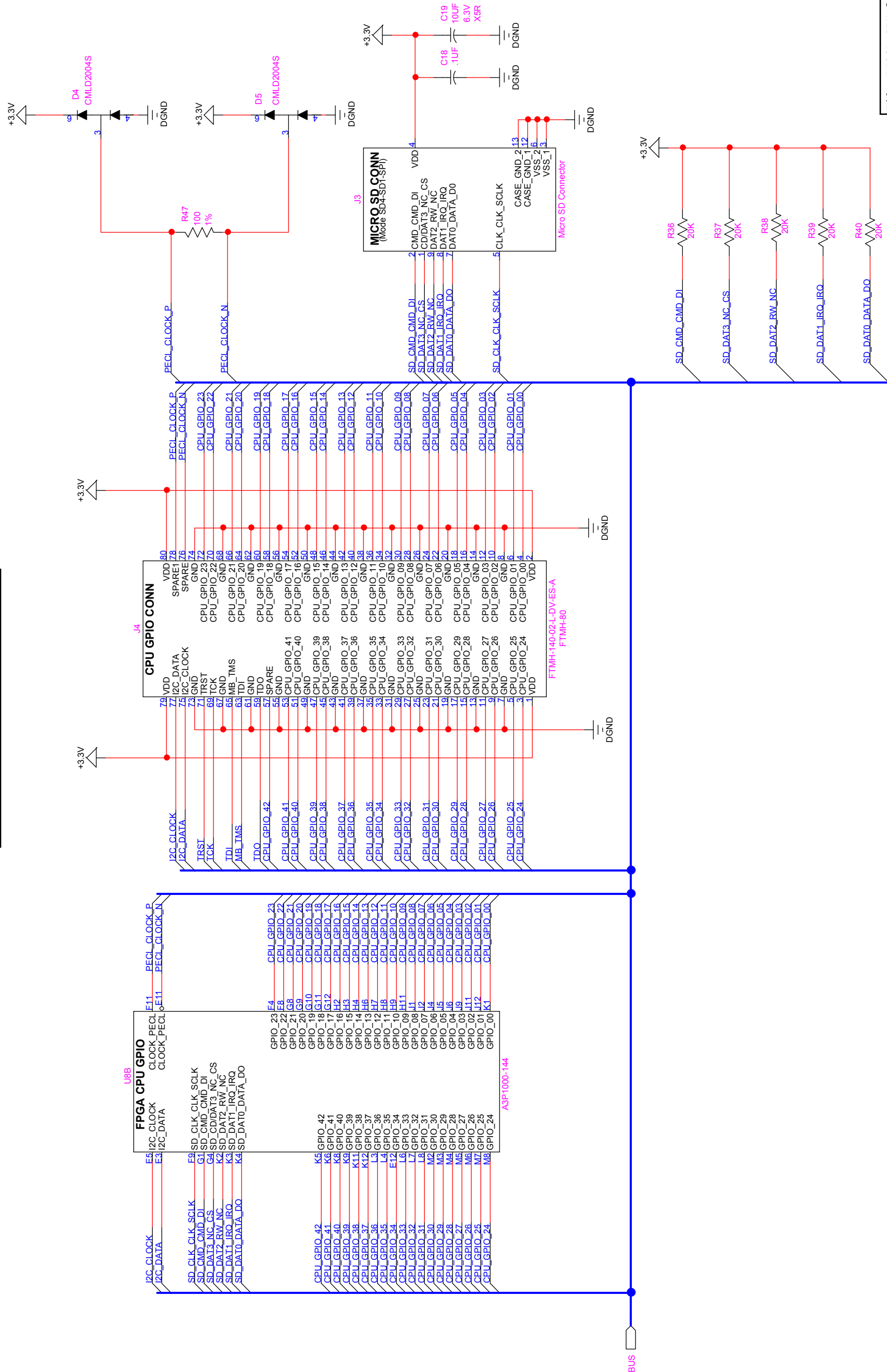
Traces SDI CLOCK and SDRAM_CLOCK must have equal lengths.

UART_RTS_N tied low selects Internal PLL as a strapping option. EXT_OE_N tied high selects SYSTEM RESET to be active low as a strapping option.

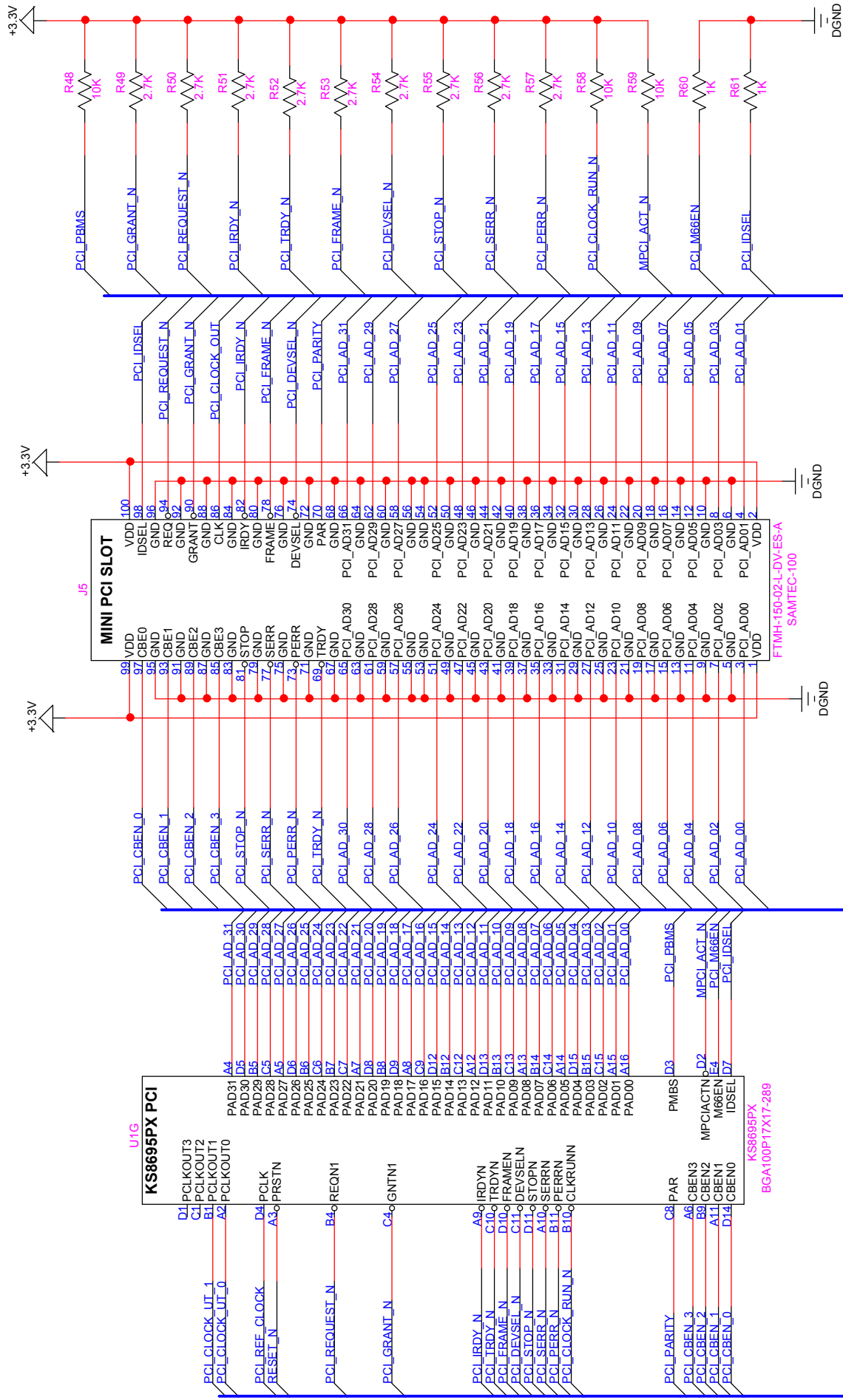
LINUX CONSOLE PORT AND DEBUG LEDS



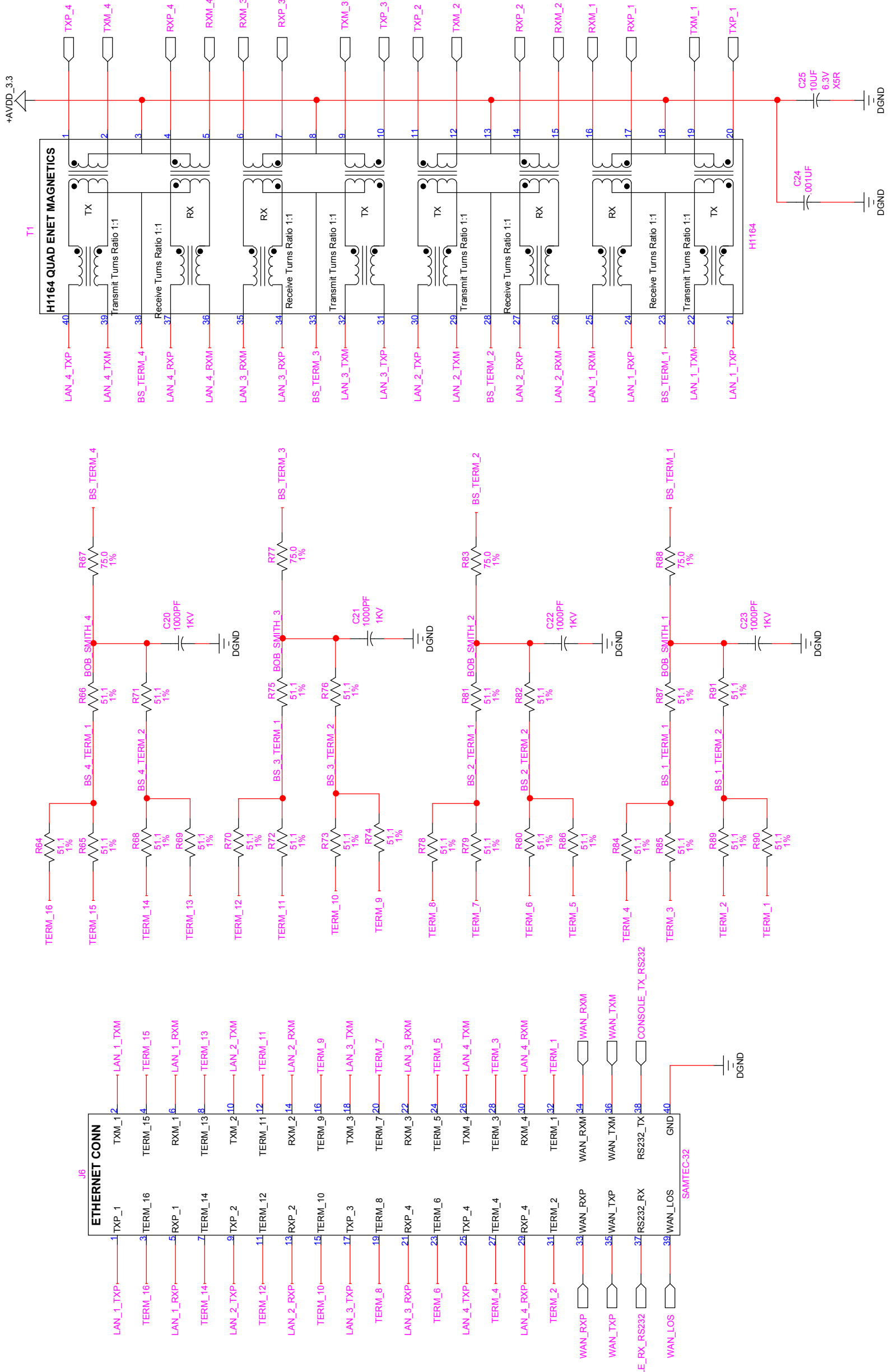
CPU FPGA GPIO



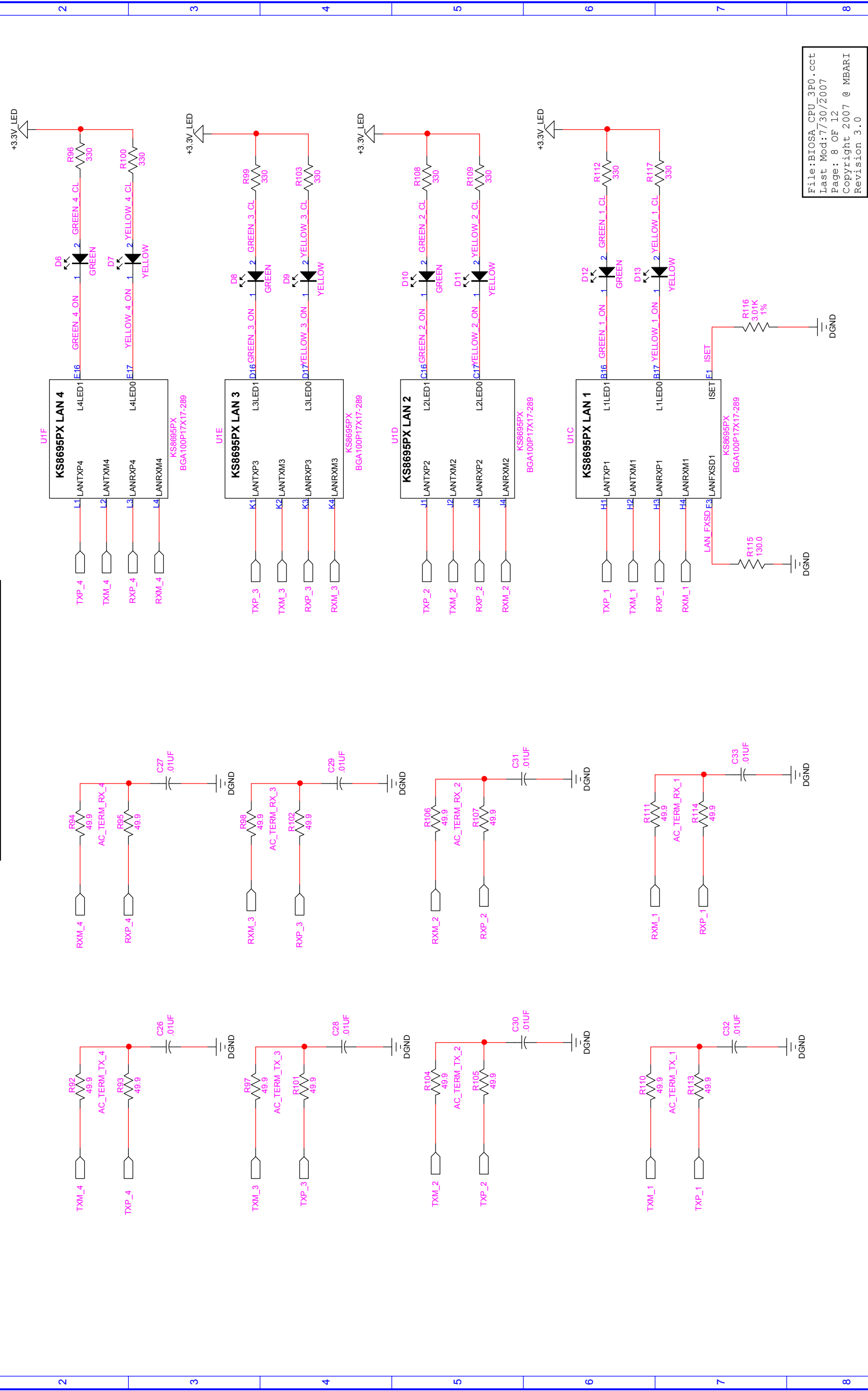
CPU PCI INTERFACE



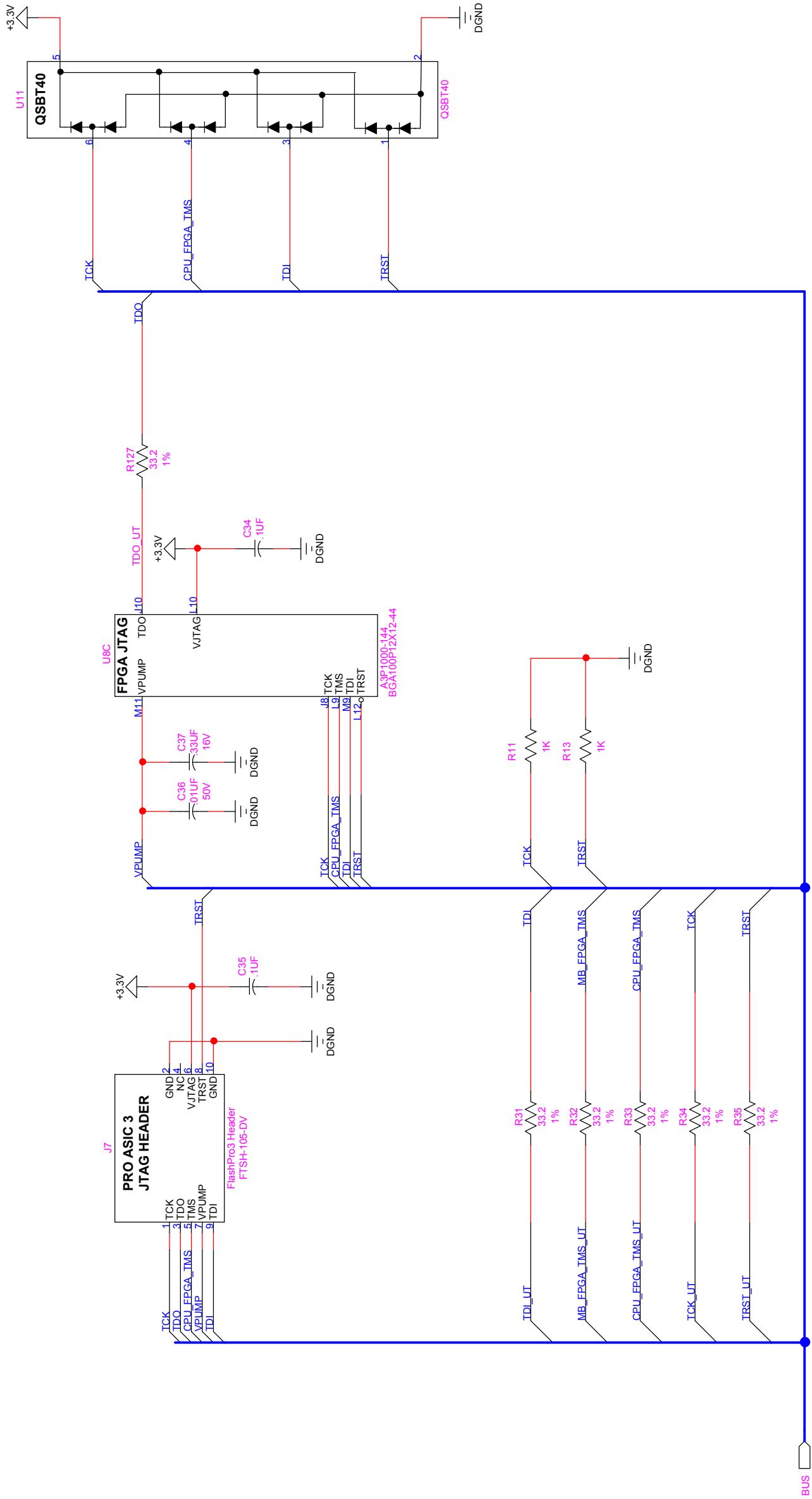
ETHERNET ISOLATION & BOB SMITH TERMINATIONS



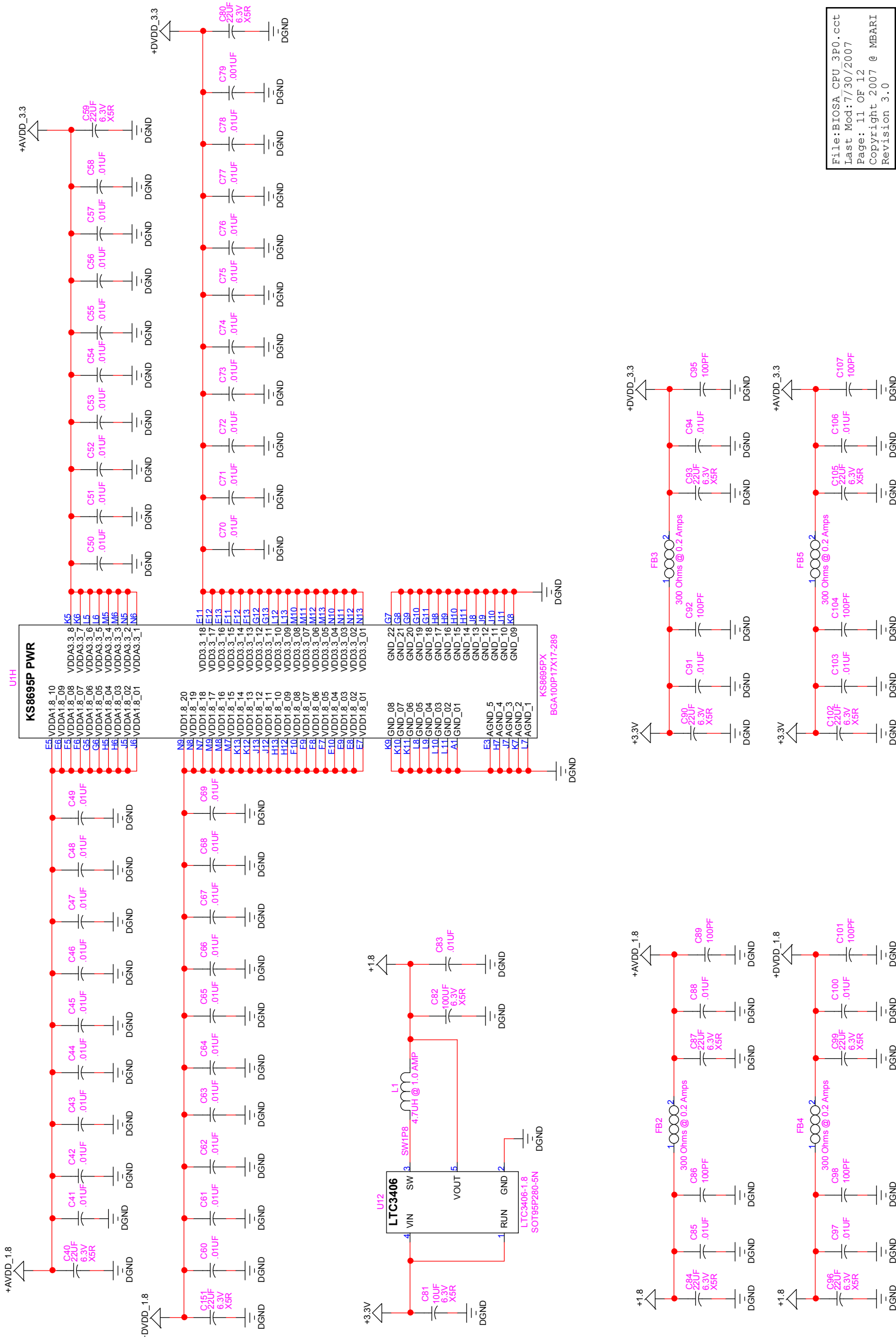
ETHERNET PORTS



FPGA PROGRAMMING INTERFACE



CPU POWER DISTRIBUTION



FPGA, STORAGE AND SD POWER DISTRIBUTION

