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CENTAUR KS8695P Integrated Multi-Port PCI Gateway Solution

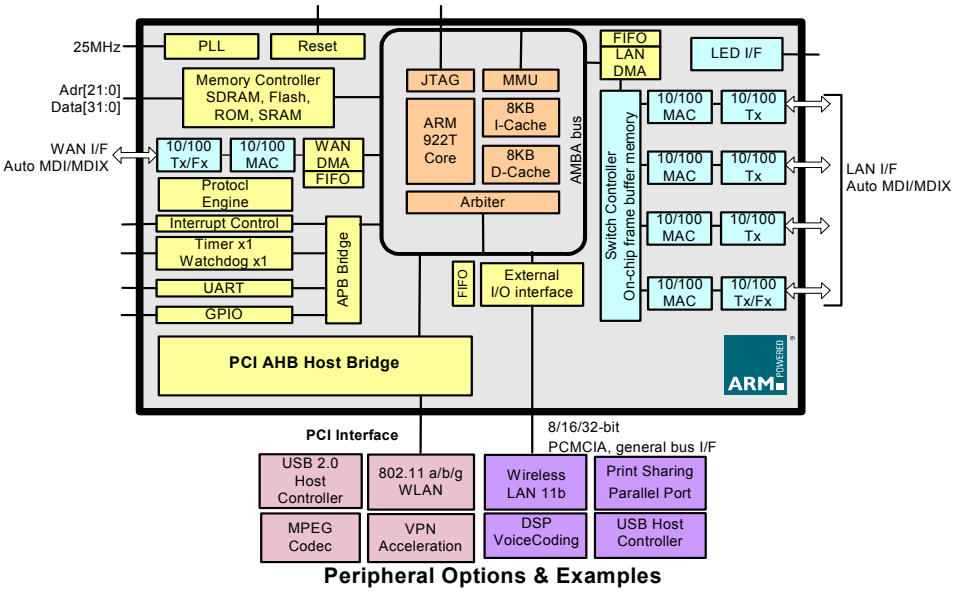
Overview

The CENTAUR KS8695P "Multi-Port PCI Gateway Solution", featuring *XceleRouter*™ Technology, offers the next level of integration, performance and overall BOM cost savings to empower OEMs with the ability to provide their customers with feature-rich, low-cost solutions for the residential gateway and small office environment. The integration of a PCI arbiter that supports 3 external masters opens the door for the designer to incorporate a variety of productivity enhancing system interfaces, including the burgeoning 802.11 a/g/b wireless LAN. Add to this a high-performance ARM 922T CPU with 8KB I-cache and 8KB D-cache and an MMU for Linux and WinCE support; proven wire-speed switching technology that includes 802.1Q tag-based VLAN and Quality of Service support; 5 Patented mixed-signal, low-powered Fast Ethernet transceivers with corresponding MAC units; An advanced memory interface with programmable 8/16/32-bit data and 22-bit address bus with up to 64MB of total memory space for Flash, ROM, SRAM, SDRAM, and external peripherals; A protocol engine to accelerate packet processing; and you have an equation for success in the small office and home office market segment.

Feature Highlights

- **ARM922T High-Performance CPU Core**
  - 185 MIPS ARM922T core at 166Mhz
  - 8KB I-cache and 8KB D-cache
  - Memory Management Unit (MMU) for Linux and WinCE
  - 32-bit ARM & 16-bit Thumb instruction sets
- **33 MHz 32-bit PCI Interface**
  - PCI 2.1
  - Supports bus mastership or guest mode
  - Supports normal and memory mapped I/O
  - Support for miniPCI and Cardbus peripherals
- **Integrated Ethernet Transceivers & Switch Engine**:
  - Five 10/100 Ethernet transceivers and MACs
  - 100Base-Fx mode option on the WAN port and 1 LAN Port.
  - Automatic MDI/MDIX crossover, all ports
  - Wire-speed, non-blocking switch
  - 802.1Q tag-based VLAN (16 VLANs, full-range VID) and Port-based VLAN
  - QoS / CoS packet prioritization support: per-port, 802.1P and DiffServ based.

Figure 1 CENTAUR KS8695P Internal Block Diagram



- 64KB On-chip frame buffer SRAM
- VLAN ID & 802.1P tag/untag opt. per port
- 802.1D spanning tree protocol support
- Programmable rate-limiting per port, 0 to 100 Mbps, ingress & egress, rate options for high & low priority
- Extensive MIB counter management support
- IGMP Snooping for multicast packet filtering
- Dedicated 1K-entry look-up engine
- Port mirroring / monitoring / sniffing
- Broadcast storm protection with % control global and per port basis
- Full & half-duplex flow control

- ***XceleRouter™*** Technology
- TCP/UDP/IP packet header checksum generation to offload CPU tasks
- IPv4 packet filtering on checksum errors
- Automatic error packet discard
- DMA engine with burst mode support for efficient WAN, LAN data transfers.
- FIFOs for back-to-back packet transfers.

- **Memory and External I/O Interfaces**
- 8/16/32-bit wide shared data path for SDRAM/ROM/SRAM/Flash & External I/O.
- Total memory space up to 64 MB
- Intel/AMD-type Flash support

- **Peripheral Support**
- 8/16/32-bit External I/O interface supporting PCMCIA or generic CPU/DSP host I/F.
- Sixteen general-purpose I/O (GPIO)
- Two 32-bit Timer counters (one watchdog)
- Interrupt controller

- **System Design**
- 289 PBGA package (19mmx19mm) saves board real estate
- Two power supplies: 1.8V core and Ethernet Rx supply, 3.3V I/O and Ethernet Tx supply
- Built-in LED controls

- **Debugging**
- ARM922T JTAG debug interface
- UART for console port or modem back up

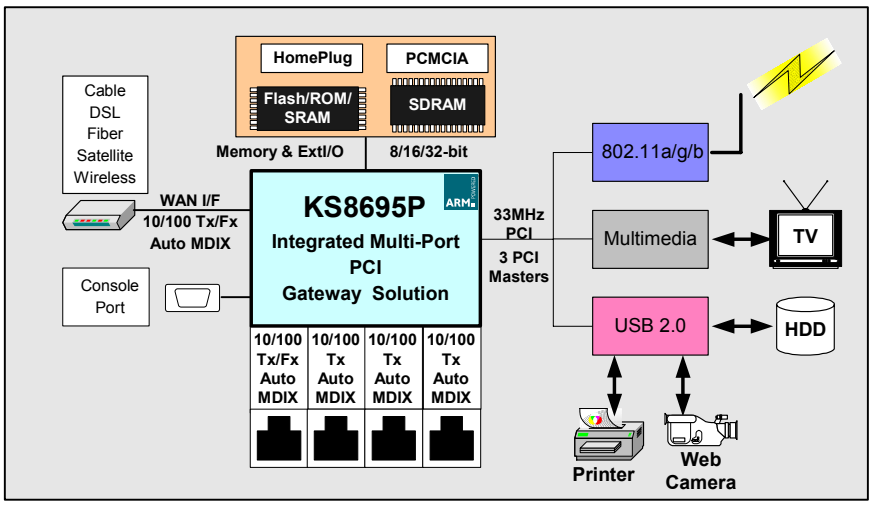
- **Power Management**
- CPU & system clock speed step-down options
- Low power Ethernet Transceivers
- Per port power down and Ethernet transmit disable

- **Reference HW/SW Evaluation Kit**
- Hardware evaluation board
- Board support package including firmware, source code
- Documentation for design & programming
- Complete hardware & software reference designs are available.

Applications

- RG + Combo 802.11a/b/g Access Point
- Multi-port Broadband Gateway
- Multi-port Firewall & VPN Appliances
- Multi-port VoIP Gateway
- Fiber-to-the-Home Managed CPE

Figure 2 KS8695P PCI Gateway System Options



Revision History

Revision	Date	Summary of Changes
0.9	5/13/03	Preliminary
0.91	6/4/03	Corrected WRSTPLS sets WRSTO to active low when '1', and active high when '0'.
0.92	6/10/03	Changed pin A1 to GND. Changed pin E3, H7, J7, K7, L7 to AGND. Changed figure 5 WRSTPLS to pull up.
0.93	7/11/03	Removed PCI 2.2 compliance. Removed TM from Centaur. Added LANFXSD1 signal description.
0.94	7/17/03	Updated DC Electrical Characteristics
0.95	8/11/03	Added addressing description to memory controller, and address pin description table 11. Changed PRSTN to input in Table 10.
1.0	9/2/03	Changed figure 1. Removed old register address tables and replaced with figure 11. Added Memory interface examples, figures 7,8,9. Added memory interface description, section 2.5.
1.1	9/29/03	Changed Figure 2.

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1.0 Functional Description

1.1 Introduction

Micrel's KS8695P, a member of the **CENTAUR** line of integrated processors, is a high-performance router-on-a-chip solution for Ethernet and 802.11 a/g/b based embedded systems. Designed for use in communication routers, the KS8695P integrates a PCI to AHB bridge solution for interfacing with 32-bit PCI, MiniPCI and Cardbus devices. In addition, it also integrates a proven 3rd generation 5-port managed switch, an ARM9 RISC processor with MMU, 5 PHY transceivers with corresponding MAC units and Micrel's XceleRouter Technology.

The KS8695P is built around an outstanding CPU core: the 16/32-bit ARM922T RISC processor. The ARM922T is a scalable, high-performance, microprocessor that was developed for integrated system-on-a-chip applications.

The KS8695P offers configurable 8-Kbyte Instruction Cache and 8-Kbyte Data Cache that reduces the memory access latency for high-performance applications. Its simple, elegant, and fully static design is particularly suitable for cost-effective, power-sensitive applications.

The KS8695P contains five 10/100 physical layer transceivers (PHY), four for the Local Area Network (LAN), and one for the Wide Area Network (WAN). It also contains the corresponding five Media Access Control (MAC) units with an integrated layer 2 managed switch. The integration of the switch and the analog PHYs make the KS8695P an extremely cost-effective solution for SOHO router applications because it saves board space and BOM cost. The layer 2 switch contains a 16Kx32 SRAM on-chip memory for frame buffering. The embedded frame buffer memory is designed with a 1.4Gbps on-chip memory bus. This allows the KS8695P to perform non-blocking frame switching/routing on the fly for many applications.

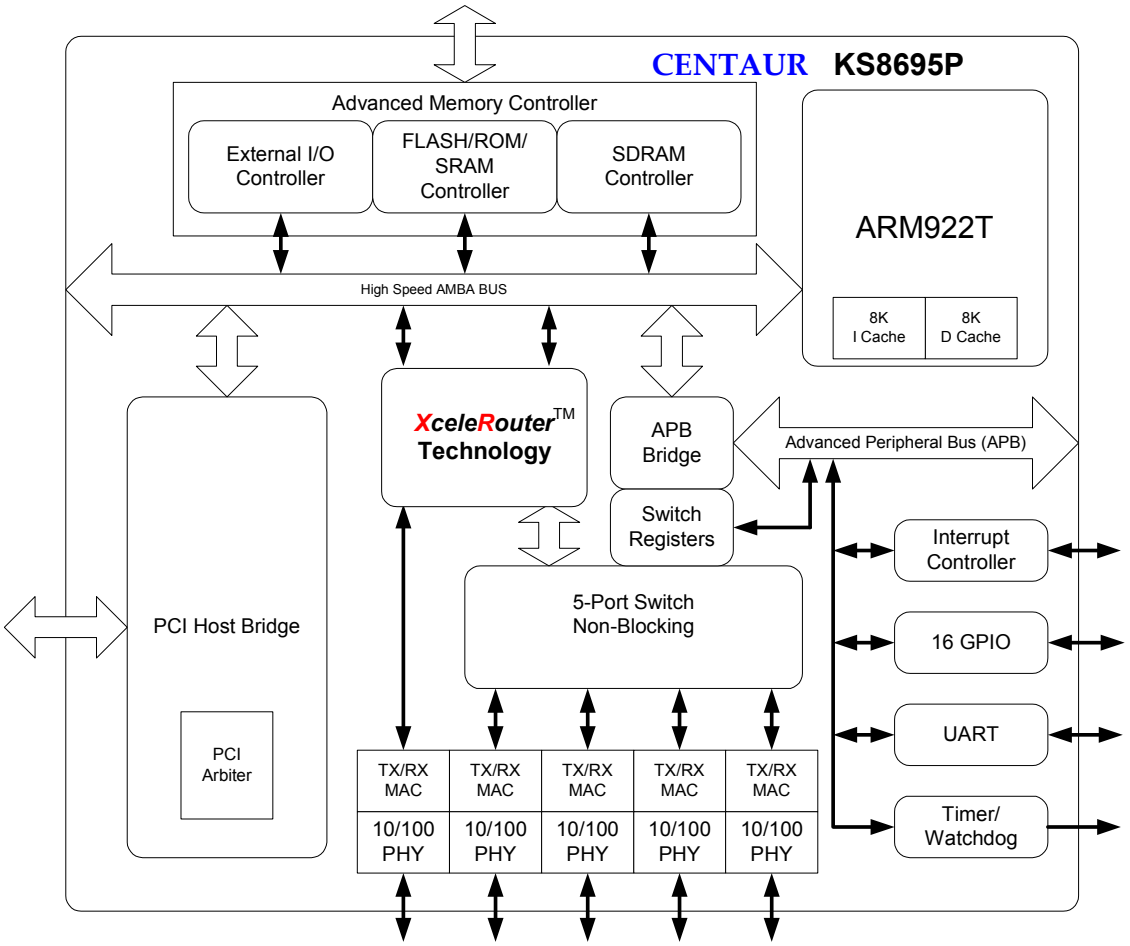
On the media side, the KS8695P supports 10BaseT, and 100BaseTX as specified by the IEEE 802.3 committee, as well as 100 Base FX on WAN port and one LAN port.

The KS8695P supports two modes of operation in the PCI bus environment, Host Bridge Mode, and Guest Bridge Mode. In the Host bridge mode, the ARM9 processor acts as the Host of the entire system. It configures other PCI devices and coordinates their transactions, including initiating transactions between the PCI devices and AHB bus subsystem. An on-chip PCI arbiter is included to determine the PCI bus ownership among PCI master devices.

In Host Bridge Mode, all I/O registers, including those for the embedded switch, can be configured by the ARM922T processor through the on-chip AMBA bus interface. In Guest Bridge Mode, all of the I/O registers can be programmed by either the external Host CPU on the PCI bus, or the local ARM922T host processor through the AMBA bus.

In Guest Bridge mode, the KS8695P functions as a slave on the PCI bus. The on-chip PCI arbiter is disabled. Either the ARM9 CPU or the PCI Host CPU can configure the KS8695P subsystem. In either case, the KS8695P memory subsystem is accessible from either the PCI Host or the ARM9 CPU. Communications between the external Host CPU and the ARM922T can be accomplished through message passing or through shared memory.

Figure 3 KS8695P Functional Block Diagram



1.2 CPU Features

- 166MHz ARM922T RISC processor core.
- On-chip AMBA Bus 2.0 interfaces.
- 16-bit Thumb programming to relax memory requirement
- 8-Kbyte Instruction Cache and 8-Kbyte Data Cache
- Little-Endian mode supported.
- Configurable Memory Management Unit
- Supports reduced CPU and System clock speed for power saving

1.3 PCI to AHB Bridge Features

- Support 33MHz, 32-bit DATA PCI Bus.
- Integrated PCI bridge support for interfacing with 32-bit mini-PCI or CardBus devices.
- Independent AHB and PCI Clock speed
- Support 125MHz AHB speed.
- Supports PCI revision 2.1 protocols.
- Supports AHB Bus 2.0 interfaces.
- Supports both regular and memory-mapped I/O on PCI interface.
- Integrated PCI Arbiter with power-on option to enable or disable.
- Support Round Robin arbitration with 3 external PCI devices and one internal device.
- Supports AHB burst transfers up to 16 data words.
- Configurable PCI registers by Host CPU ARM922T.
- Supports Bus mastership from PCI to AHB or AHB to PCI bus.

1.4 Switch Engine

- 5 port 10/100 Integrated switch with 1 WAN and 4 LAN Physical Layer Transceivers.
- 16Kx32 on-chip SRAM for frame buffering.
- 1.4Gbps on-chip memory bandwidth for wire-speed frame switching.
- 10Mbps, 100Mbps modes of operations for both full and half duplex
- Supports 802.1Q Tag-based VLAN and port-based VLAN
- Supports 802.1p based priority, DiffServ priority and port-based priority.
- Integrated address Look-Up engine, supports 1 K absolute MAC addresses.
- Automatic address learning, address aging and address migration.
- Broadcast storm protection.
- Full duplex IEEE 802.3x flow control.
- Half duplex back pressure flow control.
- Supports IGMP snooping
- Spanning tree protocol support

1.5 Advanced Memory Controller Features

- Supports glueless connection 2 Banks of ROM/SRAM/FLASH memory with programmable 8/16/32 bit data bus and programmable access timing.
- Supports glueless connection to 2 SDRAM Banks with programmable 8/16/32 bit data bus and programmable RAS/CAS latency
- Supports 3 External I/O Banks with programmable 8/16/32 bit data bus and programmable access timing.
- Programmable system clock speed for power management.
- Automatic address line mapping for 8/16/32 bit accesses on Flash/ROM/SRAM and SDRAM interfaces.

1.6 Direct Memory Access (DMA) Engines

- Independent MAC DMA engine with programmable burst mode for WAN port.
- Independent MAC DMA engine with programmable burst mode for LAN ports.
- Supports little endian byte ordering for memory buffers and descriptors.
- Contains large independent receive and transmit FIFOs (3KB receive/ 3KB transmit) for back-to-back packet receive, and guaranteed no-underrun packet transmit.
- Data alignment logic and scatter gather capability.

1.7 Protocol Engine

- Supports IPv4 IP Header/TCP/UDP Packet checksum generation for host CPU offloading.
- Supports IPv4 Packet filtering based on checksum errors

1.8 Network Interface

- Features 5 media access control (MAC) units and 5 physical transceiver units (PHY).
- Supports 10 BaseT, 100 BaseTx on all LAN ports and WAN port. Also supports 100BaseFx on WAN port and one LAN port.
- Supports automatic CRC generation and checking.
- Supports automatic error packet discard.
- Supports IEEE 802.3 Auto-Negotiation algorithm of full-duplex and half-duplex operation for 10Mb/s, 100Mb/s.
- Supports full/half-duplex operation on PHY interfaces.
- Fully compliant with IEEE 802.3 Ethernet standards.
- IEEE 802.3 full-duplex flow control and half-duplex backpressure collision flow control.
- Supports MDI/ MDI-X auto crossover.

1.9 Peripherals

- 28 Interrupt sources, including 4 external interrupt sources.
- Normal or fast interrupt mode (IRQ, FIQ) supported.
- Prioritized interrupt handling.
- 16 programmable general purpose I/O. Pins individually configurable to input, output, or I/O mode for dedicated signals.
- 2 programmable 32-bit timers with watchdog timer capability
- High speed UART interface up to 115 kbps.

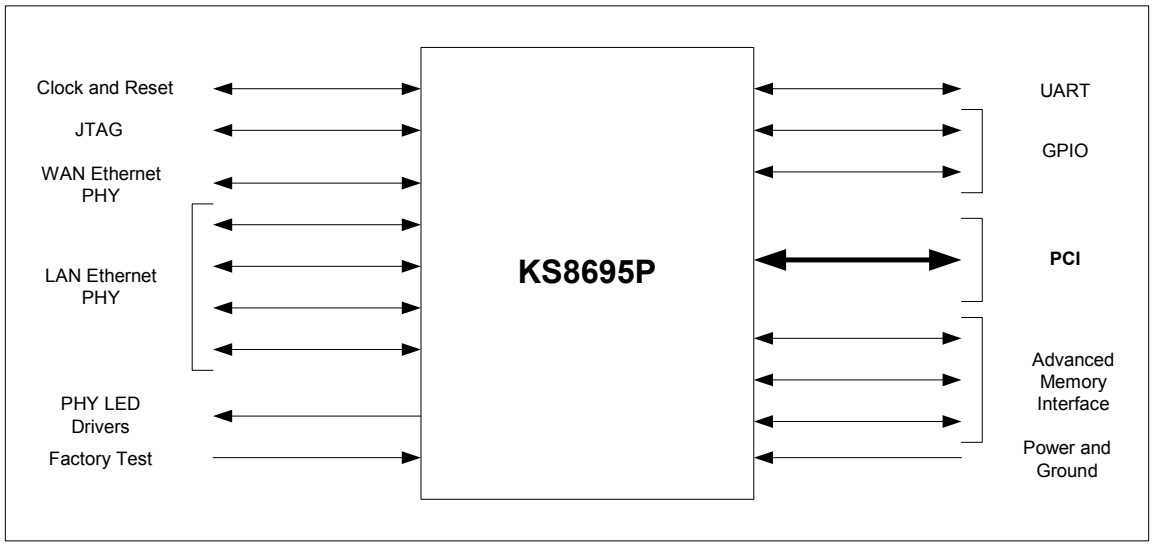
1.10 Other Features

- Integrated PLL to generate CPU and system clocks.
- JTAG development interface for ICE connection.
- 19mmx19mm 289 pin PBGA.
- 1.8V CMOS for Core, 3.3V for I/O

2.0 Signal Description

2.1 System Level Hardware Interfaces

Figure 4 System Level Interfaces



At the system level the KS8695P Features the following interfaces:

- Clock Interface for Crystal or External Oscillator.
- JTAG Development Interface
- 1 WAN Ethernet Physical Interface
- 4 LAN Ethernet Physical Interfaces
- PHY LED Drivers
- 1 High Speed UART Interface
- 16 GPIO pins
- 33 MHz, 32-bit PCI Interface Supporting 3 External Masters
- Advanced Memory Interface
    - Programmable Synchronous Bus Rate
    - Programmable Asynchronous Interface Timing
    - Independently Programmable Data Bus Width for Static and Synchronous Memory
    - Glueless Connection to SDRAM
    - Glueless Connection to Flash Memory or ROM
- Factory Test
- Power and Ground

2.2 Configuration Pins

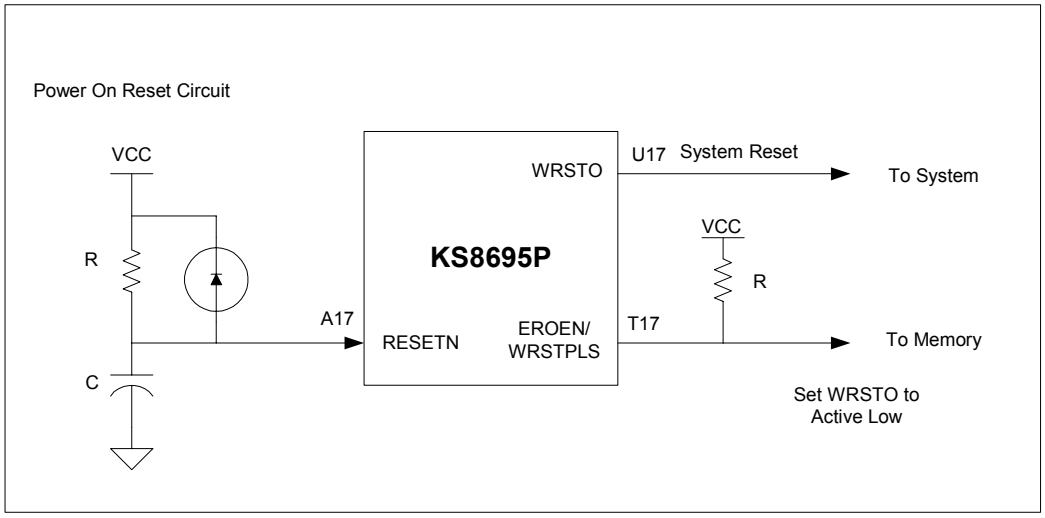
Table 1 Configuration Pins

Configuration	Pin Name	Pin #	Settings
Bank0 Flash data width	B0SIZE[1:0]	E14,E15	'00'= reserved '01' = byte wide '10' = half word wide (16 bits) '11' = word wide (32 bits)
WRSTO polarity	EROEN/WRSTPLS	U17	'0' = active high '1' = active low
CPU Clock Select	URTSN/CPUCLKSEL	M15	'0' = normal mode (PLL) '1' = bypass internal PLL
PCI Bridge Mode Configuration	PBMS	D3	'0' = guest bridge mode '1' = host bridge mode

2.3 Reset

The KS8695P has a single reset input that can be driven by a system-reset circuit or a simple power on reset circuit. The KS8695P also features a reset output (WRSTO) that can be used to reset other devices in the system. WRSTO can be configured as either an active high reset or an active low reset through a strap in option on pin U17 as shown in table 1. The KS8695P also has a built in watchdog timer. Once the user programs the watchdog timer, if the timer should expire, the KS8695P will reset itself, and also assert WRSTO to reset the other devices in the system. The following is an illustration of a typical system which uses the KS8695P WRSTO as the system reset.

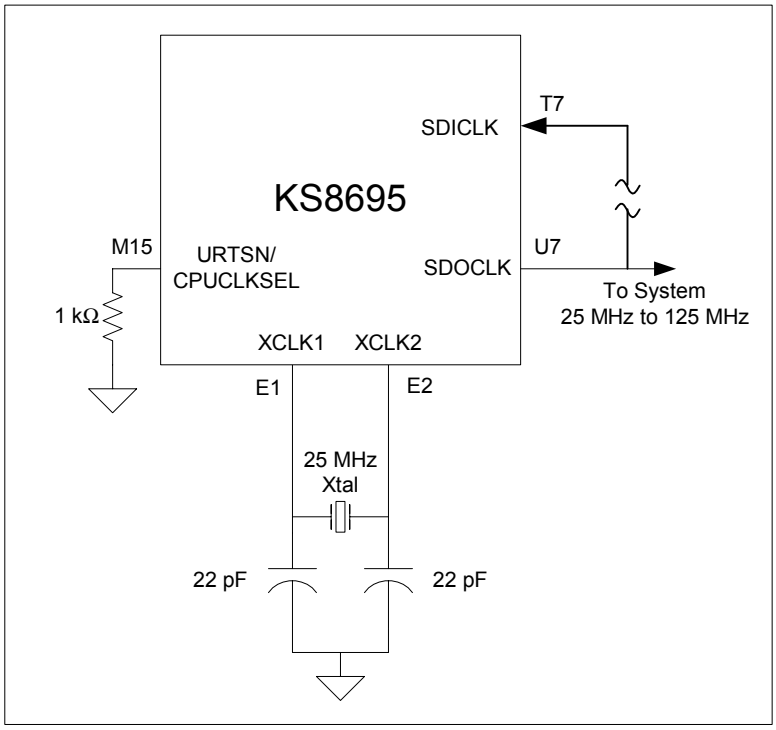
Figure 5 Example Reset Circuit



2.4 System Clock

The clock to the KS8695P can be supplied by either a 25 MHz +/- 100 ppm crystal or by an oscillator. If an oscillator is used it shall be connected to the X1 input (pin E1) on the KS8695P. If a crystal is used, it shall be connected with a circuit like the one shown below. The 25 MHz input clock is used by an internal PLL to generate the programmable SDOCLK. SDOCLK is the system clock, and can be programmed from 25 MHz to 125 MHz using System Clock and Bus Control Register at offset 0x0004. The CPUCLKSEL strap in option on pin M15 needs to be pulled low for normal operation. SDICLK is used to register the data read from the SDRAM back into the KS8695P. The system designer must ensure that SDRAM timing will be met when routing SDOCLK back to SDICLK.

Figure 6 Typical Clock Circuit



2.5 Memory Interface

The KS8695P has a glueless interface for SDRAM, and static memory, ie ROM, SRAM, Flash. It supports up to 2 banks of SDRAM, up to 2 banks of static memory, and 3 banks of external I/O. The total address space for the KS8695P is 64 Megabytes. This includes SDRAM, static memory, external I/O, and the KS8695P's own 64 kbytes of register space. The memory interface for the SDRAM and static memory has a special automatic address mapping feature. This feature allows the designer to directly connect address bit 0 on the memory to ADDR[0] on the KS8695P, and address bit 1 on the memory to ADDR[1] on the memory, regardless of whether the designer is trying to achieve word, half word, or byte addressing. The KS8695P memory controller takes care of the address mapping internally. This also allows the designer the ability to use the maximum amount of address bits, instead of losing one or two because of address mapping. For external I/O, however, the designer still needs to take care of the address mapping.

Figure 7 Static Memory Interface Examples

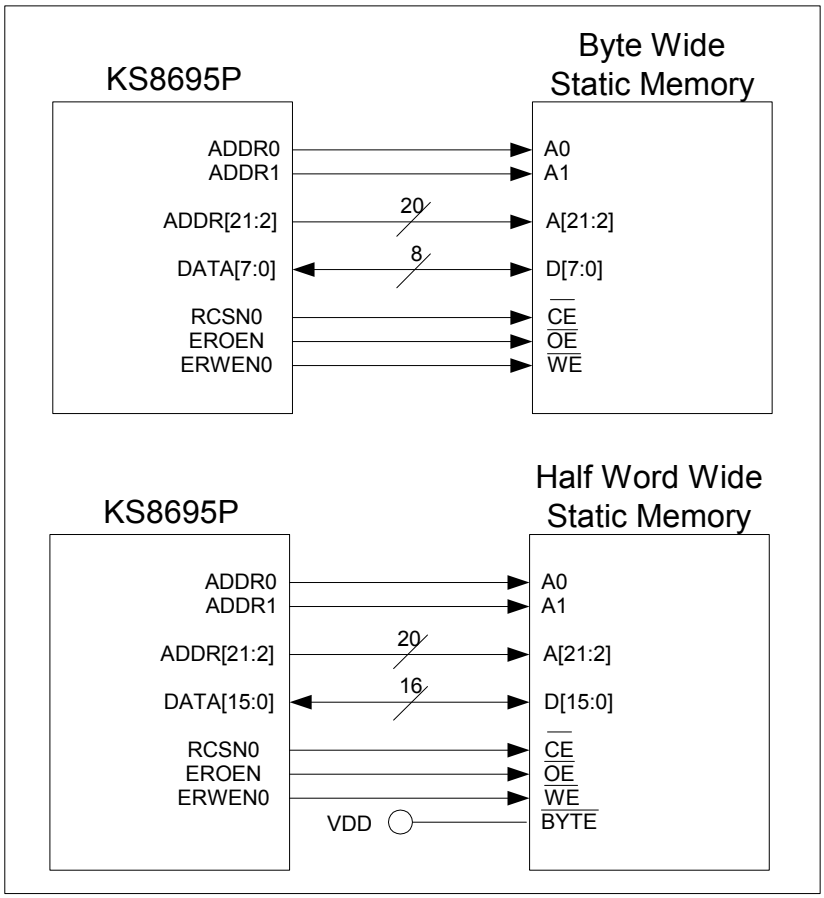


Figure 8 SDRAM Interface Examples

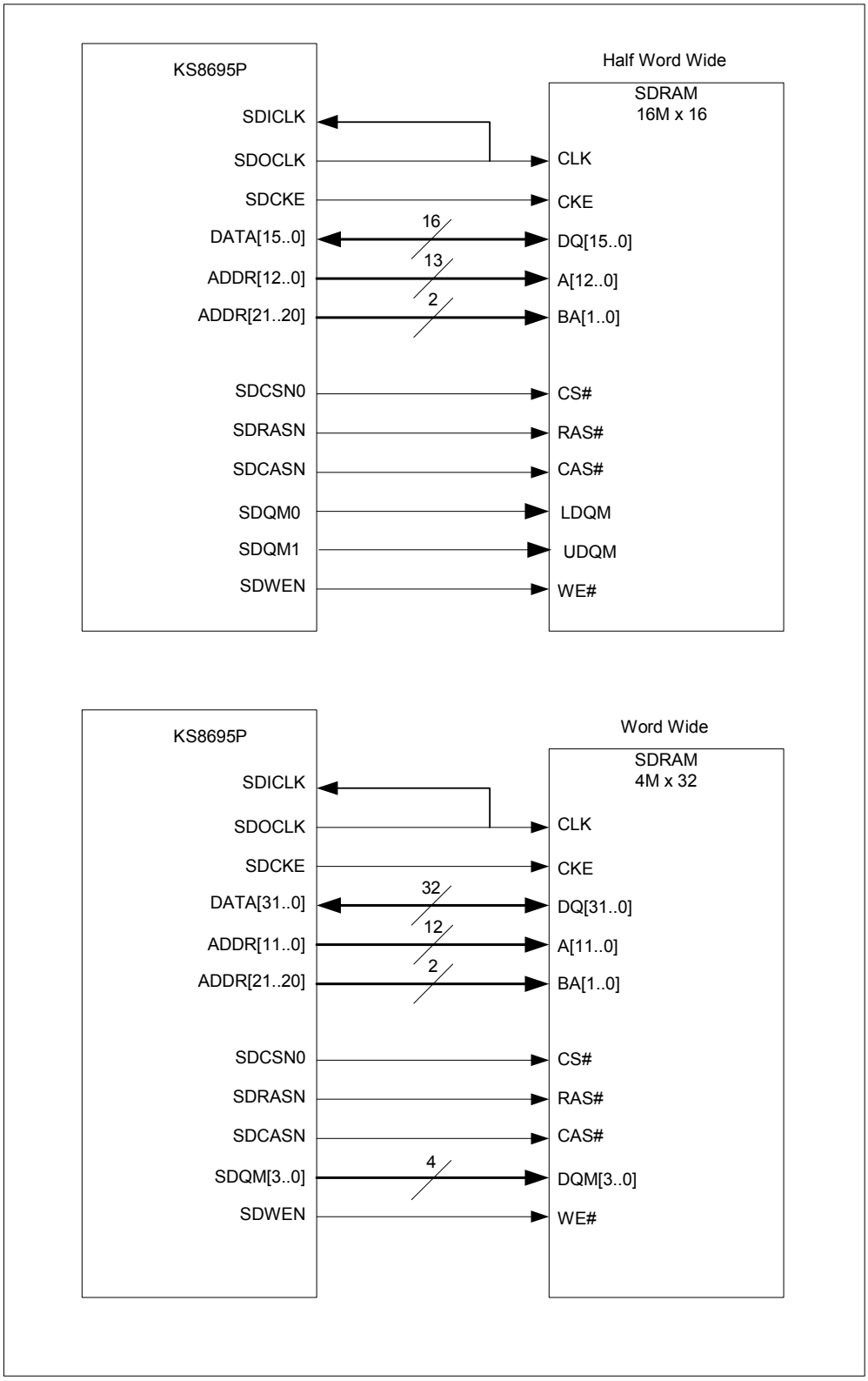
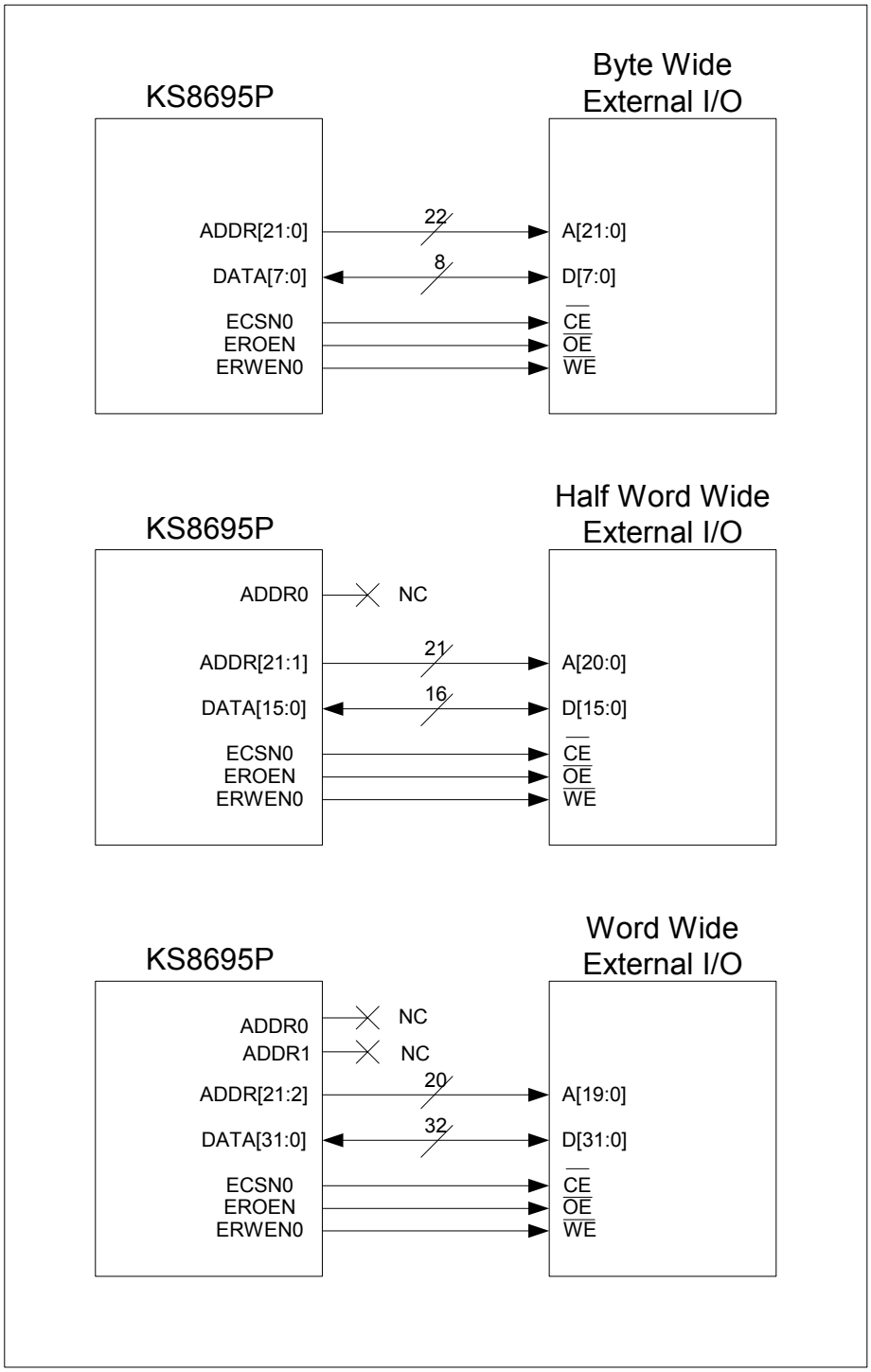


Figure 9 External I/O Interface Examples



2.6 Signal Descriptions by Group

Table 2 Signal Type Key

Type	Description
I	Input
O	Output
I/O	Bi-directional
O/I	Output in normal mode; input pin during reset
Pwr	Power pin
Gnd	Ground pin

Note: Some signals are dual purpose and may occur in more than one group.

Table 3 Clock and Reset Pins

PIN	Pin Name	I/O Type	Pin Description
E1	XCLK1 / CPUCLK	I	**External Clock In.** This signal is used as the source clock for the transmit clock of the internal MAC and PHY. The clock frequency should be 25 MHz ± 100ppm. The XCLK1 signal is also used as the reference clock signal for the internal PLL to generate the 125 MHz internal system clock. **CPUCLK:** factory clock test input when the internal PLL is disabled (factory test signal).
E2	XCLK2	I	**External Clock In.** Used with XCLK1 pin when other polarity of crystal is needed. This is unused for oscillator clock input.
M15	URTSN / CPUCLKSEL	O/I	**Normal mode: UART Request to Send**. Active low output. **During reset: CPU Clock Select**. Select CPU clock source. CPUCLKSEL=0 (normal mode), the internal PLL clock output is used as the CPU clock source. CPUCLKSEL=1 (factory test signal), the external clock to the CPUCLK pin is used as the internal CPU clock source.
A17	RESETN	I	**KS8695P Chip Reset**. Active low input asserted for at least 256 system clock (40 ns) cycles to reset the KS8695P. When in the reset state, all the output pins are tri-stated and all open drain signals are floating.
U17	WRSTO	O	**Watchdog Timer Reset Output. This signal is asserted** for at least 200 msec, **if RESETN is asserted or** when the internal watchdog timer expires.
T17	EROEN / WRSTPLS	O/I	**Normal mode: ROM/SRAM/FLASH and External I/O Output Enable**. Active low. When asserted, this signal controls the output enable port of the specified device. **During reset: Watchdog Timer Reset Polarity Setting**. WRSTPLS=1, active low; WRSTPLS=0, active high. No default.

Table 4 JTAG Interface Pins

PIN	Pin Name	I/O Type	Pin Description
G14	TCK	I	**JTAG Test Clock**
G15	TMS	I	**JTAG Test Mode Select**
F14	TDI	I	**JTAG Test Data In**
F15	TDO	O	**JTAG Test Data Out**
F16	TRSTN	I	**JTAG Test Reset.** Active low.

Table 5 WAN Ethernet Physical Interface Pins

PIN	Pin Name	I/O Type	Pin Description
G1	WANTXP	O	**WAN PHY Transmit signal +** (differential).
G2	WANTXM	O	**WAN PHY Transmit signal -** (differential).
G3	WANRXP	I	**WAN PHY Receive signal +** (differential).
G4	WANRXM	I	**WAN PHY Receive signal -** (differential).
F2	WANFXSD	I	**WAN Fiber Signal Detect.** Signal Detect Input when the WAN port is operated in 100Base-Fx 100Mb fiber mode.

Table 6 LAN Ethernet Physical Interface Pins

PIN	Pin Name	I/O Type	Pin Description
H1 J1 K1 L1	LANTXP1 LANTXP2 LANTXP3 LANTXP4	I	**LAN Port[4:1] PHY Transmit signal +** (differential).
H2 J2 K2 L2	LANTXM1 LANTXM2 LANTXM3 LANTXM4	I	**LAN Port[4:1] PHY Transmit signal -** (differential).
H3 J3 K3 L3	LANRXP1 LANRXP2 LANRXP3 LANRXP4	O	**LAN Port[4:1] PHY Receive signal +** (differential).
H4 J4 K4 L4	LANRXM1 LANRXM2 LANRXM3 LANRXM4	O	**LAN Port[4:1] PHY Receive signal -** (differential).
F1	ISET	I	**Set PHY transmit output current. Connect to ground through a 3.01 kOhm 1% resistor.**
F3	LANFXSD1	I	**LAN1 Fiber Signal Detect.** Signal detect input when the LAN1 port is operated in 100 Base-FX 100 Mb fiber mode.

Table 7 PHY LED Drivers

PIN	Pin Name	I/O Type	Pin Description
E15	WLED0 / B0SIZE0	O/I	**Normal mode: WAN LED indicator 0.** Programmable via WAN Misc. Control Register bits [2:0]. '000' = Speed;'001' = Link; '010' = Full/Half duplex; '011' = Collision; '100' = TX/RX activity; '101' = Full duplex collision; '110' = Link/Activity. **During reset: Bank 0 Data Access Size**. Bank 0 is used for the boot program. B0SIZE[1:0] are used to specify the size of the bank 0 data bus width as follows: '01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved.
E14	WLED1 / B0SIZE1	O/I	**Normal mode: WAN LED indicator 1.** Programmable via WAN Misc. Control Register bits [6:4]. '000' = Speed;'001' = Link; '010' = Full/Half duplex; '011' = Collision; '100' = TX/RX activity; '101' = Full duplex collision; '110' = Link/Activity. **During reset: Bank 0 Data Access Size**. Bank 0 is used for the boot program. B0SIZE[1:0] are used to specify the size of the bank 0 data

			bus width as follows: '01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved.
B17 C17 D17 E17	L1LED0 L2LED0 L3LED0 L4LED0	O	**LAN Port[4:1] LED indicator 0**. Programmable via Switch Control 0 Register bits [27:25]. '000' = Speed;'001' = Link; '010' = Full/Half duplex; '011' = Collision; '100' = TX/RX activity; '101' = Full duplex collision; '110' = Link/Activity.
B16 C16 D16 E16	L1LED1 L2LED1 L3LED1 L4LED1	O	**LAN Port[4:1] LED indicator 1**. Programmable via Switch Control 0 Register bits [24:22]. '000' = Speed; '001' = Link; '010' = Full/Half duplex; '011' = Collision; '100' = TX/RX activity; '101' = Full duplex collision; '110' = Link/Activity.

Table 8 UART Pins

PIN	Pin Name	I/O Type	Pin Description
N16	URXD	I	**UART Receive Data**
N14	UTXD	O	**UART Transmit Data**
N15	UDTRN / DBGENN	O	**UART Data Terminal Ready**. Active low. **Debug enable** (factory test signal).
M16	UDSRN	I	**UART Data Set Ready.** Active low
M15	URTSN / CPUCLKSEL	O/I	**Normal mode: UART Request to Send**. Active low output. **During reset: CPU Clock Select**. Select CPU clock source. CPUCLKSEL=0 (normal mode), the internal PLL clock output is used as the CPU clock source. CPUCLKSEL=1 (factory test signal), the external clock to the CPUCLK pin is used as the internal CPU clock source.
M14	UCTSN / BISTEN	I	**UART Clear to Send.** **BIST enable** (factory test signal).
L15	UDCDN / SCANEN	I	**UART Data Carrier Detect.** **Scan enable** (factory test signal).
L14	URIN / TSTRST	I	**UART Ring Indicator.** **Chip test reset** (factory test signal).

Table 9 GENERAL PURPOSE I/O Pins

PIN	Pin Name	I/O Type	Pin Description
G17	GPIO0 / EINT0	I/O	**General Purpose I/O Pin**. / **External Interrupt Request pin**.
G16	GPIO1 / EINT1	I/O	**General Purpose I/O Pin**. / **External Interrupt Request pin**.
H17	GPIO2 / EINT2	I/O	**General Purpose I/O Pin**. / **External Interrupt Request pin**.
H16	GPIO3 / EINT3	I/O	**General Purpose I/O Pin**. / **External Interrupt Request pin**.
H15	GPIO4 / TOUT0	I/O	**General Purpose I/O Pin**. / **Timer 0 output pin**.
H14	GPIO5 / TOUT1	I/O	**General Purpose I/O Pin**. / **Timer 1 output pin**.
J17	GPIO6	I/O	**General Purpose I/O Pin**.
J16	GPIO7	I/O	**General Purpose I/O Pin**.
J15	GPIO8	I/O	**General Purpose I/O Pin**.
J14	GPIO9	I/O	**General Purpose I/O Pin**.
K17	GPIO10	I/O	**General Purpose I/O Pin**.
K16	GPIO11	I/O	**General Purpose I/O Pin**.
K15	GPIO12	I/O	**General Purpose I/O Pin**.
K14	GPIO13	I/O	**General Purpose I/O Pin**.
L17	GPIO14	I/O	**General Purpose I/O Pin**.
L16	GPIO15	I/O	**General Purpose I/O Pin**.

Table 10 PCI Interface Pins

PIN	Pin Name	I/O Type	Pin Description
A3	PRSTN	I	**PCI Reset**. Active Low This signal is an input used to reset the KS8695P PCI logic. If the KS8695P is the host, use the RESETN signal to drive this input. If the KS8695P is a guest, use the system reset to drive this signal.
D4	PCLK	I	**PCI Bus Clock**. This signal provides the timing for the PCI bus transactions. This signal is used to drive the PCI bus interface and the internal PCI logic. All PCI bus signals are sampled on the rising edges of the PCLK. PCLK can operate from 20MHz to 33MHz. For host mode, use a PCLKOUT signal to drive this input. In guest mode, use the system PCI clock to drive this input.
C2	GNT3N	O	**PCI Bus Grant 3.** Active Low In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the device connected to REQ3N. In Guest Bridge Mode, this signal is reserved.
C3	GNT2N	O	**PCI Bus Grant 2.** Active Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the device connected to REQ2N. In Guest Bridge Mode, this signal is reserved.
C4	GNT1N	O	**PCI Bus Grant 1.** Active Low. In Host Bridge Mode, this is an output signal from the internal PCI arbiter to grant PCI bus access to the device connected to REQ1N. In Guest Bridge Mode, this signal is an output to indicate that the KS8695P is requesting to access the PCI bus as a PCI master. In guest bridge mode, this is basically the KS8695P's request output.
B2	REQ3N	I	**PCI Bus Request 3.** Active Low. In Host Bridge Mode, this is an input signal from the external PCI device to request PCI bus access. In Guest Bridge Mode, this signal is reserved.
B3	REQ2N	I	**PCI Bus Request 2.** Active Low. In Host Bridge Mode, this is an input signal from the external PCI device to request PCI bus access. In Guest Bridge Mode, this signal is reserved.
B4	REQ1N	I	**PCI Bus Request 1** Active Low. In Host Bridge Mode, this is an input signal from the external PCI device to request PCI bus access. In Guest Bridge Mode, this is an input signal from an external PCI bus arbiter granting access to the bus. In guest bridge mode this is basically the KS8695P's grant input.
A4 D5 B5 C5 A5 D6 B6 C6 B7 C7	PAD31 PAD30 PAD29 PAD28 PAD27 PAD26 PAD25 PAD24 PAD23 PAD22	I/O	**32-bit PCI Address and Data.** PCI bus transactions consist of an address phase followed by one or more data phases. Address and data signals are multiplexed on the same pins. For a PCI write transaction the source of the data will be the KS8695P. For a PCI read transaction, the data source will be the target. The KS8695P supports both read and write burst transactions. In the case of a read transaction, a special data turn around cycle is needed between the address phase and the data phase(s).

A7 D8 B8 D9 A8 C9 D12 B12 C12 A12 D13 B13 C13 A13 B14 C14 A14 D15 B15 C15 A15 A16	PAD21 PAD20 PAD19 PAD18 PAD17 PAD16 PAD15 PAD14 PAD13 PAD12 PAD11 PAD10 PAD9 PAD8 PAD7 PAD6 PAD5 PAD4 PAD3 PAD2 PAD1 PAD0		
A6 B9 A11 D14	CBEN3 CBEN2 CBEN1 CBEN0	I/O	**PCI Commands and Byte Enable.** Active Low. The PCI command and byte enable signals are multiplexed on the same pins. During the first clock cycle of a PCI transaction, the CBEN bus contains the command for the transaction. The PCI transaction consists of the address phases and one or more data phases. During the data phases of the transaction, the bus carries the byte enable for the current data phases.
C8	PAR	I/O	**Parity** PCI Bus parity is even across PAD[31:0] and CBEN[3:0]. The KS8695P generates PAR during the address phase and write data phases as a bus master, and during read data phases as a target. It checks for correct PAR during the read data phase as a bus master, during every address phase as a bus slave, and during write data phases as a target.
D10	FRAMEN	I/O	**PCI Bus Frame Signal.** Active Low. FRAMEN is an indication of an active PCI bus cycle. It is asserted at the beginning of a PCI transaction, i.e. the address phase, and deasserted before the final transfer of the data phase of the transaction.
A9	IRDYN	I/O	**PCI Initiator Ready Signal** Active Low. This signal is asserted by a PCI master to indicate a valid data phase on the PAD bus during data phases of a write transaction. During a read transaction, it indicates that the master is ready to accept data from the target. A target will monitor the IRDYN signal when a data phase is completed on any rising edge of the PCI clock when both IRDYN and TRDYN are asserted. Wait cycles are inserted until both IRDYN and TRDYN are asserted together.
C10	TRDYN	I/O	**PCI Target Ready Signal.** Active Low. This signal is asserted by a PCI slave to indicate a valid data phase on the PAD bus during a read transaction. During a write transaction, it indicates that the slave is ready to accept data from the target. A PCI initiator will monitor the TRDYN signal when a data phase is completed on any rising edge of the PCI clock when both IRDYN and

			TRDYN are asserted. Wait cycles are inserted until both IRDYN and TRDYN are asserted together.
C11	DEVSELN	I/O	**PCI Device Select Signal.** Active Low. This signal is asserted when the KS8695P is selected as a target during a bus transaction. When the KS8695P is the initiator of the current bus access, it expects the target to assert DEVSELN within 5 PCI bus cycles, confirming the access. If the target does not assert DEVSELN within the required bus cycles, the KS8695P aborts the bus cycle. To meet the timing requirement, the KS8695P asserts this signal in a medium speed decode timing. (2 bus cycles)
D7	IDSEL	I	**Initialization Device Select**. Active High. It is used as a chip select during configuration read and write transactions.
D11	STOPN	I/O	**PCI Stop Signal.** Active Low. This signal is asserted by the PCI target to indicate to the bus master that it is terminating the current transaction. The KS8695P responds to the assertion of STOPN when it is the bus master, either to disconnect, retry, or abort.
B11	PERRN	I/O	**PCI Parity Error Signal.** Active Low. The KS8695P asserts PERRN when it checks and detects a bus parity error. When it generates the PAR output, the KS8695P monitors for any reported parity error on PERRN. When the KS8695P is the bus master and a parity error is detected, the KS8695P sets error bits in the control status registers. It completes the current data burst transaction, then stops the operation. After the Host clears the system error, the KS8695P continues its operation.
A10	SERRN	O	**PCI System Error Signal.** Active Low. If an address parity error is detected, the KS8695P asserts the SERRN signal two clocks after the failing address.
E4	M66EN	I	**PCI 66MHz Enable** When asserted, this signal indicates the PCI Bus segment is operating at 66 MHz. This pin is mainly used in Guest bridge mode when the PCLK is driven by an external Host bridge.
D1	PCLKOUT3	O	**PCI Clock output 3.**
C1	PCLKOUT2	O	**PCI Clock output 2.**
B1	PCLKOUT1	O	**PCI Clock output 1.**
A2	PCLKOUT0	O	**PCI Clock output 0.**
B10	CLKRUNN	I/O	This is a CardBus only signal. The CLKRUNN signal is used by portable CardBus devices to request that the system turn on the bus clock. Output is always active in cardbus and miniPCI modes.
D2	MPCIACTN	O	**Mini-PCI Active**. This signal is asserted by the PCI device to indicate that its current function requires fulll system performance. MPCIACTN is an open drain output signal. In miniPCI mode, this signal is always low.
D3	PBMS	I	**PCI Bridge Mode Select** Selects the operating mode for the PCI Bridge. When PBMS is High, the Host Bridge Mode is selected and the on chip PCI bus arbiter is enabled. When PBMS is Low, the Guest Bridge Mode is selected and the on-chip arbiter is disabled.

Table 11 ADVANCED MEMORY INTERFACE (SDRAM/ROM/FLASH/SRAM/EXTERNAL I/O)

PIN	Pin Name	I/O Type	Pin Description
T7	SDICLK	I	**SDRAM Clock In.** SDRAM Clock Input for the SDRAM memory controller interface.
U7	SDOCLK	O	**System/SDRAM Clock Out**. Output of the internal system clock, it is also used as the clock signal for SDRAM interface.
P4	ADDR21/BA1	O	**Address Bit 21/Bank Address Input 1.** Address bit 21 for asynchronous accesses. Bank Address Input bit 1 for SDRAM accesses.
P3	ADDR20/BA0	O	**Address Bit 20/Bank Address Input 0.** Address bit 20 for asynchronous accesses. Bank Address Input bit 0 for SDRAM accesses.
M3 M2 M1 N4 N3 N2 N1 P2 P1 R3 R2 R1 T2 T1 U1 U2 T3 U3 T4 U4	ADDR[19] ADDR[18] ADDR[17] ADDR[16] ADDR[15] ADDR[14] ADDR[13] ADDR[12] ADDR[11] ADDR[10] ADDR[9] ADDR[8] ADDR[7] ADDR[6] ADDR[5] ADDR[4] ADDR[3] ADDR[2] ADDR[1] ADDR[0]	O	**Address Bus.** The 22-bit address bus (including ADDR[21:20] above) covers 4M word memory space shared by ROM/SRAM/FLASH, SDRAM, and external I/O banks. During the SDRAM cycles, the internal address bus is used to generate RAS and CAS addresses for the SDRAM. The number of column address bits in the SDRAM banks can be programmed from 8 to 11 bits via the SDRAM control registers. ADDR[12:0] are the SDRAM address, and ADDR[21:20] are the SDRAM bank address. During other cycles, the ADDR[21:0] is the byte address of the data transfer. For SDRAM and FLASH/ROM/SRAM, connect all address lines, i.e. A0 to A0, A1 to A1, etc… The memory controller will automatically take care of address line adjustments for 8/16/32 bit accesses. For External I/O devices, the user will need to connect address lines appropriately for 8/16/32 bit accesses.
P7 R7 P8 R8 T8 U8 P9 R9 T9 U9 P10 R10 T10 U10 P11 R11 T11 U11 P12 R12 T12	DATA[31] DATA[30] DATA[29] DATA[28] DATA[27] DATA[26] DATA[25] DATA[24] DATA[23] DATA[22] DATA[21] DATA[20] DATA[19] DATA[18] DATA[17] DATA[16] DATA[15] DATA[14] DATA[13] DATA[12] DATA[11]	I/O	**External DATA Bus.** 32-bit bi-directional data bus for data transfer. The KS8695P also supports 8-bit, and 16-bit data bus widths.

U12 P13 R13 T13 U13 P14 R14 T14 U14 T15 U15	DATA[10] DATA[9] DATA[8] DATA[7] DATA[6] DATA[5] DATA[4] DATA[3] DATA[2] DATA[1] DATA[0]		
R4 P5	SDCSN[1] SDCSN[0]	O	**SDRAM Chip Select**. Active low. The KS8695P supports up to two SDRAM banks. One SDCSN output is provided for each bank.
R5	SDRASN	O	**SDRAM Row Address Strobe**, Active low. The Row Address Strobe pin for SDRAM.
T5	SDCASN	O	**SDRAM Column Address Strobe**, Active low. The Column Address Strobe pin for SDRAM.
U5	SDWEN	O	**SDRAM Write Enable**. Active low. The write enable signal for SDRAM.
P6 R6 T6 U6	SDQM[3] SDQM[2] SDQM[1] SDQM[0]	O	**SDRAM Data Input/Output Mask.** Data Input/Output mask signals for SDRAM. The SDQM is sampled high and is an output mask signal for write accesses and an output enable signal for read accesses. Input data are masked during a Write cycle. The SDQM0/1/2/3 correspond to DATA[7:0], DATA[15:8], DATA[23:16] and DATA[31:24], respecitvely.
U16 T16 R16	ECSN[2] ECSN[1] ECSN[0]	O	**External I/O Device Chip Select**. Active low. Three External I/O banks are provided for external memory-mapped I/O operations. Each I/O bank stores up to 16Kbytes. The ECSNx signals indicate which of the three I/O banks is selected.
P16	EWAITN	I	**External Wait**. Active low. This signal is asserted when an external I/O device or a ROM/SRAM/FLASH bank needs more access cycles than those defined in the corresponding control register.
R15 P15	RCSN[1] RCSN[0]	O	**ROM/SRAM/FLASH Chip select**. Active low. The KS8695P can access up to two external ROM/SRAM/FLASH memory banks. The RCSN pins can be controlled to map the CPU addresses into physical memory banks.
T17	EROEN/ WRSTPLS	O/I	**Normal mode: External I/O & ROM/SRAM/FLASH Output Enable**. Active low. When asserted, this signal controls the output enable port of the specified memory device. **During reset: Watchdog Timer Reset Polarity Setting**. WRSTPLS=1, active low; WRSTPLS=0, active high. No default.
M17	ERWEN0 / TESTACK	O	**External I/O & ROM/SRAM/FLASH Write Byte Enable**. Active low. When asserted, the ERWENx controls the byte write enable of the memory device(except SDRAM). **ARM CPU test signal** (factory test signal)
N17	ERWEN1 / TESTREQB	O	**External I/O & ROM/SRAM/FLASH Write Byte Enable**. Active low. When asserted, the ERWENx controls the byte write enable of the memory device (except SDRAM). **ARM CPU test signal** (factory test signal)
P17	ERWEN2 / TESTREQA	O	**External I/O & ROM/SRAM/FLASH Write Byte Enable**. Active low. When asserted, the ERWENx controls the byte write enable of the memory device except SDRAM). **ARM CPU test signal** (factory test signal)

R17	ERWEN3 / TICTESTENN	O	**External I/O & ROM/SRAM/FLASH Write Byte Enable**. Active low. When asserted, the ERWENx controls the byte write enable of the memory device (except SDRAM). **ARM CPU test signal** (factory test signal)
E15	WLED0/ B0SIZE0	O/I	**Normal mode: WAN LED indicator 0.** Programmable via WAN Misc. Control Register bits [2:0]. 000 = Speed; 001 = Link; 010 = Full/Half duplex; 011 = Collision; 100 = TX/RX activity; 101 = Full duplex collision; 110 = Link/Activity. **During reset: Bank 0 Data Access Size**. Bank 0 is used for the boot program. B0SiZE[1:0] are used to specify the size of the bank 0 data bus width as follows: '01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved.
E14	WLED1 / B0SIZE1	O/I	**Normal mode: WAN LED indicator 1.** Programmable via WAN Misc. Control Register bits [6:4]. 000 = Speed; 001 = Link; 010 = Full/Half duplex; 011 = Collision; 100 = TX/RX activity; 101 = Full duplex collision; 110 = Link/Activity. **During reset: Bank 0 Data Access Size**. Bank 0 is used for the boot program. B0SIZE[1:0] are used to specify the size of the bank 0 data bus width as follows: '01' = one byte, '10' = half-word, '11' = one word, and '00' = reserved.

Table 12 Test Pins

PIN	Pin Name	I/O Type	Pin Description
F17	TESTEN	I	**Chip test enable** (factory test signal), pull down if not used.
M4	TEST1	I	**PHY test pin** (factory test signal), No Connect in normal operation.
F4	TEST2	I	**PHY test pin** (factory test signal), No Connect in normal operation.

Table 13 Power and Ground Pins

PIN	Pin Name	I/O Type	Pin Description
E5 E6 F5 F6 G5 G6 H5 H6 J5 J6	VDDA1.8	PWR	**1.8V analog VDD.**
E7 E8 E9 E10 F7 F8 F9 F10 M7 M8 M9 H12 H13	VDD1.8	PWR	**1.8V digital core VDD.**

J12 J13 K12 K13 N7 N8 N9			
K5 K6 L5 L6 M5 M6 N5 N6	VDDA3.3	PWR	**3.3V analog VDD.**
E11 E12 E13 F11 F12 F13 G12 G13 L12 L13 M10 M11 M12 M13 N10 N11 N12 N13	VDD3.3	PWR	**3.3V digital I/O VDD.**
E3 H7 J7 K7 L7	AGND	GND	**Analog Ground**
A1 G7 G8 G9 G10 G11 H8 H9 H10 H11 J8 J9 J10 J11 K8 K9 K10	GND	GND	**Ground**

K11 L8 L9 L10 L11			

Table 14 Signal List Alphabetized by Pin Name

Pin#	Pin Name	Type	Brief Description
U4	ADDR0	O	Address Bit
T4	ADDR1	O	Address Bit
R3	ADDR10	O	Address Bit
P1	ADDR11	O	Address Bit
P2	ADDR12	O	Address Bit
N1	ADDR13	O	Address Bit
N2	ADDR14	O	Address Bit
N3	ADDR15	O	Address Bit
N4	ADDR16	O	Address Bit
M1	ADDR17	O	Address Bit
M2	ADDR18	O	Address Bit
M3	ADDR19	O	Address Bit
U3	ADDR2	O	Address Bit
P3	ADDR20/BA0	O	Address Bit/Bank Address bit 0 for SDRAM interface
P4	ADDR21/BA1	O	Address Bit/Bank Address bit 1 for SDRAM interface
T3	ADDR3	O	Address Bit
U2	ADDR4	O	Address Bit
U1	ADDR5	O	Address Bit
T1	ADDR6	O	Address Bit
T2	ADDR7	O	Address Bit
R1	ADDR8	O	Address Bit
R2	ADDR9	O	Address Bit
E3	AGND	Gnd	Analog Signal Ground
H7	AGND	Gnd	Analog Signal Ground
J7	AGND	Gnd	Analog Signal Ground
K7	AGND	Gnd	Analog Signal Ground
L7	AGND	Gnd	Analog Signal Ground
D14	CBEN0	I/O	PCI Commands and Byte Enable 0. Active Low.
A11	CBEN1	I/O	PCI Commands and Byte Enable 1. Active Low.
B9	CBEN2	I/O	PCI Commands and Byte Enable 2. Active Low.
A6	CBEN3	I/O	PCI Commands and Byte Enable 3. Active Low.
B10	CLKRUNN	I/O	Cardbus clock run request signal. Active Low.
U15	DATA0	I/O	External DATA Bit
T15	DATA1	I/O	External DATA Bit
U12	DATA10	I/O	External DATA Bit
T12	DATA11	I/O	External DATA Bit
R12	DATA12	I/O	External DATA Bit
P12	DATA13	I/O	External DATA Bit
U11	DATA14	I/O	External DATA Bit
T11	DATA15	I/O	External DATA Bit
R11	DATA16	I/O	External DATA Bit
P11	DATA17	I/O	External DATA Bit

U10	DATA18	I/O	External DATA Bit
T10	DATA19	I/O	External DATA Bit
U14	DATA2	I/O	External DATA Bit
R10	DATA20	I/O	External DATA Bit
P10	DATA21	I/O	External DATA Bit
U9	DATA22	I/O	External DATA Bit
T9	DATA23	I/O	External DATA Bit
R9	DATA24	I/O	External DATA Bit
P9	DATA25	I/O	External DATA Bit
U8	DATA26	I/O	External DATA Bit
T8	DATA27	I/O	External DATA Bit
R8	DATA28	I/O	External DATA Bit
P8	DATA29	I/O	External DATA Bit
T14	DATA3	I/O	External DATA Bit
R7	DATA30	I/O	External DATA Bit
P7	DATA31	I/O	External DATA Bit
R14	DATA4	I/O	External DATA Bit
P14	DATA5	I/O	External DATA Bit
U13	DATA6	I/O	External DATA Bit
T13	DATA7	I/O	External DATA Bit
R13	DATA8	I/O	External DATA Bit
P13	DATA9	I/O	External DATA Bit
C11	DEVSELN	I/O	PCI Device Select Signal. Active Low.
R16	ECSN0	O	External I/O Device Chip Select. Active low
T16	ECSN1	O	External I/O Device Chip Select. Active low
U16	ECSN2	O	External I/O Device Chip Select. Active low
T17	EROEN / WRSTPLS	O/I	ROM/SRAM/FLASH and External I/O Output Enable. Active low. /WRSTO polarity select.
M17	ERWEN0 / TESTACK	O	External I/O & ROM/SRAM/FLASH Write Byte Enable. Active low.
N17	ERWEN1 / TESTREQB	O	External I/O & ROM/SRAM/FLASH Write Byte Enable. Active low.
P17	ERWEN2 / TESTREQA	O	External I/O & ROM/SRAM/FLASH Write Byte Enable. Active low.
R17	ERWEN3 / TICTESTENN	O	External I/O & ROM/SRAM/FLASH Write Byte Enable. Active low.
P16	EWAITN	I	External Wait. Active low.
D10	FRAMEN	I/O	PCI Bus Frame Signal. Active Low.
A1	GND	Gnd	Signal Ground
G7	GND	Gnd	Signal Ground
G8	GND	Gnd	Signal Ground
G9	GND	Gnd	Signal Ground
G10	GND	Gnd	Signal Ground
G11	GND	Gnd	Signal Ground
H8	GND	Gnd	Signal Ground
H9	GND	Gnd	Signal Ground
H10	GND	Gnd	Signal Ground
H11	GND	Gnd	Signal Ground
J8	GND	Gnd	Signal Ground
J9	GND	Gnd	Signal Ground
J10	GND	Gnd	Signal Ground

J11	GND	Gnd	Signal Ground
K8	GND	Gnd	Signal Ground
K9	GND	Gnd	Signal Ground
K10	GND	Gnd	Signal Ground
K11	GND	Gnd	Signal Ground
L8	GND	Gnd	Signal Ground
L9	GND	Gnd	Signal Ground
L10	GND	Gnd	Signal Ground
L11	GND	Gnd	Signal Ground
C4	GNT1N	O	PCI Bus Grant 2. Active low. Output for host bridge mode and guest bridge mode.
C3	GNT2N	O	PCI Bus Grant 2. Active low. Output for host bridge mode. Not used in guest bridge mode.
C2	GNT3N	O	PCI Bus Grant 3. Active low. Output for host bridge mode. Not used in guest bridge mode.
G17	GPIO0 / EINT0	I/O	General Purpose I/O Pin. / External Interrupt Request pin.
G16	GPIO1 / EINT1	I/O	General Purpose I/O Pin. / External Interrupt Request pin.
K17	GPIO10	I/O	General Purpose I/O Pin.
K16	GPIO11	I/O	General Purpose I/O Pin.
K15	GPIO12	I/O	General Purpose I/O Pin.
K14	GPIO13	I/O	General Purpose I/O Pin.
L17	GPIO14	I/O	General Purpose I/O Pin.
L16	GPIO15	I/O	General Purpose I/O Pin.
H17	GPIO2 / EINT2	I/O	General Purpose I/O Pin. / External Interrupt Request pin.
H16	GPIO3 / EINT3	I/O	General Purpose I/O Pin. / External Interrupt Request pin.
H15	GPIO4 / TOUT0	I/O	General Purpose I/O Pin. / Timer 0 output pin.
H14	GPIO5 / TOUT1	I/O	General Purpose I/O Pin. / Timer 1 output pin.
J17	GPIO6	I/O	General Purpose I/O Pin.
J16	GPIO7	I/O	General Purpose I/O Pin.
J15	GPIO8	I/O	General Purpose I/O Pin.
J14	GPIO9	I/O	General Purpose I/O Pin.
D7	IDSEL	I	Initialization Device Select. Active High.
A9	IRDYN	I/O	PCI Initiator Ready Signal. Active Low.
F1	ISET		Set PHY transmit output current. Connect to ground with 3.01 kOhm 1% resistor.
B17	L1LED0	O	LAN Port 1 LED programmable indicator 0. Active Low
B16	L1LED1	O	LAN Port 1 LED programmable indicator 1. Active Low
C17	L2LED0	O	LAN Port 2 LED programmable indicator 0. Active Low
C16	L2LED1	O	LAN Port 2 LED programmable indicator 1. Active Low
D17	L3LED0	O	LAN Port 3 LED programmable indicator 0. Active Low
D16	L3LED1	O	LAN Port 3 LED programmable indicator 1. Active Low
E17	L4LED0	O	LAN Port 4 LED programmable indicator 0. Active Low
E16	L4LED1	O	LAN Port 4 LED programmable indicator 1. Active Low
H4	LANRXM1	I	LAN Port 1 PHY Receive signal - (differential).
J4	LANRXM2	I	LAN Port 2 PHY Receive signal - (differential).
K4	LANRXM3	I	LAN Port 3 PHY Receive signal - (differential).
L4	LANRXM4	I	LAN Port 4 PHY Receive signal - (differential).
H3	LANRXP1	I	LAN Port 1 PHY Receive signal + (differential).
J3	LANRXP2	I	LAN Port 2 PHY Receive signal + (differential).
K3	LANRXP3	I	LAN Port 3 PHY Receive signal + (differential).

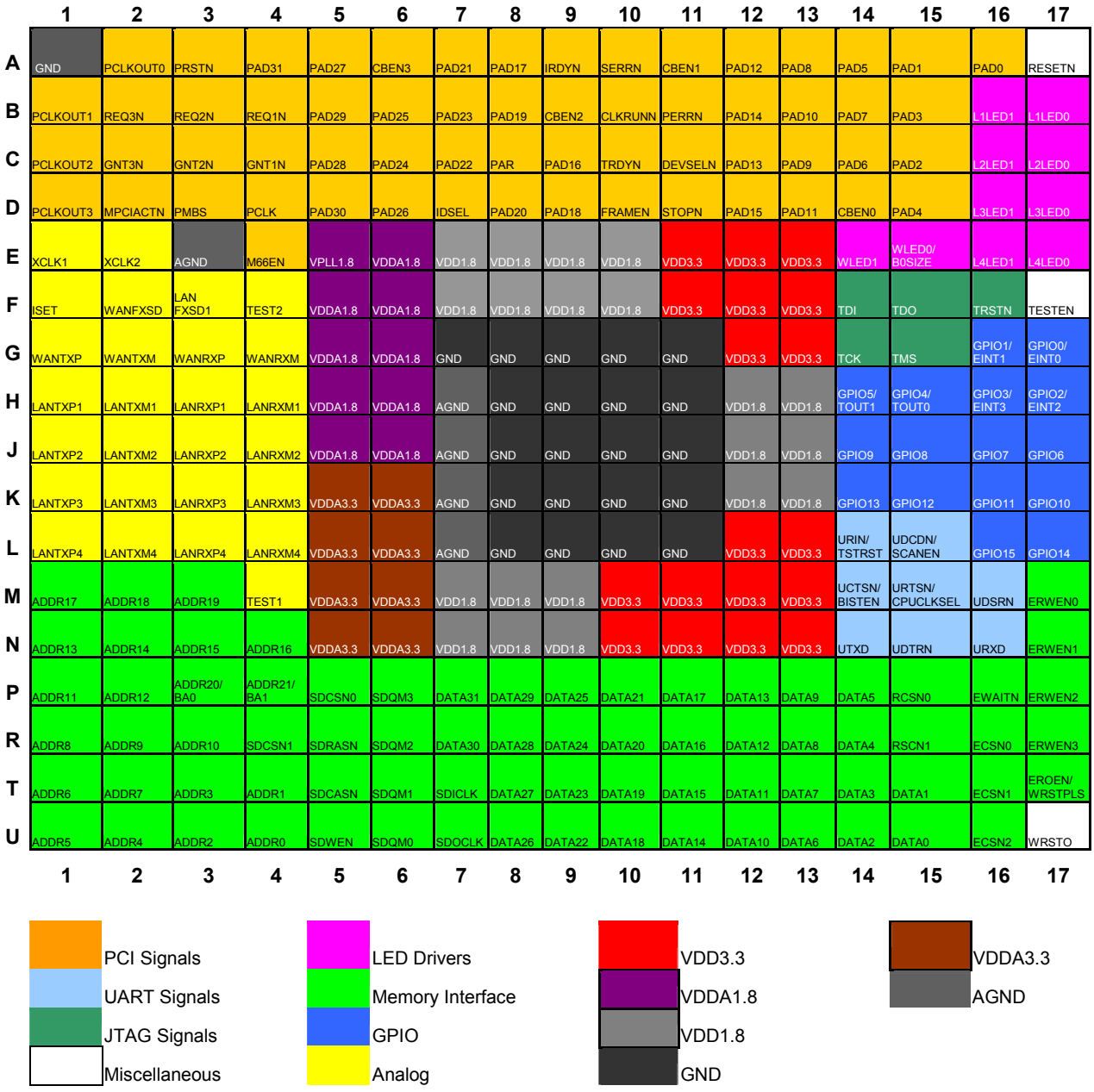
L3	LANRXP4	I	LAN Port 4 PHY Receive signal + (differential).
H2	LANTXM1	O	LAN Port 1 PHY Transmit signal - (differential).
J2	LANTXM2	O	LAN Port 2 PHY Transmit signal - (differential).
K2	LANTXM3	O	LAN Port 3 PHY Transmit signal - (differential).
L2	LANTXM4	O	LAN Port 4 PHY Transmit signal - (differential).
H1	LANTXP1	O	LAN Port 1 PHY Transmit signal + (differential).
J1	LANTXP2	O	LAN Port 2 PHY Transmit signal + (differential).
K1	LANTXP3	O	LAN Port 3 PHY Transmit signal + (differential).
L1	LANTXP4	O	LAN Port 4 PHY Transmit signal + (differential).
E4	M66EN	I	PCI 66 MHz Enable.
D2	MPCIACTN	O	MiniPCI Active Signal. Active Low.
A16	PAD0	I/O	PCI Address and Data 0
A15	PAD1	I/O	PCI Address and Data 1
B13	PAD10	I/O	PCI Address and Data 10
D13	PAD11	I/O	PCI Address and Data 11
A12	PAD12	I/O	PCI Address and Data 12
C12	PAD13	I/O	PCI Address and Data 13
B12	PAD14	I/O	PCI Address and Data 14
D12	PAD15	I/O	PCI Address and Data 15
C9	PAD16	I/O	PCI Address and Data 16
A8	PAD17	I/O	PCI Address and Data 17
D9	PAD18	I/O	PCI Address and Data 18
B8	PAD19	I/O	PCI Address and Data 19
C15	PAD2	I/O	PCI Address and Data 2
D8	PAD20	I/O	PCI Address and Data 20
A7	PAD21	I/O	PCI Address and Data 21
C7	PAD22	I/O	PCI Address and Data 22
B7	PAD23	I/O	PCI Address and Data 23
C6	PAD24	I/O	PCI Address and Data 24
B6	PAD25	I/O	PCI Address and Data 25
D6	PAD26	I/O	PCI Address and Data 26
A5	PAD27	I/O	PCI Address and Data 27
C5	PAD28	I/O	PCI Address and Data 28
B5	PAD29	I/O	PCI Address and Data 29
B15	PAD3	I/O	PCI Address and Data 3
D5	PAD30	I/O	PCI Address and Data 30
A4	PAD31	I/O	PCI Address and Data 31
D15	PAD4	I/O	PCI Address and Data 4
A14	PAD5	I/O	PCI Address and Data 5
C14	PAD6	I/O	PCI Address and Data 6
B14	PAD7	I/O	PCI Address and Data 7
A13	PAD8	I/O	PCI Address and Data 8
C13	PAD9	I/O	PCI Address and Data 9
C8	PAR	I/O	PCI Parity
D3	PBMS	I	PCI Bridge Mode Select. ‘1’ = Host bridge mode. ‘0’ = Guest bridge mode.
D4	PCLK	I	PCI Bus Clock

A2	PCLKOUT0	O	PCI Clock Output 0
B1	PCLKOUT1	O	PCI Clock Output 1
C1	PCLKOUT2	O	PCI Clock Output 2
D1	PCLKOUT3	O	PCI Clock Output 3
B11	PERRN	I/O	PCI Parity Error Signal. Active Low.
A3	PRSTN	I	PCI Reset. Active Low
P15	RCSN0	O	ROM/SRAM/FLASH Chip select. Active low.
R15	RCSN1	O	ROM/SRAM/FLASH Chip select. Active low.
B4	REQ1N	I	PCI Bus Request 1. Active Low. Input for host bridge mode and guest brige mode.
B3	REQ2N	I	PCI Bus Request 2. Active Low. Input for host bridge mode, not used in guest mode.
B2	REQ3N	I	PCI Bus Request 3. Active Low. Input for host bridge mode, not used in guest mode.
A17	RESETN	I	KS8695 Chip Reset. Active low.
T5	SDCASN	O	SDRAM Column Address Strobe, active low.
P5	SDCSN0	O	SDRAM Chip Select. Active low chip select pins for SDRAM
R4	SDCSN1	O	SDRAM Chip Select. Active low chip select pins for SDRAM
T7	SDICLK	I	SDRAM Clock In
U7	SDOCLK	O	System/SDRAM Clock Out
U6	SDQM0	O	SDRAM Data Input/Output Mask.
T6	SDQM1	O	SDRAM Data Input/Output Mask.
R6	SDQM2	O	SDRAM Data Input/Output Mask.
P6	SDQM3	O	SDRAM Data Input/Output Mask.
R5	SDRASN	O	SDRAM Row Address Strobe, active low.
U5	SDWEN	O	SDRAM Write Enable. Active low.
A10	SERRN	O	PCI System Error Signal. Active Low.
D11	STOPN	I/O	PCI Stop Signal. Active Low.
G14	TCK	I	JTAG Test Clock
F14	TDI	I	JTAG Test Data In
F15	TDO	O	JTAG Test Data Out
M4	TEST1	I	PHY test pin (factory test signal)
F4	TEST2		PHY test pin (factory test signal)
F17	TESTEN	I	Chip test enable (factory test signal)
G15	TMS	I	JTAG Test Mode Select
C10	TRDYN	I/O	PCI Target Ready Signal. Active Low.
F16	TRSTN	I	JTAG Test Reset. Active low.
M14	UCTSN / BISTEN	I	UART Data Set Ready. Active low./BIST enable (factory test signal).
L15	UDCDN / SCANEN	I	UART Data Carrier Detect./Scan enable (factory test signal).
M16	UDSRN	I	UART Data Set Ready. Active low
N15	UDTRN / DBGENN	O	UART Data Terminal Ready. Active low. /Debug enable (factory test signal).
L14	URIN / TSTRST	I	UART Ring Indicator/Chip test reset (factory test signal)
M15	URTSN / CPUCLKSEL	O/I	UART Request to Send/CPU Clock Select
N16	URXD	I	UART Receive Data
N14	UTXD	O	UART Transmit Data
E7	VDD1.8	Pwr	1.8V digital core VDD.
E8	VDD1.8	Pwr	1.8V digital core VDD.
E9	VDD1.8	Pwr	1.8V digital core VDD.
E10	VDD1.8	Pwr	1.8V digital core VDD.

F7	VDD1.8	Pwr	1.8V digital core VDD.
F8	VDD1.8	Pwr	1.8V digital core VDD.
F9	VDD1.8	Pwr	1.8V digital core VDD.
F10	VDD1.8	Pwr	1.8V digital core VDD.
M7	VDD1.8	Pwr	1.8V digital core VDD.
M8	VDD1.8	Pwr	1.8V digital core VDD.
M9	VDD1.8	Pwr	1.8V digital core VDD.
H12	VDD1.8	Pwr	1.8V digital core VDD.
H13	VDD1.8	Pwr	1.8V digital core VDD.
J12	VDD1.8	Pwr	1.8V digital core VDD.
J13	VDD1.8	Pwr	1.8V digital core VDD.
K12	VDD1.8	Pwr	1.8V digital core VDD.
K13	VDD1.8	Pwr	1.8V digital core VDD.
N7	VDD1.8	Pwr	1.8V digital core VDD.
N8	VDD1.8	Pwr	1.8V digital core VDD.
N9	VDD1.8	Pwr	1.8V digital core VDD.
E11	VDD3.3	Pwr	3.3V digital I/O circuitry VDD
E12	VDD3.3	Pwr	3.3V digital I/O circuitry VDD
E13	VDD3.3	Pwr	3.3V digital I/O circuitry VDD
F11	VDD3.3	Pwr	3.3V digital I/O circuitry VDD.
F12	VDD3.3	Pwr	3.3V digital I/O circuitry VDD
F13	VDD3.3	Pwr	3.3V digital I/O circuitry VDD
G12	VDD3.3	Pwr	3.3V digital I/O circuitry VDD
G13	VDD3.3	Pwr	3.3V digital I/O circuitry VDD
L12	VDD3.3	Pwr	3.3V digital I/O circuitry VDD.
L13	VDD3.3	Pwr	3.3V digital I/O circuitry VDD
M10	VDD3.3	Pwr	3.3V digital I/O circuitry VDD.
M11	VDD3.3	Pwr	3.3V digital I/O circuitry VDD.
M12	VDD3.3	Pwr	3.3V digital I/O circuitry VDD.
M13	VDD3.3	Pwr	3.3V digital I/O circuitry VDD.
N10	VDD3.3	Pwr	3.3V digital I/O circuitry VDD.
N11	VDD3.3	Pwr	3.3V digital I/O circuitry VDD.
N12	VDD3.3	Pwr	3.3V digital I/O circuitry VDD.
N13	VDD3.3	Pwr	3.3V digital I/O circuitry VDD.
E5	VDDA1.8	Pwr	1.8V analog VDD.
E6	VDDA1.8	Pwr	1.8V analog VDD.
F5	VDDA1.8	Pwr	1.8V analog VDD.
F6	VDDA1.8	Pwr	1.8V analog VDD.
G5	VDDA1.8	Pwr	1.8V analog VDD.
G6	VDDA1.8	Pwr	1.8V analog VDD.
H5	VDDA1.8	Pwr	1.8V analog VDD.
H6	VDDA1.8	Pwr	1.8V analog VDD.
J5	VDDA1.8	Pwr	1.8V analog VDD.
J6	VDDA1.8	Pwr	1.8V analog VDD.
K5	VDDA3.3	Pwr	3.3V analog VDD
K6	VDDA3.3	Pwr	3.3V analog VDD

L5	VDDA3.3	Pwr	3.3V analog VDD
L6	VDDA3.3	Pwr	3.3V analog VDD
M5	VDDA3.3	Pwr	3.3V analog VDD
M6	VDDA3.3	Pwr	3.3V analog VDD
N5	VDDA3.3	Pwr	3.3V analog VDD
N6	VDDA3.3	Pwr	3.3V analog VDD
F2	WANFXSD	I	WAN Fiber Signal Detect
G4	WANRXM	I	WAN PHY Receive signal - (differential).
G3	WANRXP	I	WAN PHY Receive signal + (differential).
G2	WANTXM	O	WAN PHY Transmit signal - (differential).
G1	WANTXP	O	WAN PHY Transmit signal + (differential).
E15	WLED0 / B0SIZE0	O/I	WAN LED programmable indicator 0. / Bank 0 Size bit 0
E14	WLED1 / B0SIZE1	O/I	WAN LED programmable indicator 1. / Bank 0 Size bit 1
U17	WRSTO	O	Watchdog timer reset output
E1	XCLK1	I	External Clock In
E2	XCLK2	I	External Clock In (negative polarity)

Figure 10 KS8695P Pin Mapping (Top View)



3.0 Address Map and Register Description

3.1 Memory Map

Upon power up, the KS8695P memory map is configured as shown below.

Table 15 Default Memory Map

Address Range	Region Size	Description
0x03FF0000-0x03FFFFFF	64 kbytes	KS8695P System Configuration Register Space
0x02000000-0x03FEFFFF	32Mbytes	Not Configured
0x00000000-0x01FFFFFF	32 Mbytes	Flash Bank 0

The default base address for the the KS8695P system configuration registers is 0x03ff0000. After power up, the user is free to remap the memory for his/her specific application. Here is an example of the memory space remapped for operation:

Table 16 Memory Map Example

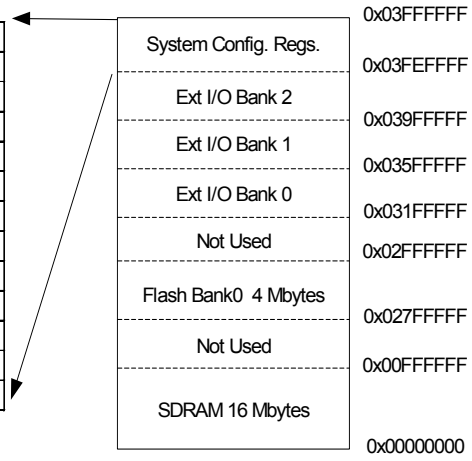
Address Range	Region Size	Description
0x03FF0000-0x03FFFFFF	64 kbyte	KS8695P System Configuration Register Space
0x03E00000-0x03FEFFFF	2 Mbyte	Disabled, Not Used
0x03200000-0x036FFFFF	5 Mbyte	Spare (External I/O)
0x02C00000-0x031FFFFF	6 Mbyte	Reserved FLASH Space, Not Used
0x02800000-0x02BFFFFF	4 Mbyte	FLASH
0x02000000-0x027FFFFF	8 Mbyte	Disabled, Not Used
0x00000000-0x01FFFFFF	32 Mbyte	SDRAM

3.2 Register Description

The KS8695P System Configuration Registers (SCR's) are located in a block of 64 kbytes in the host memory address space. After power up and initialization, the user can re-map the SCR's to a desired offset. The SCR's are 32 bits wide. They are 32-bit word aligned and must be accessed using word instructions. A description of the KS8695P System Configuration Registers follows. The AHB-PCI Bridge configuration registers are also included in the SCR's. A subset of the AHB-PCI Bridge configuration registers is also accessible to an external PCI host when the KS8695P is configured in PCI guest mode. Refer to the Detailed Register description document for more information, including bit definitions. If you don't have the document contact your Micrel Sales Representative.

Figure 11 System Registers

Address Range	Description
0x0000 – 0x0004	System Registers
0x2000 – 0x2224	PCI-AHB Bridge Configuration Registers
0x4000 – 0x4040	Memory Controller Interface Registers
0x6000 – 0x60FC	WAN DMA Registers
0x8000 – 0x80FC	LAN DMA Registers
0xA000 – 0xA0FC	Reserved
0xE000 – 0xE020	UART Registers
0xE200 – 0xE234	Interrupt Controller Registers
0xE400 – 0xE410	Timer Registers
0xE600 – 0xE608	General Purpose I/O Registers
0xE800 – 0xE850	Switch Engine Configuration Registers
0xEA00- 0xEA18	Miscellaneous Registers



4.0 Electrical Characteristics

4.1 Absolute Maximum Ratings

Stresses greater than those listed in this table may cause permanent damage to the device. Operation of the device at these or any other conditions above those specified in the operating sections of this specification is not implied. Maximum conditions for extended periods may affect reliability. Unused inputs must always be tied to an appropriate logic voltage level.

Table 17 Absolute Maximum Ratings

Description	Pins	Value
Storage Temperature	N/A	- 55 °C to 150 °C
Supply Voltages	VDDA1.8, VDD1.8	-0.5 V to 2.4 V
	VDDA3.3, VDD3.3	-0.5 V to 4.0 V
Input Voltage	All Inputs	-0.5 V to 4.0 V
Output Voltage	All Outputs	-0.5 V to 4.0 V

4.2 Recommended Operating Conditions

Table 18 Recommended Operating Conditions

Parameter	Sym	Min	Typ	Max	Unit
Supply Voltages	VDDA1.8, VDD1.8	1.7	1.8	1.9	V
	VDDA3.3, VDD3.3	3.0	3.3	3.6	V
Ambient Operating Temperature	T_A	0		70	°C
Max. Junction Temperature	T_J			150	°C

4.3 DC Electrical Characteristics

Table 19 DC Electrical Characteristics

Supply Current (including TX output driver current)						
100BaseTX operation – All ports 100 % Utilization, SDOCLK = 125 MHz		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
100BaseTX (analog TX)	I_{tx}	VDDA3.3 = 3.3 V		0.243		A
100BaseTX (analog Rx)	I_{rx}	VDDA1.8 = 1.8 V		0.124		A
100BaseT (digital IO)	I_{ddio}	VDD3.3 = 3.3 V		0.033		A
100BaseT (digital core)	I_{ddc}	VDD1.8 = 1.8 V		0.235		A
10BaseTX operation – All ports 100 % Utilization, SDOCLK = 125 MHz		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
10BaseT (analog TX)	I_{tx}	VDDA3.3 = 3.3 V		0.328		A
10BaseT (analog Rx)	I_{rx}	VDDA1.8 = 1.8 V		0.072		A
10BaseT (digital IO)	I_{ddio}	VDD3.3 = 3.3 V		0.025		A
10BaseT (digital core)	I_{ddc}	VDD1.8 = 1.8 V		0.234		A
Auto Negotiation Mode, SDOCLK = 125 MHz		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
10BaseT (transmitter)	I_{tx}	VDDA3.3 = 3.3 V		0.046		A
10BaseT (analog Rx)	I_{rx}	VDDA1.8 = 1.8 V		0.07		A

10BaseT (digital IO)	I_{ddio}	VDD3.3 = 3.3 V		0.021		A
10BaseT (digital core)	I_{ddc}	VDD1.8 = 1.8 V		0.233		A
TTL Inputs (PCI, LED, Memory Interface, UART)		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Input High Voltage	V_{ih}		½ VDD3.3 + 0.4 V			V
Input Low Voltage	V_{il}				½ VDD3.3 –0.4 V	V
Input Current (excluding pull up / pull down)	I_{in}	V_{in} = GND ~ VDD3.3	-10		10	µA
TTL Outputs (PCI, LED, Memory Interface, UART)		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Output High Voltage	V_{oh}	I_{oh} = - 8 mA	VDD3.3 - 0.4			V
Output Low Voltage	V_{ol}	I_{ol} = 8 mA			0.4 V	V
Output Tri-state Leakage	$\|I_{oz}\|$				10	µA
100BaseTX Transmit **Measured differentially after 1:1 transformer**		**Test Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Peak Differential Output Voltage	V_o	100 Ω termination on the differential output.	0.95		1.05	V
Output Voltage Imbalance	V_{imb}	100 Ω termination on the differential output			2	%
Rise/Fall time	T_r/T_f		3		5	ns
Rise/Fall time Imbalance			0		0.5	ns
Duty Cycle Distortion					± 0.5	ns
Overshoot					5	%
Reference Voltage of ISET	V_{set}			0.5		V

Output Jitters		Peak to peak		0.7	1.4	ns
10BaseT Receive						
Squelch Threshold	V_{sq}	5 MHz square wave		400		mV
10BaseT Transmit (measured differentially after 1:1 transformer) VDDAT= 2.5V						
Peak Differential Output Voltage	V_p	100 Ω termination on the differential output.		2.3		V
Jitters Added		100 Ω termination on the differential output.			± 3.5	ns
Rise/Fall time				28	30	ns

4.4 Functional Timing Specifications

For PCI Timing please refer to PCI specification version 2.1

Figure 12 Reset Timing

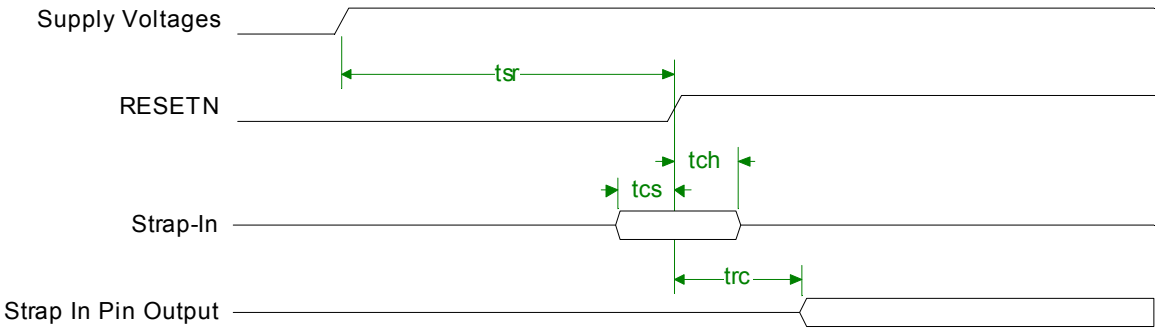


Table 20 Reset Timing Parameters

Parameter	Description	Min	Max	Units
t_{sr}	Stable supply voltages to reset high	10		ms
t_{cs}	Configuration setup time	50		ns
t_{ch}	Configuration hold time	50		ns
t_{rc}	Reset to Strap-In pin output	50		us

Figure 13 Static Memory Read Cycle

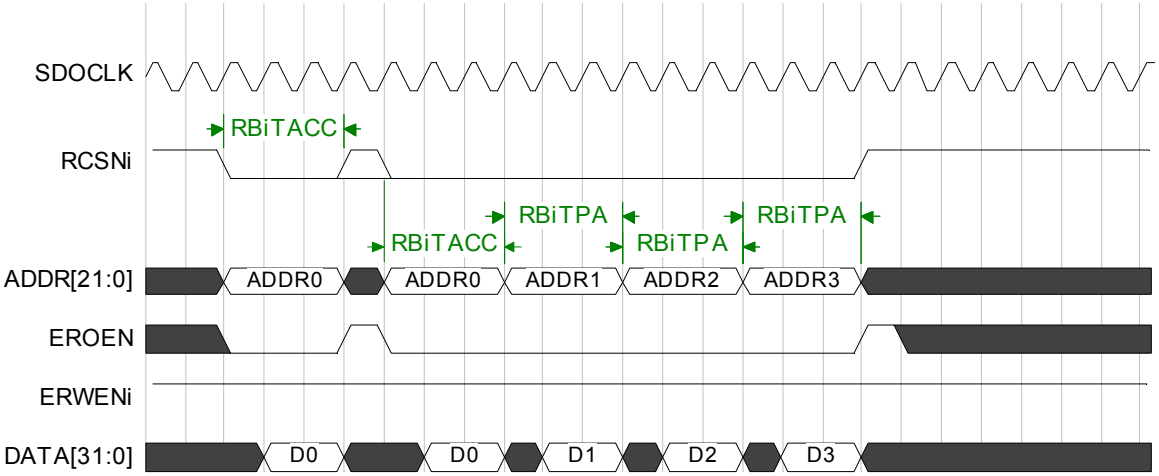


Figure 14 Static Memory Write Cycle

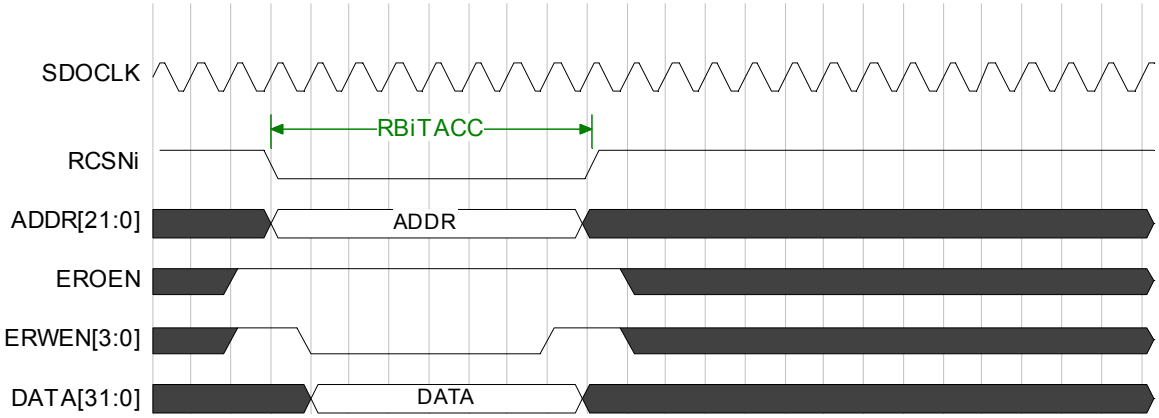


Table 21 Static Memory Timing Parameters

Parameter	Description	Registers
RBiTACC	Programmable Bank i access time	0x4010
RBiTPA	Programmable Bank i page address access time	0x4014

Figure 15 External I/O Read and Write Cycles

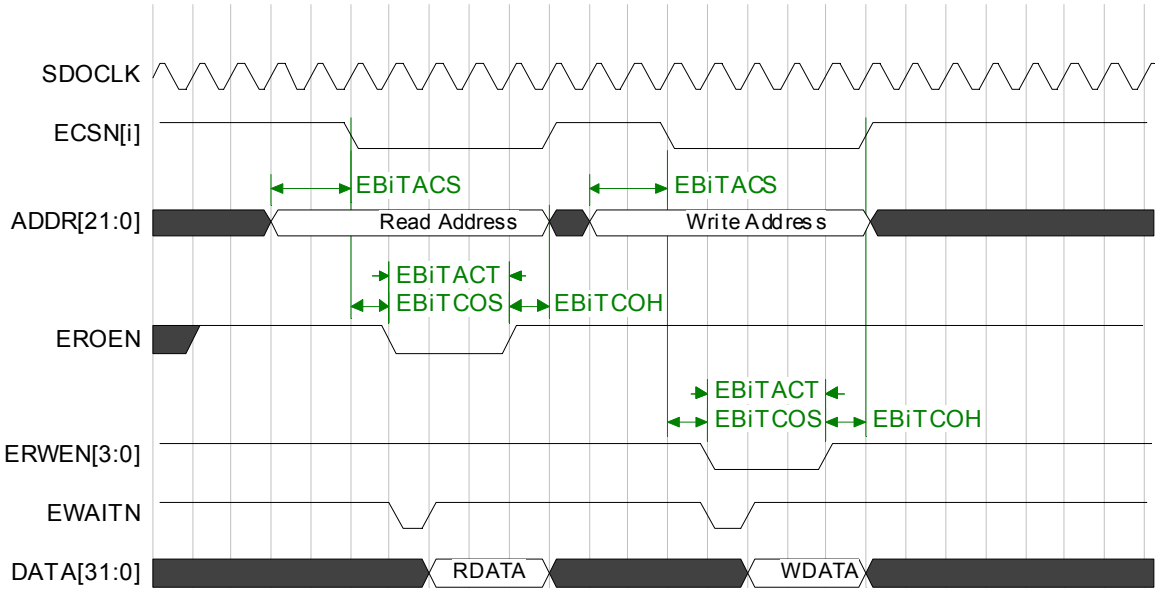


Table 22 External I/O Timing Parameters

Parameter	Description	Registers
EBiTACS	Programmable Bank i address setup time before chip select	0x4000 0x4004 0x4008
EBiTACT	Programmable Bank i Write Enable/Output Enable Access Time	
EBiTCOS	Programmable Bank i Chip Select Setup Time before OEN	
EBiTCOH	Programmable Bank i Chip Select Hold Time	

Figure 16 SDRAM Read Timing

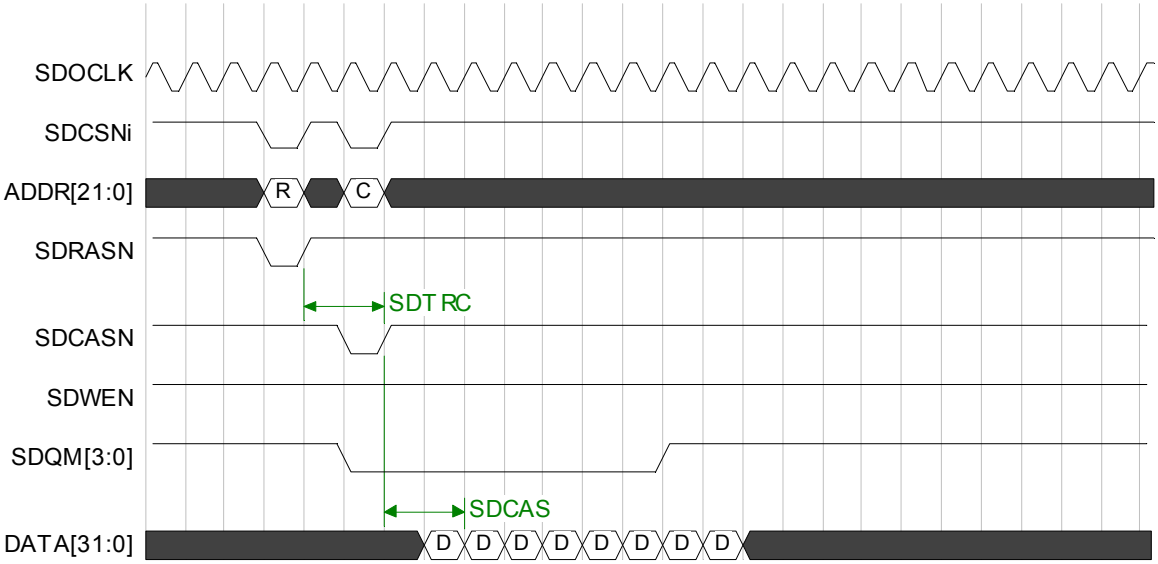


Figure 17 SDRAM Write Timing

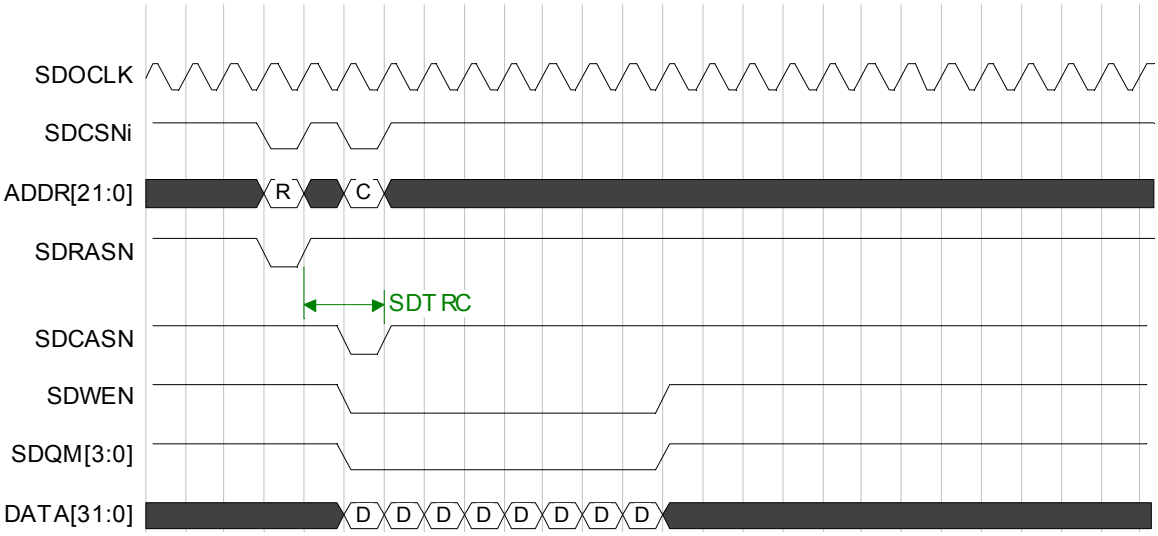
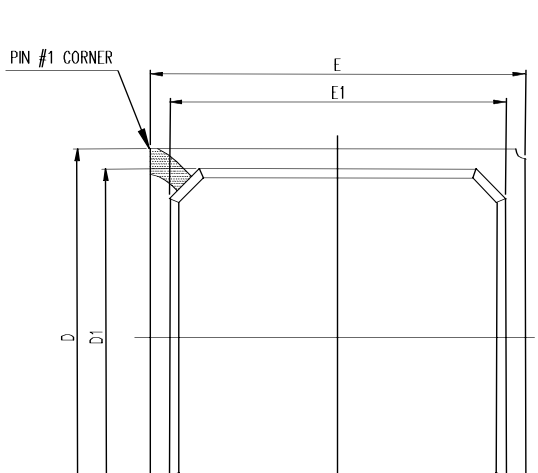


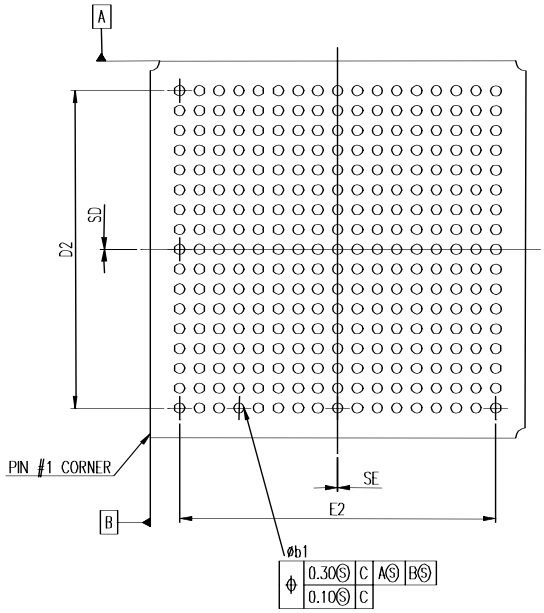
Table 23 SDRAM Timing Parameters

Parameter	Description	Register
SDTRC	Programmable SDRAM RAS to CAS Latency	0x4038
SDCAS	Programmable SDRAM CAS Latency	

5.0 Mechanical Specifications

5.1 Package Outline and Dimensions





SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM	MAX.	MIN.	NOM	MAX.
A		2.11	2.26		0.083	0.089
A1	0.33	0.38	0.43	0.013	0.015	0.017
A2	1.63		1.83	0.064		0.072
b1	0.51	0.53	0.55	0.020	0.021	0.022
b	0.48	0.50	0.52	0.019	0.020	0.020
D1	16.90	17.00	17.10	0.665	0.669	0.673
E1	16.90	17.00	17.10	0.665	0.669	0.673
e	1.00 BSC.			0.039 BSC.		
JEDEC	MO-151					

A (FOR PUNCH CUTTING)

SYMBOL	MIN.	NOM	MAX.
D	18.95	19.00	19.05
E	18.95	19.00	19.05

B (FOR ROUNTING CUTTING)

SYMBOL	MIN.	NOM	MAX.
D	18.85	19.00	19.15
E	18.85	19.00	19.15

N	SE(mm)	SD(mm)	E2(mm)	D2(mm)	JEDEC(Ref.)
289	0.00 BSC.	0.00 BSC.	16.00 BSC.	16.00 BSC.	

UNLESS OTHERWISE SPECIFIED	DECIMAL .X ± .XX ±.10 .XXX ±.05	ANGULAR ±3°	THIRD ANGLE PROJECTION :	
DRAWN	Vivian Lin 2003.04.11		UNIT: mm	SCALE: 5:1
CHECKED	Vivian Lin 2003.04.11		JEDEC NO.: MO-151(Ref.)	
APPROVED	Dave Yang		PACKAGE CODE : PBAQF	
APPROVED	Paul Sun		DWG. NO.: PD-PBAQ289F-SBMA	REV.:A

TITLE: Package outline drawing dimension for PBGA19*19mm family, Ball Pitch 1.0mm(mold height 1.17mm , SS thick. 0.56mm)

DOC. NO.: PD-PBAQ289F-SBMA | REV.: A | SHEET : 1 | A3

5.2 Thermal Information

Table 24 Thermal Information

Parameter	Description	Airflow			Unit
		0 m/s	1 m/s	2 m/s	
Θ_{JA}	Thermal Resistance Junction to Ambient No Heatspreader (2W input)	29.86	21.86	21.54	°C/W
Θ_{JC}	Thermal Resistance Junction to Case No Heatspreader (2W input)	8.34	N/A	N/A	°C/W

5.3 Part Ordering Information

Part Ordering Number: **KS8695P**
Evaluation Kit Ordering Number: **KS8695P-EVAL**

5.4 Contact Information

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Eastern Area Sales Office 93 Branch St. Medford, NJ 08055 USA Tel: (609) 654-0078 Fax: (609) 654-0989	
CENTRAL USA	**ASIA**
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