# Application Notes for E2O Communications Small Form-Factor Fixed (SFF) Transceivers

## Introduction

This set of Application Notes is intended as a guide to assist the system designer with integrating an E2O EM Series SFF fiber optic transceiver into their network system. Refer to Table 1 for a listing of E2O transceiver Part Nos. covered by this Application Note. Please refer to the data sheets for product description, features, performance specifications, and ordering options. Included in this document are schematics showing recommended system interface circuits for both AC and AC/DC coupled transceiver options to aid in PC (host) board design.

**Table 1. Transceiver Applicability Listing**

| Model Number | Optical Connector | Application | Data Rate | Voltage Supply (V) | Coupling | Signal Detect |
|---|---|---|---|---|---|---|
| EM125-L3TA | LC | Gigabit Ethernet | 1.25 | 3.3 | AC | TTL |
| EM106-L3TA | LC | Fibre Channel | 1.06 | 3.3 | AC | TTL |
| EM212-L3TA | LC | Fibre Channel | 2.125/1.06 | 3.3 | AC | TTL |
| EM250-L3TA | LC | InfiniBand | 2.50/1.25 | 3.3 | AC | TTL |
| EM125-L3TF | LC | Gigabit Ethernet | 1.25 | 3.3 | AC/DC | TTL |
| EM106-L3TF | LC | Fibre Channel | 1.06 | 3.3 | AC/DC | TTL |
| EM212-L3TF | LC | Fibre Channel | 2.125/1.06 | 3.3 | AC/DC | TTL |
| EM250-L3TF | LC | InfiniBand | 2.50/1.25 | 3.3 | AC/DC | TTL |
| EM125-M3TA | MTRJ | Gigabit Ethernet | 1.25 | 3.3 | AC | TTL |
| EM106-M3TA | MTRJ | Fibre Channel | 1.06 | 3.3 | AC | TTL |
| EM125-M3TF | MTRJ | Gigabit Ethernet | 1.25 | 3.3 | AC/DC | TTL |
| EM106-M3TF | MTRJ | Fibre Channel | 1.06 | 3.3 | AC/DC | TTL |

## Optical and Electrical Interconnections

The transceiver's transmitter section is designed to receive differential Positive Emitter Coupled Logic (PECL) signals at data rates up to 2.50 Gbps (depending on the particular model selected). Each differential input line is AC coupled. The transceiver's receiver section is designed to output differential Positive Emitter Coupled Logic (PECL) signals at data rates up to 2.50 Gbps (depending on the particular model selected). Each differential output line is AC or DC coupled depending on the user's requirements.

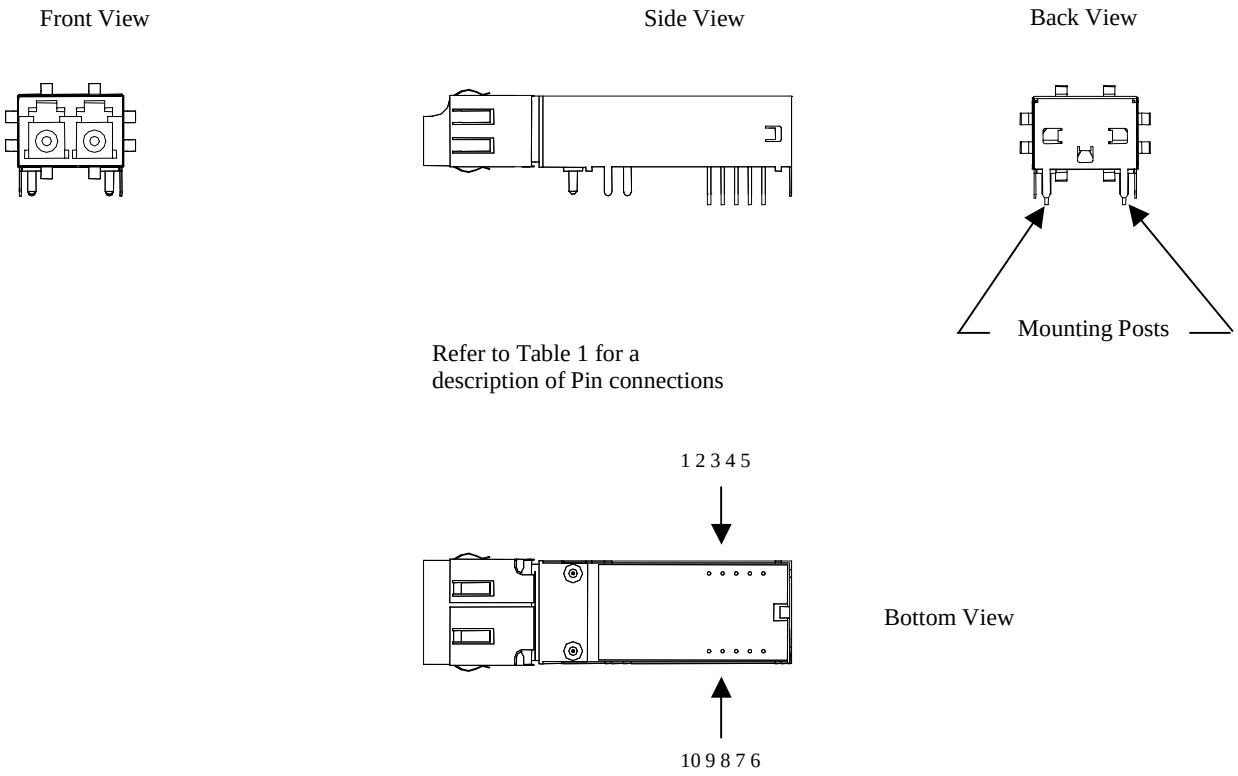
The transceivers use the industry standard LC or MTRJ optical fiber connector and the 2x5 electrical connector. Refer to Table 2 for a listing of Pinout descriptions for the 2x5 electrical connector. The Pin numbers correspond to Pin locations indicated in the module front view shown in Figure 1.

All 10 pins should be soldered or firmly connected to plate thru holes on the system PC board. The two ground pins 1 and 7 (Receiver and Transmitter Signal Grounds) should be connected to a single PC board ground plane that is as large and rigid as possible. The system user provides PECL data to the differential inputs of the transmitter on Pins 9 (Data Non-inverted) and 10 (Data Inverted). The receiver provides differential output data back to the system on Pins 5 (Data Non-inverted) and 4 (Data Inverted).

**Table 1. Pinout Descriptions**

| Pin | Symbol | Functional Description |
|---|---|---|
| Mounting Posts | | The mounting posts are provided for transceiver mechanical attachment to the circuit board. They should not be connected to the circuit ground but can be connected to the chassis ground. |
| 1 | $V_{EER}$ | Receiver Signal Ground |
| 2 | $V_{CCR}$ | +3.3 Volt Receiver Power Supply |
| 3 | SD | Signal Detect is a TTL output. A high level indicates a valid optical signal. |
| 4 | RD- | Receiver Data Inverted Differential Output |
| 5 | RD+ | Receiver Data Non-inverted Differential Output |
| 6 | $V_{CCT}$ | +3.3V Transmitter Power Supply |
| 7 | $V_{EET}$ | Transmitter Signal Ground |
| 8 | TXdis | Transmitter Disable |
| 9 | TD+ | Transmitter Data Non-inverted Differential Input |
| 10 | TD- | Transmitter Data Inverted Differential Input |

**Figure 1. Pin and Mounting Post Locations**




Note: This diagram is for illustration of pin and mounting post locations only (actual module shown is with LC optical connector).

System to Transceiver Interface Design Guidelines

The transceivers use PECL for high speed interfacing. For this reason it is necessary that the transceiver's transmitter and receiver PECL interfaces to the system are compatible. In order to prevent unwanted reflections between the system and the transceiver module, it is necessary to have both a 50Ω impedance matched transmission line as well as a 50Ω termination load.

AC and AC/DC coupled options are available for the EM Series SFF-LC and MTRJ Transceivers. Included in these Application Notes are interface schematics intended to serve as suggested PC board designs when using the particular coupling option. For the AC coupled option, both the transmitter and receiver are AC coupled. Refer to Figure 2 for the recommended system to transceiver interface for the AC coupled option. For the AC/DC coupled option the transmitter side is AC coupled while the receiver side is DC coupled. Refer to Figure 3 for the recommended system to transceiver interface for the AC/DC coupled option. The AC/DC option maybe used with DC/DC as well as AC/DC interfaces.

Both the AC and AC/DC coupled transceiver options internally provide the correct bias level for PECL compatibility in the transmitter section. Also, on both options the transceiver internally includes a 100Ω differential termination for the two differential input lines (TD- and TD+). For this reason, additional 50Ω terminations should not be externally connected to the transmitter input lines. For both coupling options, the system interface must provide for the proper PECL biasing level and 50Ω termination for the receiver output lines, as described below.

For the AC coupled module, the receiver outputs (RD+ and RD-) are PECL compatible with an AC swing of 600mV – 800mV. The bias and impedance matching network shown is only required if the receiving device does not have internal bias and 50 ohm termination. Refer to the receiving device (i.e. SERDES chip) for the proper bias voltage level. R1 with R2, and similarly R3 with R4, provide a voltage divider to set the proper bias for the receiving device. These resistor values must be selected such that both the proper bias is obtained, and R1//R2 and R3//R4 are each equal to 50 ohms. It is important to note that even if a bias is not required at the interface, a 50 ohm termination is still required at either the interface or at the receiving device (if on chip termination is not available).

For the AC/DC coupled module, the receiver outputs (RD+ and RD-) are PECL compatible with an AC swing of 600mV – 800mV and standard PECL bias level (+2V for $V_{CCR}$ = +3.3V). The bias and impedance matching network with blocking capacitors shown is only required if the receiving device is not compatible with the standard PECL provided by the receiver outputs. If not compatible, refer to the receiving device (i.e. SERDES chip) for the proper bias voltage level. R1 with R2, and similarly R3 with R4, provide a voltage divider to set the proper bias for the receiving device. These resistor values must be selected such that both the proper bias is obtained, and R1//R2 and R3//R4 are each equal to 50 ohms. It is important to note that even if a bias is not required at the interface, a 50 ohm termination is required at either the interface or at the receiving device (if on chip termination is not available).

Another difference between system interfaces for the two coupling options is the inclusion of the 180Ω resistors for the AC/DC coupled option to allow for current sinking from the open emitter outputs of RD- and RD+.

The transceiver uses a balanced differential pairs scheme for both the transmitter and receiver differential pairs. The differential amplifier operates on the principle of summation of inverted data and non-inverted data signals, which are 180 degrees out of phase, and common mode rejection of line noise and voltage reflections equal in phase and amplitude. For this reason, PC board differential pair transmission lines must be designed and laid out with equal length. The PC board DC power traces should be as wide as possible for low impedance.

The transmitter section features a disable function on Pin 8 which requires a +3.3V TTL input DC coupled from the system to be operational. The transmitter is disabled in the presence of a TTL high level and enabled in the presence of a TTL low level. If this feature is not needed, Pin 8 should be connected to system ground.

The receiver's signal detection provides a TTL output on Pin 3. Due to infrequent state changes, the signal detect output is meant to only be externally DC coupled to an output monitor line and should not be grounded. Signal detect should be left open if not terminated.

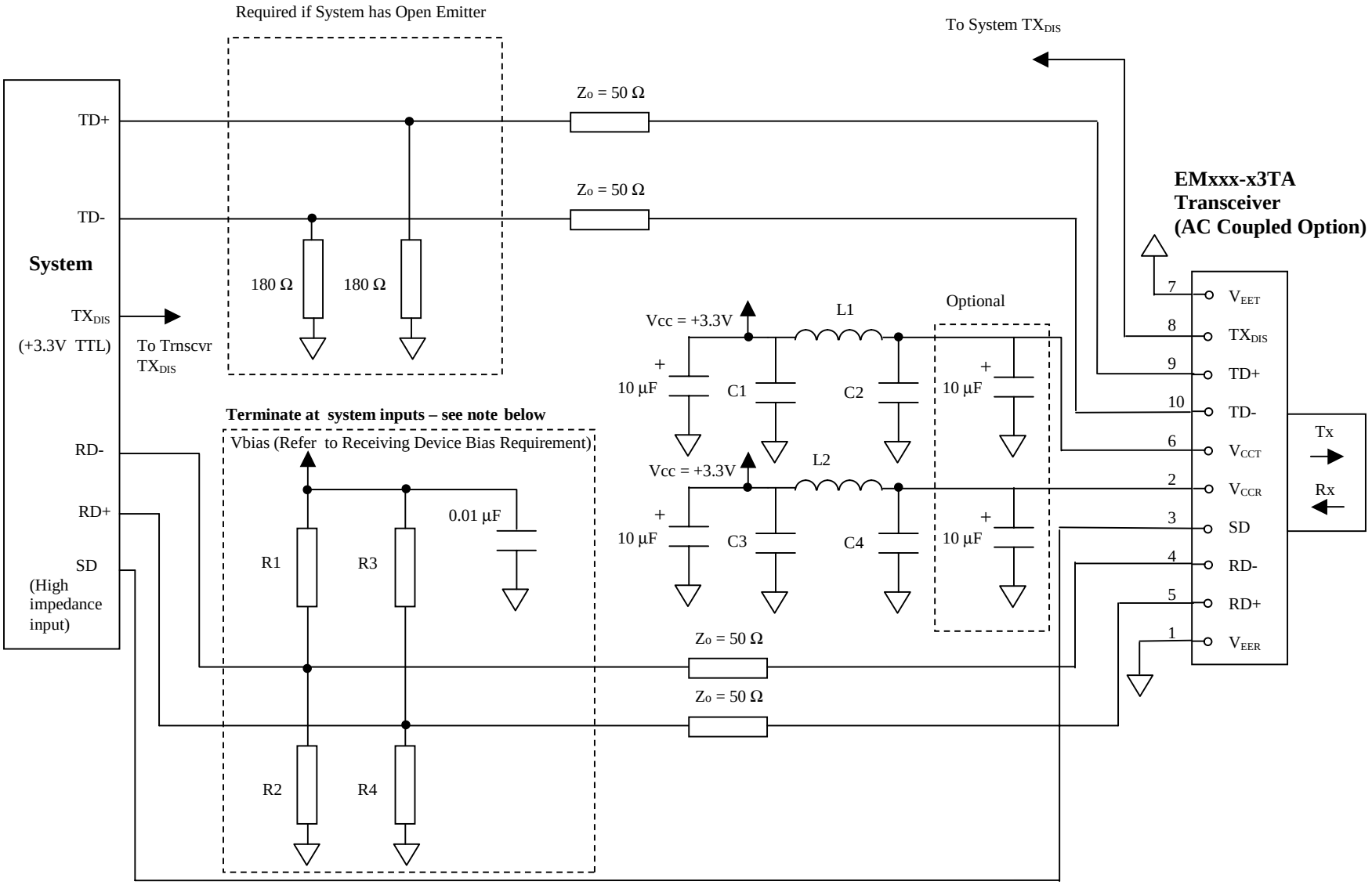
Power Supply Noise Filtering

The power supply for the transceiver must be adequately filtered to prevent noise on the positive supply from degrading module performance. The filter must be effective across a wide frequency range, greater than twice the data rate. Similarly, noise originating from the module must be filtered to prevent it from degrading system performance.

The positive power supply for the receiver on Pin 2 and the positive power supply for the transmitter on Pin 6 should not be tied together to prevent crosstalk between the receiver and the transmitter. Pins 2 and 6 should each have their own LC π-filter acting as an RF choke placed as close as possible to the pin connection.

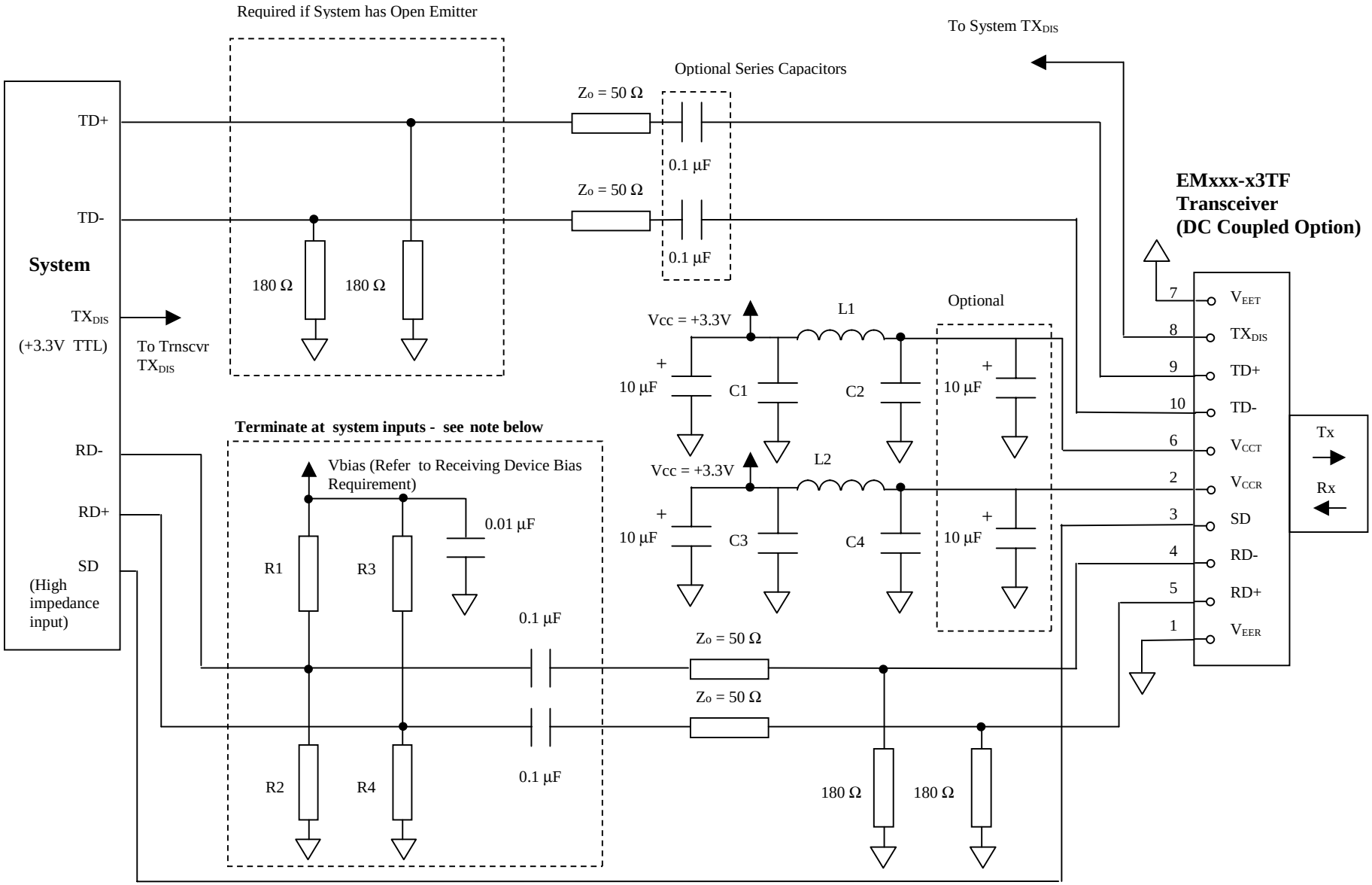
E2O recommends a noise filtering circuit as shown in both Figures 2 and 3. The capacitors should have minimal high frequency impedance and their values adequate to ground RF crosstalk noise. To reduce high frequency noise, a value of 0.01 to 0.1 μF should be adequate for C1 - C4. A large capacitor such as the 10 μF shown is recommended for filtering out low frequency noise. The inductors should adequately block high frequencies but with a maximum current rating greater than 300mA. A value of 0.5 to 1 μH should be adequate for L1 and L2.

**Figure 2. Recommended System to Transceiver Interface for AC Coupled Option**




**Note: Complete bias and impedance matching network above only required if receiving device, i.e., SERDES chip, does not have internal bias. However, if receiving device does not have 50 ohm termination, it must be provided here. Contact E2O for further assistance.**

## Figure 3. Recommended System to Transceiver Interface for AC/DC Coupled Option




**Note: Complete biasing and impedance matching network and blocking capacitors above only required if receiving device not compatible with standard PECL provided by E2O transceiver. However, if receiving device does not have 50 ohm termination, it must be provided here. Contact E2O for further assistance.**