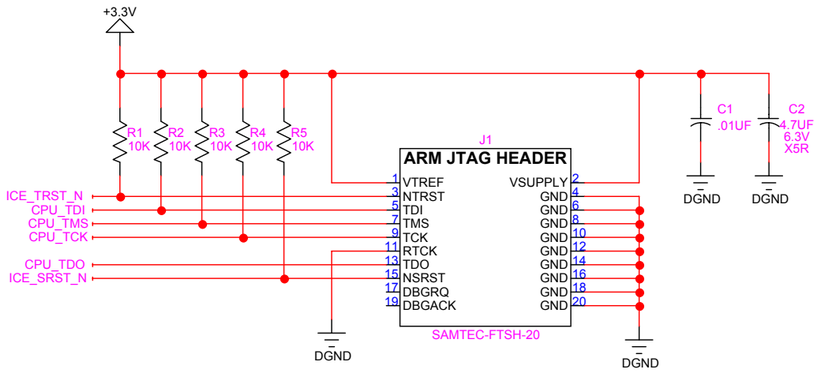
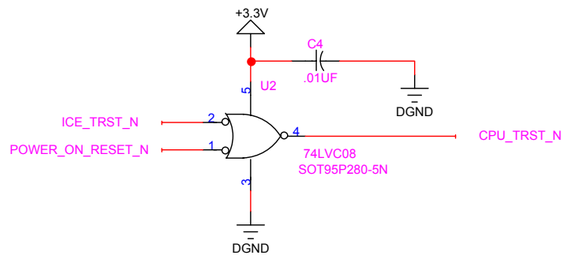
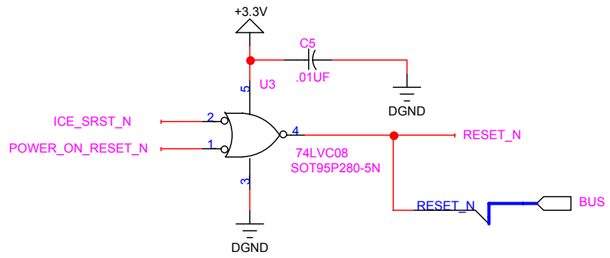
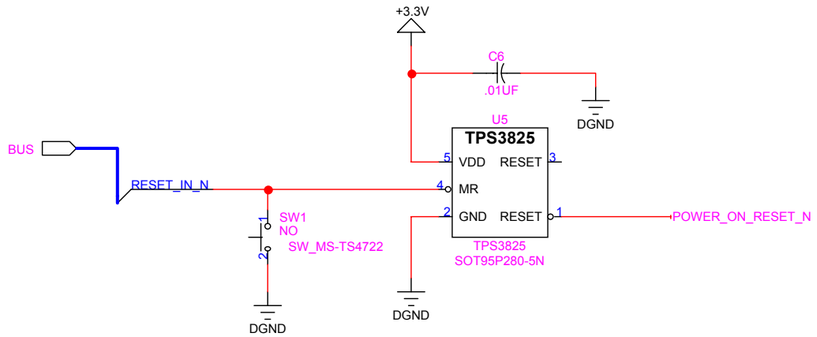
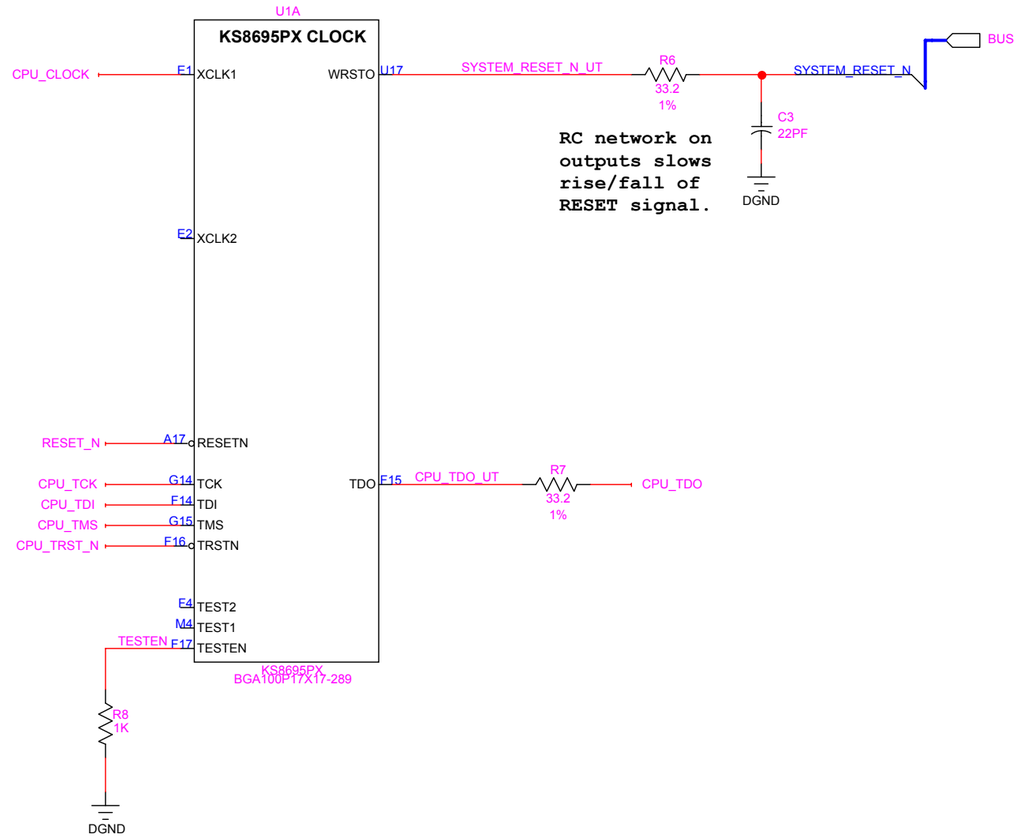
# CPU CLOCK & JTAG

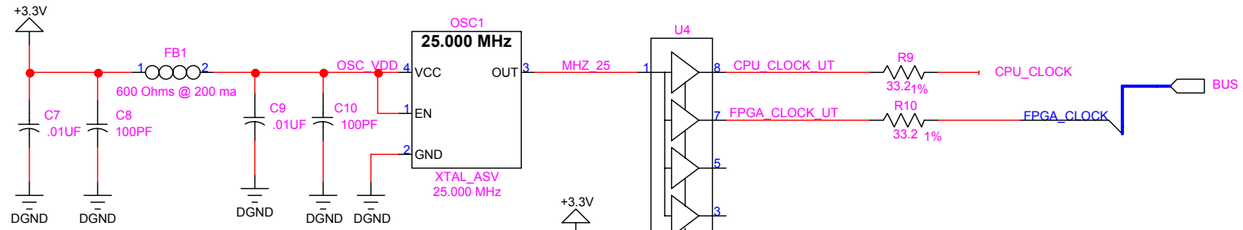
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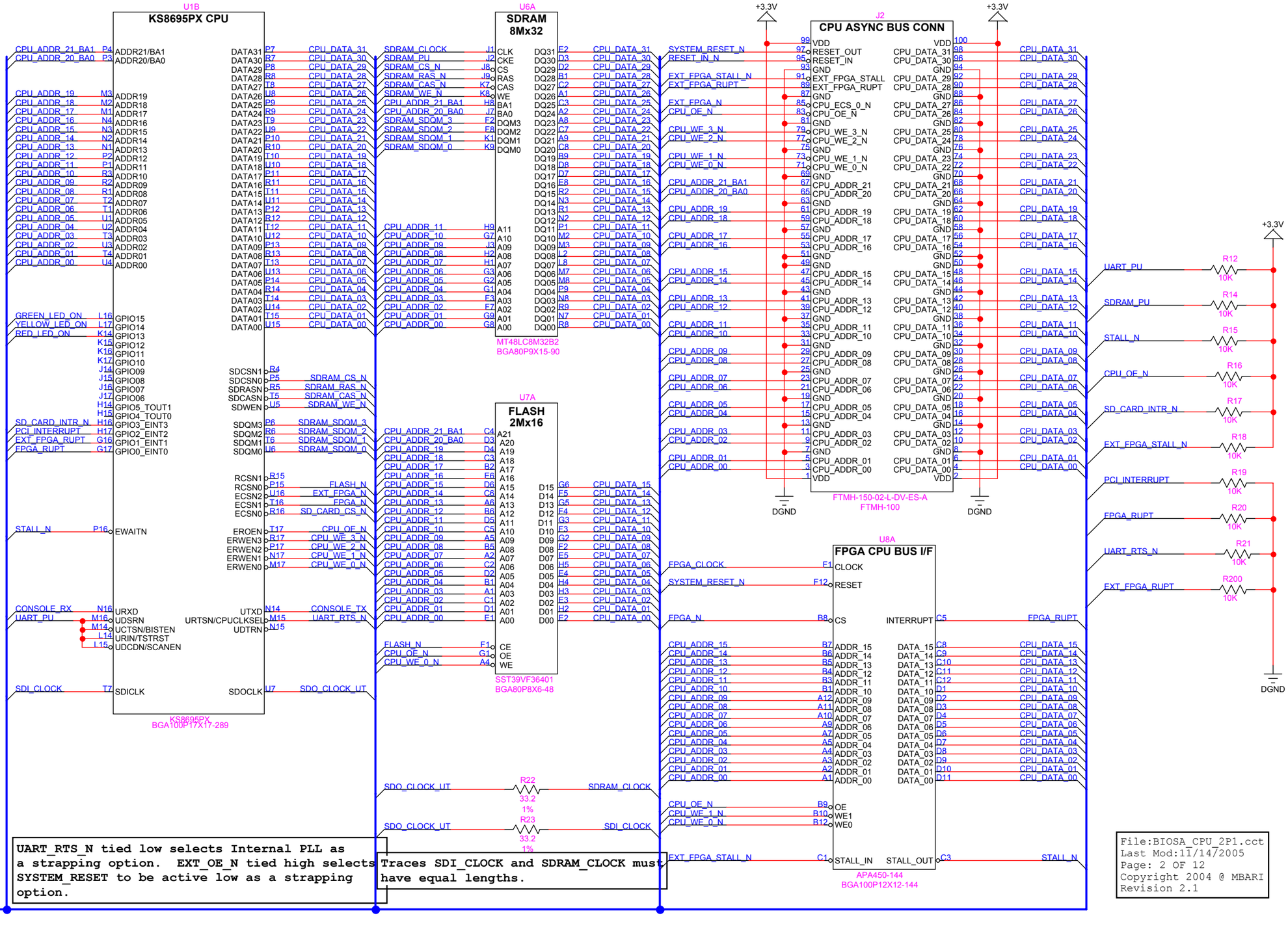
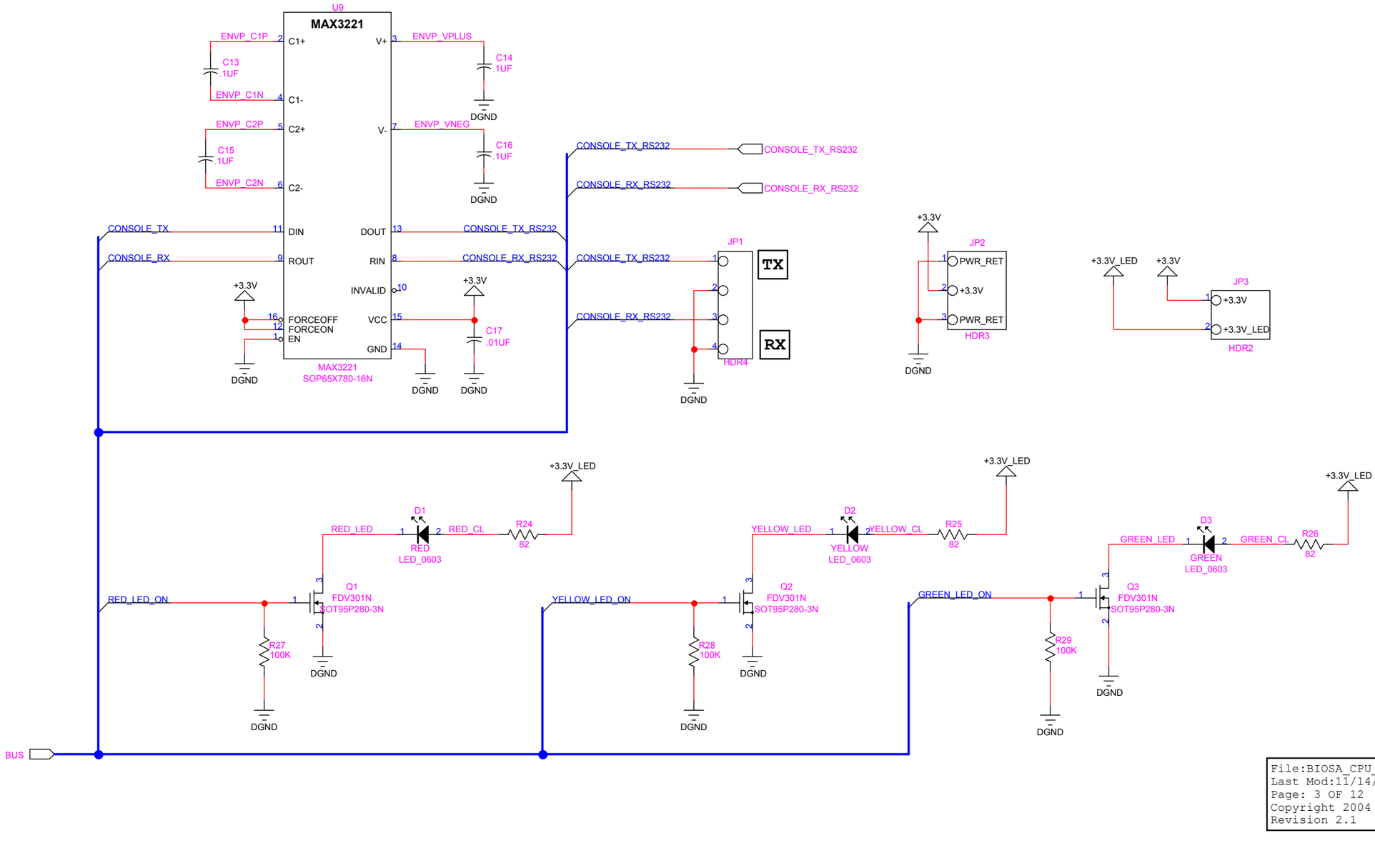
# CPU, MEMORY, CONSOLE & ASYNC BUS



# LINUX CONSOLE PORT AND DEBUG LEDS

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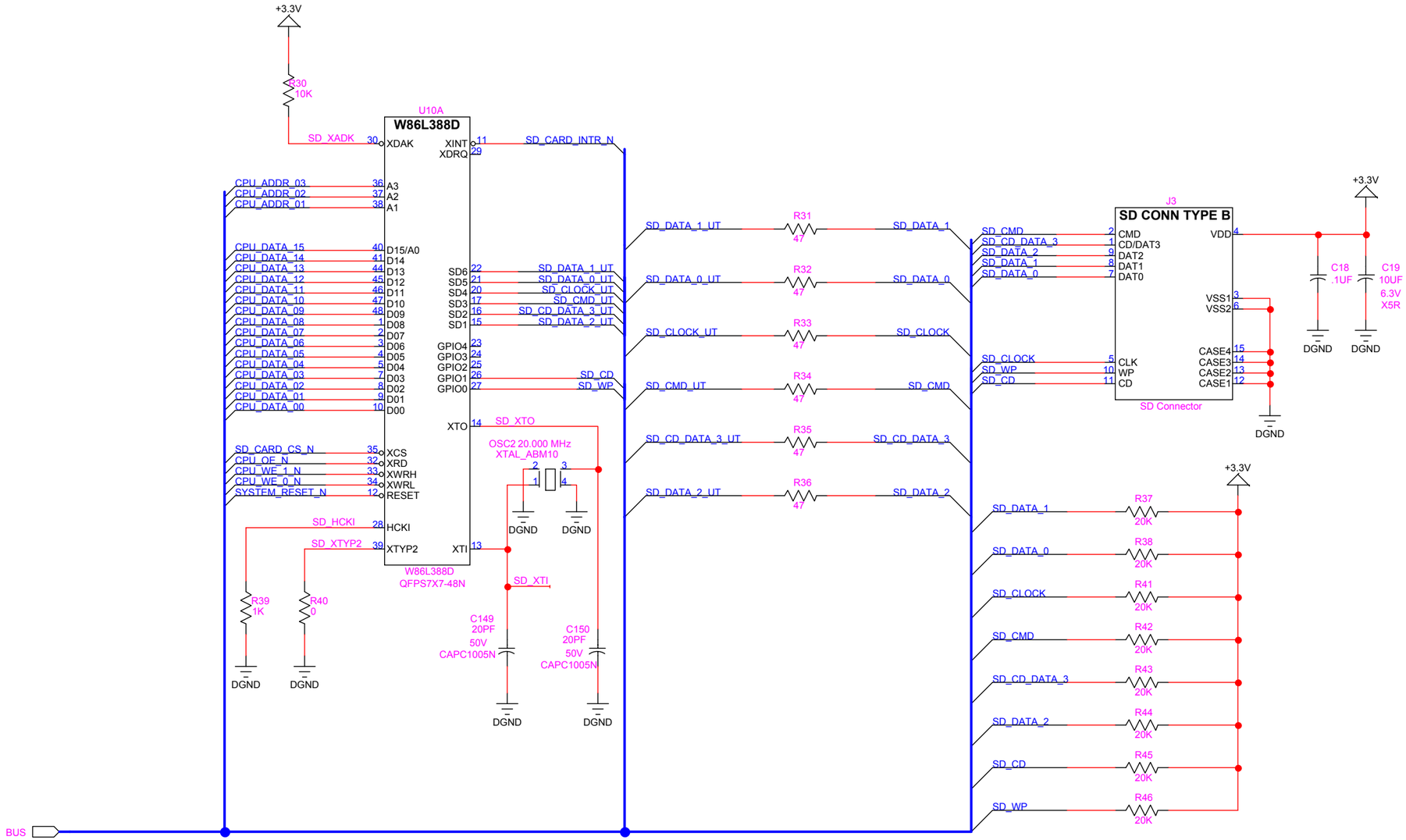
# SD/MMC MEMORY CARD INTERFACE





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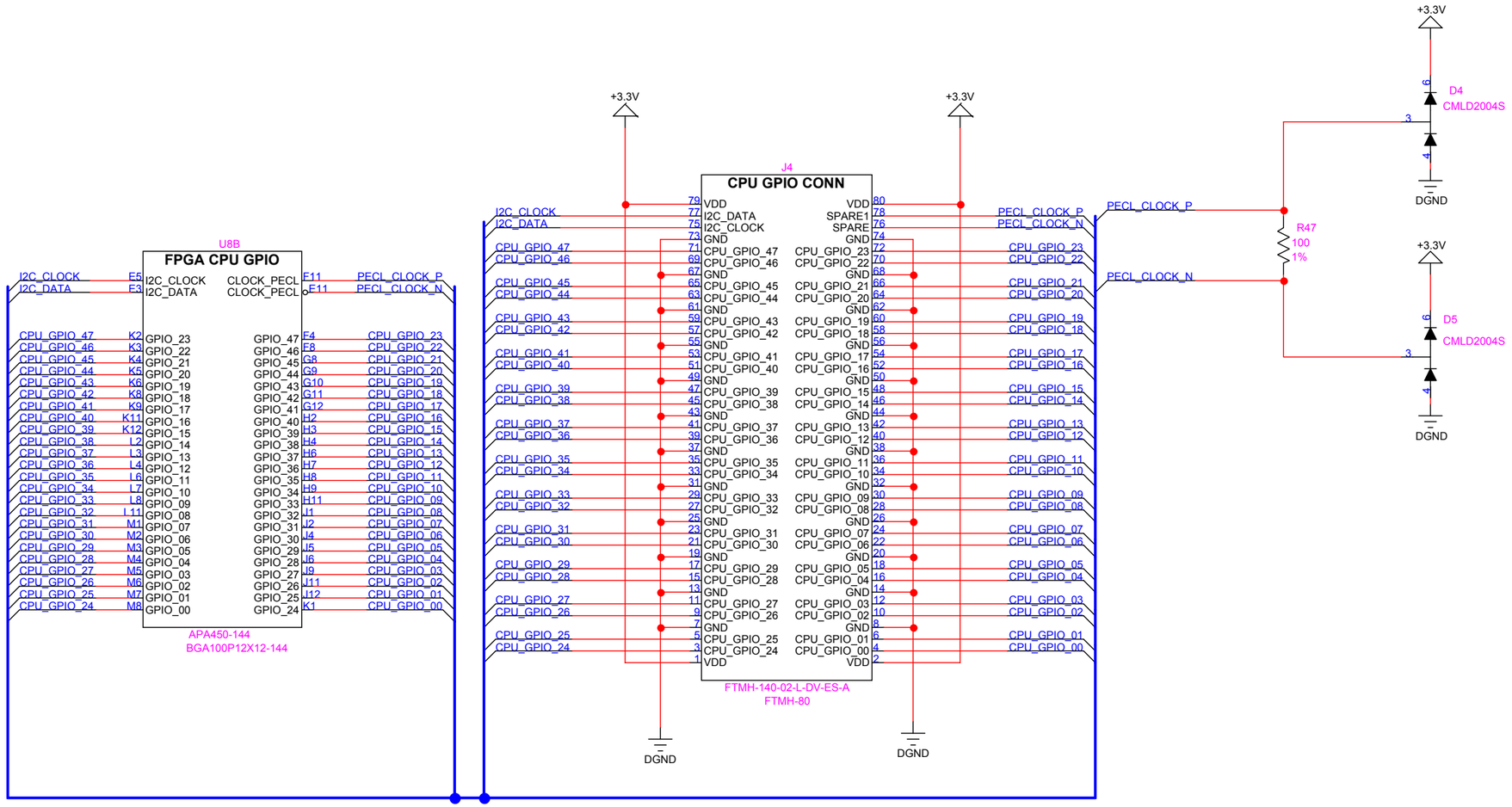
# CPU FPGA GPIO

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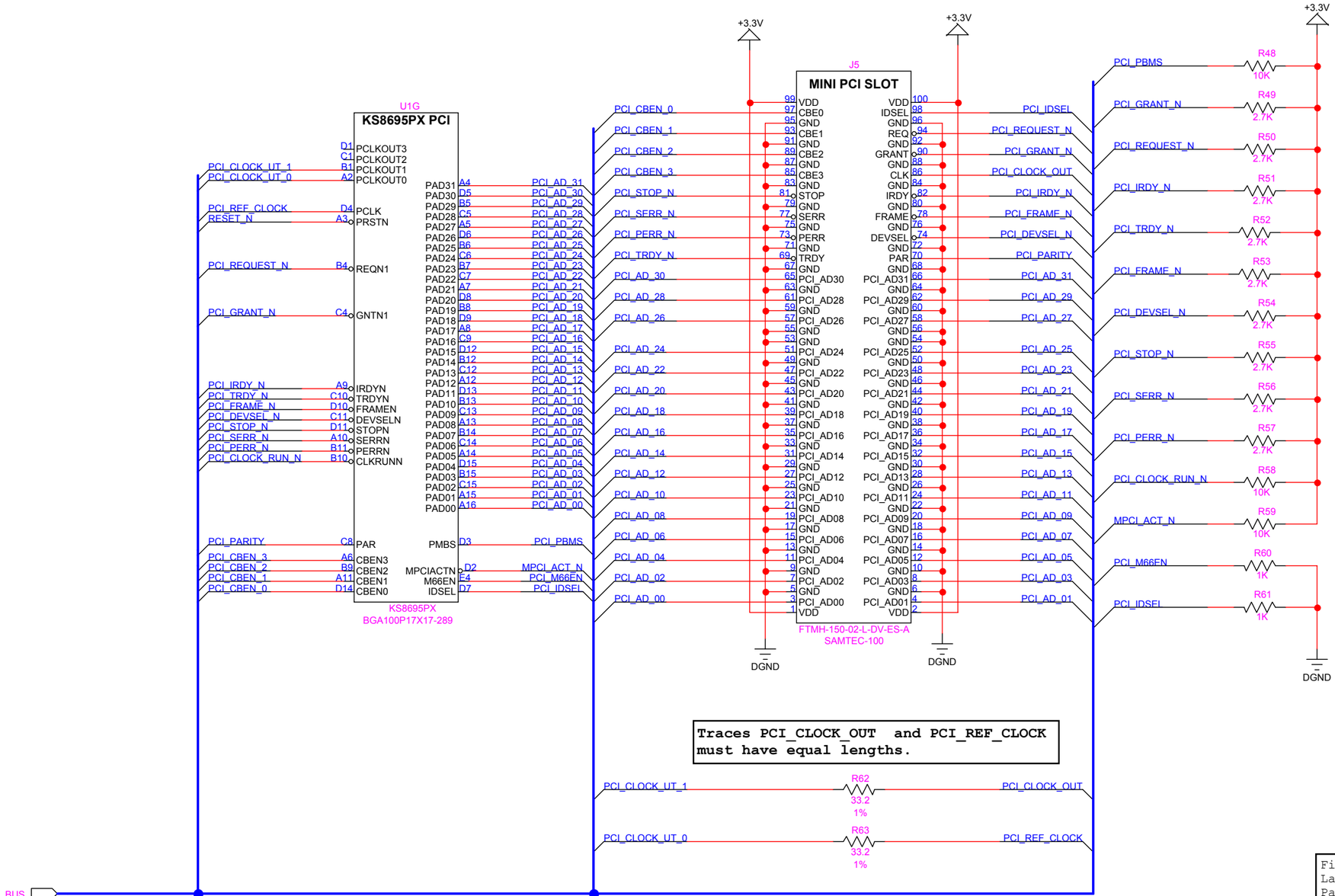
# CPU PCI INTERFACE

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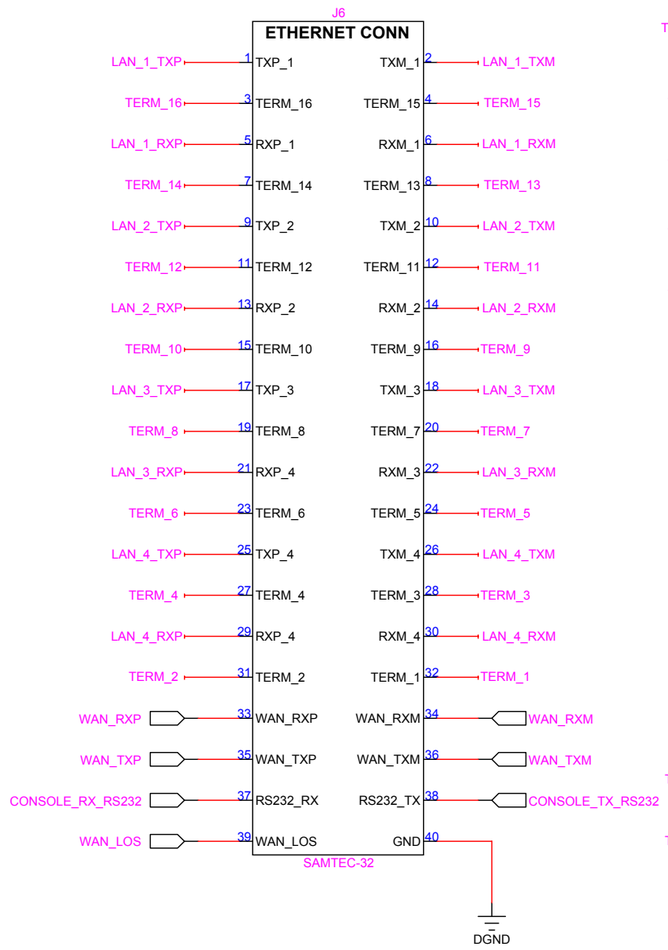
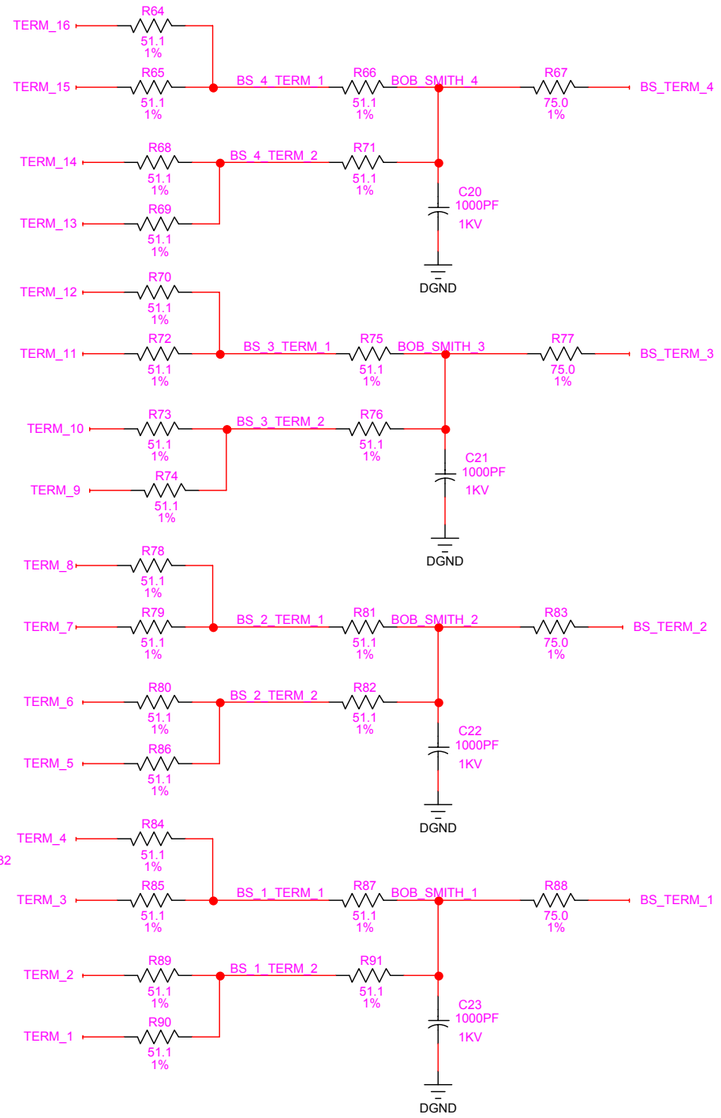
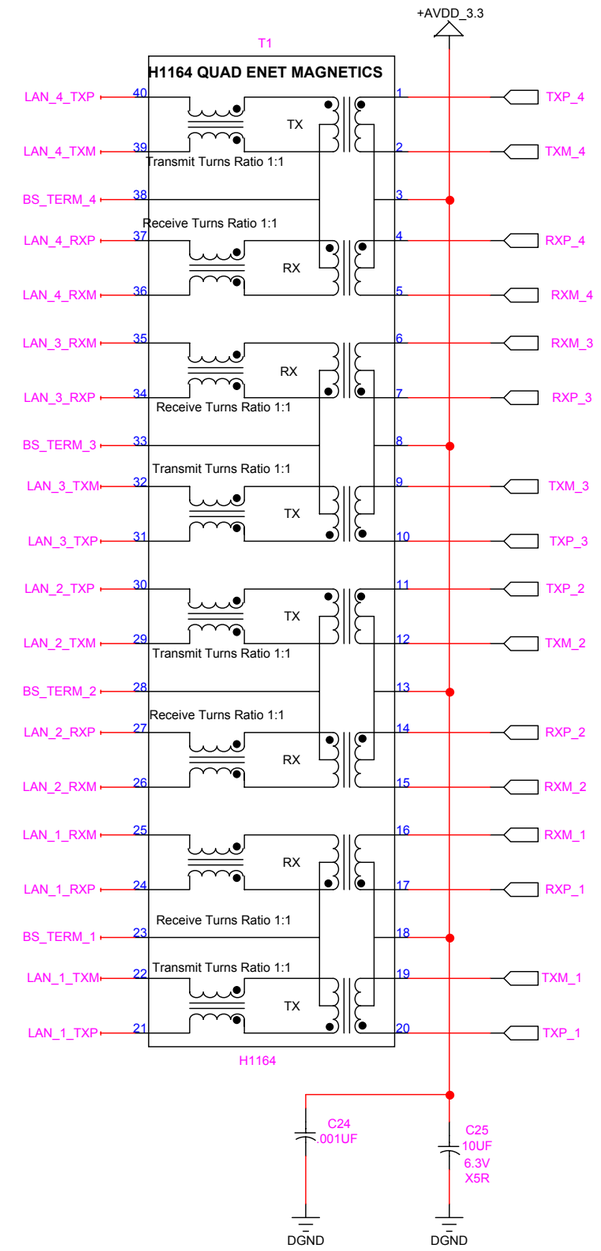
# ETHERNET ISOLATION & BOB SMITH TERMINATIONS

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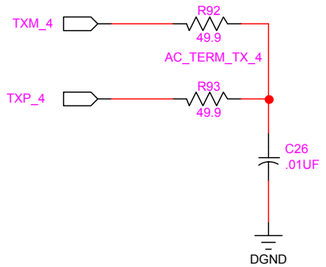
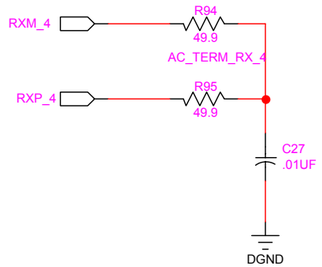
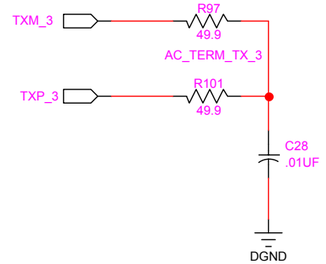
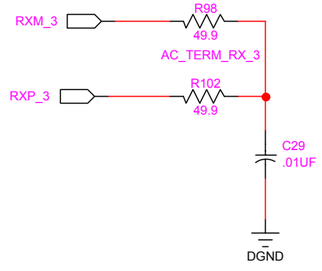
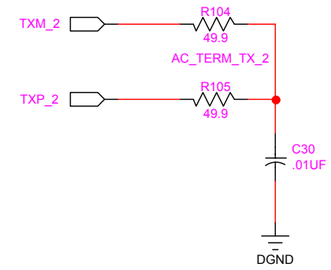
# ETHERNET PORTS

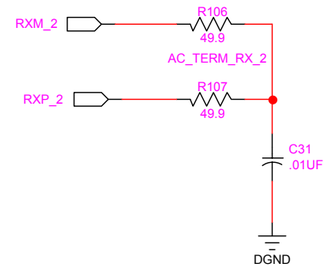


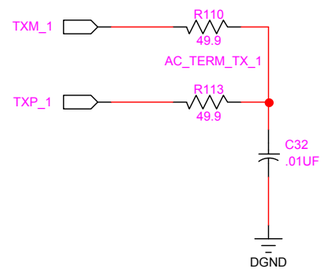



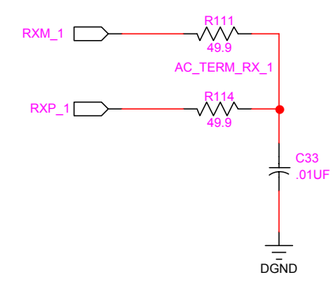



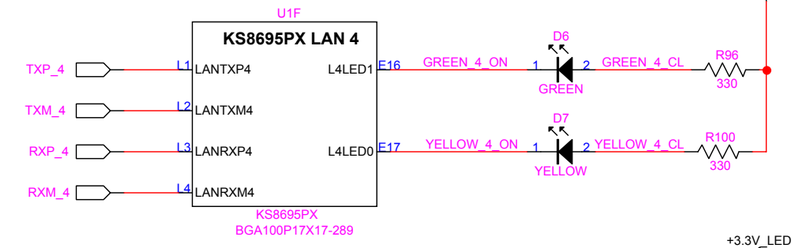



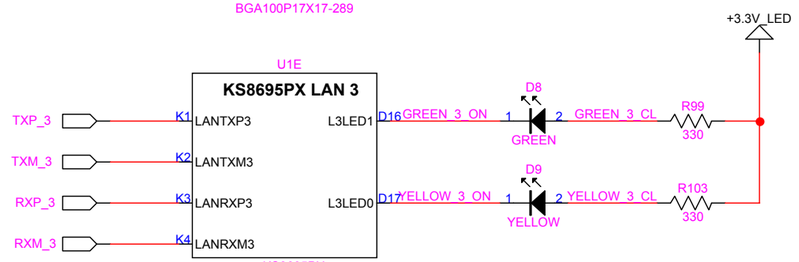



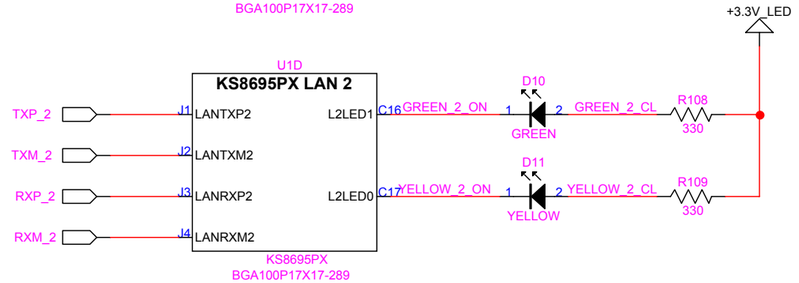



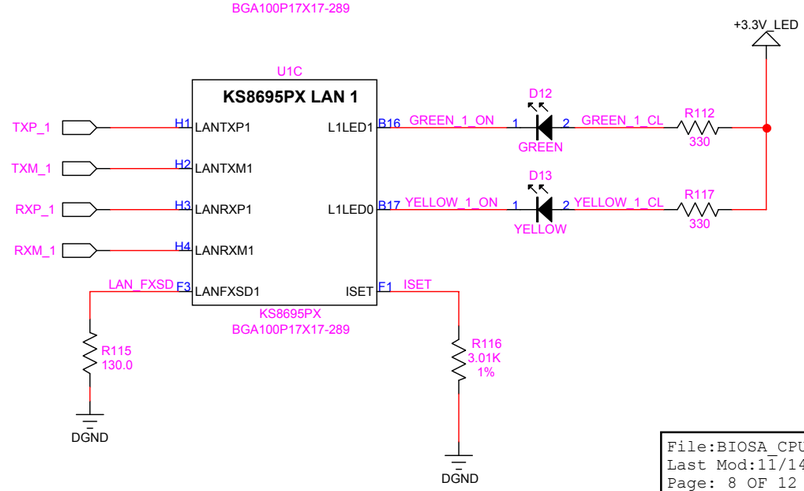

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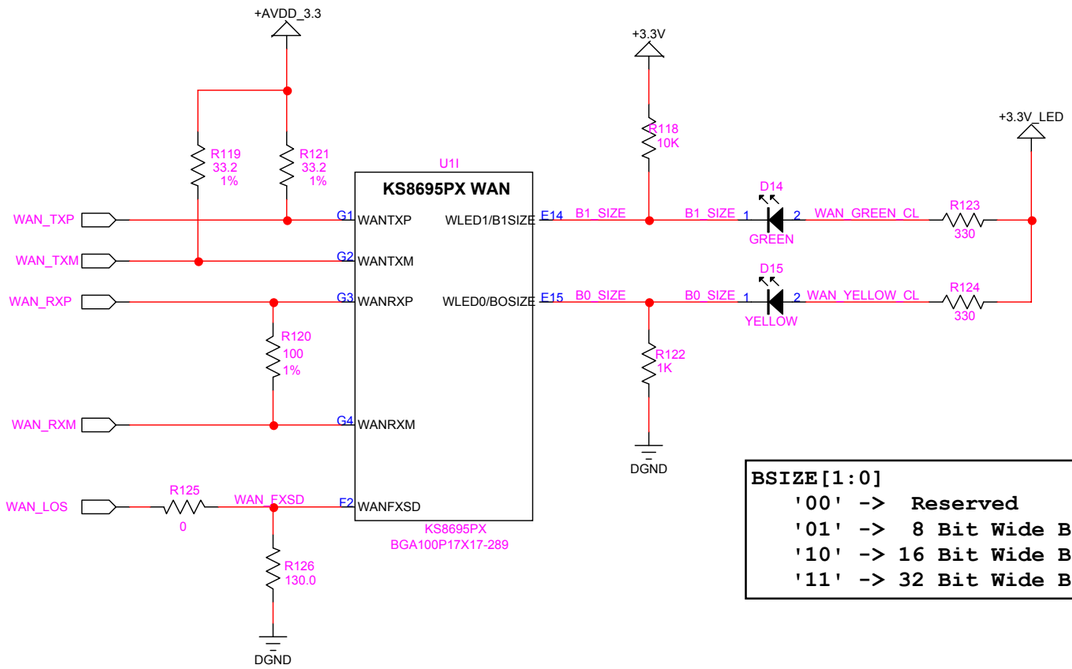
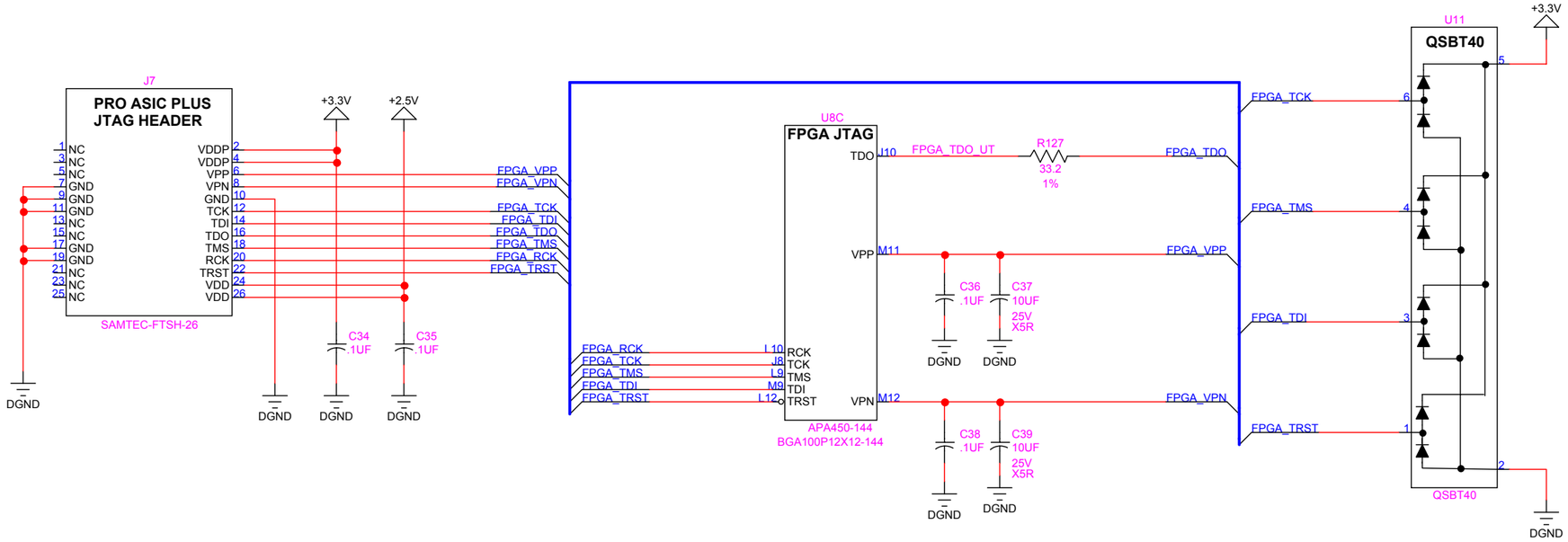
# ETHERNET FIBER PORT




**BSIZE[1:0]**
- '00' -> Reserved
- '01' -> 8 Bit Wide Boot
- '10' -> 16 Bit Wide Boot
- '11' -> 32 Bit Wide Boot

# FPGA PROGRAMMING INTERFACE

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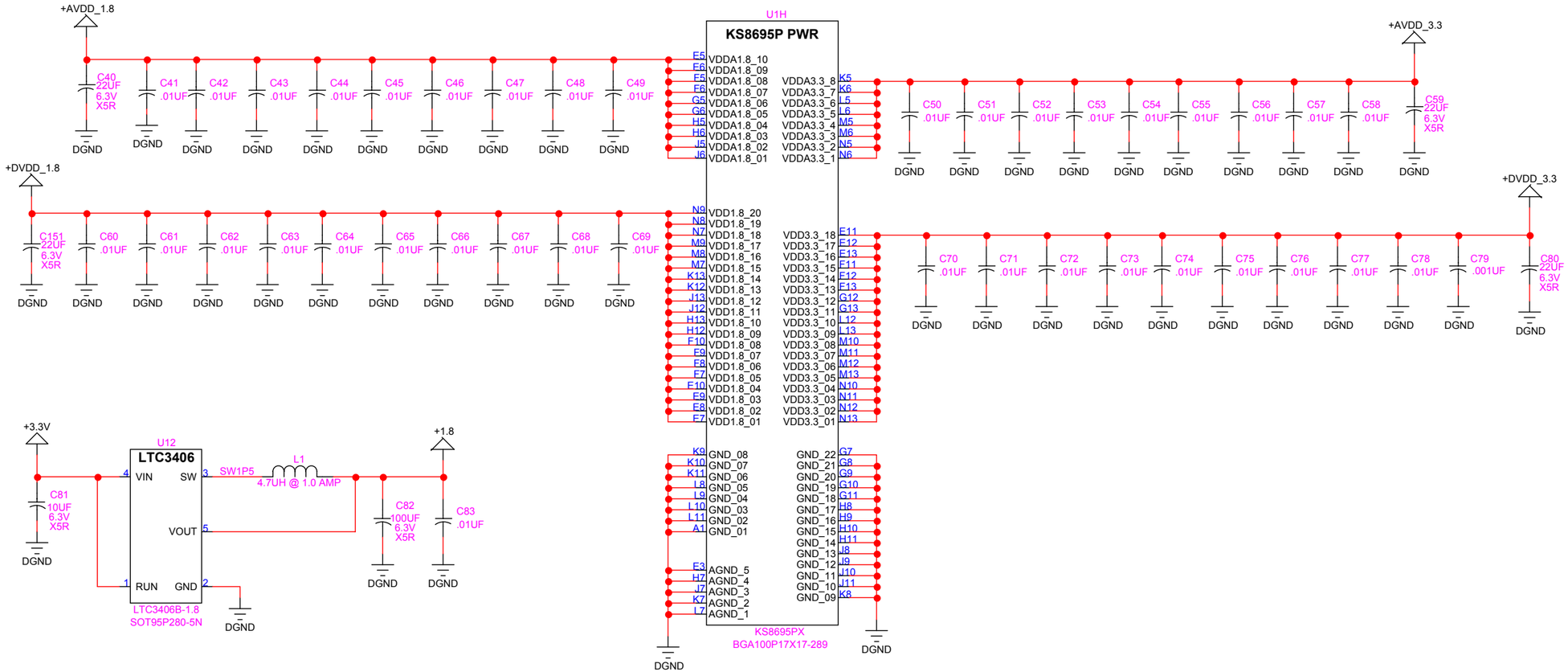
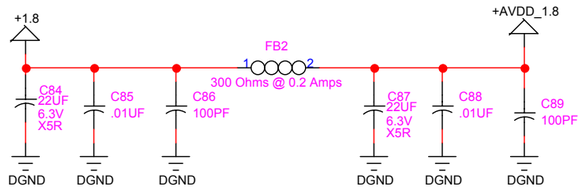
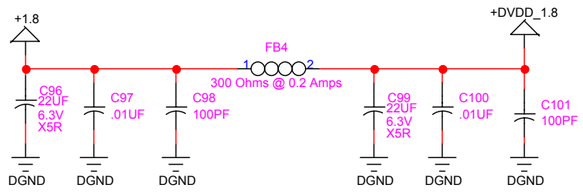
# CPU POWER DISTRIBUTION

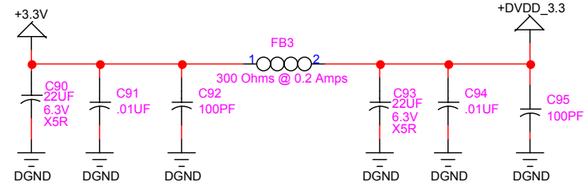


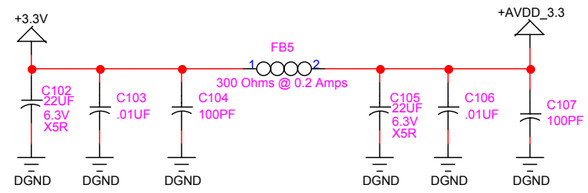




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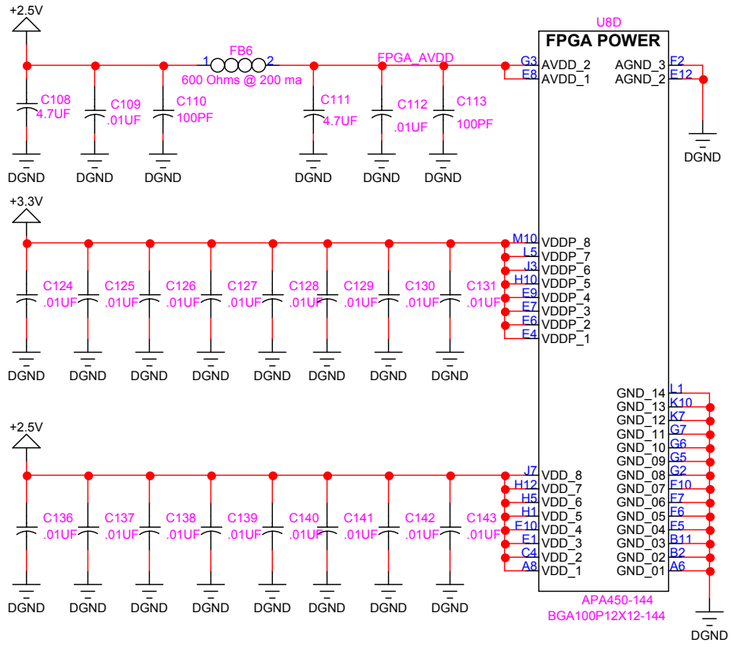
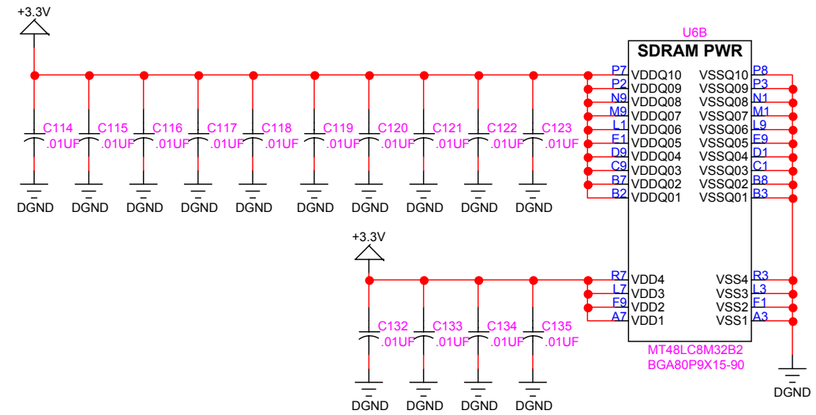
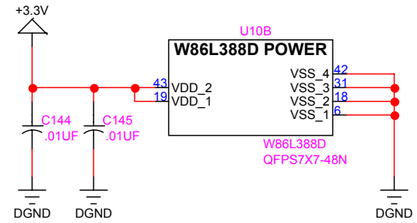
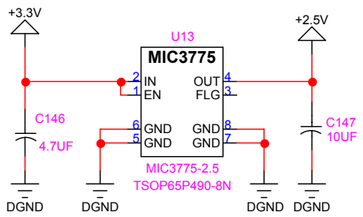
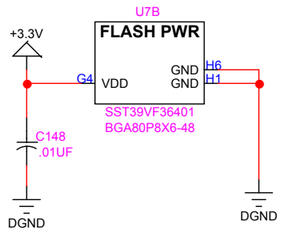
# FPGA, STORAGE AND SD POWER DISTRIBUTION

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