

N-Channel 60-V (D-S) Fast Switching MOSFET

PRODUCT SUMMARY

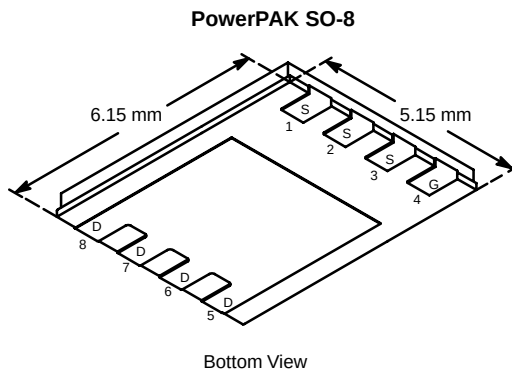
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
60	0.022 @ $V_{GS} = 10$ V	10.3
	0.031 @ $V_{GS} = 4.5$ V	8.7

FEATURES

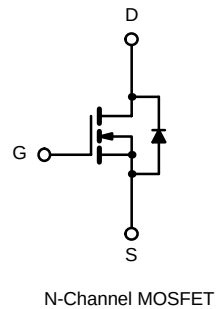
- TrenchFET® Power MOSFET
- New Low Thermal Resistance PowerPAK® Package with Low 1.07-mm Profile
- PWM Optimized for Fast Switching
- 100% R_g Tested

APPLICATIONS

- Primary Side Switch for 24-V DC/DC Applications
- Secondary Synchronous Rectifier



Ordering Information: Si7850DP-T1



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter		Symbol	10 secs	Steady State	Unit
Drain-Source Voltage		V _{DS}	60		V
Gate-Source Voltage		V _{GS}	± 20		
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	10.3	6.2	A
	T _A = 85°C		7.5	4.5	
Continuous Source Current		I _S	3.7	1.5	
Pulsed Drain Current		I _{DM}	40		
Avalanche Current ^b		I _{AS}	15		
Single Avalanche Energy ^b		E _{AS}	11		mJ
Maximum Power Dissipation ^a	T _A = 25°C	P _D	4.5	1.8	W
	T _A = 85°C		2.3	0.9	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	-55 to 150		°C

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	22	28	$^\circ\text{C/W}$
		58	70	
Maximum Junction-to-Case (Drain)	R_{thJC}	2.6	3.3	

Notes

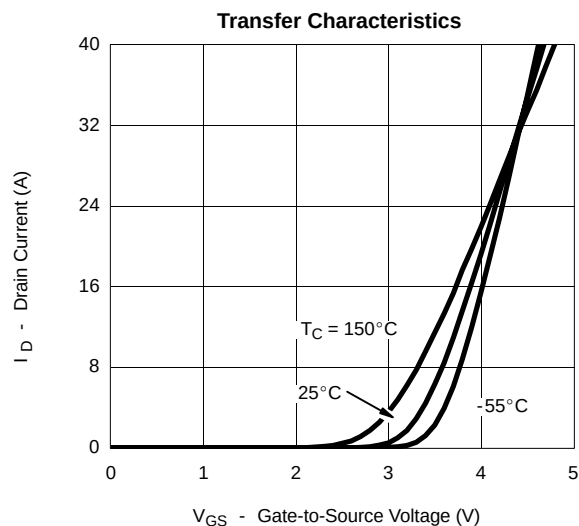
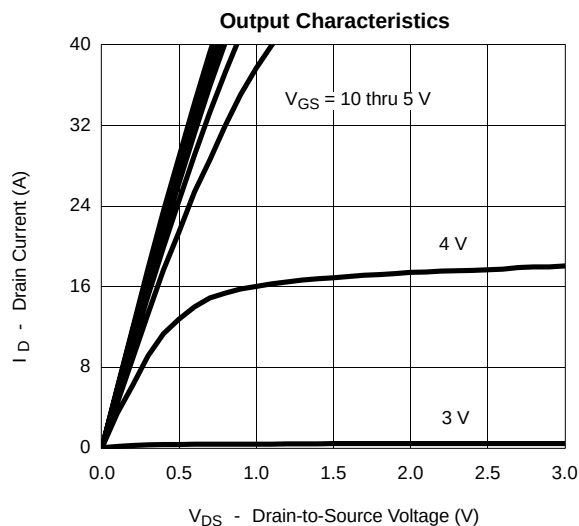
- Surface Mounted on 1" x 1" FR4 Board.
- Guaranteed by design, not subject to production testing.

MOSFET SPECIFICATIONS ($T_J = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$	60			V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1			
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$			20	
On-State Drain Current ^{NO TAG}	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	40			A
Drain-Source On-State Resistance ^{NO TAG}	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 10.3\text{ A}$		0.018	0.022	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 8.7\text{ A}$		0.025	0.031	
Forward Transconductance ^{NO TAG}	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 10.3\text{ A}$		26		S
Diode Forward Voltage ^{NO TAG}	V_{SD}	$I_S = 3.8\text{ A}, V_{GS} = 0\text{ V}$		0.85	1.2	V
Dynamic^{NO TAG}						
Total Gate Charge	Q_g	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_D = 10.3\text{ A}$		18	27	nC
Gate-Source Charge	Q_{gs}			3.4		
Gate-Drain Charge	Q_{gd}			5.3		
Gate-Resistance	R_G		0.5	1.4	2.2	Ω
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 30\text{ V}, R_L = 30\text{ }\Omega$ $I_D \cong 1\text{ A}, V_{GEN} = 10\text{ V}, R_G = 6\text{ }\Omega$		10	20	ns
Rise Time	t_r			10	20	
Turn-Off Delay Time	$t_{d(off)}$			25	50	
Fall Time	t_f			12	24	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = 3.8\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		50	80	

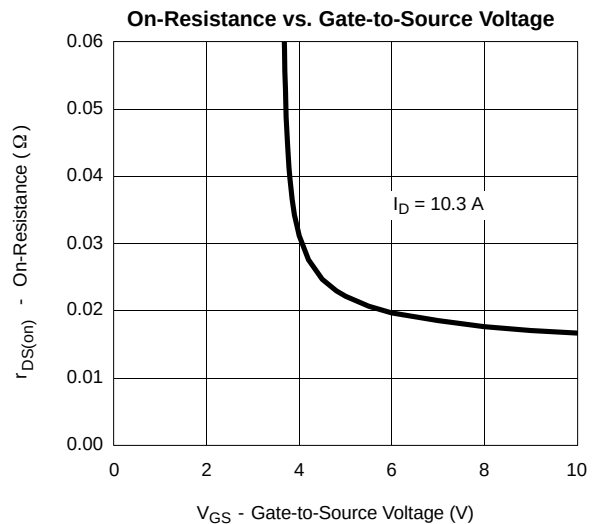
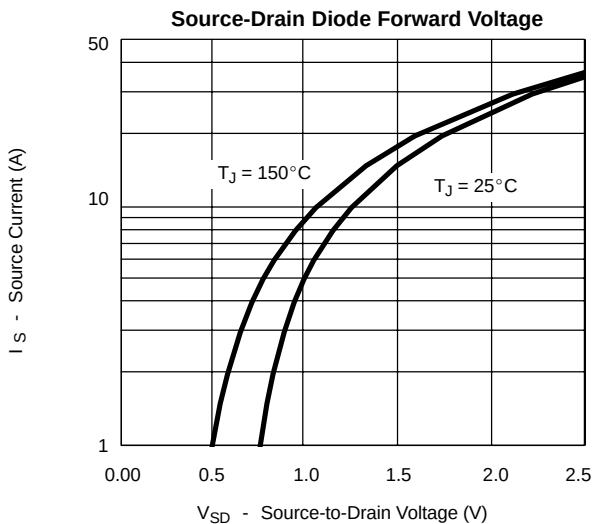
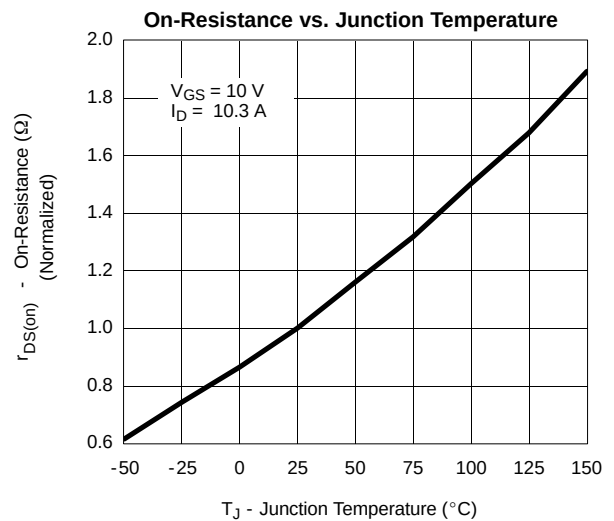
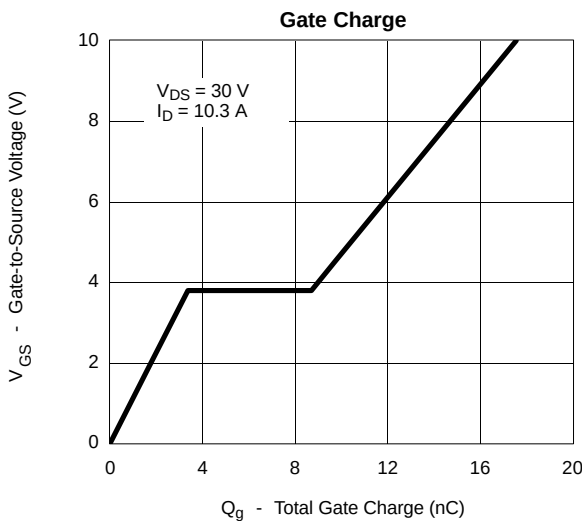
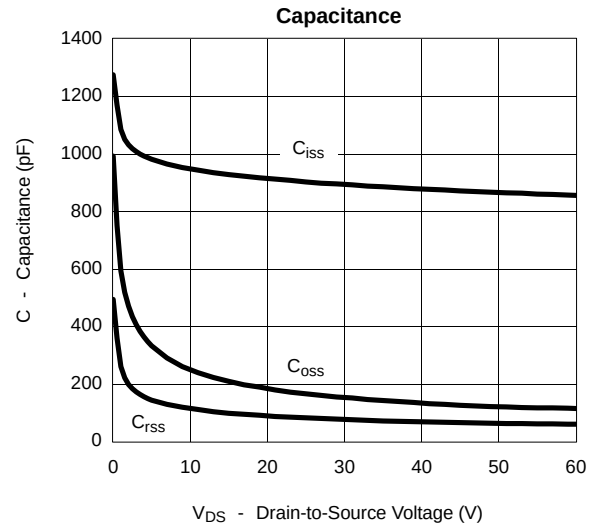
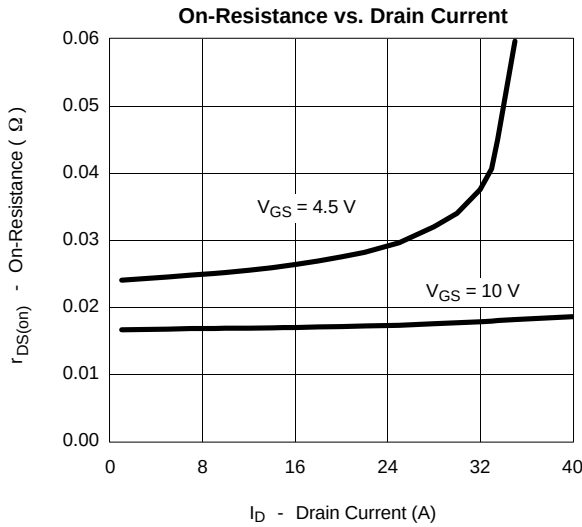
Notes

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



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