# Package

## FAQs

June 2003

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# I. Physical Dimensions

## 1. What is a package footprint?

A package footprint is the actual layout used to attach a package to a PCB. See an example of a package footprint under the "EIA Standard Board Layout Drawing" section on the following web page:
http://www.actel.com/docs/sockets/RecPCBdesign.pdf

## 2. What is the flatness limit for all BGA packaged ICs?

Flatness refers to the amount of allowable package bend of the plane of the solder balls and bend of the plane of the package surface bearing the solder balls (Figure 1). Actel's packages satisfy the JEDEC standards for flatness on all BGA, FBGA, and CS packages. For the actual values, please refer to Actel's *Mechanical Drawings* document located at: http://www.actel.com/documents/PckgMechDrwngs.pdf.

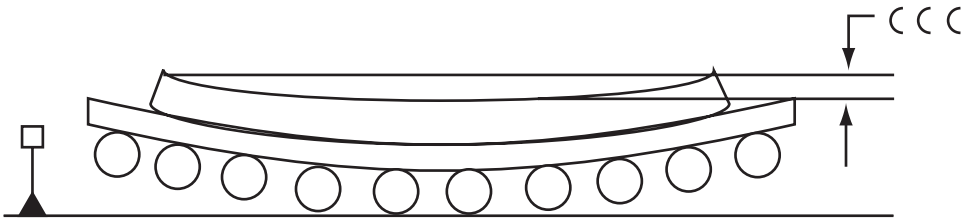

**Figure 1:** Diagram of Flatness Measurement (from JEDEC Standard 95, page 4.17-17/A)

## 3. What are the die sizes for Actel's FPGAs?

The die size is proprietary information and is not made available publicly. For inquiries, contact your local sales representative.

## 4. What is BSC (Basic Spacing between Centers)?

To specify package mechanical dimensions, we frequently use the term BSC, which means Basic Spacing between Centers. This is a theoretical true position dimension and has no tolerance (Figure 2).

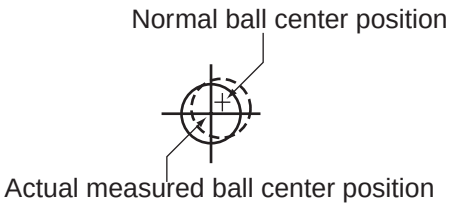


**Figure 2:** Diagram of BSC Measurement. (From JEDEC Standard 95, page 4.17-11/A)

## 5. What is the Land Size for Actel's BGA Package?

The land size of Actel's BG313, BG272, BG329 are 0.75+/-0.03mm in diameter with solder mask defined open at 0.63+/-0.03mm, which is about 25mils.

## 6. Where can I get information about Total Weights for Actel Devices in various packages?

The latest package weight information is available in the *Package Characteristics and Weights* document located at: http://www.actel.com/docs/package/PckgCharWeights.pdf

Note: Weights are approximate values. For greater accuracy, we recommend weighing the parts yourself. There may be slight variations from lot to lot.

## 7. Where can I get Hermetic Package Mechanical configuration information (cavity, weight, lid size and heat sink size)?

Hermetic Package Mechanical configuration is available on Actel's website: http://www.actel.com/documents/HermeticPckg.pdf

## 8. What packaging considerations must be taken into account when changing a design from A54SX08-VQ100 to A54SX08A?

In order to transition from the A54SX08-VQ100 to Actel's A54SX08A devices, you must make a package switch from the VQ100 to the TQ100.

These two packages have an identical footprint, but the package height is different:

SX – VQ100 Package Height = 1.2mm

SX-A – TQ100 Package Height = 1.6mm

Additionally, the pinouts are basically the same, except that the $V_{CCR}$ pins on the SX device will be "no connects" on the SX-A device. The $V_{CCR}$ reference voltage was eliminated on the SX-A devices to enable a "hot swappable" feature.

# II. Materials

## 9. What materials are used in Actel's Plastic Leaded packages?

PLCC – Plastic Leaded Chip Carrier

- Leadframe Material: Cu 151
- Composition: 99.9%Cu & 0.1%Zr.
- Filler Type: Ag
- Wire Type: 1.2 mil Au
- Composition: 99.99% Au
- Lead Finish Type: Solder Plate
- Composition: 85%(Sn)/15%(Pb)

PQFP – Plastic Quad Flat Package

- Leadframe Material: Cu 7025
- Composition: 96.2%Cu, 3.0%Ni, 0.65%Si & 0.15%Mg
- Filler Type: Ag
- Wire Type: 1.0 or 1.2 mil Au
- Composition: 99.99% Au
- Heat sink: Anodized Aluminum

- Lead Finish Type: Solder Plate
- Composition: 85%(Sn)/15%(Pb)

TQFP – Thin Quad Flat Package

- Leadframe Material: Cu 64T
- Composition: 96.17%Cu, 0.30%Cr, 0.27%Sn & 0.26%Zn
- Filler Type: Ag
- Wire Type: 1.0 or 1.2 mil Au
- Composition: 99.99% Au
- Lead Finish Type: Solder Plate
- Composition: 85%(Sn)/15%(Pb)

VQFP – Very Thin Quad Flat Package

- Leadframe Material: Cu 64T
- Composition: 96.17%Cu, 0.30%Cr, 0.27%Sn & 0.26%Zn
- Filler Type: Ag
- Wire Type: 1.0 or 1.2 mil Au
- Composition: 99.99% Au
- Lead Finish Type: Solder Plate
- Composition: 85%(Sn)/15%(Pb)

RQFP – Plastic Quad Flat Package (Exposed Heat sink)

- Leadframe Material: Cu 64T
- Composition: 96.17%Cu, 0.30%Cr, 0.27%Sn & 0.26%Zn
- Filler Type: Ag
- Wire Type: 1.2 mil Au
- Composition: 99.99% Au
- Heat sink: Copper Alloy
- Lead Finish Type: Solder Plate
- Composition: 85%(Sn)/15%(Pb)

## 10. What materials are used in Actel's Plastic Array packages?

PBGA – Plastic Ball Grid Array

- Substrate: BT (Bismaleimide Triazine) - laminate
- Filler Type: Ag
- Wire Type: 1.0 or1.2 mil Au
- Composition: 99.99% Au
- Solder Ball Composition: 62%Sn, 36%Pb & 2%Ag or 63%Sn/37%Pb
- Ball Pitch: 1.27 mm

FBGA – Fine Pitch Ball Grid Array

- Substrate: BT (Bismaleimide Triazine) - laminate
- Filler Type: Ag

- Wire Type: 1.0 mil Au
- Composition: 99.99% Au
- Solder Ball Composition: 63%Sn/37%Pb
- Ball Pitch: 1.0mm

## 11. What materials are used in Actel's Hermetic packages?

CQFP – Ceramic Quad Flat Package

- Leadframe Raw Material: Kovar
- Composition: 53%Fe, 29%Ni, 17%Co, 1%Others
- Finish: Gold over Nickel
- Substrate: Alumina
- Composition: 98%Al2O3
- Bond Finger Bare Material: Tungsten
- Finish: Gold over Nickel
- Type: Cyanate Ester Paste
- Wire Type: 1.3 mil Al or 1.0 mil Au
- Lid Raw Material: Kovar
- Finish: Gold over Nickel
- Preform Material: 80%Au/20%Sn
- Lead Finish: Gold or Solder Dip (63%Sn/37%Pb)

CPGA – Ceramic Pin Grid Array

- Leadframe Raw Material: Kovar
- Composition: 53%Fe, 29%Ni, 17%Co, 1%Others
- Finish: Gold over Nickel
- Substrate: Alumina
- Composition: 98%Al2O3
- Bond Finger Bare Material: Tungsten
- Finish: Gold over Nickel
- Type: Cyanate Ester Paste
- Wire Type: 1.3 mil Al
- Lid Raw Material: Kovar
- Finish: Gold over Nickel
- Preform Material: 80%Au/20%Sn
- Lead Finish: Gold or Solder Dip (63%Sn/37%Pb)

## 12. What materials are used in Actel's CSP packages?

CSP – Chip Scale Package

- Substrate: BT (Bismaleimide Triazine) - laminate
- Filler Type: Ag
- Wire Type: 1.0 mil Au
- Composition: 99.99% Au
- Solder Ball Composition: 62%Sn/36%Pb/2.0%Ag
- Ball Pitch: 0.8 mm

## 13. When using BGA, FBGA, and CS packages, what PCB material is recommended for use?

The PCB material can be FR-4 (Military-type GF) or FR-5 (Military-type GH).

## 14. Which Actel packages are hermetically sealed?

Actel's CQFP, CCGA and CPGA packages are hermetically sealed.

## 15. For CQFP packages, there is a small metal "lid" on the base of the package. Is the die attached to this? Is it a heat sink for the die?

The die is not attached to this lid, and it is not a heat sink. There is an air cavity between the die and the lid. It is metal so it does conduct some heat away from the package, but the die is not directly connected to it such as in the RQ packages.

## 16. Do the PQFP packages have a heat sink? If so, what material is used?

Yes, there is heat sink employed called a heat spreader. The material is Aluminum.

## 17. Which Actel package has an internal cavity?

CQFP, CPGA, and CCGA packages have an internal cavity. The plastic packages have a drop-in heat spreader.

## 18. What is the lead-free package?

Japan now requires all semiconductors manufactured in that country to have lead-free packaging. Most Japanese-based companies are insisting that all of their vendors comply with the regulations. Europe is moving in the same direction with its Wastes from Electric and Electronic Equipment (WEEE) directive, which requires the replacement of lead in electrical and electronic equipment by January 1, 2007. One of the critical requirements is that lead-free packages should pass 260 °C surface mount temperature.

Maximum operating temperature and other package characteristics will not change. The surface mount reflow temp is 260 °C for lead-free package and 220 °C for non lead-free package

# III. Moisture/Soldering

## 19. What is the specification for the various moisture sensitivity levels?

It is defined in JEDEC standard J-STD-020-B *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface-Mount Devices* located at: http://www.jedec.org/download/search/jstd020b.pdf

## 20. What are the moisture sensitivity levels of Actel devices?

All of Actel's plastic packages have a moisture sensitivity rating of level 3, except for RQFP and CS packages, which have level 4 and 2, respectively. The BGA package is also a level 3 device. Hermetic packages are not moisture sensitive, so there is no moisture sensitivity level for ceramic packages such as CQFP, CPGA, and CCGA packages. Actel has a program in place to improve the moisture sensitivity across our existing plastic packages.

## 21. What are the storage conditions for moisture sensitivity levels 3 and 4?

Storage condition for moisture sensitivity level 3:

- Floor Life: The allowable time period after removal from a moisture barrier bag and before the solder reflow processes for a moisture-sensitive device to be exposed to a factory ambient not exceeding 30°C, 60% RH and168 hours.
- Safe Storage: Dry SMD packages held in a controlled humidity condition such as the floor life clock remains at zero. Acceptable safe storage conditions for SMD packages classified as Level 3 are listed below:
  - Dry Pack: Dry packed SMD in an intact Moisture Barrier Bag will have a calculated shelf life of at least 12 months from the bag seal date shown on the caution or bar code level.
  - Dry Atmosphere Cabinet: Storage cabinet, which maintains low humidity by purging with dry air or nitrogen at 25 +/-5°C. The cabinet must be capable of recovering to their stated humidity rating within one hour from routine excursions such as door opening/closing.
  - Dry Cabinet at 5% RH: SMD packages not sealed in a Moisture Barrier Bags may be placed in a dry atmosphere cabinet, maintained at not greater than 5%RH.

Storage condition for moisture sensitivity level 4:

- Floor Life: The allowable time period after removal from a moisture barrier bag and before the solder reflow processes for a moisture-sensitive device to be exposed to a factory ambient not exceeding 30°C, 60% RH and 72 hours.
- Safe Storage: Same as above.

## 22. Why does Actel recommend that some devices be baked?

Certain device packages are sensitive to moisture. The recommended bake times will dry out any moisture that the plastic package has absorbed while sitting in the open. We base our bake times on moisture de-absorption data from our assembly plants.

## 23. Is there any reason not to bake the devices for 24 hours? If so, is the limitation due to lead oxidation causing poor solderability or is there another reason?

There is no problem associated with 24 hour dry bake; we prefer a shorter time to avoid any soldering problems.

## 24. Is there a recommended maximum number of bake cycles?

There is no recommended maximum limit for bake cycles.

## 25. What is the recommend baking process?

All of Actel's plastic packages have a moisture sensitivity rating of level 3, except for RQFP and CS packages, which have level 4 and 2, respectively.Actel's recommends baking the parts at 125°C. See the table below for the bake time:

| Package Type | Maximum Exposure Time to Ambient Condition Prior to Surface Mount | Bake Time at 125°C | Moisture Level |
|---|---|---|---|
| **BGA 144/256/272/313/329/420/456/484** | 168 hours | 8 hours | Level 3 |
| **PQFP 100/144/160/208/240** | 168 hours | 8 hours | Level 3 |
| **RQFP 208/24072** | hours | 8 hours | Level 4 |
| **TQFP 64/100144/176** | 168 hours | 5 hours | Level 3 |
| **VQFP 80/100** | 168 hours | 5 hours | Level 3 |
| **PLCC 44/68/84** | 168 hours | 8 hours | Level 3 |
| **CS 49/128/180** | 168 hours | 8 hours | Level 2 |

## 26. Does Actel dry pack all their devices?

All packages are dry-packed except for CQFP and CPGA packages.

## 27. Where can I find the temperature profile for reflow soldering?

For more information, see the following documents:

*Sample Temperature Profile for I/R or Convection Reflow* at: http://www.actel.com/docs/sockets/temp_graph.pdf

*Solder Reflow Profile for Lead-Free Packages* at:http://www.actel.com/documents/Solder_Reflow_LeadFree.pdf

# IV. Miscellaneous

## 28. What is JEDEC?

The JEDEC Solid State Technology Association, once known as the Joint Electron Device Engineering Council, is the semiconductor engineering standardization body of the Electronic Industries Alliance (EIA), a trade association that represents all areas of the electronics industry. Many of today's packaging standards are defined by JEDEC specification, and these specs will be referenced from time to time. More information is available at: http://www.jedec.org/

## 29. Can Actel's FPGAs be purchased in die form?

You must contact your local sales representative for bare die purchase information.

## 30. What are the recommended sockets for Actel FPGAs?

The recommended sockets for Actel FPGAs can be found on Actel's website at: http://www.actel.com/docs/sockets/SocketRec.pdf

## 31. What are the die bond pin assignments for PGA and BGA Packages?

Contact Actel Technical Support (800) 262-1060 to obtain the wire bond diagrams for the device you are using. The linked files below are cross-reference charts that list the die pad number and the pin to which it corresponds on all BGA and PGA packages.

| | | |
|---|---|---|
| 1010PG84 | 1020PG84 | 1225PG84 |
| 1240PG132 | 1280PG176 | 14100BG313 |
| 14100PG257 | 1415PG100 | 1425PG133 |
| 1440PG175 | 1460BG225 | 1460PG207 |

Please note that VSS and VKS = GND, all $V_{PP}$ and VSV=$V_{CC}$

## 32. Do you have any information on Forming and Trimming the Leads for CQFP Packages?

Ceramic Quad Flat packages (CQFP) are an industry standard for applications operating in extreme conditions and high reliability expectations. Military applications routinely choose CQFPs due to its high reliability characteristics. These characteristics include package reliability at high temperatures and resistance to moisture due to being hermetically sealed. Actel provides a range of CQFP packages for all Actel devices. For more information on the specific devices, refer to Actel's website at www.actel.com.

The following link(http://www.actel.com/docs/sockets/sy-cq196.pdf) shows a drawing of a CQFP package. The bottom of the first page shows a CQFP package in its frame, also referred to as a Ceramic Tie Bar, and the package leads are attached to the frame. CQFPs are shipped from Actel with these frames attached. CQFP devices are programmed by inserting the package into a CQFP programming adapter on an Actel Activator. The next step is to trim and form the leads (Gullwing shape) to surface mount the device onto the circuit board. We recommend that this procedure be handled by vendors that specialize in trimming and forming leads. One such vendor is Fancort Industries, Inc. To get more information regarding trimming and forming leads for CQFP packages, you may contact Fancort Industries per below:

Fancort Industries, Inc.
31 Fairfield
West Caldwell, NJ 07006
Phone (201) 575-0610
Fax (201) 575-9234

The 84-pin CQFP package is shipped and handled differently than the other CQFP packages. For the 84-pin CQFP, each device and its frame is placed inside a chip carrier and then shipped. The 84-pin CQFP device is programmed by inserting the package with chip carrier into a CQFP programming adapter on an Actel Activator. Once the device is programmed and ready to be surface mounted onto the circuit board, the carrier must be removed. The CQFP package is unloaded from the carrier using a carrier extraction tool. One such carrier extraction tool is manufactured by Wells, who also manufactures the chip carriers. The part number for the carrier extraction tool is T-0315-9. Wells can be contacted per below. The next step is to trim and form the leads (Gullwing shape) to surface mount the device onto the circuit board as with the other CQFP packages.

## 33. Are lids on Actel's ceramic packages grounded?

Yes, lids on all Actel ceramic packages including Ceramic Pin Grid Array (CPGA) and Ceramic Quad Flat Pack (CQFP) are grounded.

## 34. Are there any recommendations to connect the heat sink to board GND?

The heat sink is connected to an internal package GND panel so it is not necessary to connect the heat sink to board GND.

## 35. Are there any recommendations for the epoxy used on a PCB for system and package vibration tests?

No, we don't provide a recommendation. The tester should follow the standard testing method, and the epoxy material is dependant on the test condition.

## 36. Does Actel perform the PIND (Particle Impact Noise Detection) test on any devices?

We do PIND for RH, RT, and RP devices.

## 37. What is a "lot number" and "date code" and where can they be found on an Actel FPGA?

To trace a device's lot history from qualification test records, Actel must have the lot number of the device under investigation. The lot number allows Actel to identify the Silicon ingot and wafer from which the device was fabricated.

For most Actel FPGAs, the Lot Number is printed on the bottom side of the package and the Date Code is on the top side, although there are exceptions. In either case, the Lot Number is easy to identify, given the following example:

Lot Number: 2ACT312381

Date Code: 9919

These values indicate that the device is fabricated 19th week, 1999, and the wafer is from the lot number #2ACT312381

## 38. What is the difference between RQFP and PQFP packages?

RQFP has an exposed heat slug while PQFP does not.

## 39. Why do I see notches on the leads of the CQFP Package?

The notches are placed on the package pins during rework to attain compliance with the package lead specifications. The form factor of this rework is clearly defined on MIL-STD-1835B, Notice 2, detail G on page 136 (see sketch) and note 11 on page 141. See a detailed explanation on Actel's website:
http://www.actel.com/docs/package/LeadRework.pdf

For more information, call **1.888.99.ACTEL** or visit our website at **http://www.actel.com**

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