

# ProASIC<sup>PLUS</sup> Flash Family FPGAs



## Features and Benefits

### High Capacity

- 75,000 to 1 million System Gates
- 27k to 198kbits of Two-Port SRAM
- 66 to 712 User I/Os

### Reprogrammable Flash Technology

- 0.22μ 4LM Flash-based CMOS Process
- Live at Power-Up, Single-Chip Solution
- No Configuration Device Required
- Retains Programmed Design during Power-Down/Power-Up Cycles

### Performance

- 3.3V, 32-bit PCI (up to 50 MHz)
- Two Integrated PLLs
- External System Performance up to 150 MHz

### Secure Programming

- The Industry's Most Effective Security Key (FlashLock<sup>TM</sup>) Prevents Read Back of Programming Bitstream

### Low Power

- Low Impedance Flash Switches
- Segmented Hierarchical Routing Structure
- Small, Efficient, Configurable (Combinatorial or Sequential) Logic Cells

### High Performance Routing Hierarchy

- Ultra Fast Local and Long Line Network
- High Speed Very Long Line Network
- High Performance, Low Skew, Splittable Global Network

## ProASIC<sup>PLUS</sup> Product Profile

| Device                        | APA075 | APA150   | APA300   | APA450        | APA600        | APA750   | APA1000   |
|-------------------------------|--------|----------|----------|---------------|---------------|----------|-----------|
| Maximum System Gates          | 75,000 | 150,000  | 300,000  | 450,000       | 600,000       | 750,000  | 1,000,000 |
| Maximum Registers             | 3,072  | 6,144    | 8,192    | 12,288        | 21,504        | 32,768   | 56,320    |
| Embedded RAM Bits             | 27k    | 36k      | 72k      | 108k          | 126k          | 144k     | 198k      |
| Embedded RAM Blocks (256 X 9) | 12     | 16       | 32       | 48            | 56            | 64       | 88        |
| LVPECL                        | 2      | 2        | 2        | 2             | 2             | 2        | 2         |
| PLL                           | 2      | 2        | 2        | 2             | 2             | 2        | 2         |
| Global Networks               | 4      | 4        | 4        | 4             | 4             | 4        | 4         |
| Maximum Clocks                | 24     | 32       | 32       | 48            | 56            | 64       | 88        |
| Maximum User I/Os             | 158    | 242      | 290      | 344           | 454           | 562      | 712       |
| JTAG ISP                      | Yes    | Yes      | Yes      | Yes           | Yes           | Yes      | Yes       |
| PCI                           | Yes    | Yes      | Yes      | Yes           | Yes           | Yes      | Yes       |
| Package (by pin count)        |        |          |          |               |               |          |           |
| TQFP                          | 100    | 100      |          |               |               |          |           |
| PQFP                          | 208    | 208      | 208      | 208           | 208           | 208      | 208       |
| PBGA                          |        | 456      | 456      | 456           | 456           | 456      | 456       |
| FBGA                          | 144    | 144, 256 | 144, 256 | 144, 256, 484 | 256, 484, 676 | 676, 896 | 896, 1152 |

- 100% Routability and Utilization

### I/O

- Schmitt-Trigger Option on Every Input
- Mixed 2.5V/3.3V Support with Individually-Selectable Voltage and Slew Rate
- Bidirectional Global I/Os
- Compliance with PCI Specification Revision 2.2
- Boundary-Scan Test IEEE Std. 1149.1 (JTAG) Compliant
- Pin Compatible Packages across ProASIC<sup>PLUS</sup> Family

### Unique Clock Conditioning Circuitry

- PLL with Flexible Phase, Multiply/Divide and Delay Capabilities
- Internal and/or External Dynamic PLL Configuration
- Two LVPECL Differential Pairs for Clock or Data Inputs

### Standard FPGA and ASIC Design Flow

- Flexibility with Choice of Industry-Standard Front-End Tools
- Efficient Design through Front-End Timing and Gate Optimization

### ISP Support

- In-System Programming (ISP) via JTAG Port

### SRAMs and FIFOs

- ACTgen Netlist Generation Ensures Optimal Usage of Embedded Memory Blocks
- 24 SRAM and FIFO Configurations with Synchronous and Asynchronous Operation Up to 150 MHz



## General Description

The ProASIC<sup>PLUS</sup> family of devices, Actel's second generation Flash FPGAs, offers enhanced performance over Actel's ProASIC family. It combines the advantages of ASICs with the benefits of programmable devices through nonvolatile Flash technology. This enables engineers to create high-density systems using existing ASIC or FPGA design flows and tools. In addition, the ProASIC<sup>PLUS</sup> family offers a unique clock conditioning circuit based on two on-board phase-locked loops (PLLs). The family offers up to 1 million system gates, supported with up to 198kbits of 2-port SRAM and up to 712 user I/Os, all providing 50 MHz PCI performance.

Advantages to the designer extend beyond performance. Unlike SRAM-based FPGAs, four levels of routing hierarchy simplify routing, while the use of Flash technology allows all functionality to be live at power-up. No external Boot PROM is required to support device programming. While on-board security mechanisms prevent all access to the program information, reprogramming can be performed in-system to support future design iterations and field upgrades. The device's architecture mitigates the complexity of ASIC migration at higher user volume. This makes ProASIC<sup>PLUS</sup> a cost-effective solution for applications in the networking, communications, computing, and avionics markets.

The ProASIC<sup>PLUS</sup> family achieves its nonvolatility and reprogrammability through an advanced Flash-based 0.22µm LVC MOS process with four-layer metal. Standard CMOS design techniques are used to implement logic and control functions, including the PLLs and LVPECL inputs. This results in predictable performance fully compatible with gate arrays.

The ProASIC<sup>PLUS</sup> architecture provides granularity comparable to gate arrays. The device core consists of a Sea-of-Tiles<sup>TM</sup>. Each tile can be configured as a flip-flop, latch, or 3-input/1-output logic function by programming the

appropriate Flash switches. The combination of fine granularity, flexible routing resources, and abundant Flash switches allow 100% utilization and over 95% routability for highly congested designs. Tiles and larger functions are interconnected through a 4-level routing hierarchy.

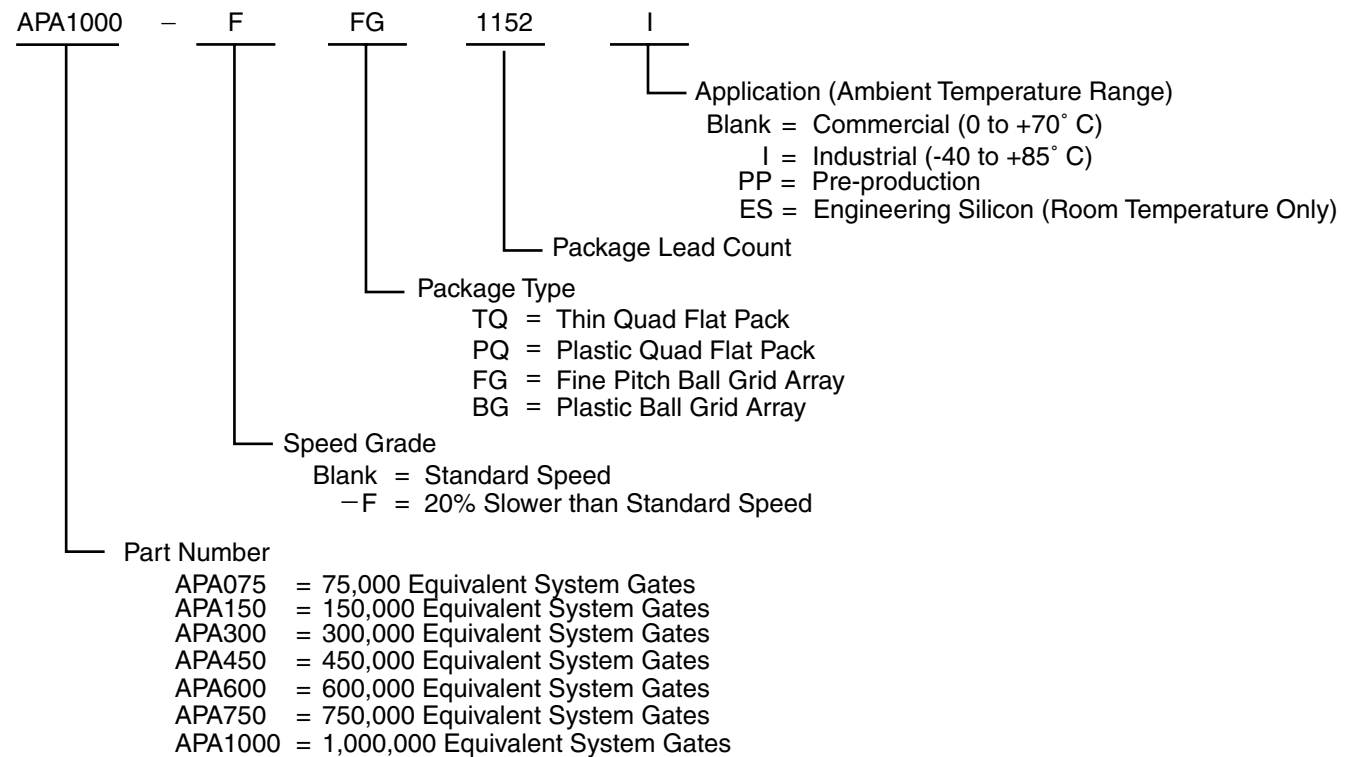
Embedded 2-port SRAM blocks with built-in FIFO/RAM control logic can have user-defined depth and width. Users can also select programming for synchronous or asynchronous operation, as well as parity generations or checking.

The unique clock conditioning circuitry in each device includes two clock conditioning blocks. Each block provides a PLL core, delay lines, phase shifts (0°, 90°, 180°, 270°), and clock multipliers/dividers, as well as the circuitry needed to provide bidirectional access to the PLL. The PLL block contains four programmable frequency dividers, which allow the incoming clock signal to be divided by a wide range of factors from 1 to 64. The clock conditioning circuit also delays or advances the incoming reference clock up to 4 ns (in increments of 0.25 ns). The PLL can be configured internally or externally during operation without redesigning or reprogramming the part. In addition to the PLL, there are two LVPECL differential input pairs to accommodate high speed clock and data inputs.

To support customer needs for more comprehensive, lower cost board-level testing, Actel's ProASIC<sup>PLUS</sup> devices are fully compatible with IEEE Standard 1149.1 for test access port and boundary-scan test architecture. For more information concerning the Flash FPGA implementation, please refer to the "Boundary Scan" section on page 13.

ProASIC<sup>PLUS</sup> devices are available in a variety of high-performance plastic packages. Those packages and the performance features discussed above are described in more detail in the following sections.

## Ordering Information



## Plastic Device Resources

| User I/Os |                 |                 |                 |                 |                 |                 |                 |                 |                  |
|-----------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| Device    | TQFP<br>100-Pin | PQFP<br>208-Pin | PBGA<br>456-Pin | FBGA<br>144-Pin | FBGA<br>256-Pin | FBGA<br>484-Pin | FBGA<br>676-Pin | FBGA<br>896-Pin | FBGA<br>1152-Pin |
| APA075    | 66              | 158             |                 | 100             |                 |                 |                 |                 |                  |
| APA150    | 66              | 158             | 242             | 100             | 186             |                 |                 |                 |                  |
| APA300    |                 | 158             | 290             | 100             | 186             |                 |                 |                 |                  |
| APA450    |                 | 158             | 344             | 100             | 186             | 344             |                 |                 |                  |
| APA600    |                 | 158             | 356             |                 | 186             | 370             | 454             |                 |                  |
| APA750    |                 | 158             | 356             |                 |                 |                 | 454             | 562             |                  |
| APA1000   |                 | 158             | 356             |                 |                 |                 |                 | 642             | 712              |

### Package Definitions

TQFP = Thin Quad Flat Pack, PQFP = Plastic Quad Flat Pack, PBGA = Plastic Ball Grid Array, FBGA = Fine Pitch Ball Grid Array

## Product Availability

|                                            | Speed Grade |     | Application |    |
|--------------------------------------------|-------------|-----|-------------|----|
|                                            | Std.        | -F* | C           | I  |
| <b>APA075 Device</b>                       |             |     |             |    |
| 100-Pin Thin Quad Flat Pack (TQFP)         | ✓           | ✓   | ✓           | ✓  |
| 208-Pin Plastic Quad Flat Pack (PQFP)      | ✓           | ✓   | ✓           | ✓  |
| 144-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| <b>APA150 Device</b>                       |             |     |             |    |
| 100-Pin Thin Quad Flat Pack (TQFP)         | ✓           | ✓   | ✓           | ✓  |
| 208-Pin Plastic Quad Flat Pack (PQFP)      | ✓           | ✓   | ✓           | ✓  |
| 456-Pin Plastic Ball Grid Array (PBGA)     | ✓           | ✓   | ✓           | ✓  |
| 144-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| 256-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| <b>APA300 Device</b>                       |             |     |             |    |
| 208-Pin Plastic Quad Flat Pack (PQFP)      | ✓           | ✓   | ✓           | ✓  |
| 456-Pin Plastic Ball Grid Array (PBGA)     | ✓           | ✓   | ✓           | ✓  |
| 144-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| 256-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| <b>APA450 Device</b>                       |             |     |             |    |
| 208-Pin Plastic Quad Flat Pack (PQFP)      | ✓           | ✓   | ✓           | ✓  |
| 456-Pin Plastic Ball Grid Array (PBGA)     | ✓           | ✓   | ✓           | ✓  |
| 144-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| 256-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| 484-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| <b>APA600 Device</b>                       |             |     |             |    |
| 208-Pin Plastic Quad Flat Pack (PQFP)      | ✓           | ✓   | ✓           | ✓  |
| 456-Pin Plastic Ball Grid Array (PBGA)     | ✓           | ✓   | ✓           | ✓  |
| 256-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| 484-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| 676-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| <b>APA750 Device</b>                       |             |     |             |    |
| 208-Pin Plastic Quad Flat Pack (PQFP)      | ✓           | ✓   | ✓           | ✓  |
| 456-Pin Plastic Ball Grid Array (PBGA)     | ✓           | ✓   | ✓           | ✓  |
| 676-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| 896-Pin Plastic Ball Grid Array (FBGA)     | ✓           | ✓   | ✓           | ✓  |
| <b>APA1000 Device</b>                      |             |     |             |    |
| 208-Pin Plastic Quad Flat Pack (PQFP)      | ✓           | ✓   | ✓           | ✓  |
| 456-Pin Plastic Ball Grid Array (PBGA)     | ✓           | ✓   | ✓           | ✓  |
| 896-Pin Fine Pitch Ball Grid Array (FBGA)  | ✓           | ✓   | ✓           | ✓  |
| 1152-Pin Fine Pitch Ball Grid Array (FBGA) | PQ          | PQ  | PQ          | PQ |

**Note:** \*-F parts are only available as commercial temperature devices.

Applications: C = Commercial    Availability: ✓ = Available  
I = Industrial    PQ = Pending Qualification

## ProASIC<sup>PLUS</sup> Architecture

The proprietary ProASIC<sup>PLUS</sup> architecture provides granularity comparable to gate arrays.

The ProASIC<sup>PLUS</sup> device core consists of a Sea-of-Tiles™ (Figure 1). Each tile can be configured as a 3-input logic function (e.g., NAND gate, D-Flip-Flop, etc.) by programming the appropriate Flash switch interconnections (Figure 2 on page 6 and Figure 3 on page 6). Tiles and larger functions are connected with any of the four levels of routing hierarchy. Flash cells are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Flash switches are programmed to connect signal lines to the appropriate logic cell inputs and outputs. Dedicated high-performance lines are connected as needed for fast, low-skew global signal distribution throughout the core. Maximum core utilization is possible for virtually any design.

ProASIC<sup>PLUS</sup> devices also contain embedded two-port SRAM blocks with built-in FIFO/RAM control logic. Programming options include synchronous or asynchronous operation, two-port RAM configurations, user defined depth and width, and parity generation or checking. Please see

the “Embedded Memory Configurations” section on page 21 for more information.

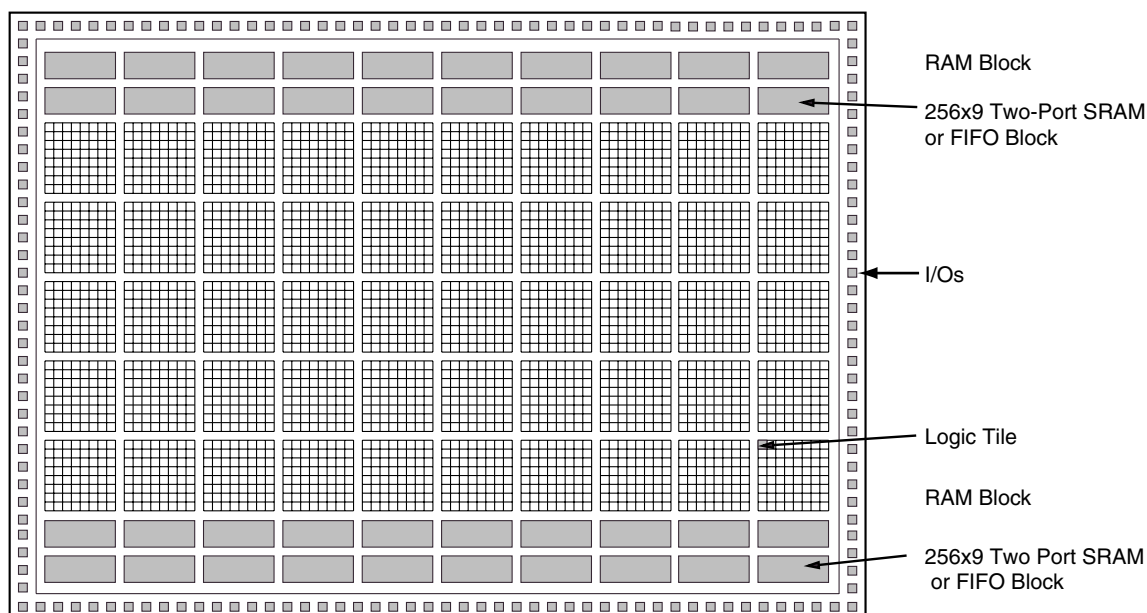
### Flash Switch

Unlike SRAM FPGAs, ProASIC<sup>PLUS</sup> uses a live on power-up ISP Flash switch as its programming element.

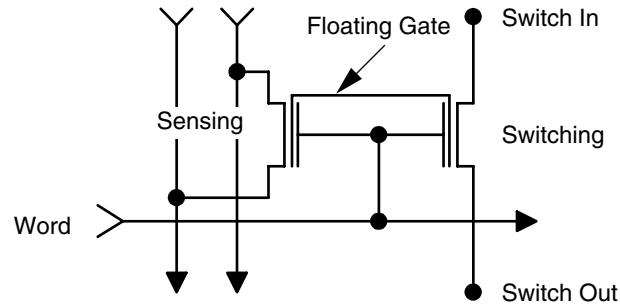
In the ProASIC<sup>PLUS</sup> Flash switch, two transistors share the floating gate, which stores the programming information. One is the sensing transistor, which is only used for writing and verification of the floating gate voltage. The other is the switching transistor. It can be used in the architecture to connect/separate routing nets or to configure logic. It is also used to erase the floating gate (Figure 2 on page 6).

### Logic Tile

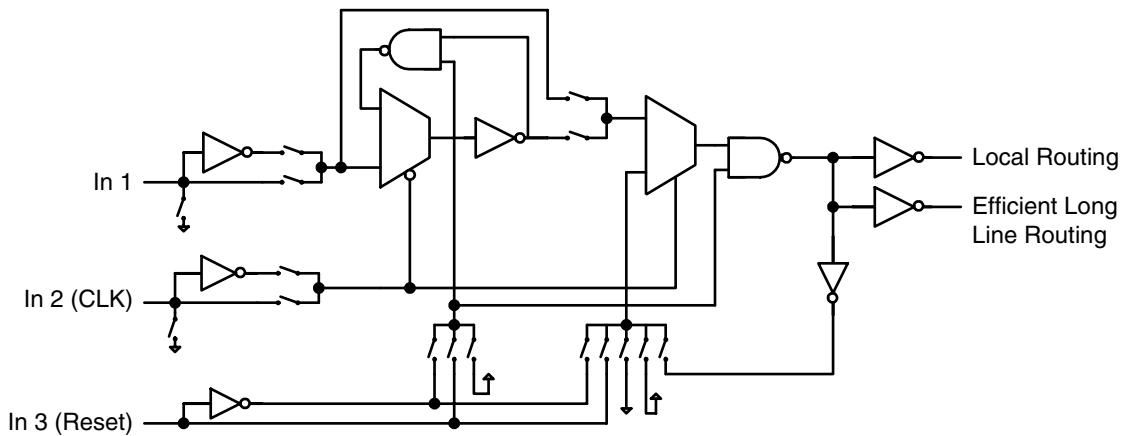
The logic tile cell (Figure 3 on page 6) has three inputs (any or all of which can be inverted) and one output (which can connect to both ultra fast local and efficient long line routing resources). Any three-input, one-output logic function (except a three input XOR) can be configured as one tile. The tile can be configured as a latch with clear or set or as a flip-flop with clear or set. Thus, the tiles can flexibly map logic and sequential gates of a design.



**Figure 1** • The ProASIC<sup>PLUS</sup> Device Architecture



**Figure 2 • Flash Switch**



**Figure 3 • Core Logic Tile**

### Routing Resources

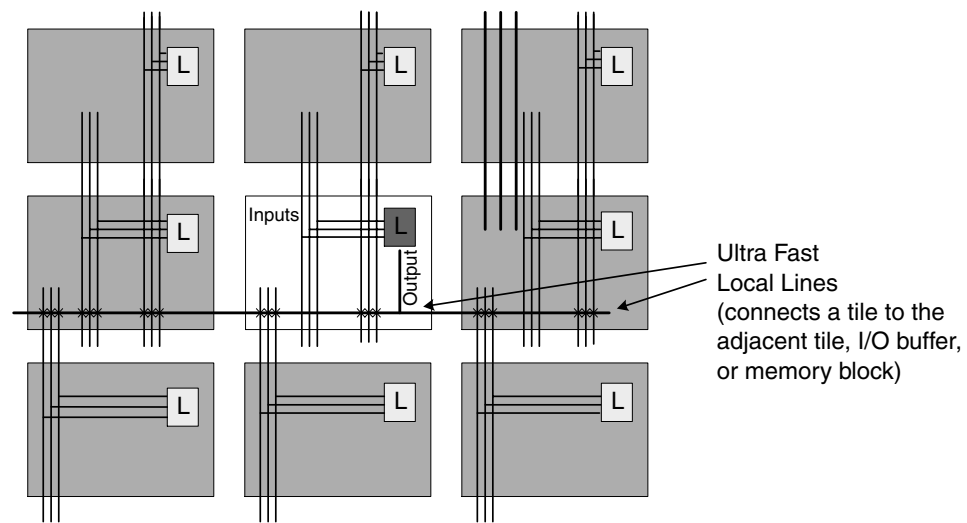
The routing structure of the ProASIC<sup>PLUS</sup> devices is designed to provide high performance through a flexible four-level hierarchy of routing resources: ultra fast local resources, efficient long line resources, high speed very long line resources, and high performance global networks.

The ultra-fast local resources are dedicated lines that allow the output of each tile to connect directly to every input of the eight surrounding tiles (Figure 4 on page 7).

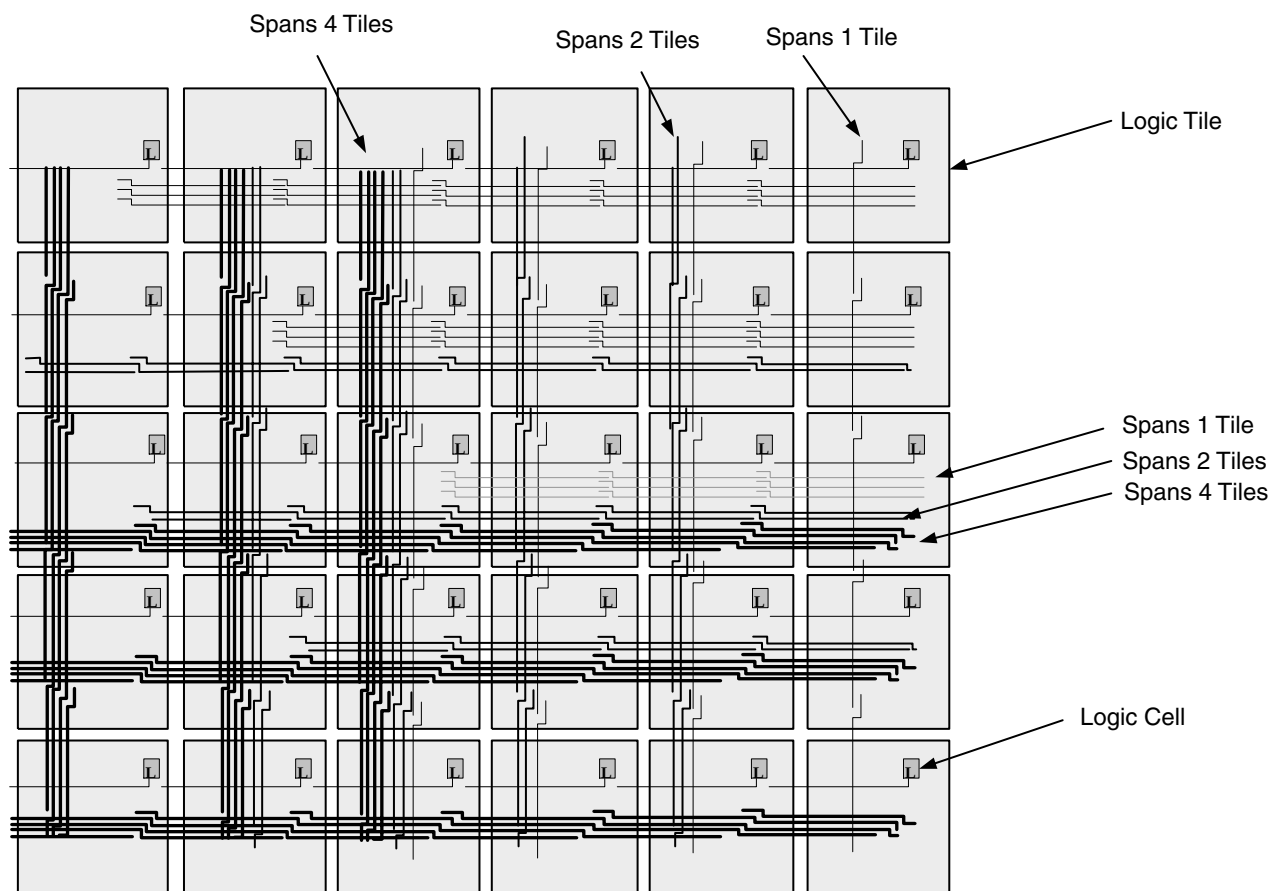
The efficient long line resources provide routing for longer distances and higher fanout connections. These resources vary in length (spanning 1, 2, or 4 tiles), run both vertically and horizontally, and cover the entire ProASIC<sup>PLUS</sup> device (Figure 5 on page 7). Each tile can drive signals onto the efficient long line resources, which can in turn, access every input of every tile. Active buffers are inserted automatically by routing software to limit the loading effects due to distance and fanout.

The high-speed very long line resources, which span the entire device with minimal delay, are used to route very long or very high fanout nets. (Figure 6 on page 8).

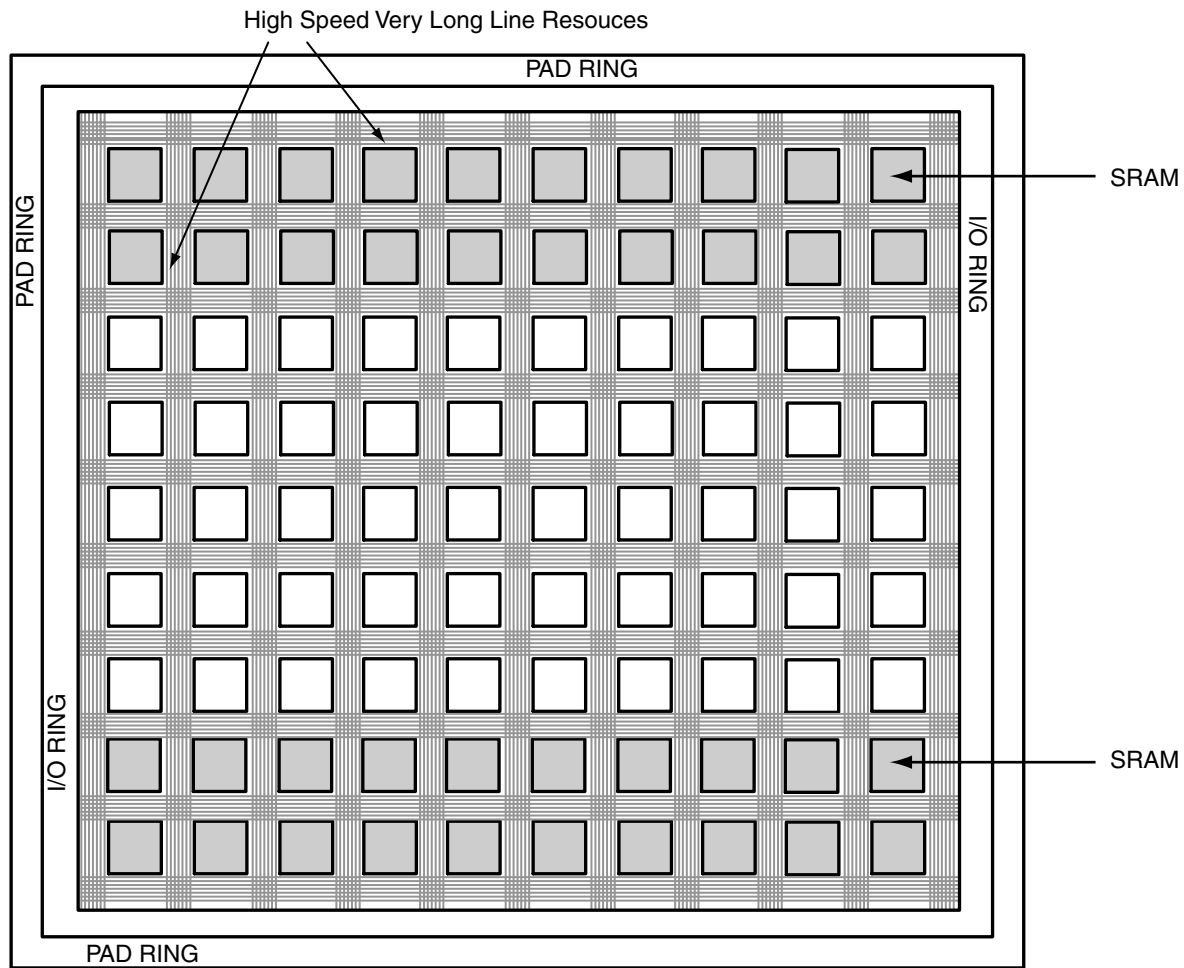
The high-performance global networks are low skew, high fanout nets that are accessible from external pins or from internal logic (Figure 7 on page 9). These nets are typically used to distribute clocks, resets, and other high fanout nets requiring a minimum skew. The global networks are implemented as clock trees, and signals can be introduced at any junction. These can be employed hierarchically with signals accessing every input on all tiles.



**Figure 4 • Ultra Fast Local Resources**



**Figure 5 • Efficient Long Line Resources**



**Figure 6 • High Speed Very Long Line Resources**



## Clock Resources

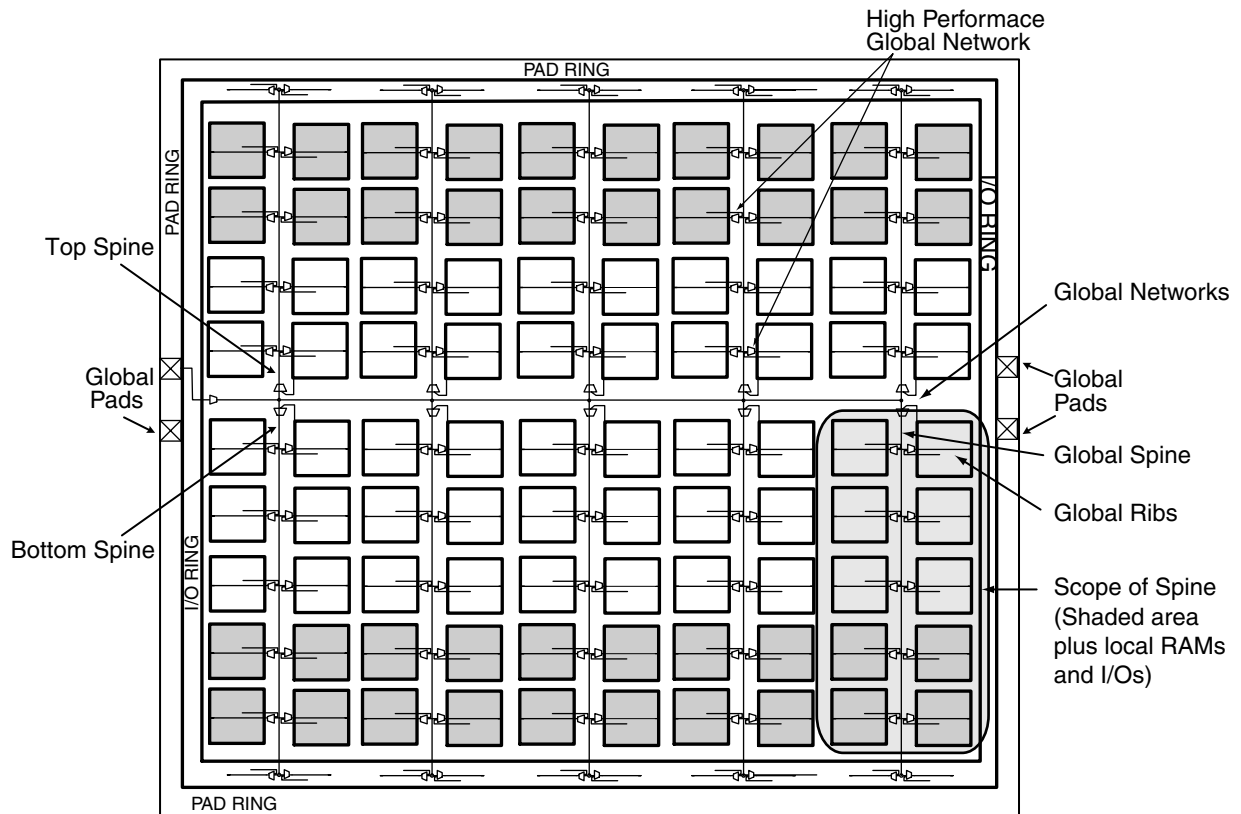
The ProASIC<sup>PLUS</sup> family offers powerful and flexible control of circuit timing through the use of analog circuitry. Each chip has two clock conditioning blocks containing a phase-locked loop (PLL) core, delay lines, phase shifter (0°, 90°, 180°, 270°), clock multiplier/dividers and all the circuitry needed for the selection and interconnection of inputs to the global network (thus providing bidirectional access to the PLL). This permits the PLL block to drive inputs and/or outputs via the two global lines on each side of the chip (four total lines). This circuitry is discussed in more detail in the “APA Clock Management System” section on page 15.

## Clock Trees

One of the main architectural benefits of ProASIC<sup>PLUS</sup> is the set of power and delay friendly global networks. ProASIC<sup>PLUS</sup> offers 4 global trees. Each of these trees is

based on a network of spines and ribs that reach all the tiles in their regions (Figure 7). This flexible clock tree architecture allows users to map up to 88 different internal/external clocks in an APA1000 device. Details on the clock spines and various numbers of the family are given in Table 1 on page 10.

The flexible use of the ProASIC<sup>PLUS</sup> clock spine allows the designer to cope with several design requirements. Users implementing clock resource intensive applications can easily route external or gated internal clocks using global routing spines. Users can also drastically reduce delay penalties and save buffering resources by mapping critical high-fanout nets to spines. For design hints on using these features, refer to Actel's *Efficient Use of ProASIC Clock Trees* application note.



**Note:** This figure shows routing for only one global path.

**Figure 7 • High Performance Global Network**

**Table 1 • Clock Spines**

|                               | APA075 | APA150 | APA300 | APA450 | APA600 | APA750 | APA1000 |
|-------------------------------|--------|--------|--------|--------|--------|--------|---------|
| Top Spine Height Tiles        | 16     | 24     | 32     | 32     | 48     | 64     | 80      |
| Tiles in Each Top Spine       | 512    | 768    | 1,024  | 1,024  | 1,536  | 2,048  | 2,560   |
| Bottom Spine Height           | 16     | 24     | 32     | 32     | 48     | 64     | 80      |
| Tiles in Each Bottom Spine    | 512    | 768    | 1,024  | 1,024  | 1,536  | 2,048  | 2,560   |
| Global Clock Networks (Trees) | 4      | 4      | 4      | 4      | 4      | 4      | 4       |
| Clock Spines/Tree             | 6      | 8      | 8      | 12     | 14     | 16     | 22      |
| Total Spines                  | 24     | 32     | 32     | 48     | 56     | 64     | 88      |
| Total Tiles                   | 3,072  | 6,144  | 8,192  | 12,288 | 21,504 | 32,768 | 56,320  |

### Array Coordinates

During many place-and-route operations in Actel's Designer software tool, it is possible to set constraints that require array coordinates.

Table 2 is provided as a reference. The array coordinates are measured from the lower left (0,0). They can be used in region constraints for specific groups, designated by a wildcard, and containing core cells, I/Os and memories.

The IO coordinates have a North, East, West and South (N E W S) side and an offset, which starts at 1 and increases from left to right or from bottom to top. The corner I/Os belong to the North or the South side. These coordinates are used in fixed placement constraints.

Core cell coordinates start at the lower left corner (1,1) or (1,5) if memories are present at the bottom. Memory coordinates use the same system and are indicated in Table 2. For more information on how to use constraints, see the *Designer* user's guide for ProASIC<sup>PLUS</sup> software tools.

**Table 2 • Array Coordinates**

| Device  | Logic Tile |   |      |     | Memory Rows |          | All  |          |
|---------|------------|---|------|-----|-------------|----------|------|----------|
|         | Min.       |   | Max. |     | Bottom      | Top      |      |          |
|         | x          | y | x    | y   | y           | y        | Min. | Max.     |
| APA075  | 1          | 1 | 96   | 32  | –           | 33, 35   | 0,0  | 97, 37   |
| APA150  | 1          | 1 | 128  | 48  | –           | 49, 51   | 0,0  | 129, 53  |
| APA300  | 1          | 5 | 128  | 68  | 1, 3        | 69, 71   | 0,0  | 129, 73  |
| APA450  | 1          | 5 | 192  | 68  | 1, 3        | 69, 71   | 0,0  | 193, 73  |
| APA600  | 1          | 5 | 224  | 100 | 1, 3        | 101, 103 | 0,0  | 225, 105 |
| APA750  | 1          | 5 | 256  | 132 | 1, 3        | 133, 135 | 0,0  | 257, 137 |
| APA1000 | 1          | 5 | 352  | 164 | 1, 3        | 165, 167 | 0,0  | 353, 169 |

## Input/Output Blocks

To meet complex system demands, the ProASIC<sup>PLUS</sup> family offers devices with a large number of user I/O pins, up to 712 on the APA1000. If the I/O pad powers  $V_{DDP}$  at 3.3V, each I/O can be selectively configured at the 2.5V and 3.3V threshold levels. Table 3 shows the available supply voltage configurations (the PLL block uses an independent 2.5V supply on the AVDD and AGND pins). All I/Os include ESD protection circuits. Each I/O has been tested to 2000V to the human body model (per JESD22 (HMB)).

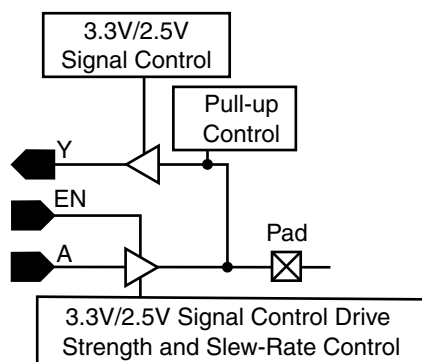
Six or seven standard I/O pads are grouped with a GND pad and either a  $V_{DD}$  or  $V_{DDP}$  pad. Two reference bias signals circle the chip. One protects the cascaded output drivers while the other creates a virtual  $V_{DD}$  supply for the I/O ring.

I/O pads are fully configurable to provide the maximum flexibility and speed. Each pad can be configured as an input, an output, a tristate driver, or a bidirectional buffer (Figure 8 and Table 4 on page 12).

**Table 3 • ProASIC<sup>PLUS</sup> Power Supply Voltages**

|                     | $V_{DDP}$ |            |
|---------------------|-----------|------------|
|                     | 2.5V      | 3.3V       |
| Input Compatibility | 2.5V      | 3.3V, 2.5V |
| Output Drive        | 2.5V      | 3.3V, 2.5V |

**Note:**  $V_{DD}$  is always 2.5V.



**Figure 8 • I/O Block Schematic Representation**

## Power-up Sequencing

While ProASIC<sup>PLUS</sup> devices are live at power-up, the order of  $V_{DD}$  and  $V_{DDP}$  power-up is important during system start-up.  $V_{DD}$  should be powered up before (or coincident with)  $V_{DDP}$  on ProASIC<sup>PLUS</sup> devices. Failure to follow these guidelines may result in undesirable pin behavior during system start-up.

## LVPECL Input Pads

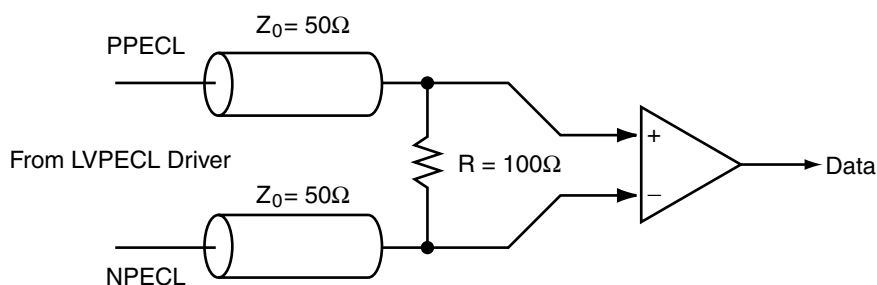
In addition to standard I/O pads and power pads, ProASIC<sup>PLUS</sup> devices have a LVPECL input pad on the east and west sides of the device, along with AVDD and AGND pins to power the PLL block. The LVPECL input pad cell differs from the standard I/O cell. It is operated from  $V_{DD}$  only. Since it is exclusively an input, it requires no output signal, output enable signal, or output configuration bits. As a special high-speed differential input, it also does not require pull ups.

The LVPECL pad cell consists of an input buffer (containing a low voltage differential amplifier) and a signal and its complement, PPECL (I/P) (PECLN) and NPECL (PECLREF). Recommended termination for LVPECL inputs is shown in Figure 9 on page 12. The LVPECL pad cell compares voltages on the PPECL (I/P) pad and the NPECL pad and sends the results to the global MUX (Figure 12 on page 16). This high speed, low skew output essentially controls the clock conditioning circuit.

LVPECLs are designed to meet LVPECL JEDEC receiver standard levels (Table 5 on page 12).

**Table 4 • I/O Features**

| Function                                                                  | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |
|---------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| I/O pads configured as inputs have the following features:                | <ul style="list-style-type: none"> <li>Individually selectable 2.5V or 3.3V threshold levels</li> <li>Optional pull-up resistor</li> <li>Optionally configurable as Schmitt trigger input. The Schmitt trigger input option can be configured as an input only, not a bidirectional buffer. This input type may be slower than a standard input under certain conditions and has typical hysteresis of 0.35V. I/O macros with an "S" in the standard I/O library have added Schmitt capabilities</li> <li>3.3V PCI Compliant</li> </ul>   |
| I/O pads configured as outputs have the following features:               | <ul style="list-style-type: none"> <li>Individually selectable 2.5V or 3.3V compliant output signals. If pads are configured for 2.5V operation, they are compliant with 2.5V level signals as defined by JEDEC JESD 8-5. If pads are configured for 3.3V operation, they are compliant with the standard as defined by JEDEC JESD 8-A (LVTTTL and LVCMOS)</li> <li>3.3V PCI compliant</li> <li>Ability to drive LVTTTL and LVCMOS levels</li> <li>Selectable drive strengths</li> <li>Selectable slew rates</li> <li>Tristate</li> </ul> |
| I/O pads configured as bidirectional buffers have the following features: | <ul style="list-style-type: none"> <li>Individually selectable 2.5V or 3.3V output signals and threshold levels. If pads are configured for 2.5V operation, they are compliant with 2.5V level signals as defined by JEDEC JESD 8-5. If pads are configured for 3.3V operation, they are compliant with the standard as defined by JEDEC JESD 8-A (LVTTTL and LVCMOS)</li> <li>3.3V PCI compliant</li> <li>Optional pull-up resistor</li> <li>Selectable drive strengths</li> <li>Selectable slew rates</li> <li>Tristate</li> </ul>      |


**Figure 9 • Recommended Termination for LVPECL Inputs**
**Table 5 • LVPECL Receiver Specifications**

| Symbol          | Parameter                  | Min. | Max             | Units |
|-----------------|----------------------------|------|-----------------|-------|
| V <sub>IH</sub> | Input High Voltage         | 1.49 | 2.72            | V     |
| V <sub>IL</sub> | Input Low Voltage          | 0.86 | 2.125           | V     |
| V <sub>ID</sub> | Differential Input Voltage | 0.3  | V <sub>DD</sub> | V     |

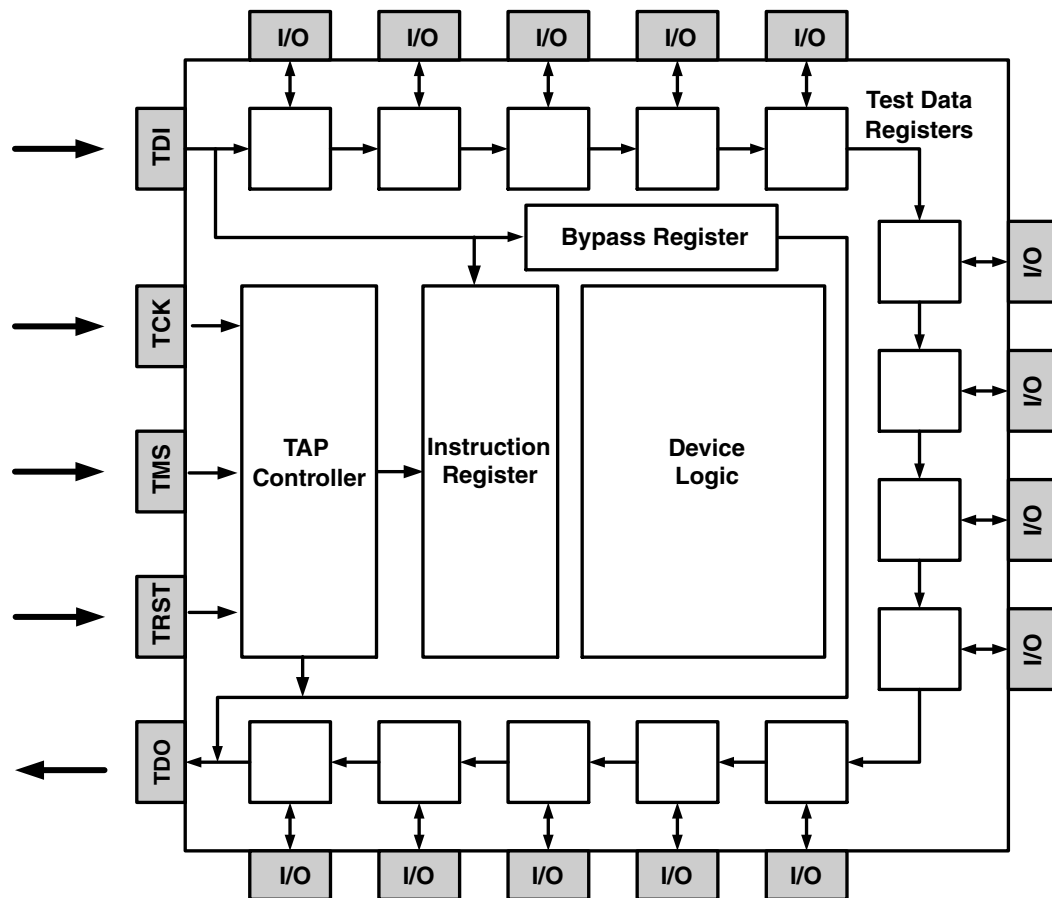
## Boundary Scan

ProASIC<sup>PLUS</sup> devices are compatible with IEEE Standard 1149.1, which defines a set of hardware architecture and mechanisms for cost-effective board-level testing. The basic ProASIC<sup>PLUS</sup> boundary-scan logic circuit is composed of the TAP (test access port), TAP controller, test data registers, and instruction register (Figure 10). This circuit supports all mandatory IEEE 1149.1 instructions (EXTEST, SAMPLE/PRELOAD and BYPASS) and the optional IDCODE instruction (Table 6).

Each test section is accessed through the TAP, which has five associated pins: TCK (test clock input), TDI and TDO

(test data input and output), TMS (test mode selector) and TRST (test reset input). TMS, TDI and TRST are equipped with pull-up resistors to ensure proper operation when no input data is supplied to them. These pins are dedicated for boundary-scan test usage.

The TAP controller is a four-bit state machine (16 states) that operates as shown in Figure 11 on page 14. The '1's and '0's represent the values that must be present at TMS at a rising edge of TCK for the given state transition to occur. IR and DR indicate that the instruction register or the data register is operating in that state.



**Figure 10** • ProASIC<sup>PLUS</sup> JTAG Boundary Scan Test Logic Circuit

**Table 6** • Boundary-Scan Opcodes

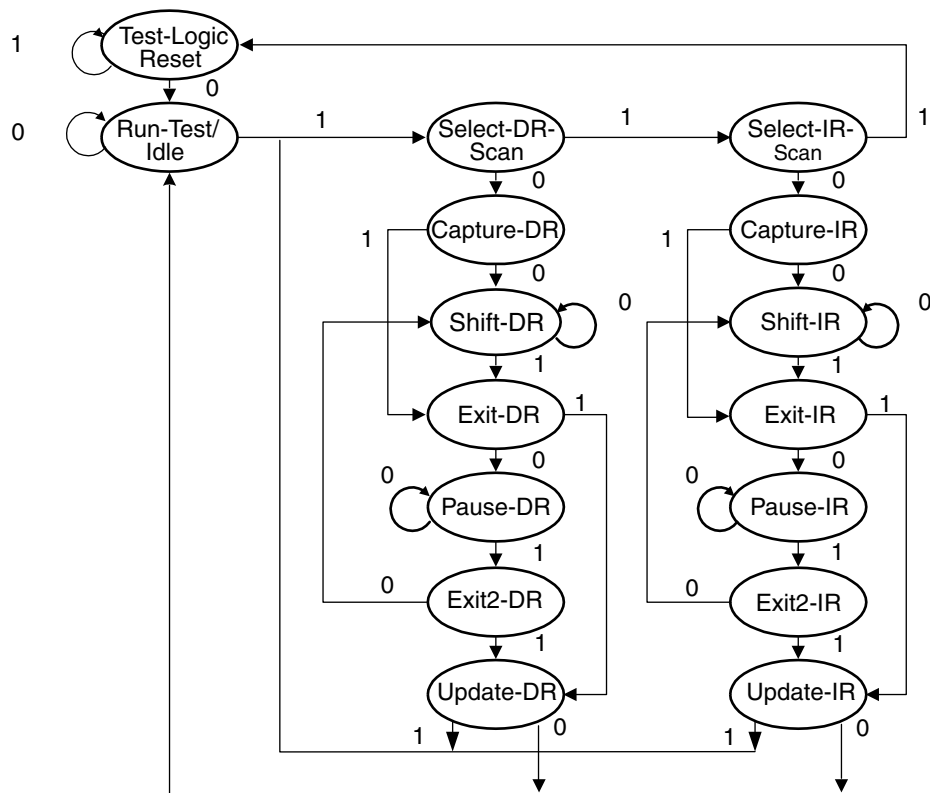
|                | Hex Opcode |
|----------------|------------|
| EXTEST         | 00         |
| SAMPLE/PRELOAD | 01         |
| IDCODE         | 0F         |
| CLAMP          | 05         |
| BYPASS         | FF         |

The TAP controller receives two control inputs (TMS and TCK) and generates control and clock signals for the rest of the test logic architecture. On power-up, the TAP controller enters the Test-Logic-Reset state. To guarantee a reset of the controller from any of the possible states, TMS must remain high for five TCK cycles. The TRST pin may also be used to asynchronously place the TAP controller in the Test-Logic-Reset state.

ProASIC<sup>PLUS</sup> devices support three types of test data registers: bypass, device identification, and boundary scan. The bypass register is selected when no other register needs to be accessed in a device. This speeds up test data transfer to other devices in a test data path. The 32-bit device

identification register is a shift register with four fields (LSB, ID number, part number and version). The boundary-scan register observes and controls the state of each I/O pin.

Each I/O cell has three boundary-scan register cells, each with a serial-in, serial-out, parallel-in, and parallel-out pin. The serial pins are used to serially connect all the boundary-scan register cells in a device into a boundary scan register chain, which starts at the TDI pin and ends at the TDO pin. The parallel ports are connected to the internal core logic tile and the input, output, and control ports of an I/O buffer to capture and load data into the register to control or observe the logic state of each I/O.



**Figure 11 • TAP Controller State Diagram**

## Timing Control and Characteristics

### APA Clock Management System

#### Introduction

ProASIC<sup>PLUS</sup> devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC<sup>PLUS</sup> family contains two phase-locked loop (PLL) blocks which perform the following functions:

- Clock Phase Adjustment via Programmable Delay (250 ps steps from -4 ns to +8 ns)
- Clock Skew Minimization
- Clock Frequency Synthesis

Each PLL has the following key features:

- Input Frequency Range ( $f_{IN}$ ) = 1.5 to 180 MHz
- Feedback Frequency Range ( $f_{VCO}$ ) = 1.5 to 180 MHz
- Output Frequency Range ( $f_{OUT}$ ) = 6 to 180 MHz
- Output Phase Shift = 0°, 90°, 180°, and 270°
- Output Duty Cycle = 50%
- Low Output Jitter (max at 25° C)
  - $f_{VCO} < 10$  MHz. Jitter  $\pm 1\%$  or better
  - $10 \text{ MHz} < f_{VCO} < 60$  MHz. Jitter  $\pm 2\%$  or better
  - $f_{VCO} > 60$  MHz. Jitter  $\pm 1\%$  or better
- Maximum Acquisition Time = 80  $\mu$ s
- Low Power Consumption – 6.9 mW (max – analog supply) + 7.0  $\mu$ W/MHz (max – digital supply)

#### Physical Implementation

Each side of the chip contains a clock conditioning circuit based upon a 180 MHz phase-locked loop (PLL) block (Figure 12 on page 16). Two global multiplexed lines extend along each side of the chip to provide bidirectional access to the PLL on that side (neither MUX can be connected to the opposite side's PLL). Each global line has optional LVPECL input pads (described below). The global lines may be driven by either the LVPECL global input pad or the outputs from the PLL block or both. Each global line can be driven by a different output from the PLL. The two signals available to drive the global networks are as follows (Figure 13 on page 17):

#### Global A

- Output from Global MUX A
- Conditioned version of PLL output ( $f_{OUT}$ )
  - Delayed or advanced
  - 0°, 90°, 180°, and 270° phase shift (with optional time advance)
- Divided version of either of the above

- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)<sup>1</sup>

#### Global B

- Output from Global MUX B
- Delayed or advanced version of  $f_{OUT}$
- Divided version of either of the above
- Further delayed version of either of the above (0.25 ns, 0.50 ns, or 4.00 ns delay)<sup>1</sup>

#### Functional Description

Each PLL block contains four programmable dividers as shown in Figure 12 on page 16. These allow frequency scaling of the input clock signal as follows:

- The n divider divides the input clock by integer factors from 1 to 16.
- The m divider in the feedback path allows multiplication of the input clock by integer factors ranging from 1 to 6.
- The two dividers together can implement any combination of multiplication and division resulting in a clock frequency between 24 and 240 MHz exiting the PLL core. This clock has a fixed 50% duty cycle.
- The output frequency of the PLL core is given by the following formula ( $f_{REF}$  is the reference clock frequency):
 
$$f_{OUT} = f_{REF} * (\text{DividerM})/(\text{DividerN})$$
- The third and fourth dividers (u and v) permit the signals applied to the global network to each be further divided by integer factors ranging from 1 to 4.

The implementations:

$$f_{GLB} = \text{DividerM}/(\text{DividerN} * \text{DividerU})$$

$$f_{GLA} = \text{DividerM}/(\text{DividerN} * \text{DividerV})$$

enable the user to define a wide range of frequency multipliers and divisors. The clock conditioning circuit can advance or delay the clock up to 4 ns (in increments of 0.25 ns) relative to the positive edge of the incoming reference clock. The system also allows for the selection of output frequency clock phases of 0°, 90°, 180°, and 270°.

Prior to the application of signals to the rib drivers, they pass through programmable delay units, one per global network. These units permit the delaying of global signals relative to other signals to assist in the control of input set-up times. Not all possible combinations of input and output modes can be used. The degrees of freedom available in the bidirectional global pad system and in the clock conditioning circuit have been restricted. This avoids unnecessary and unwieldy design kit and software work.

<sup>1</sup> This mode is available through the delay feature of the Global MUX driver.

### Lock Signal

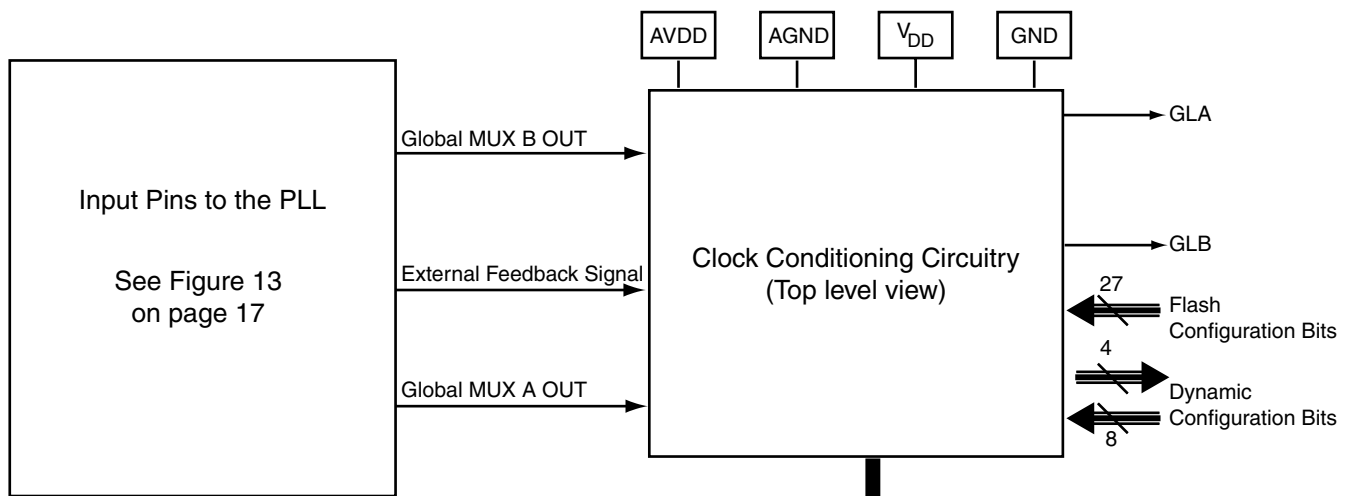
A Lock signal (Active High) is provided (using the ACTgen PLL development tool) to indicate that the PLL has locked to the incoming clock signal. Users can employ the Lock signal as a soft reset of the logic driven by GLB and/or GLA.

### PLL Configuration Options

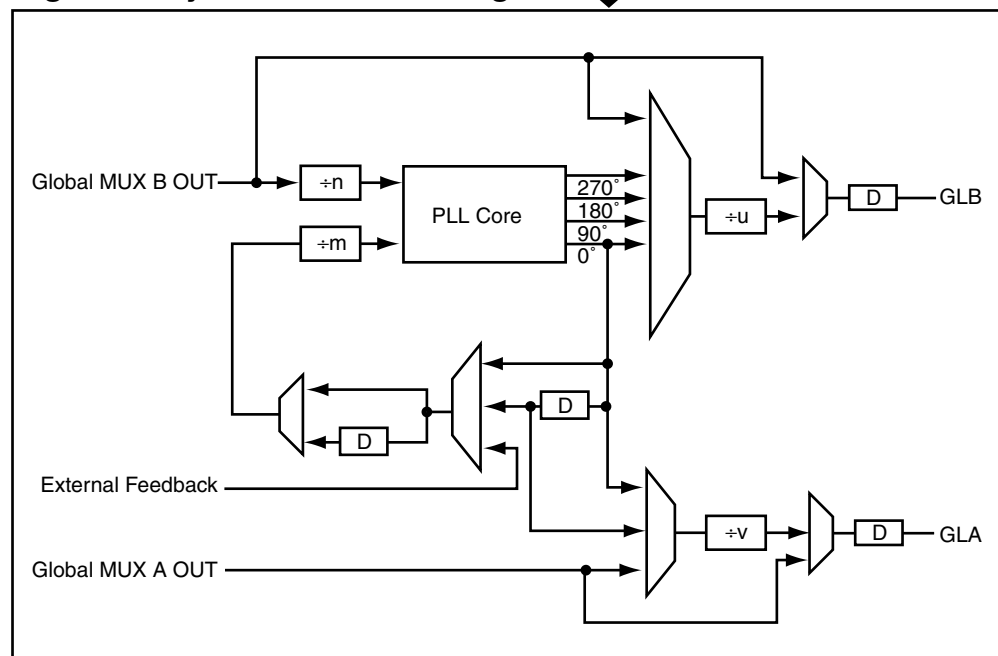
The PLL can be configured during design (via Flash-configuration bits set in the programming bitstream) or dynamically during device operation, thus eliminating the need for complete reprogramming. The dynamic configuration bits are loaded into a serial-in/parallel-out

shift register provided in the clock conditioning circuit of each PLL and then latched into the PLL block. The JTAG ports can be used along with built-in user JTAG interface hardware to load the configuration shift register externally. Another option is internal dynamic configuration via user-designed hardware. Refer to Actel's *ProASIC<sup>PLUS</sup> PLL Dynamic Reconfiguration Using JTAG* application note for more information.

For information on the clock conditioning circuit, refer to the, Actel's *Using ProASIC<sup>PLUS</sup> Clock Conditioning Circuits* application note.

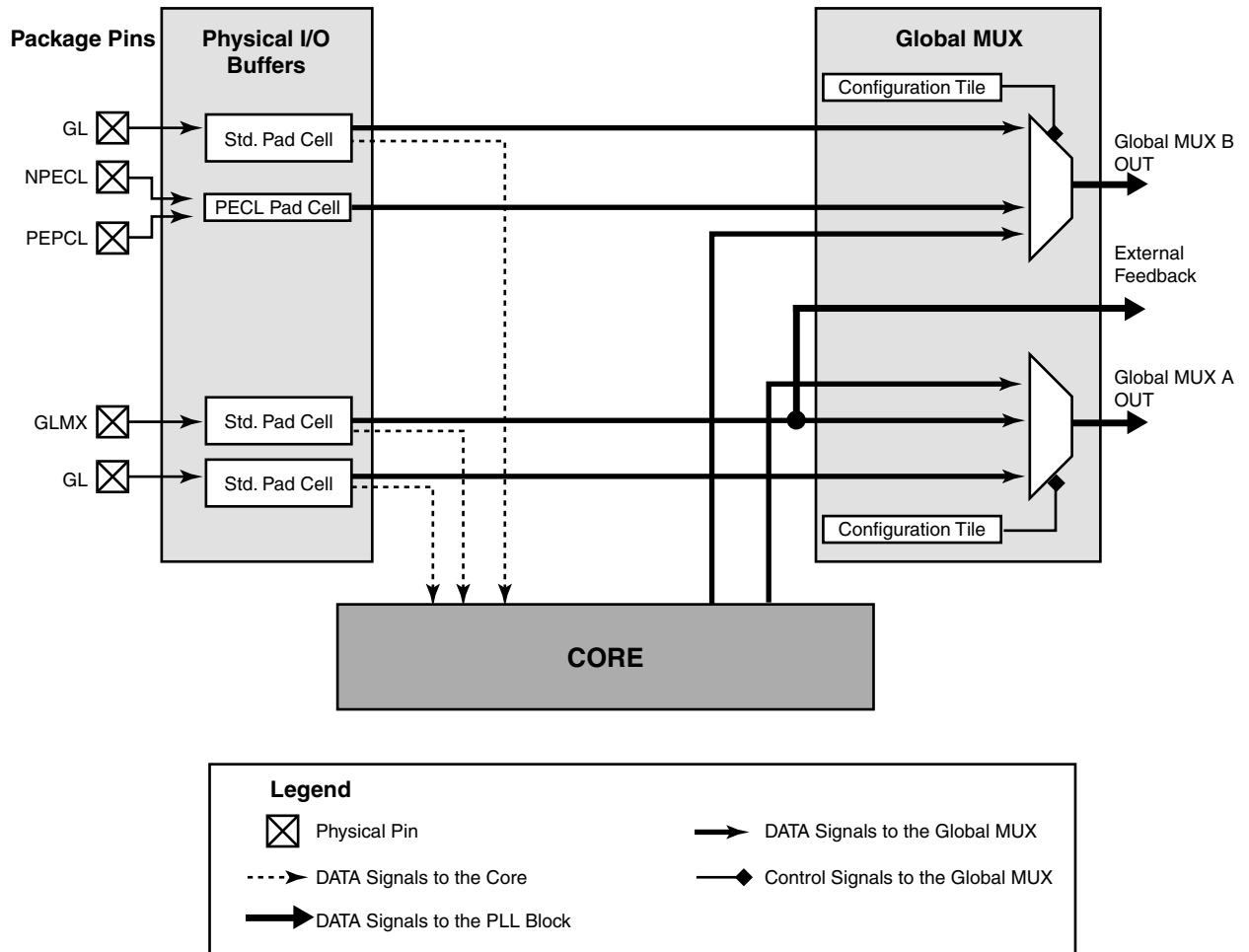


### Clock Conditioning Circuitry Detailed Block Diagram



**Figure 12 • PLL Block – Top-Level View and Detailed PLL Block Diagram**





**Note:** When a signal from an I/O tile is connected to the core, it cannot be connected to the Global MUX at the same time.

**Figure 13 • Input Connectors to ProASIC<sup>PLUS</sup> Clock Conditioning Circuitry**

## Sample Implementations

### Frequency Synthesis

Figure 14 on page 18 illustrates an example where the PLL is used to multiply a 33 MHz external clock up to 133 MHz. Figure 15 on page 18 uses two dividers to synthesize a 50 MHz output clock from a 40 MHz input reference clock. The input frequency of 40 MHz is multiplied by 5 and divided by 4, giving an output clock (GLB) frequency of 50 MHz. When dividers are used, a given ratio can be generated in multiple ways, allowing the user to stay within the operating frequency ranges of the PLL. For example, in this case the input divider could have been 2 and the output divider also 2, giving us a division of the input frequency by 4 to go with the feedback loop division (effective multiplication) by 5.

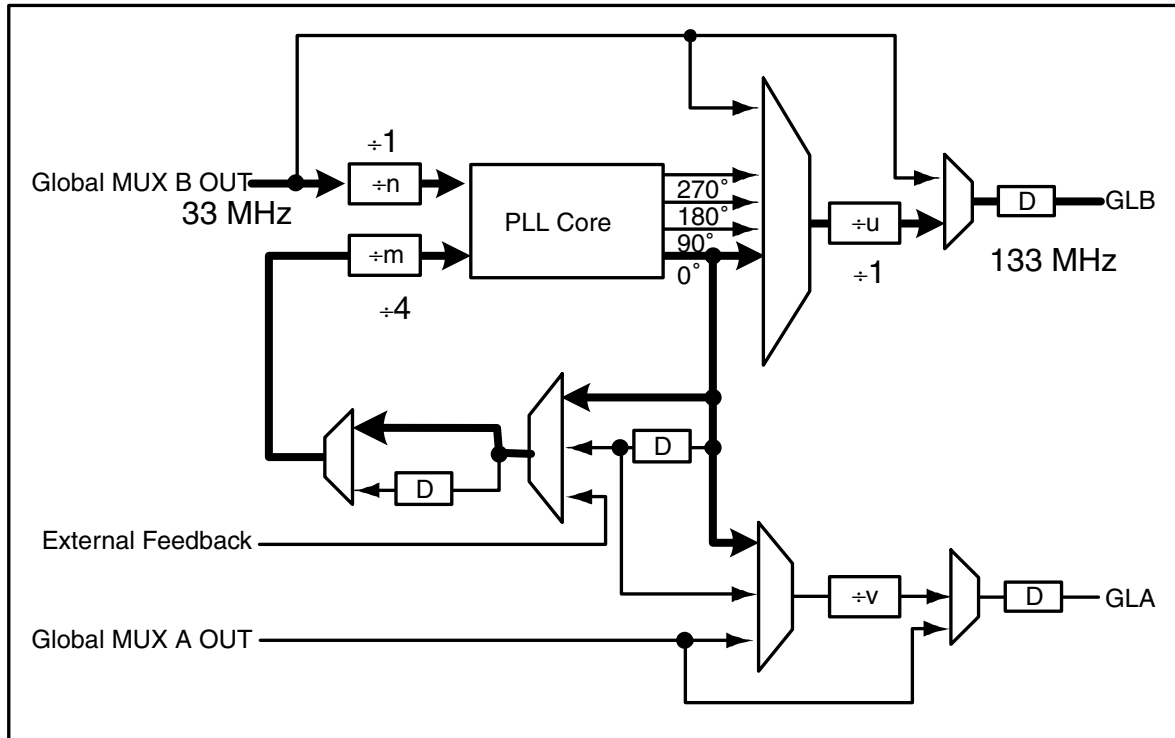
### Adjustable Clock Delay

Figure 16 on page 19 illustrates the delay of the input clock by employing one of the adjustable delay lines. This is easily

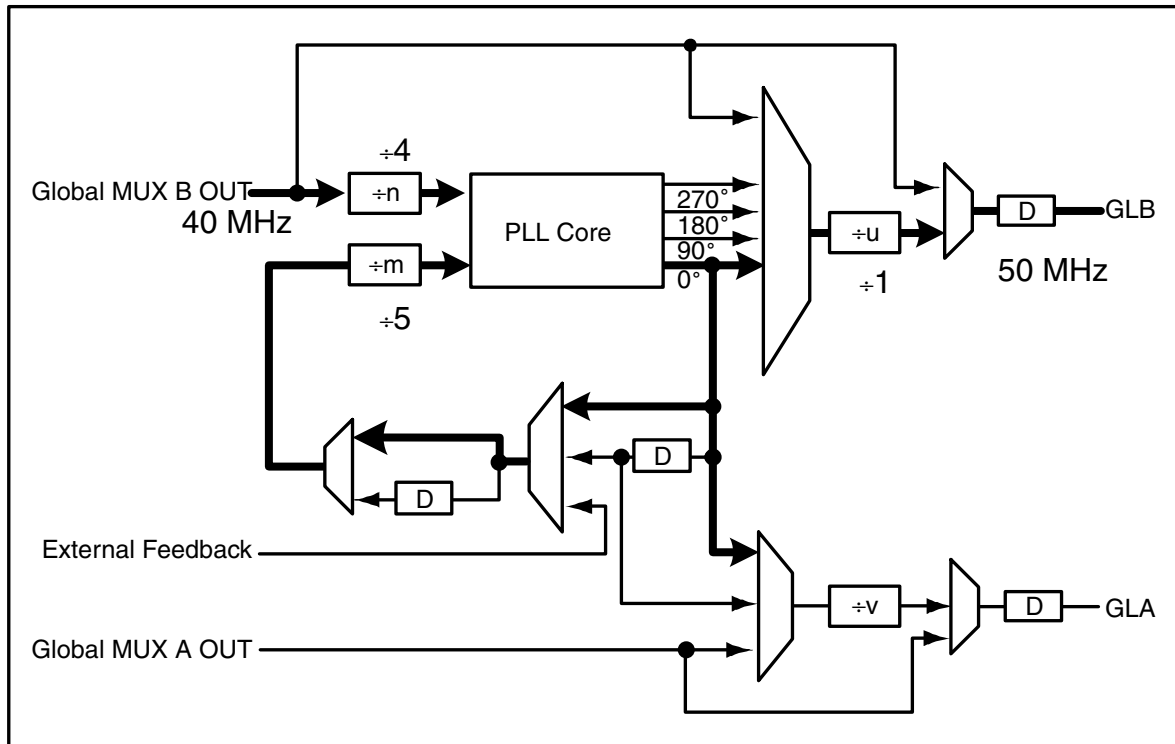
done in ProASIC<sup>PLUS</sup> by bypassing the PLL core entirely and using the output delay line. Notice also that the output clock can be effectively advanced relative to the input clock by using the delay line in the feedback path. This is shown in Figure 17 on page 19.

### Clock Skew Minimization

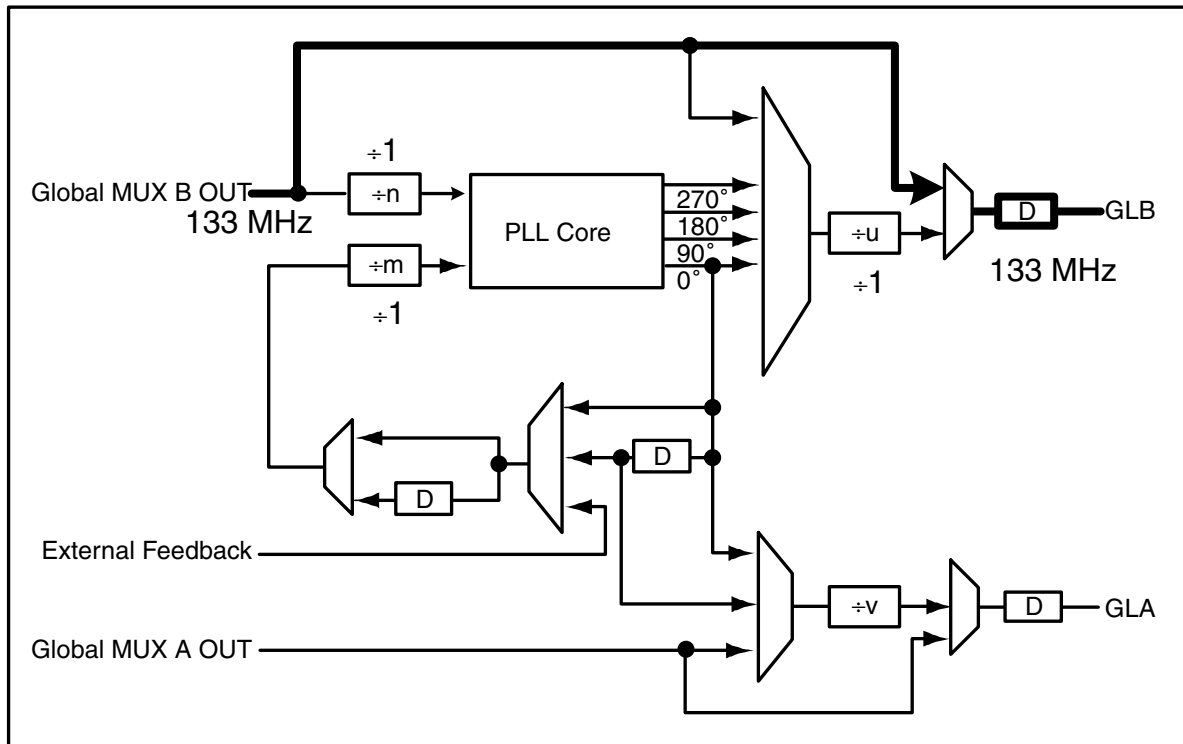
Figure 18 on page 20 indicates how feedback from the clock network can be used to create minimal skew between the distributed clock network and the "input" clock. The input clock is fed to the reference clock input of the PLL. The output clock (GLA) feeds a clock network. The feedback input to the PLL uses a clock input delayed by a routing network. The PLL then adjusts the phase of the input clock to match the delayed clock, thus providing nearly zero effective skew between the two clocks. Refer to Actel's *Using ProASIC<sup>PLUS</sup> Clock Conditioning Circuits* application note for more information.



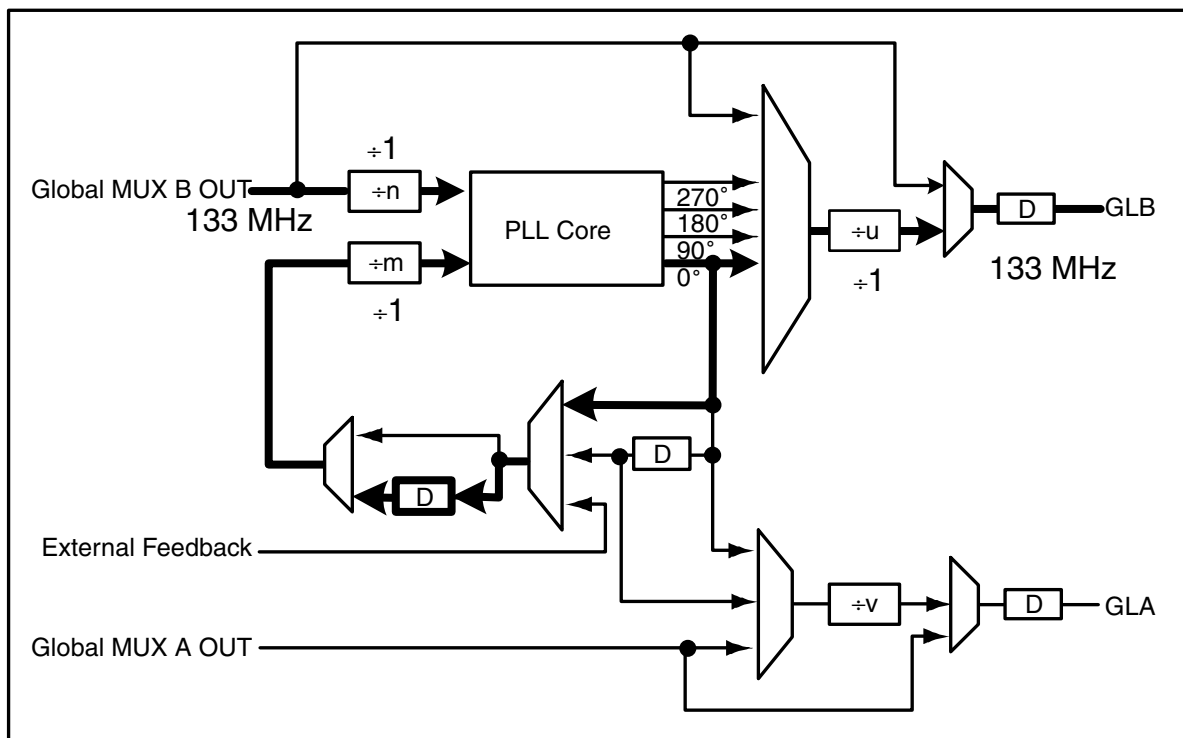
**Figure 14** • Using the PLL 33 MHz In, 133 MHz Out



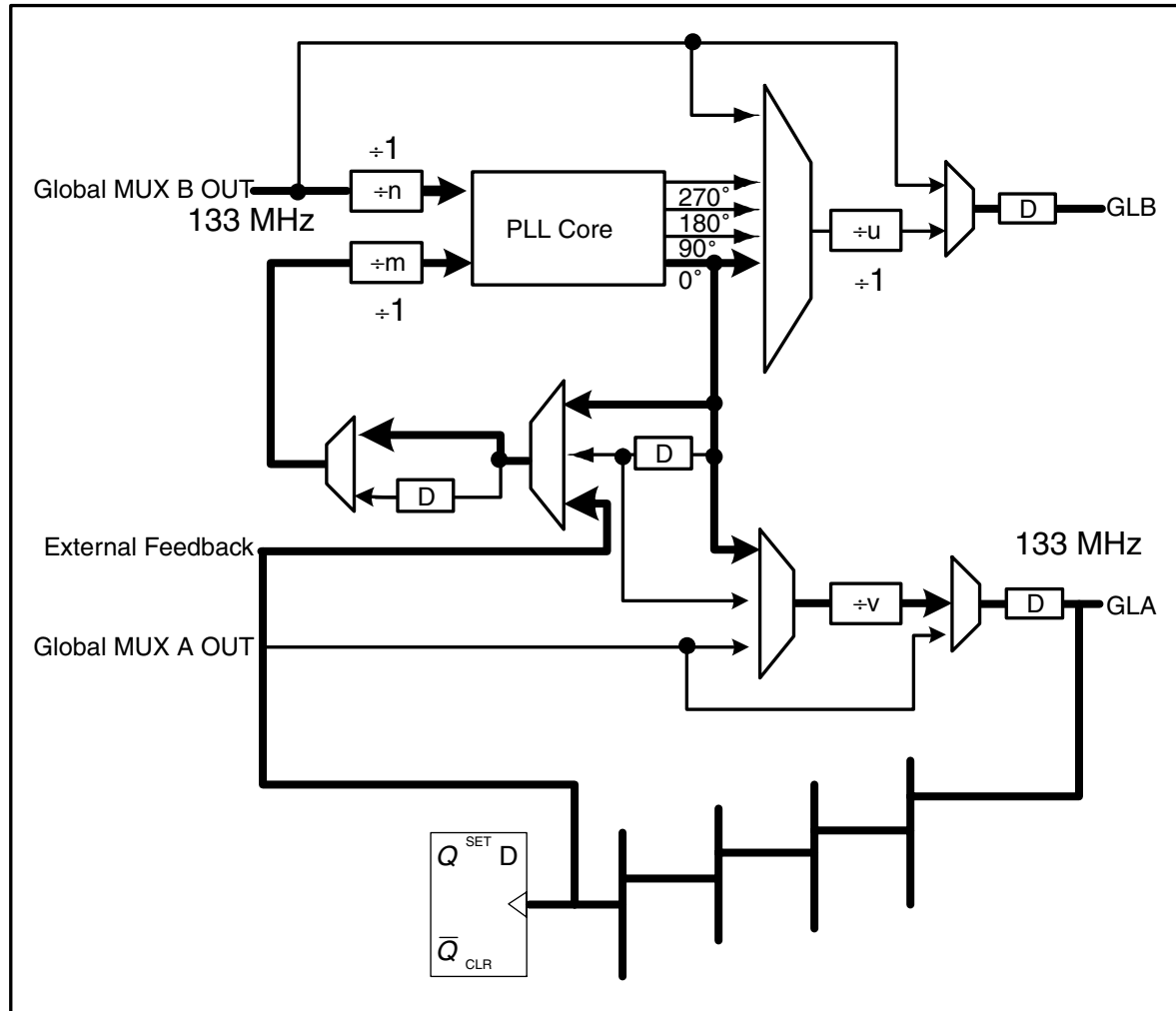
**Figure 15** • Using the PLL 40 MHz In, 50 MHz Out



**Figure 16** • Using the PLL to Delay the Input Clock



**Figure 17** • Using the PLL to "Advance" the Input Clock



**Figure 18 • Using the PLL for Clock Deskewing**

### Logic Tile Timing Characteristics

Timing characteristics for ProASIC<sup>PLUS</sup> devices fall into three categories: family dependent, device dependent, and design dependent. The input and output buffer characteristics are common to all ProASIC<sup>PLUS</sup> family members. Internal routing delays are device dependent. Design dependency means that actual delays are not determined until after placement and routing of the user's design are complete. Delay values may then be determined by using the Timer utility or performing simulation with post-layout delays.

### Critical Nets and Typical Nets

Propagation delays are expressed only for typical nets, which are used for initial design performance evaluation. Critical net delays can then be applied to the most timing critical paths. Critical nets are determined by net property assignment prior to placement and routing. Refer to the *Actel Designer User's Guide* for details on using constraints.

### Timing Derating

Since ProASIC<sup>PLUS</sup> devices are manufactured with a CMOS process, device performance will vary with temperature, voltage, and process. Minimum timing parameters reflect maximum operating voltage, minimum operating temperature, and optimal process variations. Maximum timing parameters reflect minimum operating voltage, maximum operating temperature, and worst-case process variations (within process specifications).

## PLL Electrical Specifications

| Parameter                                     | Value                | Notes                                                        |
|-----------------------------------------------|----------------------|--------------------------------------------------------------|
| <b>Frequency Ranges</b>                       |                      |                                                              |
| Reference Frequency $f_{IN}$ (min.)           | 1.5 MHz              | Clock conditioning circuitry (min.) lowest output frequency  |
| Reference Frequency $f_{IN}$ (max.)           | 180 MHz              | Clock conditioning circuitry (max.) highest output frequency |
| OSC Frequency $f_{VCO}$ (min.)                | 24 MHz               | Lowest output frequency voltage controlled oscillator        |
| OSC Frequency $f_{VCO}$ (max.)                | 180 MHz              | Highest output frequency voltage controlled oscillator       |
| Clock Conditioning Circuitry $f_{OUT}$ (min.) | 6 MHz                | Lowest input frequency clock conditioning circuitry          |
| Clock Conditioning Circuitry $f_{OUT}$ (max.) | 180 MHz              | Highest input frequency clock conditioning circuitry         |
| <b>Long Term Jitter Peak-to-Peak Max.</b>     |                      |                                                              |
| <b>Temperature</b>                            | <b>Frequency MHz</b> |                                                              |
|                                               | $f_{VCO} < 10$       | $10 < f_{VCO} < 60$ $f_{VCO} > 60$                           |
| 25°C (or higher)                              | ±1%                  | ±2%   ±0.5%                                                  |
| 0°C                                           | ±1.5%                | ±2.5%   ±1%                                                  |
| –40°C                                         | ±2.5%                | ±3.5%   ±1%                                                  |
| <b>Acquisition Time from Cold Start</b>       |                      |                                                              |
| Acquisition Time (max.)                       | 200 cycles           | Period of low reference clock frequencies                    |
| Acquisition Time (max.)                       | 80 $\mu$ s           | High reference clock frequencies                             |
| <b>Power Consumption</b>                      |                      |                                                              |
| Analog Supply Power (max*)                    | 6.9 mW               |                                                              |
| Digital Supply Current (max)                  | 7 $\mu$ W/MHz        |                                                              |
| <b>Duty Cycle</b>                             | 50% $\pm$ 0.5%       |                                                              |

**Note:** \*High clock frequency



### User Security

The ProASIC<sup>PLUS</sup> devices have FlashLock protections bits that, once programmed, block the entire programmed contents from being read externally. If locked, the user can only reprogram the device using the user-defined security key. This protects the device from being read back and duplicated. Since programmed data is stored in nonvolatile memory cells (which are actually very small capacitors), rather than in the wiring, physical deconstruction cannot be used to compromise data. This approach is further hampered by the placement of the memory cells beneath the four metal layers (whose removal cannot be accomplished without disturbing the charge in the capacitor). This is the highest security provided in the industry. For more information, refer to Actel's *Design Security in Nonvolatile Flash and Antifuse FPGAs* white paper.

### Embedded Memory Floorplan

The embedded memory is located across the top and bottom of the device in 256x9 blocks (see [Figure 1 on page 5](#)). Depending upon the device, up to 88 blocks are available to support a variety of memory configurations. Each block can be programmed as an independent memory or combined

(using dedicated memory routing resources) to form larger, more complex memories. A single memory configuration cannot include blocks from both the top and bottom memory locations.

### Embedded Memory Configurations

The embedded memory in the ProASIC<sup>PLUS</sup> family provides great configuration flexibility ([Table 7 on page 22](#)). Unlike many other programmable vendors each ProASIC<sup>PLUS</sup> block is designed and optimized as a two-port memory (1 read, 1 write). This provides 198kbits of total memory for two-port and single port usage in the APA1000 device.

Each memory can be configured as FIFO or SRAM, with independent selection of synchronous or asynchronous read and write ports ([Table 8 on page 22](#)). Additional characteristics include programmable flags as well as parity checking and generation. [Figure 19 on page 23](#) and [Figure 20 on page 24](#) show the block diagrams of the basic SRAM and FIFO blocks. [Table 9 on page 23](#) and [Table 10 on page 24](#) describe memory block SRAM and FIFO interface signals, respectively. A single memory is designed to operate at up to 150 MHz (standard speed grade). Each block contains a 256 word, 9-bit wide (1 read port, 1 write port)

memory. The memory blocks may be combined in parallel to form wider memories or stacked to form deeper memories (Figure 21 on page 25). This provides optimal bit widths of 9 (1 block), 18, 36, and 72, and optimal depths of 256, 512, 768, and 1024. Refer to Actel's *A Guide to ACTgen Macros* for more information.

Figure 22 on page 25 gives an example of optimal memory usage. Ten blocks with 23,040 bits have been used to

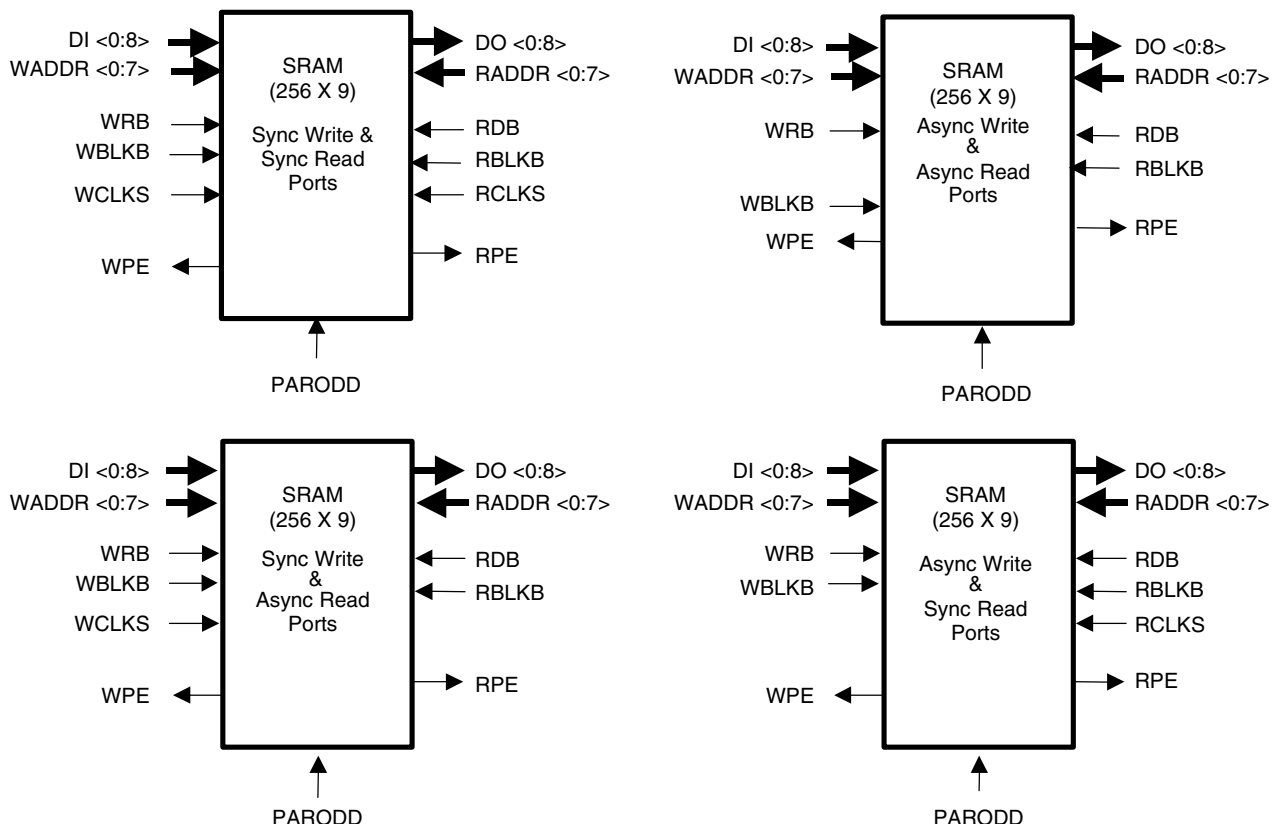
generate three memories of various widths and depths. Figure 23 on page 25 shows how memory can be used in parallel to create extra read ports. In this example, using only 10 of the 88 available blocks of the APA1000 yields an effective 6,912 bits of multiple port memories. The Actel ACTgen software facilitates building wider and deeper memories for optimal memory usage.

**Table 7 • ProASIC<sup>PLUS</sup> Memory Configurations by Device**

| Device  | Bottom | Top | Wide Maximum Size |     | Deep Maximum Size |   |
|---------|--------|-----|-------------------|-----|-------------------|---|
|         |        |     | D                 | W   | D                 | W |
| APA075  | 0      | 6   | 256               | 54  | 1,536             | 9 |
| APA150  | 0      | 16  | 256               | 144 | 2,048             | 9 |
| APA300  | 16     | 16  | 256               | 144 | 2,048             | 9 |
| APA450  | 24     | 24  | 256               | 216 | 3,072             | 9 |
| APA600  | 28     | 28  | 256               | 252 | 3,584             | 9 |
| APA750  | 32     | 32  | 256               | 288 | 4,096             | 9 |
| APA1000 | 44     | 44  | 256               | 396 | 5,632             | 9 |

**Table 8 • Basic Memory Configurations**

| Type | Write Access | Read Access             | Parity    | Library Cell Name |
|------|--------------|-------------------------|-----------|-------------------|
| RAM  | Asynchronous | Asynchronous            | Checked   | RAM256x9AA        |
| RAM  | Asynchronous | Asynchronous            | Generated | RAM256x9AAP       |
| RAM  | Asynchronous | Synchronous Transparent | Checked   | RAM256x9AST       |
| RAM  | Asynchronous | Synchronous Transparent | Generated | RAM256x9ASTP      |
| RAM  | Asynchronous | Synchronous Pipelined   | Checked   | RAM256x9ASR       |
| RAM  | Asynchronous | Synchronous Pipelined   | Generated | RAM256x9ASRP      |
| RAM  | Synchronous  | Asynchronous            | Checked   | RAM256x9SA        |
| RAM  | Synchronous  | Asynchronous            | Generated | RAM256x9SAP       |
| RAM  | Synchronous  | Synchronous Transparent | Checked   | RAM256x9SST       |
| RAM  | Synchronous  | Synchronous Transparent | Generated | RAM256x9SSTP      |
| RAM  | Synchronous  | Synchronous Pipelined   | Checked   | RAM256x9SSR       |
| RAM  | Synchronous  | Synchronous Pipelined   | Generated | RAM256x9SSRP      |
| FIFO | Asynchronous | Asynchronous            | Checked   | FIFO256x9AA       |
| FIFO | Asynchronous | Asynchronous            | Generated | FIFO256x9AAP      |
| FIFO | Asynchronous | Synchronous Transparent | Checked   | FIFO256x9AST      |
| FIFO | Asynchronous | Synchronous Transparent | Generated | FIFO256x9ASTP     |
| FIFO | Asynchronous | Synchronous Pipelined   | Checked   | FIFO256x9ASR      |
| FIFO | Asynchronous | Synchronous Pipelined   | Generated | FIFO256x9ASRP     |
| FIFO | Synchronous  | Asynchronous            | Checked   | FIFO256x9SA       |
| FIFO | Synchronous  | Asynchronous            | Generated | FIFO256x9SAP      |
| FIFO | Synchronous  | Synchronous Transparent | Checked   | FIFO256x9SST      |
| FIFO | Synchronous  | Synchronous Transparent | Generated | FIFO256x9SSTP     |
| FIFO | Synchronous  | Synchronous Pipelined   | Checked   | FIFO256x9SSR      |
| FIFO | Synchronous  | Synchronous Pipelined   | Generated | FIFO256x9SSRP     |



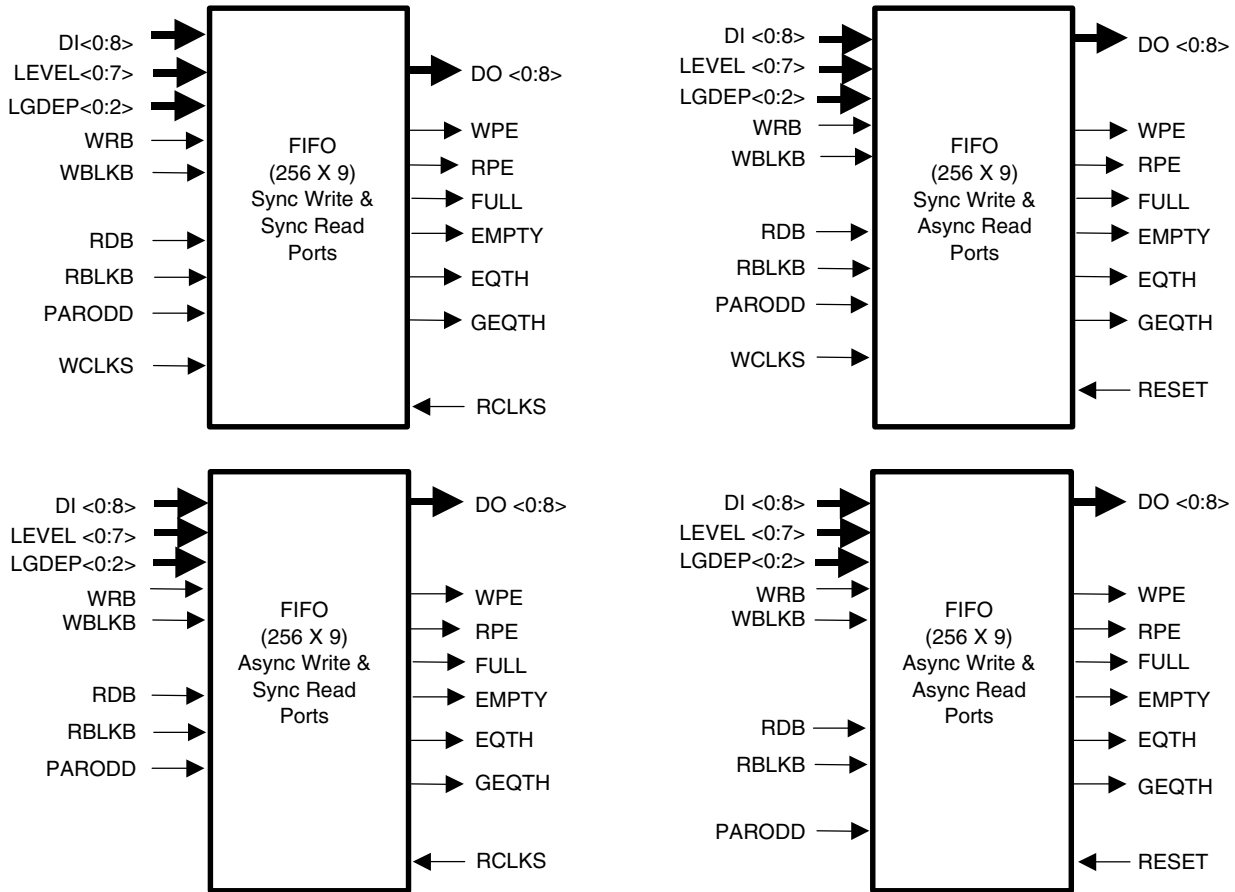
**Note:** To save area while using embedded memories, the memory blocks contain multiplexers (called DMUX) for each output signal. These DMUX cells do not consume any core logic tiles and connect directly to high speed routing resources between the memory blocks. They are used when memories are cascaded and are automatically inserted by the software tools.

**Figure 19 • Example SRAM Block Diagrams**

**Table 9 • Memory Block SRAM Interface Signals**

| SRAM Signal | Bits | In/Out | Description                                                   |
|-------------|------|--------|---------------------------------------------------------------|
| WCLKS       | 1    | IN     | Write clock used on synchronization on write side             |
| RCLKS       | 1    | IN     | Read clock used on synchronization on read side               |
| RADDR<0:7>  | 8    | IN     | Read address                                                  |
| RBLKB       | 1    | IN     | Negative true read block select                               |
| RDB         | 1    | IN     | Negative true read pulse                                      |
| WADDR<0:7>  | 8    | IN     | Write address                                                 |
| WBLKB       | 1    | IN     | Negative true write block select                              |
| DI<0:8>     | 9    | IN     | Input data bits <0:8>, <8> can be used for parity in          |
| WRB         | 1    | IN     | Negative true write pulse                                     |
| DO<0:8>     | 9    | OUT    | Output data bits <0:8>, <8> can be used for parity out        |
| RPE         | 1    | OUT    | Read parity error                                             |
| WPE         | 1    | OUT    | Write parity error                                            |
| PARODD      | 1    | IN     | Selects odd parity generation/detect when high, even when low |

**Note:** Not all signals shown are used in all modes.



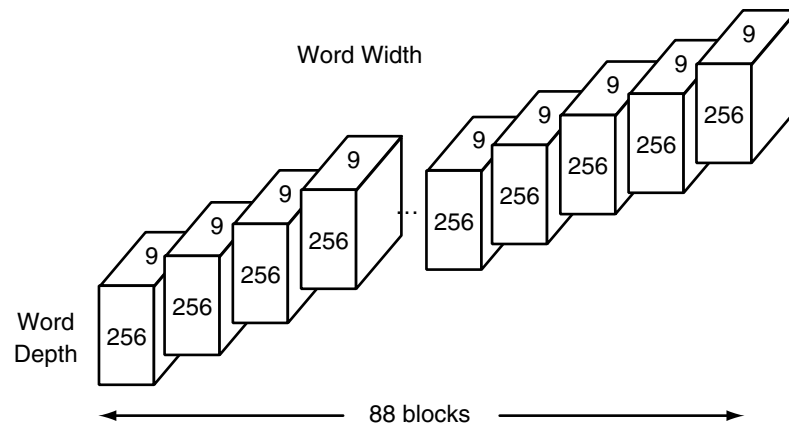
**Note:** To save area while using embedded memories, the memory blocks contain multiplexers (called DMUX) for each output signal. These DMUX cells do not consume any core logic tiles and connect directly to high speed routing resources between the memory blocks. They are used when memories are cascaded and are automatically inserted by the software tools.

**Figure 20 • Basic FIFO Block Diagrams**

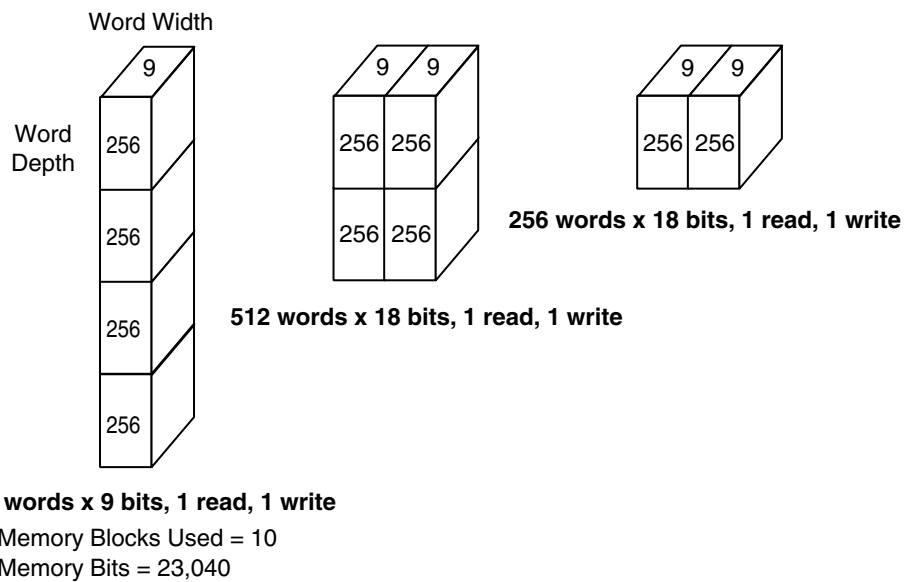
**Table 10 • Memory Block FIFO Interface Signals**

| FIFO Signal | Bits | In/Out | Description                                                                                                                                 |
|-------------|------|--------|---------------------------------------------------------------------------------------------------------------------------------------------|
| WCLKS       | 1    | IN     | Write clock used for synchronization on write side                                                                                          |
| RCLKS       | 1    | IN     | Read clock used for synchronization on read side                                                                                            |
| LEVEL <0:7> | 8    | IN     | Direct configuration implements static flag logic                                                                                           |
| RBLKB       | 1    | IN     | Negative true read block select                                                                                                             |
| RDB         | 1    | IN     | Negative true read pulse                                                                                                                    |
| RESET       | 1    | IN     | Negative true reset for FIFO pointers                                                                                                       |
| WBLKB       | 1    | IN     | Negative true write block select                                                                                                            |
| DI<0:8>     | 9    | IN     | Input data bits <0:8>, <8> will be generated if PARGEN is true                                                                              |
| WRB         | 1    | IN     | Negative true write pulse                                                                                                                   |
| FULL, EMPTY | 2    | OUT    | FIFO flags. FULL prevents write and EMPTY prevents read                                                                                     |
| EQTH, GEQTH | 2    | OUT    | EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more |
| DO<0:8>     | 9    | OUT    | Output data bits <0:8>                                                                                                                      |
| RPE         | 1    | OUT    | Read parity error                                                                                                                           |
| WPE         | 1    | OUT    | Write parity error                                                                                                                          |
| LGDEP <0:2> | 3    | IN     | Configures DEPTH of the FIFO to 2 (LGDEP+1)                                                                                                 |
| PARODD      | 1    | IN     | Selects odd parity generation/detect when high, even when low                                                                               |

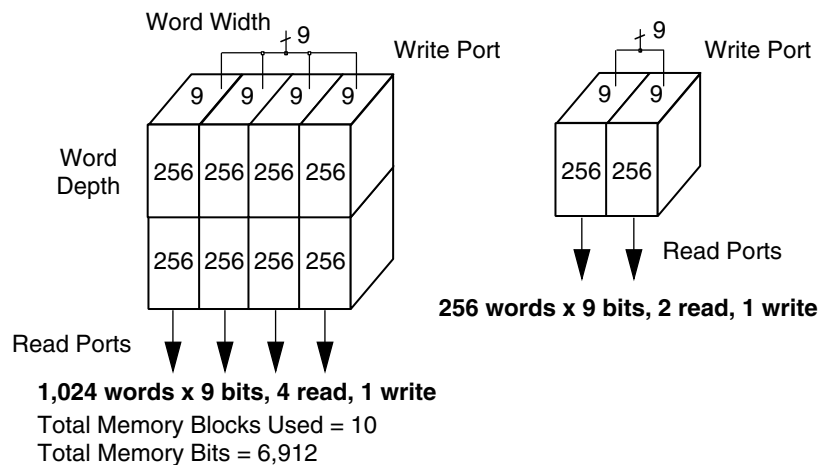




**Figure 21** • APA1000 Memory Block Architecture



**Figure 22** • Example Showing Memories with Different Widths and Depths



**Figure 23** • Multiport Memory Usage

## Design Environment

The ProASIC<sup>PLUS</sup> family of FPGAs is fully supported by both Actel's Libero<sup>TM</sup> Integrated Design Environment and Designer FPGA Development software. Actel Libero IDE is a design management environment that streamlines the design flow. Libero IDE provides an integrated design manager that seamlessly integrates design tools while guiding the user through the design flow, managing all design and log files, and passing necessary design data among tools. Additionally, Libero IDE allows users to integrate both schematic and HDL synthesis into a single flow and verify the entire design in a single environment (Figure 24 on page 27). Libero IDE includes Synplify<sup>®</sup> for Actel from Synplicity<sup>®</sup>, ViewDraw for Actel from Mentor Graphics, ModelSim<sup>TM</sup> HDL Simulator from Model Technology<sup>TM</sup>, WaveFormer Lite<sup>TM</sup> from SynaptiCAD<sup>TM</sup>, and Designer software from Actel.

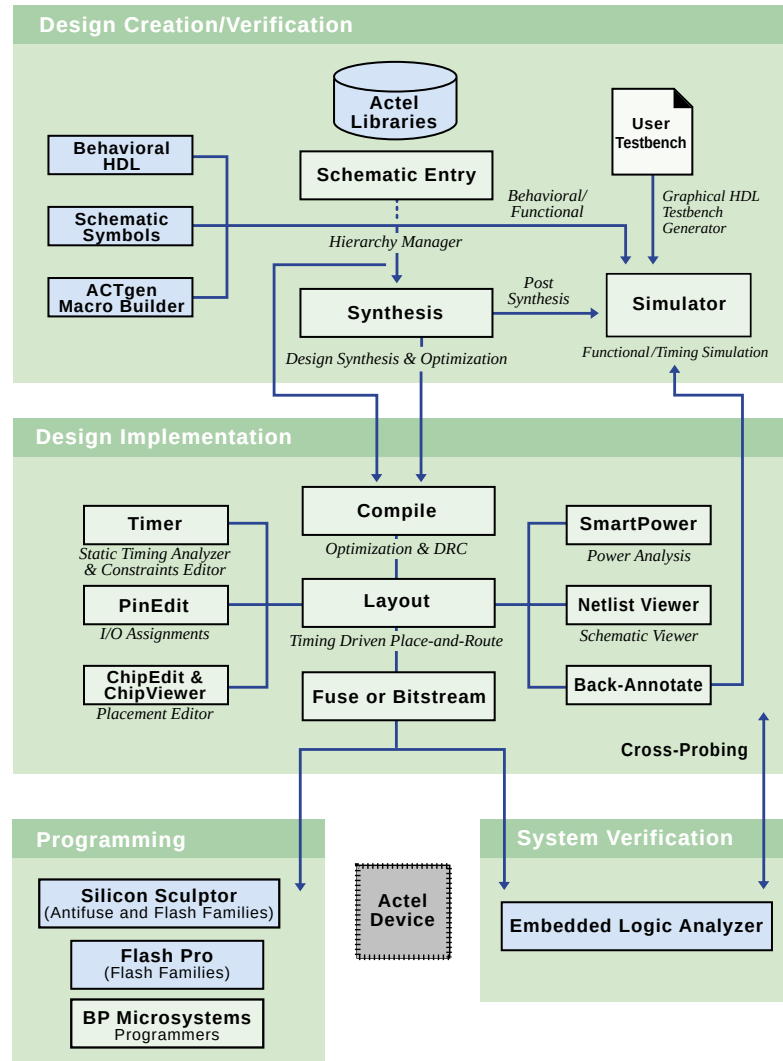
Actel's Designer software provides a comprehensive suite of backend development tools for FPGA development. The Designer software includes timing-driven place-and-route, a world-class integrated static timing analyzer and constraints editor, a design netlist schematic viewer, and SmartPower, a tool that allows the user to quickly estimate the power consumption in a design. With the Designer

software, a user can lock their design pins before layout while minimally impacting the results of place-and-route. Additionally, our back-annotation flow is compatible with all the major simulators and the simulation results can be cross-probed with an embedded logic analyzer, such as the Configurable Logic Analyzer Module provided by First Silicon Solutions Inc. Another tool included in the Designer software is the ACTgen macro builder, which easily creates popular and commonly used logic functions for implementation into your schematic or HDL design.

Actel's Designer software is compatible with the most popular FPGA design entry and verification tools from companies such as Mentor Graphics, Synplicity, Synopsys, and Cadence Design Systems. The Designer software is available for both the Windows and Unix operating systems.

For details on ProASIC<sup>PLUS</sup> programming, refer to the following application notes:

- *Performing Internal In-System Programming Using Actel's ProASIC<sup>PLUS</sup> Devices*
- *In-System Programming ProASIC 500K<sup>TM</sup> and ProASIC<sup>PLUS</sup> Devices with Silicon Sculptor and Flash Pro*

**Figure 24 • Design Flow**

## Package Thermal Characteristics

The ProASIC<sup>PLUS</sup> family is available in several package types with a range of pin counts. Actel has selected packages based on high pin count, reliability factors, and superior thermal characteristics.

Thermal resistance defines the ability of a package to conduct heat away from the silicon, through the package to the surrounding air. Junction-to-ambient thermal resistance is measured in degrees Celsius/Watt and is represented as Theta ja ( $\Theta_{ja}$ ). The lower the thermal resistance, the more efficiently a package will dissipate heat.

A package's maximum allowed power (P) is a function of maximum junction temperature ( $T_J$ ), maximum ambient operating temperature ( $T_A$ ), and junction-to-ambient

thermal resistance  $\Theta_{ja}$ . Maximum junction temperature is the maximum allowable temperature on the active surface of the IC and is 110° C. P is defined as:

$$P = \frac{T_J - T_A}{\Theta_{ja}}$$

$\Theta_{ja}$  is a function of the rate (in linear feet per minute – lfm) of airflow in contact with the package. When the estimated power consumption exceeds the maximum allowed power, other means of cooling, such as increasing the airflow rate, must be used.

| Package Type                      | Pin Count | $\Theta_{jc}$ | $\Theta_{ja}$ Still Air | $\Theta_{ja}$ 300 ft./min. | Units |
|-----------------------------------|-----------|---------------|-------------------------|----------------------------|-------|
| Thin Quad Flat Pack (TQFP)        | 100       | 14            | 51.2                    | 35                         | °C/W  |
| Plastic Quad Flat Pack (PQFP)     | 208       | 8             | 30                      | 23                         | °C/W  |
| PQFP with Heatspreader            | 208       | 3.8           | 20                      | 17                         | °C/W  |
| Fine Pitch Ball Grid Array (FBGA) | 144       | 3             | 38.8                    | 26.7                       | °C/W  |
| Fine Pitch Ball Grid Array (FBGA) | 256       | 3             | 30                      | 25                         | °C/W  |
| Plastic Ball Grid Array (PBGA)    | 456       | 3             | 13.9                    | 11.1                       | °C/W  |
| Fine Pitch Ball Grid Array (FBGA) | 484       | 3             | 22                      | 18                         | °C/W  |
| Fine Pitch Ball Grid Array (FBGA) | 676       | 3             | 15                      | 11.5                       | °C/W  |
| Fine Pitch Ball Grid Array (FBGA) | 896       | 3             | 13.2                    | 10                         | °C/W  |
| Fine Pitch Ball Grid Array (FBGA) | 1152      | 3             | 12.6                    | 9.9                        | °C/W  |

## ISP

ProASIC<sup>PLUS</sup> Devices can be programmed in situ. For more information on ISP of ProASIC<sup>PLUS</sup> devices, please refer to the *Performing Internal In-System Programming Using Actel's ProASIC<sup>PLUS</sup> Devices* and *In-System Programming ProASIC 500K<sup>TM</sup> and ProASIC<sup>PLUS</sup> Devices with Silicon Sculptor and Flash Pro* application notes.

## Calculating Power Dissipation

ProASIC<sup>PLUS</sup> device power is calculated with both a static and an active component. The active component is a function of both the number of tiles utilized and the system speed. Power dissipation can be calculated using the following formula:

$$P_{\text{total}} = P_{\text{dc}} + P_{\text{ac}}$$

where:

- $P_{\text{dc}} = 10 \text{ mW}$
- $P_{\text{ac}} = P_{\text{clock}} + P_{\text{storage}} + P_{\text{logic}} + P_{\text{inputs}} + P_{\text{outputs}} + P_{\text{memory}} + P_{\text{pll}}$

$P_{\text{clock}}$ , the clock component of power dissipation, is given by

$$P_{\text{clock}} = (P1 + P2 * R - P7 * R^2) * Fs$$

where:

- $P1 = 100 \text{ } \mu\text{W/MHz}$  is the basic power consumption of the clock tree per MHz of the clock
- $P2 = 1.3 \text{ } \mu\text{W/MHz}$  is the incremental power consumption of the clock tree per storage tile – also per MHz of the clock
- $P7 = 0.00003 \text{ } \mu\text{W/MHz}$  is a correction factor for highly loaded clock-trees
- $R =$  the number of storage tiles clocked by this clock
- $Fs =$  the clock frequency

$P_{\text{storage}}$ , the storage-tile (Register) component of AC power dissipation, is given by

$$P_{\text{storage}} = P5 * ms * Fs$$

where:

- $P5 = 1.3 \text{ } \mu\text{W/MHz}$  is the average power consumption of a storage-tile per MHz of its output toggling rate. The maximum output toggling rate is  $Fs/2$
- $ms =$  the number of storage tiles (Register) switching during each  $Fs$  cycle
- $Fs =$  the clock frequency

$P_{\text{logic}}$ , the logic-tile component of AC power dissipation, is given by

$$P_{\text{logic}} = P3 * mc * Fs$$

where:

- $P3 = 1.4 \text{ } \mu\text{W/MHz}$ , is the average power consumption of a storage-tile per MHz of its output toggling rate. The maximum output toggling rate is  $Fs/2$
- $mc =$  the number of logic tiles switching during each  $Fs$  cycle
- $Fs =$  the clock frequency

$P_{\text{outputs}}$ , the I/O component of AC power dissipation, is given by

$$P_{\text{outputs}} = (P4 + (C_{\text{load}} * V_{\text{DDP}}^2)) * p * Fp$$

where:

- $P4 = 326 \text{ } \mu\text{W/MHz}$  is the intrinsic power consumption of an output pad normalized per MHz of the output frequency. This is the total I/O current  $V_{\text{DD}} + V_{\text{DDP}}$
- $C_{\text{load}} =$  the output load
- $p =$  the number of outputs
- $Fp =$  the average output frequency

The input's component of AC power dissipation is given by

$$P_{\text{inputs}} = P8 * q * Fq$$

where:

- $P8 = 29 \text{ } \mu\text{W/MHz}$  is the intrinsic power consumption of an input pad normalized per MHz of the input frequency
- $q =$  the number of inputs
- $Fq =$  the average input frequency

$$P_{\text{pll}} = P9 * N_{\text{pll}}$$

where:

- $P9 = 6.9 \text{ mW}$ . This value has been estimated at maximum PLL clock frequency
- $N_{\text{pll}} =$  number of PLLs used

Finally,  $P_{\text{memory}}$ , the memory component of AC power consumption, is given by

$$P_{\text{memory}} = P6 * N_{\text{memory}} * F_{\text{memory}}$$

where:

- $P6 = 100.0 \text{ } \mu\text{W/MHz}$  is the average power consumption of a memory block per MHz of the clock
- $N_{\text{memory}} =$  the number of RAM/FIFO blocks (1 block = 256 words \* 9 bits)
- $F_{\text{memory}} =$  the clock frequency of the memory

The following is an APA750 example using a shift register design with 13,440 storage tiles (Register) and 0 logic tiles. This design has one clock at 10 MHz, and 24 outputs toggling at 5 MHz. We then calculate the various components as follows:

### $P_{\text{clock}}$

- $Fs = 10 \text{ MHz}$
- $R = 13,440$

$$\Rightarrow P_{\text{clock}} = (P1 + P2 * R - P7 * R^2) * Fs = 124.2 \text{ mW}$$

### $P_{\text{storage}}$

- $ms = 13,440$  (in a shift register 100% of storage-tiles are toggling at each clock cycle and  $Fs = 10 \text{ MHz}$ )

$$\Rightarrow P_{\text{storage}} = P5 * ms * Fs = 174.7 \text{ mW}$$

### $P_{\text{logic}}$

- $mc = 0$  (no logic tile in this shift-register)

$$\Rightarrow P_{\text{logic}} = 0 \text{ mW}$$

**P<sub>outputs</sub>**

- $C_{load} = 40 \text{ pF}$
- $V_{DDP} = 3.3 \text{ V}$
- $p = 24$
- $Fp = 5 \text{ MHz}$

$$\Rightarrow P_{outputs} = (P4 + C_{load} * V_{DDP}^2) * p * Fp = 87.3 \text{ mW}$$

**P<sub>inputs</sub>**

- $q = 1$
- $Fq = 10 \text{ MHz}$

$$\Rightarrow P_{inputs} = P8 * q * Fq = 0.3 \text{ mW}$$

**P<sub>memory</sub>**

$$N_{memory} = 0 \text{ (no RAM/FIFO in this shift-register)}$$

$$\Rightarrow P_{memory} = 0 \text{ mW}$$

**P<sub>ac</sub>**

$$\Rightarrow 386 \text{ mW}$$

**P<sub>total</sub>**

$$P_{dc} + P_{ac} = 396 \text{ mW}$$

## Operating Conditions

Standard and –F parts are the same unless otherwise noted. –F parts are only available as commercial.

### Absolute Maximum Ratings\*

| Parameter                             | Condition                                | Minimum | Maximum         | Units |
|---------------------------------------|------------------------------------------|---------|-----------------|-------|
| Supply Voltage Core ( $V_{DD}$ )      |                                          | –0.3    | 3.0             | V     |
| Supply Voltage I/O Ring ( $V_{DDP}$ ) |                                          | –0.3    | 4.0             | V     |
| DC Input Voltage                      |                                          | –0.3    | $V_{DDP} + 0.3$ | V     |
| PCI DC Input Voltage                  |                                          | –1.0    | $V_{DDP} + 1.0$ | V     |
| PCI DC Input Clamp Current (absolute) | $V_{IN} < -1$ or $V_{IN} = V_{DDP} + 1V$ | 10      |                 | mA    |
| LVPECL Input Voltage                  |                                          | –0.3    | $V_{DDP} + 0.5$ | V     |
| GND                                   |                                          | 0       | 0               | V     |

**Note:** \* Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. Exposure to absolute maximum rated conditions for extended periods may affect device reliability. Devices should not be operated outside the Recommended Operating Conditions.

### Programming and Storage and Operating Temperature Limits

| Product Grade | Programming Cycles | Program Retention | Storage Temperature |       | Operating                      |
|---------------|--------------------|-------------------|---------------------|-------|--------------------------------|
|               |                    |                   | Min.                | Max.  | $T_J$ Max Junction Temperature |
| Commercial    | 100                | 20 years          | –55°C               | 110°C | 110°C                          |
| Industrial    | 100                | 20 years          | –55°C               | 110°C | 110°C                          |

**Note:** This is a stress rating only. Functional operation at these or any other condition above those indicated in the operational and programming specification is not implied.

### Supply Voltages

| Mode           | $V_{DD}$ | $V_{DDP}$ |
|----------------|----------|-----------|
| Single Voltage | 2.5V     | 2.5V      |
| Mixed Voltage  | 2.5V     | 3.3V      |

| Parameter | Condition                     | Commercial/Industrial |          | Units |
|-----------|-------------------------------|-----------------------|----------|-------|
|           |                               | Minimum               | Maximum  |       |
| $V_{PP}$  | During Programming            | 15.9                  | 16.5     | V     |
|           | Normal Operation <sup>1</sup> | 0                     | 16.5     | V     |
| $V_{PN}$  | During Programming            | –13.8                 | –13.4    | V     |
|           | Normal Operation <sup>2</sup> | –13.8                 | 0        | V     |
| $I_{PP}$  | During Programming            |                       | 25       | mA    |
| $I_{PN}$  | During Programming            |                       | 10       | mA    |
| AVDD      |                               | $V_{DD}$              | $V_{DD}$ | V     |
| AGND      |                               | GND                   | GND      | V     |

**Notes:**

1. Please refer to the “VPP Programming Supply Pin” section on page 61 for more information.
2. Please refer to the “VPN Programming Supply Pin” section on page 61 for more information.

### Recommended Operating Conditions

| Parameter                                 | Symbol               | Limits          |                 |
|-------------------------------------------|----------------------|-----------------|-----------------|
|                                           |                      | Commercial      | Industrial      |
| DC Supply Voltage (2.5V I/Os)             | $V_{DD}$ & $V_{DDP}$ | $2.5V \pm 0.2V$ | $2.5V \pm 0.2V$ |
| DC Supply Voltage (Mixed 2.5V, 3.3V I/Os) | $V_{DDP}$            | $3.3V \pm 0.3V$ | $3.3V \pm 0.3V$ |
|                                           | $V_{DD}$             | $2.5V \pm 0.2V$ | $2.5V \pm 0.2V$ |
| Operating Ambient Temperature Range       | $T_A$                | 0°C to 70°C     | –40°C to 85°C   |
| Maximum Operating Junction Temperature    | $T_J$                | 110°C           | 110°C           |

**DC Electrical Specifications ( $V_{DDP} = 2.5V \pm 0.2V$ )<sup>1</sup>**

| Symbol           | Parameter                                                                        | Conditions                                     | Commercial / Industrial <sup>1,2</sup> |      |                 | Units      |
|------------------|----------------------------------------------------------------------------------|------------------------------------------------|----------------------------------------|------|-----------------|------------|
|                  |                                                                                  |                                                | Min.                                   | Typ. | Max.            |            |
| $V_{OH}$         | Output High Voltage<br>High Drive (OB25LPH)                                      | $I_{OH} = -6\text{ mA}$                        | 2.1                                    |      |                 | V          |
|                  |                                                                                  | $I_{OH} = -12\text{ mA}$                       | 2.0                                    |      |                 |            |
|                  |                                                                                  | $I_{OH} = -24\text{ mA}$                       | 1.7                                    |      |                 |            |
|                  | Low Drive (OB25LPL)                                                              | $I_{OH} = -4\text{ mA}$                        | 2.1                                    |      |                 |            |
|                  |                                                                                  | $I_{OH} = -6\text{ mA}$                        | 2.0                                    |      |                 |            |
|                  |                                                                                  | $I_{OH} = -10\text{ mA}$                       | 1.7                                    |      |                 |            |
| $V_{OL}$         | Output Low Voltage<br>High Drive (OB25LPH)                                       | $I_{OL} = 8\text{ mA}$                         |                                        |      | 0.2             | V          |
|                  |                                                                                  | $I_{OL} = 15\text{ mA}$                        |                                        |      | 0.4             |            |
|                  |                                                                                  | $I_{OL} = 24\text{ mA}$                        |                                        |      | 0.7             |            |
|                  | Low Drive (OB25LPL)                                                              | $I_{OL} = 4\text{ mA}$                         |                                        |      | 0.2             |            |
|                  |                                                                                  | $I_{OL} = 8\text{ mA}$                         |                                        |      | 0.4             |            |
|                  |                                                                                  | $I_{OL} = 15\text{ mA}$                        |                                        |      | 0.7             |            |
| $V_{IH}$         | Input High Voltage                                                               |                                                | 1.7                                    |      | $V_{DDP} + 0.3$ | V          |
| $V_{IL}$         | Input Low Voltage                                                                |                                                | -0.3                                   |      | 0.7             | V          |
| $R_{WEAKPULLUP}$ | Weak Pull-up Resistance<br>(OTB25LPU)                                            | $V_{IN} \geq 1.25V$                            | 6                                      |      | 56              | k $\Omega$ |
| HYST             | Input Hysteresis Schmitt                                                         | Table 4 on page 12                             | 0.3                                    | 0.35 | 0.45            | V          |
| $I_{IN}$         | Input Current                                                                    | with pull up ( $V_{IN} = GND$ )                | -240                                   |      | -20             | $\mu A$    |
|                  |                                                                                  | without pull up ( $V_{IN} = GND$ or $V_{DD}$ ) | -10                                    |      | 10              | $\mu A$    |
| $I_{DDQ}$        | Quiescent Supply Current<br>(standby)                                            | $V_{IN} = GND^3$ or $V_{DD}$                   | Std.                                   | 5.0  | 10              | mA         |
|                  |                                                                                  |                                                | -F                                     | 5.0  | 20              | mA         |
| $I_{OZ}$         | 3-State Output Leakage Current                                                   | $V_{OH} = GND$ or $V_{DD}$                     | Std.                                   | -10  | 10              | $\mu A$    |
|                  |                                                                                  |                                                | -F <sup>4</sup>                        | -10  | 100             | $\mu A$    |
| $I_{OSH}$        | Output Short Circuit Current High<br>High Drive (OB25LPH)<br>Low Drive (OB25LPL) | $V_{IN} = V_{SS}$                              | -120                                   |      |                 | mA         |
|                  |                                                                                  | $V_{IN} = V_{SS}$                              | -100                                   |      |                 |            |
| $I_{OSL}$        | Output Short Circuit Current High<br>High Drive (OB25LPH)<br>Low Drive (OB25LPL) | $V_{IN} = V_{DDP}$                             |                                        |      | 100             | mA         |
|                  |                                                                                  | $V_{IN} = V_{DDP}$                             |                                        |      | 30              |            |
| $C_{I/O}$        | I/O Pad Capacitance                                                              |                                                |                                        |      | 10              | pF         |
| $C_{CLK}$        | Clock Input Pad Capacitance                                                      |                                                |                                        |      | 10              | pF         |

**Notes:**

1. All process conditions. Junction Temperature: -40 to +110°C.
2. -F parts are only available as commercial.
3. No pull-up resistor.
4. This will not exceed 2mA total per device.



DC Electrical Specifications ( $V_{DDP} = 3.3V \pm 0.3V$  and  $V_{DD} = 2.5V \pm 0.2V$ )<sup>1</sup>

| Symbol                  | Parameter                                             | Conditions                                                                          |                 | Commercial / Industrial <sup>1,2</sup> |      |                                                  | Units |
|-------------------------|-------------------------------------------------------|-------------------------------------------------------------------------------------|-----------------|----------------------------------------|------|--------------------------------------------------|-------|
|                         |                                                       |                                                                                     |                 | Min.                                   | Typ. | Max.                                             |       |
| V <sub>OH</sub>         | Output High Voltage<br>3.3V I/O, High Drive (OB33P)   | I <sub>OH</sub> = −15 mA<br>I <sub>OH</sub> = −30 mA                                |                 | 0.9*V <sub>DDP</sub><br>2.4            |      |                                                  | V     |
|                         | 3.3V I/O, Low Drive (OB33L)                           | I <sub>OH</sub> = −7 mA<br>I <sub>OH</sub> = −14 mA                                 |                 | 0.9*V <sub>DDP</sub><br>2.4            |      |                                                  |       |
|                         | Output High Voltage<br>2.5V I/O, High Drive (OB25H)   | I <sub>OH</sub> = −0.1 mA<br>I <sub>OH</sub> = −0.5 mA<br>I <sub>OH</sub> = −4 mA   |                 | 2.1<br>2.0<br>1.7                      |      |                                                  | V     |
|                         | 2.5V I/O, Low Drive (OB25L)                           | I <sub>OH</sub> = −0.1 mA<br>I <sub>OH</sub> = −0.5 mA<br>I <sub>OH</sub> = −2.5 mA |                 | 2.1<br>2.0<br>1.7                      |      |                                                  |       |
| V <sub>OL</sub>         | Output Low Voltage<br>3.3V I/O, High Drive (OB33P)    | I <sub>OL</sub> = 15 mA<br>I <sub>OL</sub> = 20 mA<br>I <sub>OL</sub> = 28 mA       |                 |                                        |      | 0.1V <sub>DDP</sub><br>0.4<br>0.7                | V     |
|                         | 3.3V I/O, Low Drive (OB33L)                           | I <sub>OL</sub> = 7 mA<br>I <sub>OL</sub> = 10 mA<br>I <sub>OL</sub> = 15 mA        |                 |                                        |      | 0.1V <sub>DDP</sub><br>0.4<br>0.7                |       |
|                         | Output Low Voltage<br>2.5V I/O, High Drive (OB25H)    | I <sub>OL</sub> = 7 mA<br>I <sub>OL</sub> = 14 mA<br>I <sub>OL</sub> = 28 mA        |                 |                                        |      | 0.2<br>0.4<br>0.7                                | V     |
|                         | 2.5V I/O, Low Drive (OB25L)                           | I <sub>OL</sub> = 5 mA<br>I <sub>OL</sub> = 10 mA<br>I <sub>OL</sub> = 15 mA        |                 |                                        |      | 0.2<br>0.4<br>0.7                                |       |
| V <sub>IH</sub>         | Input High Voltage<br>3.3V LVTTTL/LVCMOS<br>2.5V Mode |                                                                                     |                 | 2<br>1.7                               |      | V <sub>DDP</sub> + 0.3<br>V <sub>DDP</sub> + 0.3 | V     |
| V <sub>IL</sub>         | Input Low Voltage<br>3.3V LVTTTL/LVCMOS<br>2.5V Mode  |                                                                                     |                 | 0.3<br>0.3                             |      | 0.8<br>0.7                                       | V     |
| R <sub>WEAKPULLUP</sub> | Weak Pull-up Resistance<br>(OTB33U)                   | V <sub>IN</sub> ≥ 1.5V                                                              |                 | 7                                      |      | 43                                               | kΩ    |
| R <sub>WEAKPULLUP</sub> | Weak Pull-up Resistance<br>(OTB25U)                   | V <sub>IN</sub> ≥ 1.5V                                                              |                 | 7                                      |      | 43                                               | kΩ    |
| I <sub>IN</sub>         | Input Current                                         | with pull up (V <sub>IN</sub> = GND)                                                |                 | −300                                   |      | −40                                              | μA    |
|                         |                                                       | without pull up (V <sub>IN</sub> = GND or V <sub>DD</sub> )                         |                 | −10                                    |      | 10                                               | μA    |
| I <sub>DDQ</sub>        | Quiescent Supply Current<br>(standby)                 | V <sub>IN</sub> = GND <sup>3</sup> or V <sub>DD</sub>                               | Std.            |                                        | 5.0  | 10                                               | mA    |
|                         |                                                       |                                                                                     | −F              |                                        | 5.0  | 20                                               | mA    |
| I <sub>OZ</sub>         | 3-State Output Leakage Current                        | V <sub>OH</sub> = GND or V <sub>DD</sub>                                            | Std.            | −10                                    |      | 10                                               | μA    |
|                         |                                                       |                                                                                     | −F <sup>4</sup> | −10                                    |      | 100                                              | μA    |

**Notes:**

1. All process conditions. Junction Temperature:  $-40$  to  $+110^\circ C$ .
2. -F parts are only available as commercial.
3. No pull-up resistor.
4. This will not exceed 2mA total per device.

**DC Electrical Specifications ( $V_{DDP} = 3.3V \pm 0.3V$  and  $V_{DD} = 2.5V \pm 0.2V$ )<sup>1</sup> (Continued)**

| Symbol    | Parameter                                                                              | Conditions                             | Commercial / Industrial <sup>1,2</sup> |      |            | Units |
|-----------|----------------------------------------------------------------------------------------|----------------------------------------|----------------------------------------|------|------------|-------|
|           |                                                                                        |                                        | Min.                                   | Typ. | Max.       |       |
| $I_{OSH}$ | Output Short Circuit Current High<br>3.3V High Drive (OB33P)<br>3.3V Low Drive (OB33L) | $V_{IN} = GND$<br>$V_{IN} = GND$       |                                        |      | 200<br>100 | mA    |
|           | 2.5V High Drive (OB25H)<br>2.5V Low Drive (OB25L)                                      | $V_{IN} = GND$<br>$V_{IN} = GND$       |                                        |      | 20<br>10   |       |
| $I_{OSL}$ | Output Short Circuit Current Low<br>3.3V High Drive<br>3.3V Low Drive                  | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{DD}$ |                                        |      | 200<br>100 | mA    |
|           | 2.5V High Drive<br>2.5V Low Drive                                                      | $V_{IN} = V_{DD}$<br>$V_{IN} = V_{DD}$ |                                        |      | 200<br>100 |       |
| $C_{I/O}$ | I/O Pad Capacitance                                                                    |                                        |                                        |      | 10         | pF    |
| $C_{CLK}$ | Clock Input Pad Capacitance                                                            |                                        |                                        |      | 10         | pF    |

**Notes:**

1. All process conditions. Junction Temperature:  $-40$  to  $+110^{\circ}C$ .
2.  $-F$  parts are only available as commercial.
3. No pull-up resistor.
4. This will not exceed 2mA total per device.

**DC Specifications (3.3V PCI Operation)<sup>1</sup>**

| Symbol    | Parameter                          | Condition              | Commercial / Industrial <sup>2,3</sup> |                 | Units   |
|-----------|------------------------------------|------------------------|----------------------------------------|-----------------|---------|
|           |                                    |                        | Min.                                   | Max.            |         |
| $V_{DD}$  | Supply Voltage for Core            |                        | 2.3                                    | 2.7             | V       |
| $V_{DDP}$ | Supply Voltage for I/O Ring        |                        | 3.0                                    | 3.6             | V       |
| $V_{IH}$  | Input High Voltage                 |                        | $0.5V_{DDP}$                           | $V_{DDP} + 0.5$ | V       |
| $V_{IL}$  | Input Low Voltage                  |                        | $-0.5$                                 | $0.3V_{DDP}$    | V       |
| $I_{IPU}$ | Input Pull-up Voltage <sup>4</sup> |                        | $0.7V_{DDP}$                           |                 | V       |
| $I_{IL}$  | Input Leakage Current <sup>5</sup> | $0 < V_{IN} < V_{CCI}$ | Std.                                   | 10              | $\mu A$ |
|           |                                    |                        | $-F$ <sup>6</sup>                      | 100             | $\mu A$ |
| $V_{OH}$  | Output High Voltage                | $I_{OUT} = -500 \mu A$ | $0.9V_{DDP}$                           |                 | V       |
| $V_{OL}$  | Output Low Voltage                 | $I_{OUT} = 1500 \mu A$ |                                        | $0.1V_{DDP}$    | V       |
| $C_{IN}$  | Input Pin Capacitance (except CLK) |                        |                                        | 10              | pF      |
| $C_{CLK}$ | CLK Pin Capacitance                |                        | 5                                      | 12              | pF      |

**Notes:**

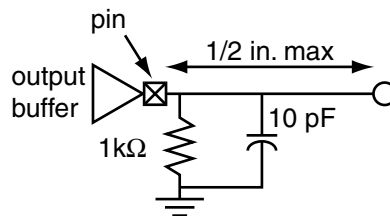
1. For PCI operation, use OTB33PH, OB33PH, IOB33PH, IB33, or IB33S macro library cell only.
2. All process conditions. Junction Temperature:  $-40$  to  $+110^{\circ}C$ .
3.  $-F$  parts are available as commercial only.
4. This specification is guaranteed by design. It is the minimum voltage to which pull-up resistors are calculated to pull a floated network. Designers with applications sensitive to static power utilization should ensure that the input buffer is conducting minimum current at this input voltage.
5. Input leakage currents include hi-Z output leakage for all bidirectional buffers with tristate outputs.
6. The sum of the leakage currents for all inputs shall not exceed 2mA per device.

## AC Specifications (3.3V PCI Revision 2.2 Operation)

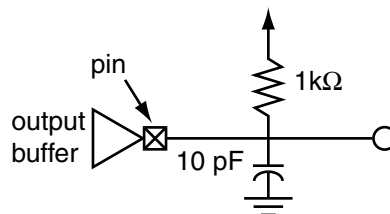
| Symbol       | Parameter              | Condition                                | Commercial / Industrial             |                                                                      | Units |
|--------------|------------------------|------------------------------------------|-------------------------------------|----------------------------------------------------------------------|-------|
|              |                        |                                          | Min.                                | Max.                                                                 |       |
| $I_{OH(AC)}$ | Switching Current High | $0 < V_{OUT} \leq 0.3V_{CCI} *$          | $-12V_{CCI}$                        |                                                                      | mA    |
|              |                        | $0.3V_{CCI} \leq V_{OUT} < 0.9V_{CCI} *$ | $(-17.1 + (V_{DDP} - V_{OUT}))$     |                                                                      | mA    |
|              |                        | $0.7V_{CCI} < V_{OUT} < V_{CCI} *$       |                                     | See equation C – page 124 of the PCI Specification document rev. 2.2 |       |
|              | (Test Point)           | $V_{OUT} = 0.7V_{CC} *$                  |                                     | $-32V_{CCI}$                                                         | mA    |
| $I_{OL(AC)}$ | Switching Current Low  | $V_{CCI} > V_{OUT} \geq 0.6V_{CCI} *$    | $16V_{DDP}$                         |                                                                      | mA    |
|              |                        | $0.6V_{CCI} > V_{OUT} > 0.1V_{CCI} 1$    | $(26.7V_{OUT})$                     |                                                                      | mA    |
|              |                        | $0.18V_{CCI} > V_{OUT} > 0 *$            |                                     | See equation D – page 124 of the PCI Specification document rev. 2.2 |       |
|              | (Test Point)           | $V_{OUT} = 0.18V_{CC} *$                 |                                     | $38V_{CCI}$                                                          | mA    |
| $I_{CL}$     | Low Clamp Current      | $-3 < V_{IN} \leq -1$                    | $-25 + (V_{IN} + 1)/0.015$          |                                                                      | mA    |
| $I_{CH}$     | High Clamp Current     | $V_{CCI} + 4 > V_{IN} \geq V_{CCI} + 1$  | $25 + (V_{IN} - V_{DDP} - 1)/0.015$ |                                                                      | mA    |
| $slew_R$     | Output Rise Slew Rate  | $0.2V_{CCI}$ to $0.6V_{CCI}$ load *      | 1                                   | 4                                                                    | V/ns  |
| $slew_F$     | Output Fall Slew Rate  | $0.6V_{CCI}$ to $0.2V_{CCI}$ load *      | 1                                   | 4                                                                    | V/ns  |

**Note:** \* Refer to the PCI Specification document rev. 2.2.

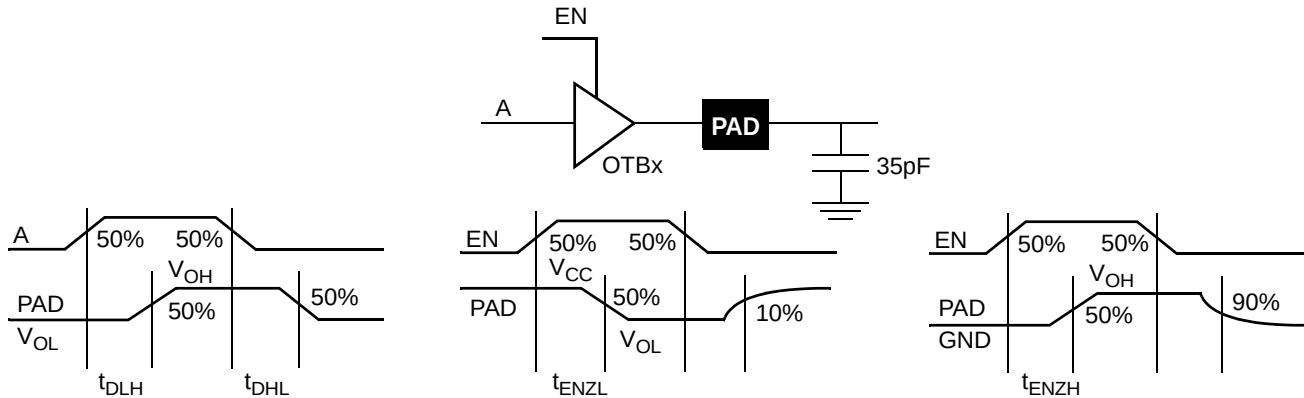
## Pad Loading Applicable to the Rising Edge PCI



## Pad Loading Applicable to the Falling Edge PCI



## Tristate Buffer Delays



## Tristate Buffer Delays

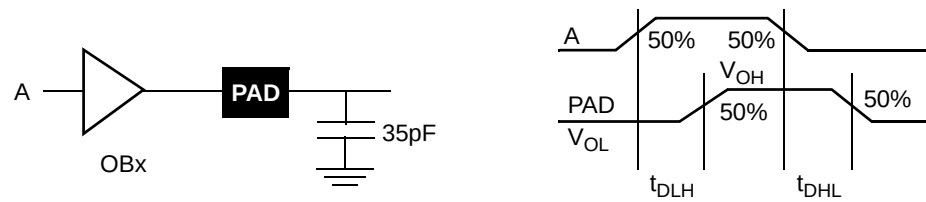
(Worst-Case Commercial Conditions,  $V_{DDP} = 3.0V$ ,  $V_{DD} = 2.3V$ , 35 pF load,  $T_J = 70^{\circ}C$ )

| Macro Type | Description                                             | Max $t_{DLH}$ <sup>1</sup> |     | Max $t_{DHL}$ <sup>2</sup> |     | Max $t_{ENZH}$ <sup>3</sup> |      | Max $t_{ENZL}$ <sup>4</sup> |      | Units |
|------------|---------------------------------------------------------|----------------------------|-----|----------------------------|-----|-----------------------------|------|-----------------------------|------|-------|
|            |                                                         | Std.                       | -F  | Std.                       | -F  | Std.                        | -F   | Std.                        | -F   |       |
| OTB33PH    | 3.3V, PCI Output Current, High Slew Rate                | 2.2                        | 2.6 | 2.0                        | 2.4 | 4.0                         | 4.8  | 3.3                         | 4.0  | ns    |
| OTB33PN    | 3.3V, High Output Current, Nominal Slew Rate            | 2.6                        | 3.1 | 2.4                        | 2.9 | 4.5                         | 5.4  | 5.0                         | 5.9  | ns    |
| OTB33PL    | 3.3V, High Output Current, Low Slew Rate                | 3.2                        | 3.8 | 3.1                        | 3.7 | 5.0                         | 5.9  | 6.2                         | 7.5  | ns    |
| OTB33LH    | 3.3V, Low Output Current, High Slew Rate                | 3.1                        | 3.7 | 3.4                        | 4.1 | 5.6                         | 6.7  | 5.5                         | 6.6  | ns    |
| OTB33LN    | 3.3V, Low Output Current, Nominal Slew Rate             | 3.9                        | 4.6 | 4.1                        | 4.9 | 6.3                         | 7.6  | 8.4                         | 10.0 | ns    |
| OTB33LL    | 3.3V, Low Output Current, Low Slew Rate                 | 4.4                        | 5.3 | 5.7                        | 6.8 | 7.0                         | 8.4  | 11.1                        | 13.3 | ns    |
| OTB25HH    | 2.5V, High Output Current, High Slew Rate               | 2.4                        | 2.9 | 2.0                        | 2.4 | 6.5                         | 7.8  | 3.2                         | 3.8  | ns    |
| OTB25HN    | 2.5V, High Output Current, Nominal Slew Rate            | 3.2                        | 3.8 | 2.9                        | 3.5 | 6.8                         | 8.1  | 4.6                         | 5.5  | ns    |
| OTB25HL    | 2.5V, High Output Current, Low Slew Rate                | 3.8                        | 4.5 | 3.2                        | 3.9 | 7.7                         | 9.2  | 5.8                         | 6.9  | ns    |
| OTB25LH    | 2.5V, Low Output Current, High Slew Rate                | 3.5                        | 4.2 | 4.4                        | 5.3 | 9.7                         | 11.7 | 4.9                         | 5.8  | ns    |
| OTB25LN    | 2.5V, Low Output Current, Nominal Slew Rate             | 5.1                        | 6.2 | 4.1                        | 5.0 | 10.4                        | 12.4 | 7.6                         | 9.1  | ns    |
| OTB25LL    | 2.5V, Low Output Current, Low Slew Rate                 | 6.4                        | 7.7 | 5.4                        | 6.5 | 11.2                        | 13.4 | 10.0                        | 12.0 | ns    |
| OTB25LPHH  | 2.5V, Low Power, High Output Current, High Slew Rate    | 5.3                        | 6.4 | 1.7                        | 2.1 | 4.8                         | 5.7  | 4.1                         | 5.0  | ns    |
| OTB25LPHN  | 2.5V, Low Power, High Output Current, Nominal Slew Rate | 5.3                        | 6.4 | 2.5                        | 3.0 | 5.6                         | 6.7  | 6.9                         | 8.3  | ns    |
| OTB25LPHL  | 2.5V, Low Power, High Output Current, Low Slew Rate     | 5.3                        | 6.4 | 3.9                        | 4.6 | 6.4                         | 7.7  | 8.7                         | 10.5 | ns    |
| OTB25LPLH  | 2.5V, Low Power, Low Output Current, High Slew Rate     | 8.3                        | 9.9 | 2.4                        | 2.9 | 6.9                         | 8.3  | 7.3                         | 8.7  | ns    |
| OTB25LPLN  | 2.5V, Low Power, Low Output Current, Nominal Slew Rate  | 8.3                        | 9.9 | 3.4                        | 4.1 | 8.0                         | 9.6  | 11.5                        | 13.8 | ns    |
| OTB25LPLL  | 2.5V, Low Power, Low Output Current, Low Slew Rate      | 8.3                        | 9.9 | 4.9                        | 5.8 | 9.2                         | 11.0 | 15.7                        | 18.8 | ns    |

### Notes:

- $t_{DLH}$  = Data-to-Pad HIGH
- $t_{DHL}$  = Data-to-Pad LOW
- $t_{ENZH}$  = Enable-to-Pad, Z to HIGH
- $t_{ENZL}$  = Enable-to-Pad, Z to LOW

## Output Buffer Delays



## Output Buffer Delays

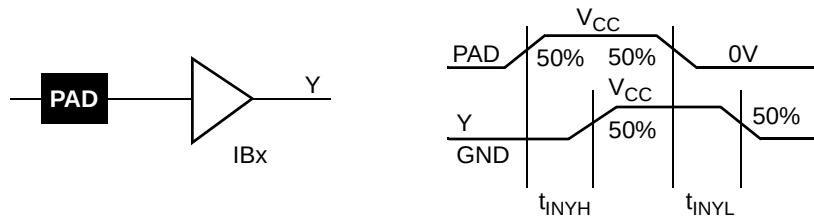
(Worst-Case Commercial Conditions,  $V_{DDP} = 3.0V$ ,  $V_{DD} = 2.3V$ , 35 pF load,  $T_J = 70^{\circ}C$ )

| Macro Type | Description                                             | Max $t_{DLH}^1$ |     | Max $t_{DHL}^2$ |     | Units |
|------------|---------------------------------------------------------|-----------------|-----|-----------------|-----|-------|
|            |                                                         | Std.            | -F  | Std.            | -F  |       |
| OB33PH     | 3.3V, PCI Output Current, High Slew Rate                | 2.2             | 2.6 | 2.0             | 2.4 | ns    |
| OB33PN     | 3.3V, High Output Current, Nominal Slew Rate            | 2.6             | 3.1 | 2.4             | 2.9 | ns    |
| OB33PL     | 3.3V, High Output Current, Low Slew Rate                | 3.2             | 3.8 | 3.1             | 3.7 | ns    |
| OB33LH     | 3.3V, Low Output Current, High Slew Rate                | 3.1             | 3.7 | 3.4             | 4.1 | ns    |
| OB33LN     | 3.3V, Low Output Current, Nominal Slew Rate             | 3.9             | 4.6 | 4.1             | 4.9 | ns    |
| OB33LL     | 3.3V, Low Output Current, Low Slew Rate                 | 4.4             | 5.3 | 5.7             | 6.8 | ns    |
| OB25HH     | 2.5V, High Output Current, High Slew Rate               | 2.4             | 2.9 | 2.0             | 2.4 | ns    |
| OB25HN     | 2.5V, High Output Current, Nominal Slew Rate            | 3.2             | 3.8 | 2.9             | 3.5 | ns    |
| OB25HL     | 2.5V, High Output Current, Low Slew Rate                | 3.8             | 4.5 | 3.2             | 3.9 | ns    |
| OB25LH     | 2.5V, Low Output Current, High Slew Rate                | 3.5             | 4.2 | 4.4             | 5.3 | ns    |
| OB25LN     | 2.5V, Low Output Current, Nominal Slew Rate             | 5.1             | 6.2 | 4.1             | 5.0 | ns    |
| OB25LL     | 2.5V, Low Output Current, Low Slew Rate                 | 6.4             | 7.7 | 5.4             | 6.5 | ns    |
| OB25LPHH   | 2.5V, Low Power, High Output Current, High Slew Rate    | 5.3             | 6.4 | 1.7             | 2.1 | ns    |
| OB25LPHN   | 2.5V, Low Power, High Output Current, Nominal Slew Rate | 5.3             | 6.4 | 2.5             | 3.0 | ns    |
| OB25LPHL   | 2.5V, Low Power, High Output Current, Low Slew Rate     | 5.3             | 6.4 | 3.9             | 4.6 | ns    |
| OB25LPLH   | 2.5V, Low Power, Low Output Current, High Slew Rate     | 8.3             | 9.9 | 2.4             | 2.9 | ns    |
| OB25LPLN   | 2.5V, Low Power, Low Output Current, Nominal Slew Rate  | 8.3             | 9.9 | 3.4             | 4.1 | ns    |
| OB25LPLL   | 2.5V, Low Power, Low Output Current, Low Slew Rate      | 8.3             | 9.9 | 4.9             | 5.8 | ns    |

**Notes:**

1.  $t_{DLH}$  = Data-to-Pad HIGH
2.  $t_{DHL}$  = Data-to-Pad LOW

## Input Buffer Delays



## Input Buffer Delays

(Worst-Case Commercial Conditions,  $V_{DDP} = 3.0V$ ,  $V_{DD} = 2.3V$ ,  $T_J = 70^{\circ}C$ )

| Macro Type | Description                                                                 | Max. $t_{INYH}^1$ |     | Max. $t_{INYL}^2$ |     | Units |
|------------|-----------------------------------------------------------------------------|-------------------|-----|-------------------|-----|-------|
|            |                                                                             | Std.              | -F  | Std.              | -F  |       |
| IB25       | 2.5V, CMOS Input Levels <sup>3</sup> , No Pull-up Resistor                  | 0.5               | 0.6 | 0.7               | 0.9 | ns    |
| IB25S      | 2.5V, CMOS Input Levels <sup>3</sup> , No Pull-up Resistor, Schmitt Trigger | 0.7               | 0.9 | 0.7               | 0.9 | ns    |
| IB25LP     | 2.5V, CMOS Input Levels <sup>3</sup> , Low Power                            | 0.8               | 1.0 | 0.8               | 1.0 | ns    |
| IB25LPS    | 2.5V, CMOS Input Levels <sup>3</sup> , Low Power, Schmitt Trigger           | 1.0               | 1.2 | 0.6               | 0.8 | ns    |
| IB33       | 3.3V, CMOS Input Levels <sup>3</sup> , No Pull-up Resistor                  | 0.8               | 1.0 | 0.5               | 0.6 | ns    |
| IB33S      | 3.3V, CMOS Input Levels <sup>3</sup> , No Pull-up Resistor, Schmitt Trigger | 1.1               | 1.3 | 0.5               | 0.6 | ns    |

### Notes:

- $t_{INYH}$  = Input Pad-to-Y HIGH
- $t_{INYL}$  = Input Pad-to-Y LOW
- LVTTL delays are the same as CMOS delays.

## Global Input Buffer Delays

(Worst-Case Commercial Conditions,  $V_{DDP} = 3.0V$ ,  $V_{DD} = 2.3V$ ,  $T_J = 70^{\circ}$ )

| Macro Type | Description                                                                 | Max. $t_{INYH}^1$ |     | Max. $t_{INYL}^2$ |     | Units |
|------------|-----------------------------------------------------------------------------|-------------------|-----|-------------------|-----|-------|
|            |                                                                             | Std.              | -F  | Std.              | -F  |       |
| GL25       | 2.5V, CMOS Input Levels <sup>3</sup> , No Pull-up Resistor                  | 1.6               | 1.9 | 1.6               | 1.9 | ns    |
| GL25S      | 2.5V, CMOS Input Levels <sup>3</sup> , No Pull-up Resistor, Schmitt Trigger | 1.7               | 2.1 | 1.4               | 1.7 | ns    |
| GL25LP     | 2.5V, CMOS Input Levels <sup>3</sup> , Low Power                            | 1.5               | 1.8 | 2.0               | 2.4 | ns    |
| GL25LPS    | 2.5V, CMOS Input Levels <sup>3</sup> , Low Power, Schmitt Trigger           | 1.7               | 2.1 | 1.7               | 2.1 | ns    |
| GL33       | 3.3V, CMOS Input Levels <sup>3</sup> , No Pull-up Resistor                  | 1.7               | 2.1 | 1.4               | 1.7 | ns    |
| GL33S      | 3.3V, CMOS Input Levels <sup>3</sup> , No Pull-up Resistor, Schmitt Trigger | 2.0               | 2.4 | 1.4               | 1.6 | ns    |
| PECL       | PPECL Input Levels                                                          | 2.4               | 2.9 | 2.0               | 2.4 | ns    |

### Notes:

- $t_{INYH}$  = Input Pad-to-Y HIGH
- $t_{INYL}$  = Input Pad-to-Y LOW
- LVTTL delays are the same as CMOS delays.

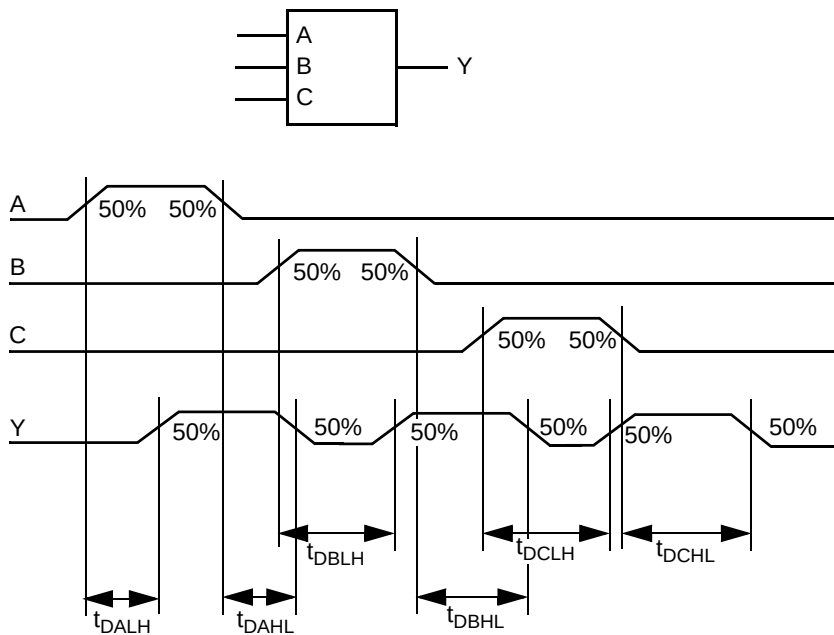
**Predicted Global Routing Delay\*****(Worst-Case Commercial Conditions,  $V_{DDP} = 3.0V$ ,  $V_{DD} = 2.3V$ ,  $T_J = 70^{\circ}C$ )**

| Parameter  | Description                              | Max. |     | Units |
|------------|------------------------------------------|------|-----|-------|
|            |                                          | Std. | –F  |       |
| $t_{RCKH}$ | Input Low to High (fully loaded row)     | 1.1  | 1.3 | ns    |
| $t_{RCKL}$ | Input High to Low (fully loaded row)     | 1.0  | 1.2 | ns    |
| $t_{RCKH}$ | Input Low to High (minimally loaded row) | 0.8  | 1.0 | ns    |
| $t_{RCKL}$ | Input High to Low (minimally loaded row) | 0.8  | 1.0 | ns    |

**Note:** \*The timing delay difference between tile locations is less than 15ps.**Global Routing Skew****(Worst-Case Commercial Conditions,  $V_{DDP} = 3.0V$ ,  $V_{DD} = 2.3V$ ,  $T_J = 70^{\circ}C$ )**

| Parameter    | Description              | Max. |     | Units |
|--------------|--------------------------|------|-----|-------|
|              |                          | Std. | –F  |       |
| $t_{RCKSWH}$ | Maximum Skew Low to High | 270  | 320 | ps    |
| $t_{RCKSHH}$ | Maximum Skew High to Low | 270  | 320 | ps    |

## Module Delays



## Sample Macrocell Library Listing\*

(Worst-Case Commercial Conditions,  $V_{DD} = 2.3V$ ,  $T_J = 70^\circ C$ )

| Cell Name | Description                                                  | Standard |         | -F      |         | Units |
|-----------|--------------------------------------------------------------|----------|---------|---------|---------|-------|
|           |                                                              | Maximum  | Minimum | Maximum | Minimum |       |
| NAND2     | 2-Input NAND                                                 | 0.6      |         | 0.7     |         | ns    |
| AND2      | 2-Input AND                                                  | 0.6      |         | 0.7     |         | ns    |
| NOR3      | 3-Input NOR                                                  | 0.6      |         | 0.7     |         | ns    |
| MUX2L     | 2-1 MUX with Active Low Select                               | 0.5      |         | 0.6     |         | ns    |
| OA21      | 2-Input OR into a 2-Input AND                                | 0.7      |         | 0.8     |         | ns    |
| XOR2      | 2-Input Exclusive OR                                         | 0.7      |         | 0.8     |         | ns    |
| LDL       | Active Low Latch (LH/HL)<br>CLK-Q LH                         | 0.5      |         | 0.6     |         | ns    |
|           | HL                                                           | 0.4      |         | 0.6     |         |       |
|           | $t_{setup}$                                                  |          | 0.8     | 0.5     | 0.6     |       |
|           | $t_{hold}$                                                   |          | 0.0     |         | 0.0     |       |
| DFFL      | Negative Edge-Triggered D-type Flip-Flop (LH/HL)<br>CLK-Q LH | 0.7      |         | 0.8     |         | ns    |
|           | HL                                                           | 0.7      |         | 0.8     |         |       |
|           | $t_{setup}$                                                  |          | 0.7     |         | 0.5     |       |
|           | $t_{hold}$                                                   |          | 0.0     |         | 0.0     |       |

**Note:** \*Intrinsic delays have a variable component, coupled to the input slope of the signal. These numbers assume an input slope typical of local interconnect.



## Recommended Operating Conditions

| Parameter                                                                 | Symbol                 | Limits                |
|---------------------------------------------------------------------------|------------------------|-----------------------|
|                                                                           |                        | Commercial/Industrial |
| Maximum Clock Frequency*                                                  | $f_{\text{CLOCK}}$     | 180 MHz               |
| Maximum RAM Frequency*                                                    | $f_{\text{RAM}}$       | 150 MHz               |
| Maximum Rise/Fall Time on Inputs*<br>• Schmitt Mode<br>• Non-schmitt Mode | $t_R/t_F$<br>$t_R/t_F$ | 100 ns<br>10 ns       |
| Maximum LVPECL Frequency*                                                 |                        | 180 MHz               |
| Maximum $t_{\text{CK}}$ Frequency (JTAG)                                  | $t_{\text{CK}}$        | 10 MHz                |

**Note:** \*–F parts will be 20% slower than standard commercial devices.

## Slew Rates Measured at C = 30pF, Nominal Power Supplies and 25°C

| Type     | Trig. Level | Rising Edge (nS) | Slew Rate (V/ns) | Falling Edge (nS) | Slew Rate (V/ns) | PCI Mode |
|----------|-------------|------------------|------------------|-------------------|------------------|----------|
| OB33PH   | 10%-90%     | 1.60             | 1.65             | 1.65              | 1.60             | Yes      |
| OB33PN   | 10%-90%     | 1.57             | 1.68             | 3.32              | 0.80             | No       |
| OB33PL   | 10%-90%     | 1.57             | 1.68             | 1.99              | 1.32             | No       |
| OB33LH   | 10%-90%     | 3.80             | 0.70             | 4.84              | 0.55             | No       |
| OB33LN   | 10%-90%     | 4.19             | 0.63             | 3.37              | 0.78             | No       |
| OB33LL   | 10%-90%     | 5.49             | 0.48             | 2.98              | 0.89             | No       |
| OB25HH   | 20%-60%     | 3.31             | 0.30             | 0.75              | 1.33             | No       |
| OB25HN   | 20%-60%     | 3.20             | 0.32             | 0.77              | 1.30             | No       |
| OB25HL   | 20%-60%     | 3.27             | 0.31             | 0.77              | 1.30             | No       |
| OB25LH   | 20%-60%     | 8.41             | 0.12             | 1.38              | 0.72             | No       |
| OB25LN   | 20%-60%     | 8.54             | 0.12             | 1.15              | 0.87             | No       |
| OB25LL   | 20%-60%     | 8.50             | 0.12             | 1.19              | 0.84             | No       |
| OB25LPHH | 10%-90%     | 1.55             | 1.29             | 1.56              | 1.28             | No       |
| OB25LPHN | 10%-90%     | 1.70             | 1.18             | 2.08              | 0.96             | No       |
| OB25LPHL | 10%-90%     | 1.97             | 1.02             | 2.09              | 0.96             | No       |
| OB25LPLH | 10%-90%     | 3.57             | 0.56             | 3.93              | 0.51             | No       |
| OB25LPLN | 10%-90%     | 4.65             | 0.43             | 3.28              | 0.61             | No       |
| OB25LPLL | 10%-90%     | 5.52             | 0.36             | 3.44              | 0.58             | No       |

**Note:** Standard and –F parts.

## Embedded Memory Specifications

This section discusses ProASIC<sup>PLUS</sup> SRAM/FIFO embedded memory and its interface signals, including timing diagrams that show the relationships of signals as they pertain to single embedded memory blocks (Table 11). Table 8 on page 22 shows basic SRAM and FIFO configurations. Simultaneous Read and Write to the same location must be done with care. On such accesses the DI bus is output to the DO bus.

### Enclosed Timing Diagrams—SRAM Mode:

- Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)
- Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)
- Asynchronous SRAM Write
- Asynchronous SRAM Read, Address Controlled, RDB=0
- Asynchronous SRAM Read, RDB Controlled
- Synchronous SRAM Write
- Embedded Memory Specifications

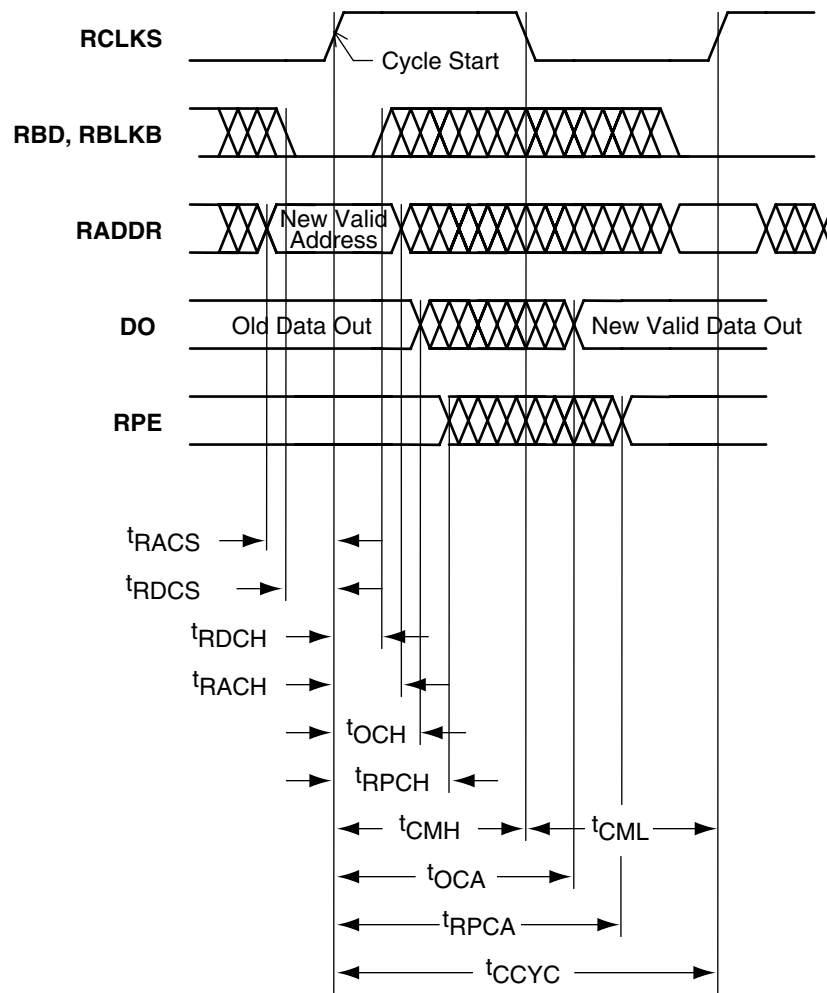
The difference between synchronous transparent and pipeline modes is the timing of all the output signals from the memory. In transparent mode, the outputs will change within the same clock cycle to reflect the data requested by the currently valid access to the memory. If clock cycles are short (high clock speed), the data requires most of the clock cycle to change to valid values (stable signals). Processing of this data in the same clock cycle is nearly impossible. Most designers add registers at all outputs of the memory to push the data processing into the next clock cycle. An entire clock cycle can then be used to process the data. To simplify use of this memory setup, suitable registers have been implemented as part of the memory primitive and are available to the user in the synchronous pipeline mode. In this mode, the output signals will change shortly after the second rising edge, following the initiation of the read access.

**Table 11 • Memory Block SRAM Interface Signals**

| SRAM Signal | Bits | In/Out | Description                                                   |
|-------------|------|--------|---------------------------------------------------------------|
| WCLKS       | 1    | IN     | Write clock used on synchronization on write side             |
| RCLKS       | 1    | IN     | Read clock used on synchronization on read side               |
| RADDR<0:7>  | 8    | IN     | Read address                                                  |
| RBLKB       | 1    | IN     | Negative true read block select                               |
| RDB         | 1    | IN     | Negative true read pulse                                      |
| WADDR<0:7>  | 8    | IN     | Write address                                                 |
| WBLKB       | 1    | IN     | Negative true write block select                              |
| DI<0:8>     | 9    | IN     | Input data bits <0:8>, <8> can be used for parity in          |
| WRB         | 1    | IN     | Negative true write pulse                                     |
| DO<0:8>     | 9    | OUT    | Output data bits <0:8>, <8> can be used for parity out        |
| RPE         | 1    | OUT    | Read parity error                                             |
| WPE         | 1    | OUT    | Write parity error                                            |
| PARODD      | 1    | IN     | Selects odd parity generation/detect when high, even when low |

**Note:** Not all signals shown are used in all modes.

## Synchronous SRAM Read, Access Timed Output Strobe (Synchronous Transparent)



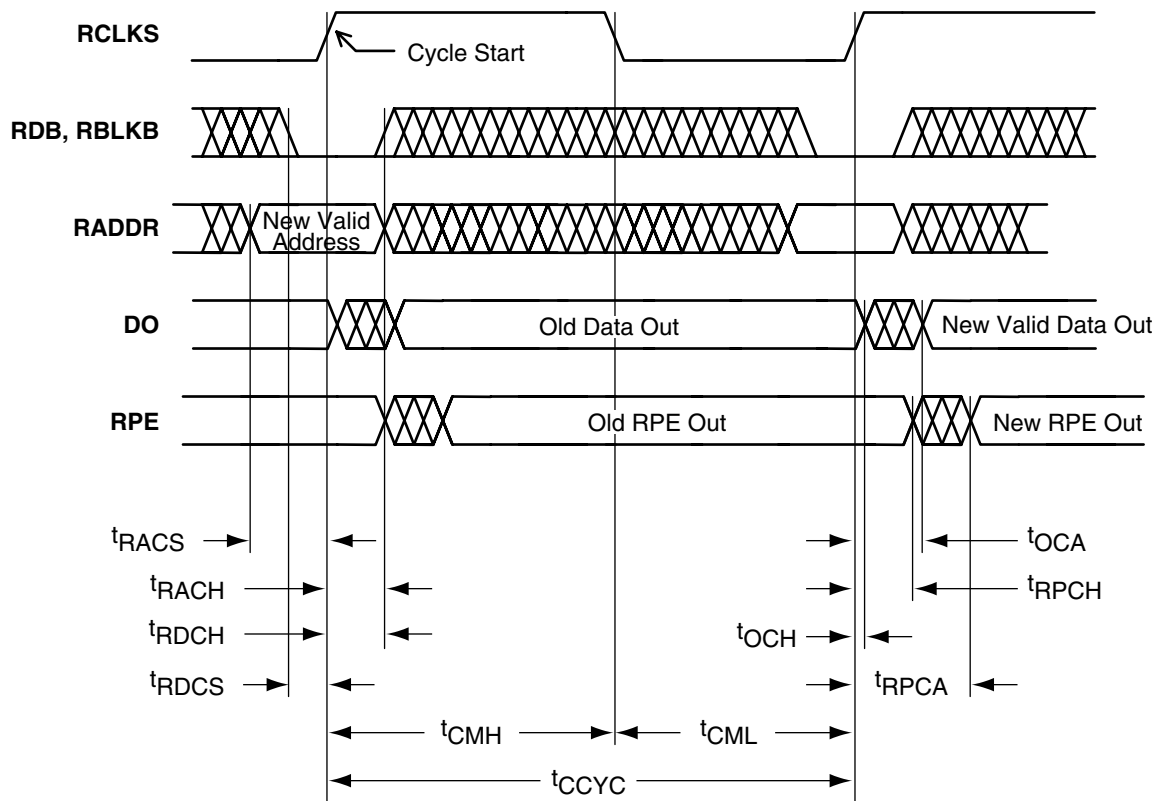
**Note:** The plot shows the normal operation status.

$T_J = 0^{\circ}\text{C to } 110^{\circ}\text{C}; V_{DD} = 2.3\text{V to } 2.7\text{V}$

| Symbol $t_{xxx}$ | Description                          | Min. | Max. | Units | Notes |
|------------------|--------------------------------------|------|------|-------|-------|
| CCYC             | Cycle time                           | 7.5  |      | ns    |       |
| CMH              | Clock high phase                     | 3.0  |      | ns    |       |
| CML              | Clock low phase                      | 3.0  |      | ns    |       |
| OCA              | New DO access from RCLKS $\uparrow$  | 7.5  |      | ns    |       |
| OCH              | Old DO valid from RCLKS $\uparrow$   |      | 3.0  | ns    |       |
| RACH             | RADDR hold from RCLKS $\uparrow$     | 0.5  |      | ns    |       |
| RACS             | RADDR setup to RCLKS $\uparrow$      | 1.0  |      | ns    |       |
| RDCH             | RDB hold from RCLKS $\uparrow$       | 0.5  |      | ns    |       |
| RDCH             | RDB setup to RCLKS $\uparrow$        | 1.0  |      | ns    |       |
| RPCA             | New RPE access from RCLKS $\uparrow$ | 9.5  |      | ns    |       |
| RPCH             | Old RPE valid from RCLKS $\uparrow$  |      | 3.0  | ns    |       |

**Note:** -F speed grade devices are 20% slower than the standard numbers.

## Synchronous SRAM Read, Pipeline Mode Outputs (Synchronous Pipelined)



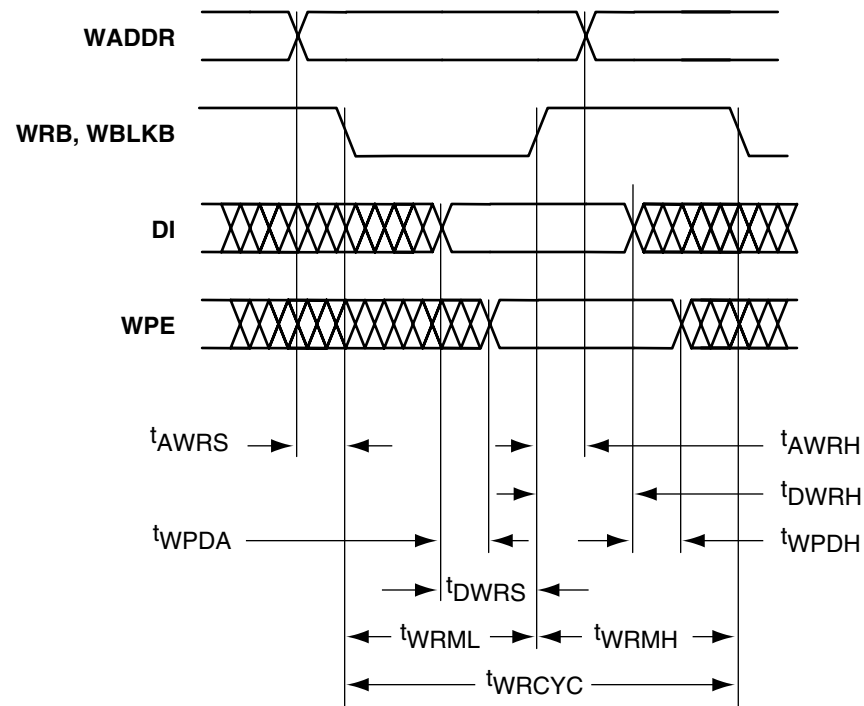
**Note:** The plot shows the normal operation status.

**T<sub>J</sub> = 0°C to 110°C; V<sub>DD</sub> = 2.3V to 2.7V**

| Symbol t <sub>xxx</sub> | Description                 | Min. | Max. | Units | Notes |
|-------------------------|-----------------------------|------|------|-------|-------|
| CCYC                    | Cycle time                  | 7.5  |      | ns    |       |
| CMH                     | Clock high phase            | 3.0  |      | ns    |       |
| CML                     | Clock low phase             | 3.0  |      | ns    |       |
| OCA                     | New DO access from RCLKS ↑  | 2.0  |      | ns    |       |
| OCH                     | Old DO valid from RCLKS ↑   |      | 0.75 | ns    |       |
| RACH                    | RADDR hold from RCLKS ↑     | 0.5  |      | ns    |       |
| RACS                    | RADDR setup to RCLKS ↑      | 1.0  |      | ns    |       |
| RDCH                    | RDB hold from RCLKS ↑       | 0.5  |      | ns    |       |
| RDCS                    | RDB setup to RCLKS ↑        | 1.0  |      | ns    |       |
| RPCA                    | New RPE access from RCLKS ↑ | 4.0  |      | ns    |       |
| RPCH                    | Old RPE valid from RCLKS ↑  |      | 1.0  | ns    |       |

**Note:** -F speed grade devices are 20% slower than the standard numbers.

## Asynchronous SRAM Write



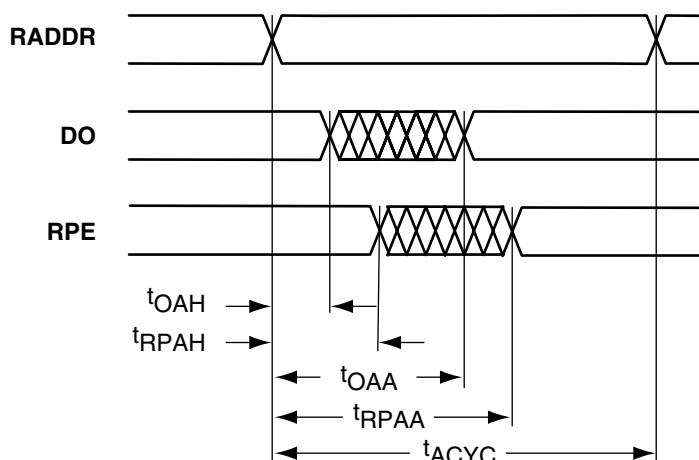
**Note:** The plot shows the normal operation status.

**T<sub>J</sub> = 0°C to 110°C; V<sub>DD</sub> = 2.3V to 2.7V**

| Symbol t <sub>xxx</sub> | Description          | Min. | Max. | Units | Notes                                    |
|-------------------------|----------------------|------|------|-------|------------------------------------------|
| AWRH                    | WADDR hold from WB ↑ | 1.0  |      | ns    |                                          |
| AWRS                    | WADDR setup to WB ↓  | 0.5  |      | ns    |                                          |
| DWRH                    | DI hold from WB ↑    | 1.5  |      | ns    |                                          |
| DWRS                    | DI setup to WB ↑     | 0.5  |      | ns    | PARGEN is inactive                       |
| DWRS                    | DI setup to WB ↑     | 2.5  |      | ns    | PARGEN is active                         |
| WPDA                    | WPE access from DI   | 3.0  |      | ns    | WPE is invalid while<br>PARGEN is active |
| WPDH                    | WPE hold from DI     |      | 1.0  | ns    |                                          |
| WRCYC                   | Cycle time           | 7.5  |      | ns    |                                          |
| WRMH                    | WB high phase        | 3.0  |      | ns    | Inactive                                 |
| WRML                    | WB low phase         | 3.0  |      | ns    | Active                                   |

**Note:** –F speed grade devices are 20% slower than the standard numbers.

# Asynchronous SRAM Read, Address Controlled, RDB=0



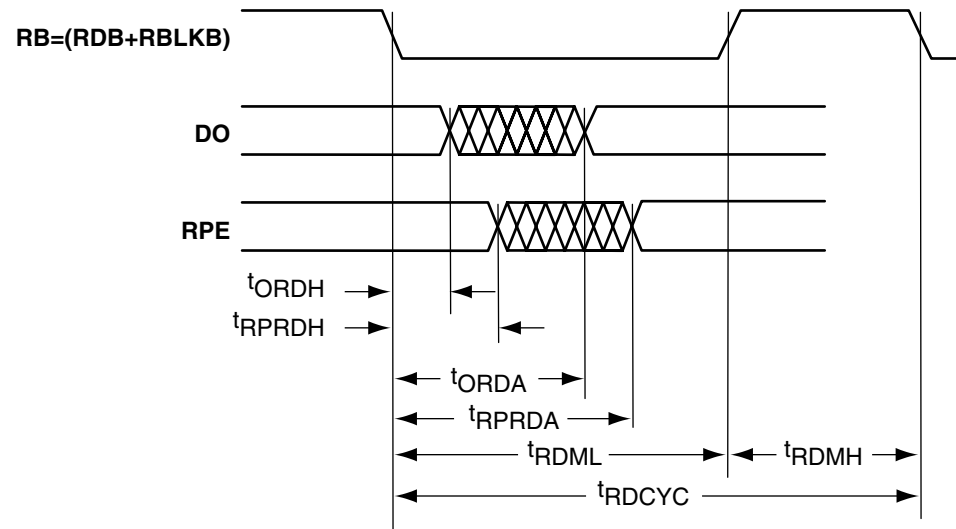
**Note:** The plot shows the normal operation status.

**T<sub>J</sub> = 0°C to 110°C; V<sub>DD</sub> = 2.3V to 2.7V**

| Symbol t <sub>xxx</sub> | Description                      | Min. | Max. | Units | Notes |
|-------------------------|----------------------------------|------|------|-------|-------|
| ACYC                    | Read cycle time                  | 7.5  |      | ns    |       |
| OAA                     | New DO access from RADDR stable  | 7.5  |      | ns    |       |
| OAHA                    | Old DO hold from RADDR stable    |      | 3.0  | ns    |       |
| RPAA                    | New RPE access from RADDR stable | 10.0 |      | ns    |       |
| RPAHA                   | Old RPE hold from RADDR stable   |      | 3.0  | ns    |       |

**Note:** -F speed grade devices are 20% slower than the standard numbers.

## Asynchronous SRAM Read, RDB Controlled



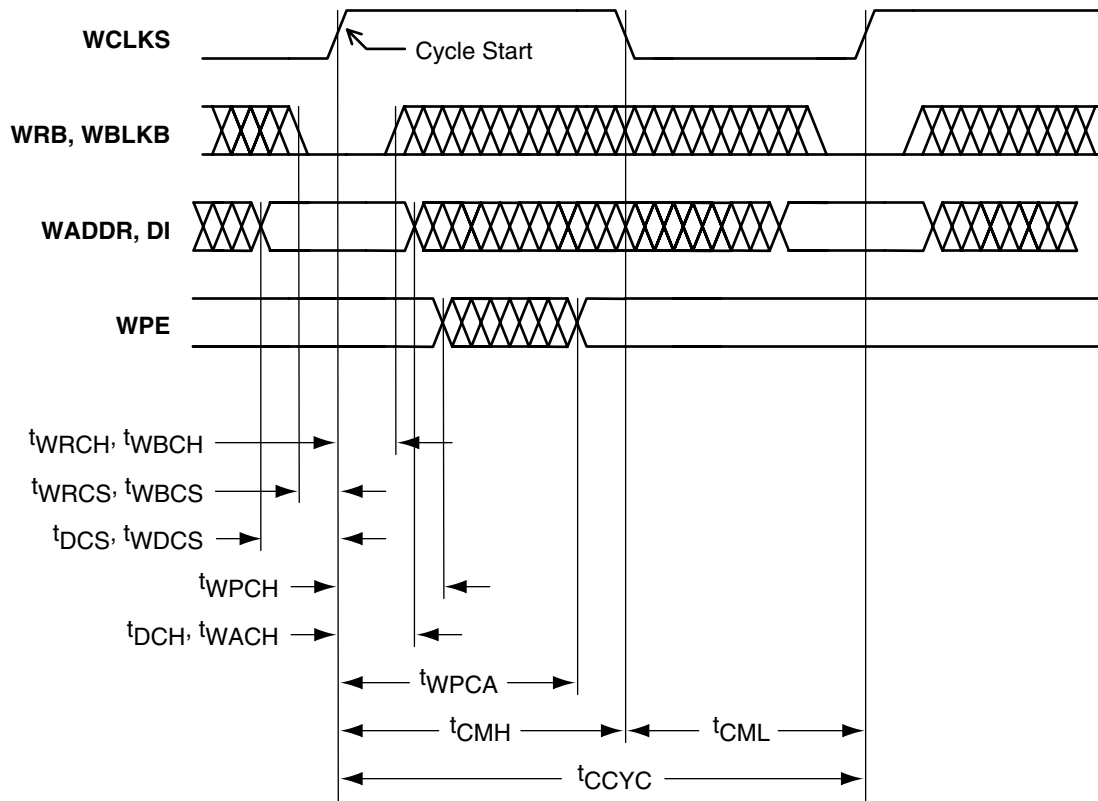
**Note:** The plot shows the normal operation status.

$T_J = 0^{\circ}\text{C to } 110^{\circ}\text{C}; V_{DD} = 2.3\text{V to } 2.7\text{V}$

| Symbol $t_{xxx}$ | Description              | Min. | Max. | Units | Notes                       |
|------------------|--------------------------|------|------|-------|-----------------------------|
| ORDA             | New DO access from RB ↓  | 7.5  |      | ns    |                             |
| ORDH             | Old DO valid from RB ↓   |      | 3.0  | ns    |                             |
| RDCYC            | Read cycle time          | 7.5  |      | ns    |                             |
| RDMH             | RB high phase            | 3.0  |      | ns    | Inactive setup to new cycle |
| RDML             | RB low phase             | 3.0  |      | ns    | Active                      |
| RPRDA            | New RPE access from RB ↓ | 9.5  |      | ns    |                             |
| RPRDH            | Old RPE valid from RB ↓  |      | 3.0  | ns    |                             |

**Note:** –F speed grade devices are 20% slower than the standard numbers.

## Synchronous SRAM Write



**Note:** The plot shows the normal operation status.

$T_J = 0^{\circ}\text{C to } 110^{\circ}\text{C}; V_{DD} = 2.3\text{V to } 2.7\text{V}$

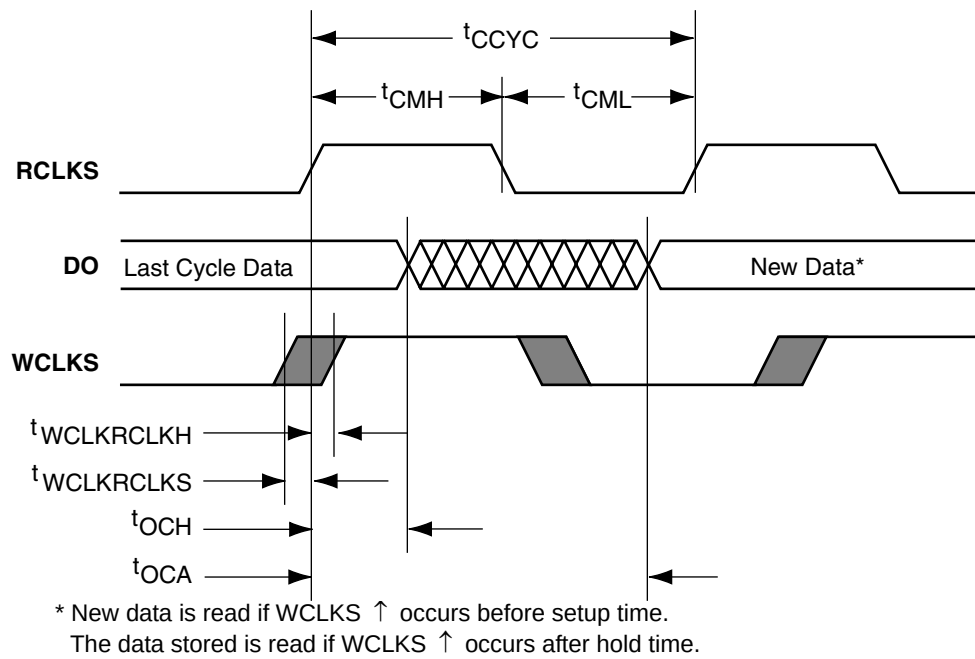
| Symbol $t_{xxx}$ | Description                   | Min. | Max. | Units | Notes                                 |
|------------------|-------------------------------|------|------|-------|---------------------------------------|
| CCYC             | Cycle time                    | 7.5  |      | ns    |                                       |
| CMH              | Clock high phase              | 3.0  |      | ns    |                                       |
| CML              | Clock low phase               | 3.0  |      | ns    |                                       |
| DCH              | DI hold from WCLKS ↑          | 0.5  |      | ns    |                                       |
| DCS              | DI setup to WCLKS ↑           | 1.0  |      | ns    |                                       |
| WACH             | WADDR hold from WCLKS ↑       | 0.5  |      | ns    |                                       |
| WDCS             | WADDR setup to WCLKS ↑        | 1.0  |      | ns    |                                       |
| WPCA             | New WPE access from WCLKS ↑   | 3.0  |      | ns    | WPE is invalid while PARGEN is active |
| WPCH             | Old WPE valid from WCLKS ↑    |      | 0.5  | ns    |                                       |
| WRCH, WBCH       | WRB & WBLKB hold from WCLKS ↑ | 0.5  |      | ns    |                                       |
| WRCS, WBCS       | WRB & WBLKB setup to WCLKS ↑  | 1.0  |      | ns    |                                       |

### Notes:

- On simultaneous read and write accesses to the same location DI is output to DO.
- F speed grade devices are 20% slower than the standard numbers.



## Synchronous Write and Read to the Same Location



**Note:** The plot shows the normal operation status.

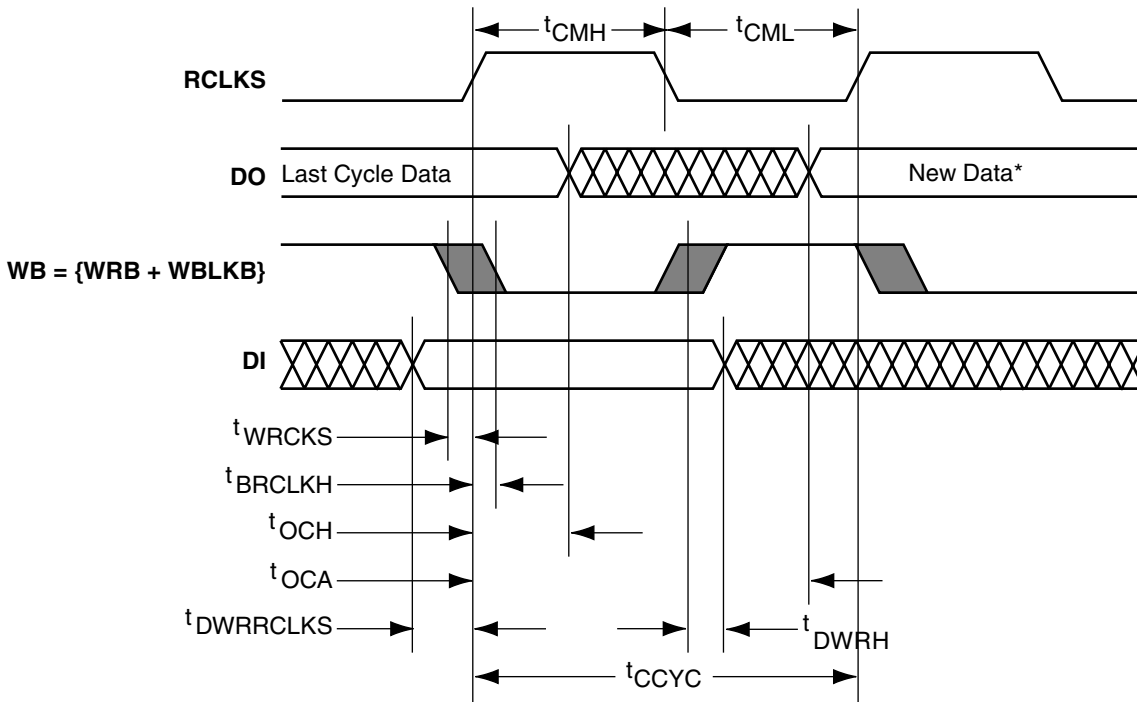
$T_J = 0^{\circ}\text{C to } 110^{\circ}\text{C}; V_{DD} = 2.3\text{V to } 2.7\text{V}$

| Symbol $t_{xxx}$ | Description                   | Min. | Max. | Units | Notes                                     |
|------------------|-------------------------------|------|------|-------|-------------------------------------------|
| CCYC             | Cycle time                    | 7.5  |      | ns    |                                           |
| CMH              | Clock high phase              | 3.0  |      | ns    |                                           |
| CML              | Clock low phase               | 3.0  |      | ns    |                                           |
| WCLKRCLKS        | WCLKS ↑ to RCLKS ↑ setup time | -0.1 |      | ns    |                                           |
| WCLKRCLKH        | WCLKS ↑ to RCLKS ↑ hold time  |      | 7.0  | ns    |                                           |
| OCH              | Old DO valid from RCLKS ↑     |      | 3.0  | ns    | OCA/OCH displayed for Access Timed Output |
| OCA              | New DO valid from RCLKS ↑     | 7.5  |      | ns    |                                           |

**Notes:**

1. This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.
2. During synchronous write and synchronous read access to the same location, the new write data will be read out if the active write clock edge occurs before or at the same time as the active read clock edge. The negative setup time insures this behavior for WCLKS and RCLKS driven by the same design signal.
3. If WCLKS changes after the hold time, the data will be read.
4. A setup or hold time violation will result in unknown output data.
5. -F speed grade devices are 20% slower than the standard numbers.

## Asynchronous Write and Synchronous Read to the Same Location



**Note:** The plot shows the normal operation status.

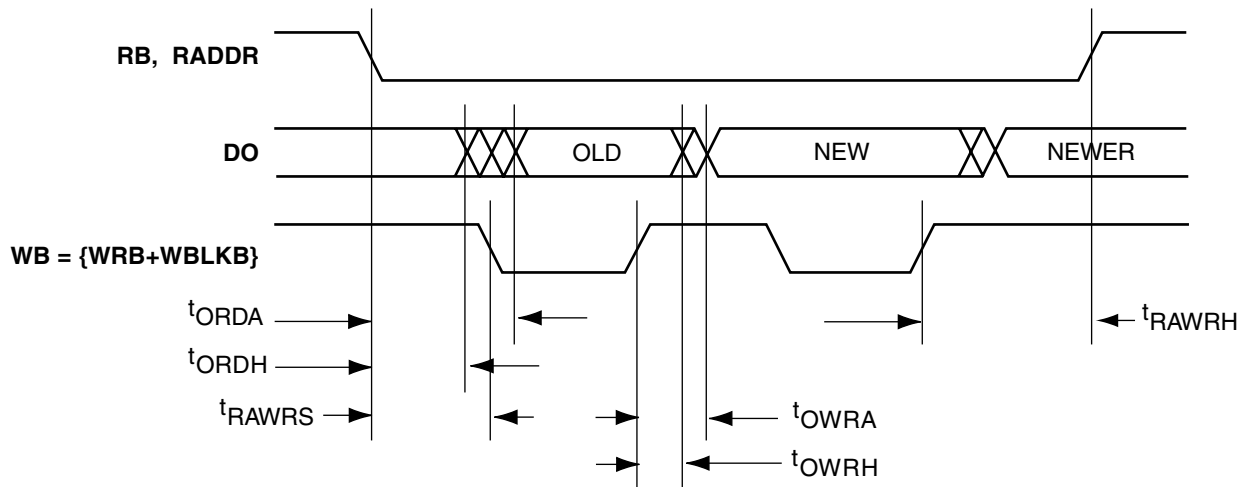
**T<sub>J</sub> = 0°C to 110°C; V<sub>DD</sub> = 2.3V to 2.7V**

| Symbol t <sub>xxx</sub> | Description                | Min. | Max. | Units | Notes                                     |
|-------------------------|----------------------------|------|------|-------|-------------------------------------------|
| CCYC                    | Cycle time                 | 7.5  |      | ns    |                                           |
| CMH                     | Clock high phase           | 3.0  |      | ns    |                                           |
| CML                     | Clock low phase            | 3.0  |      | ns    |                                           |
| WBRCLKS                 | WB ↓ to RCLKS ↑ setup time | -0.1 |      | ns    |                                           |
| WBRCLKH                 | WB ↓ to RCLKS ↑ hold time  |      | 7.0  | ns    |                                           |
| OCH                     | Old DO valid from RCLKS ↑  |      | 3.0  | ns    | OCA/OCH displayed for Access Timed Output |
| OCA                     | New DO valid from RCLKS ↑  | 7.5  |      | ns    |                                           |
| DWRCLKS                 | DI to RCLKS ↑ setup time   | 0    |      | ns    |                                           |
| DWRH                    | DI to WB ↑ hold time       |      | 1.5  | ns    |                                           |

### Notes:

1. This behavior is valid for Access Timed Output and Pipelined Mode Output. The table shows the timings of an Access Timed Output.
2. In asynchronous write and synchronous read access to the same location, the new write data will be read out if the active write signal edge occurs before or at the same time as the active read clock edge. If WB changes to low after hold time, the data will be read.
3. A setup or hold time violation will result in unknown output data.
4. -F speed grade devices are 20% slower than the standard numbers.

## Asynchronous Write and Read to the Same Location



**Note:** The plot shows the normal operation status.

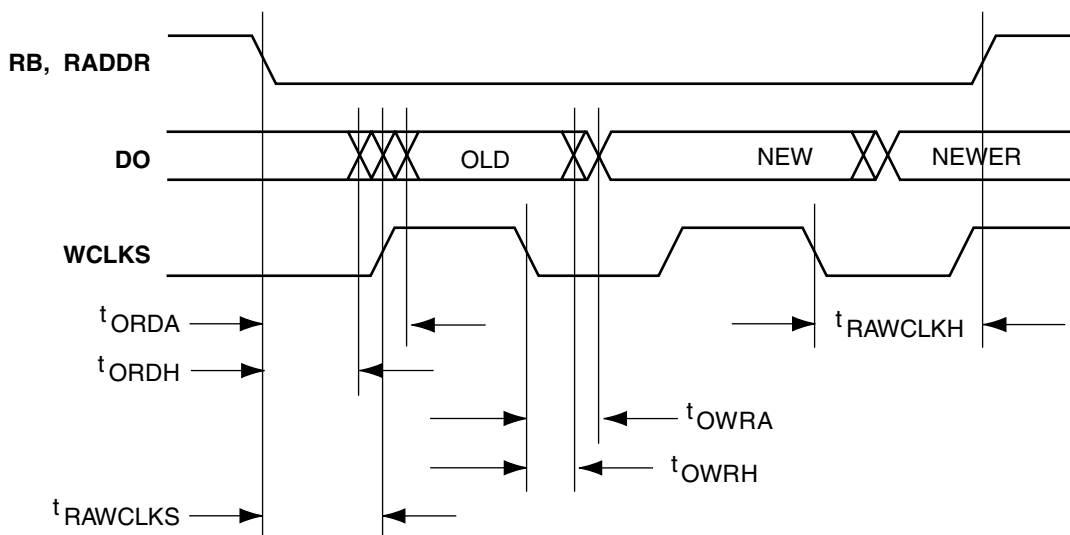
$T_J = 0^{\circ}\text{C to } 110^{\circ}\text{C}; V_{DD} = 2.3\text{V to } 2.7\text{V}$

| Symbol $t_{xxx}$ | Description             | Min. | Max. | Units | Notes |
|------------------|-------------------------|------|------|-------|-------|
| ORDA             | New DO access from RB ↓ | 7.5  |      | ns    |       |
| ORDH             | Old DO valid from RB ↓  |      | 3.0  | ns    |       |
| OWRA             | New DO access from WB ↑ | 3.0  |      | ns    |       |
| OWRH             | Old DO valid from WB ↑  |      | 0.5  | ns    |       |
| RAWRS            | RB ↓ or RADDR from WB ↓ | 5.0  |      | ns    |       |
| RAWRH            | RB ↑ or RADDR from WB ↑ | 5.0  |      | ns    |       |

**Notes:**

1. During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data.
2. Violation of RAWRS will disturb access to the OLD data.
3. Violation of RAWRH will disturb access to the NEWER data.
4. -F speed grade devices are 20% slower than the standard numbers.

## Synchronous Write and Asynchronous Read to the Same Location



**Note:** The plot shows the normal operation status.

$T_J = 0^{\circ}\text{C}$  to  $110^{\circ}\text{C}$ ;  $V_{DD} = 2.3\text{V}$  to  $2.7\text{V}$

| Symbol $t_{xxx}$ | Description                | Min. | Max. | Units | Notes |
|------------------|----------------------------|------|------|-------|-------|
| ORDA             | New DO access from RB ↓    | 7.5  |      | ns    |       |
| ORDH             | Old DO valid from RB ↓     |      | 3.0  | ns    |       |
| OWRA             | New DO access from WCLKS ↓ | 3.0  |      | ns    |       |
| OWRH             | Old DO valid from WCLKS ↓  |      | 0.5  | ns    |       |
| RAWCLKS          | RB ↓ or RADDR from WCLKS ↑ | 5.0  |      | ns    |       |
| RAWCLKH          | RB ↑ or RADDR from WCLKS ↓ | 5.0  |      | ns    |       |

### Notes:

- During an asynchronous read cycle, each write operation (synchronous or asynchronous) to the same location will automatically trigger a read operation which updates the read data.
- Violation of RAWCLKS will disturb access to OLD data.
- Violation of RAWCLKH will disturb access to NEWER data.
- F speed grade devices are 20% slower than the standard numbers.

**Asynchronous FIFO Full and Empty Transitions**

The asynchronous FIFO accepts writes and reads while not full or not empty. When the FIFO is full, all writes are inhibited. Conversely, when the FIFO is empty, all reads are inhibited. A problem is created if the FIFO is written during the transition out of full to not full or read during the transition out of empty to not empty. The exact time at which the write or read operation changes from inhibited to accepted after the read (write) signal which causes the transition from full or empty to not full or not empty is indeterminate. This indeterminate period starts 1 ns after the RB (WB) transition, which deactivates full or not empty and ends 3 ns after the RB (WB) transition for slow cycles. For fast cycles, the indeterminate period ends 3 ns (7.5 ns – RDL (WRL)) after the RB (WB) transition, whichever is later (Table 12).

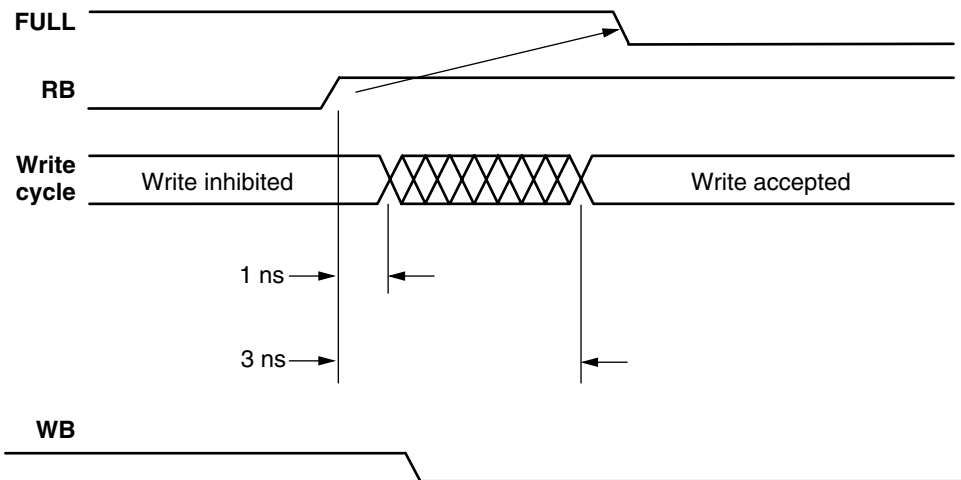
The timing diagram for write is shown in Figure 25 on page 54. The timing diagram for read is shown in Figure 26 on page 54. For basic SRAM configurations, see Table 9 on page 23.

**Enclosed Timing Diagrams – FIFO Mode:**

- Asynchronous FIFO Read
- Asynchronous FIFO Write
- Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)
- Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)
- Synchronous FIFO Write
- FIFO Reset

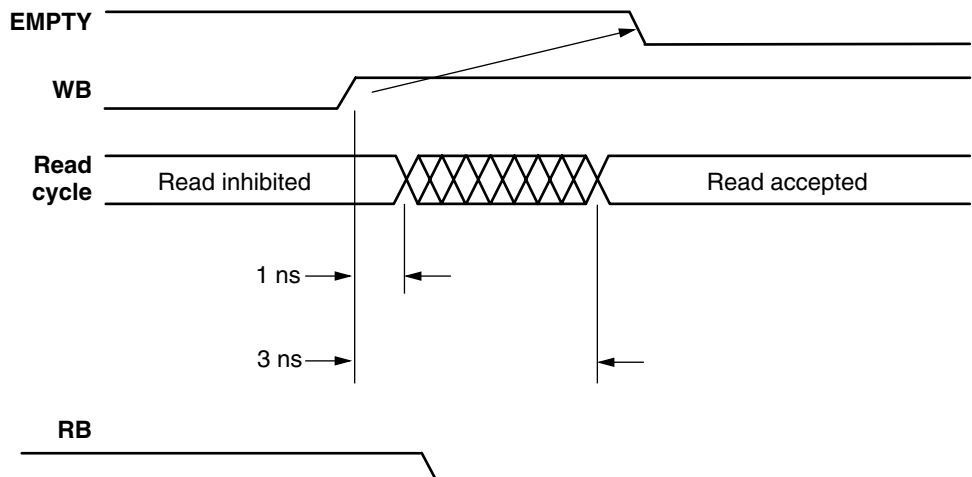
**Table 12 • Memory Block FIFO Interface Signals**

| FIFO Signal | Bits | In/Out | Description                                                                                                                                 |
|-------------|------|--------|---------------------------------------------------------------------------------------------------------------------------------------------|
| WCLKS       | 1    | IN     | Write clock used for synchronization on write side                                                                                          |
| RCLKS       | 1    | IN     | Read clock used for synchronization on read side                                                                                            |
| LEVEL <0:7> | 8    | IN     | Direct configuration implements static flag logic                                                                                           |
| RBLKB       | 1    | IN     | Negative true read block select                                                                                                             |
| RDB         | 1    | IN     | Negative true read pulse                                                                                                                    |
| RESET       | 1    | IN     | Negative true reset for FIFO pointers                                                                                                       |
| WBLKB       | 1    | IN     | Negative true write block select                                                                                                            |
| DI<0:8>     | 9    | IN     | Input data bits <0:8>, <8> will be generated if PARGEN is true                                                                              |
| WRB         | 1    | IN     | Negative true write pulse                                                                                                                   |
| FULL, EMPTY | 2    | OUT    | FIFO flags. FULL prevents write and EMPTY prevents read                                                                                     |
| EQTH, GEQTH | 2    | OUT    | EQTH is true when the FIFO holds the number of words specified by the LEVEL signal. GEQTH is true when the FIFO holds (LEVEL) words or more |
| DO<0:8>     | 9    | OUT    | Output data bits <0:8>                                                                                                                      |
| RPE         | 1    | OUT    | Read parity error                                                                                                                           |
| WPE         | 1    | OUT    | Write parity error                                                                                                                          |
| LGDEP <0:2> | 3    | IN     | Configures DEPTH of the FIFO to 2 <sup>(LGDEP+1)</sup>                                                                                      |
| PARODD      | 1    | IN     | Selects odd parity generation/detect when high, even when low                                                                               |



**Note:** –F speed grade devices are 20% slower than the standard numbers.

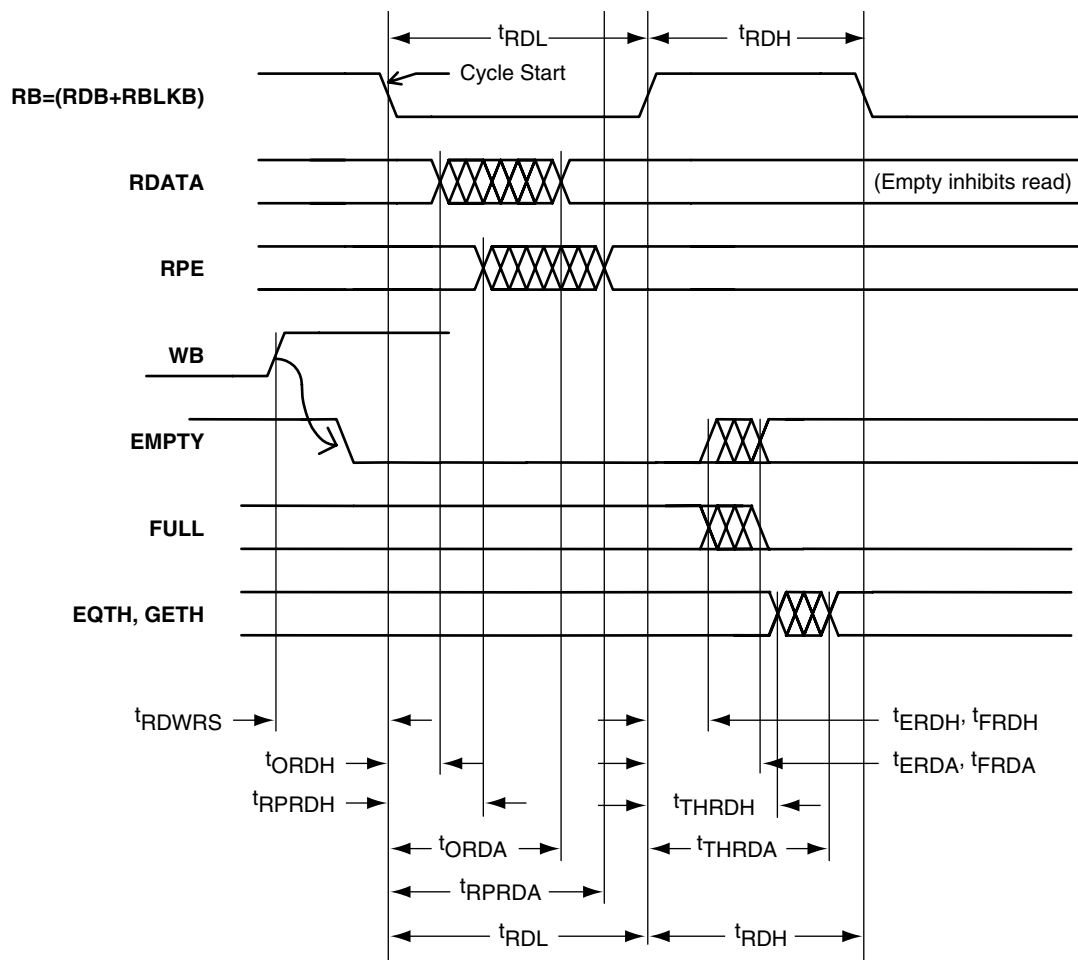
**Figure 25 • Write Timing Diagram**



**Note:** –F speed grade devices are 20% slower than the standard numbers.

**Figure 26 • Read Timing Diagram**

## Asynchronous FIFO Read



**Note:** The plot shows the normal operation status.

**T<sub>J</sub> = 0°C to 110°C; V<sub>DD</sub> = 2.3V to 2.7V**

| Symbol t <sub>xxx</sub> | Description                                             | Min.             | Max. | Units | Notes                                                                               |
|-------------------------|---------------------------------------------------------|------------------|------|-------|-------------------------------------------------------------------------------------|
| ERDH, FRDH, THRDH       | Old EMPTY, FULL, EQTH, & GETH valid hold time from RB ↑ |                  | 0.5  | ns    | Empty/full/thresh are invalid from the end of hold until the new access is complete |
| ERDA                    | New EMPTY access from RB ↑                              | 3.0 <sup>1</sup> |      | ns    |                                                                                     |
| FRDA                    | FULL↓ access from RB ↑                                  | 3.0 <sup>1</sup> |      | ns    |                                                                                     |
| ORDA                    | New DO access from RB ↓                                 | 7.5              |      | ns    |                                                                                     |
| ORDH                    | Old DO valid from RB ↓                                  |                  | 3.0  | ns    |                                                                                     |
| RDCYC                   | Read cycle time                                         | 7.5              |      | ns    |                                                                                     |
| RDWRS                   | WB ↑, clearing EMPTY, setup to RB ↓                     | 3.0 <sup>2</sup> |      | ns    | Enabling the read operation                                                         |
|                         |                                                         |                  | 1.0  | ns    | Inhibiting the read operation                                                       |
| RDH                     | RB high phase                                           | 3.0              |      | ns    | Inactive                                                                            |
| RDL                     | RB low phase                                            | 3.0              |      | ns    | Active                                                                              |
| RPRDA                   | New RPE access from RB ↓                                | 9.5              |      | ns    |                                                                                     |
| RPRDH                   | Old RPE valid from RB ↓                                 |                  | 4.0  | ns    |                                                                                     |
| THRDA                   | EQTH or GETH access from RB↑                            | 4.5              |      | ns    |                                                                                     |

**Notes:**

1. At fast cycles, ERDA and FRDA = MAX (7.5 ns – RDL), 3.0 ns.
2. At fast cycles, RDWRS (for enabling read) = MAX (7.5 ns – WRL), 3.0 ns.
3. –F speed grade devices are 20% slower than the standard numbers.

WB=(WRB+WBLKB)

Cycle Start

WDATA (Full inhibits write)

WPE

RB

FULL

EMPTY

EQTH, GETH

$t_{WRRDS}$

$t_{DWRH}$

$t_{WPDA}$

$t_{WPDH}$

$t_{DWRS}$

$t_{EWRH}, t_{FWRH}$

$t_{EWRA}, t_{FWRA}$

$t_{THWRH}$

$t_{THWRA}$

$t_{WRL}$

$t_{WRH}$

$t_{WRCYC}$

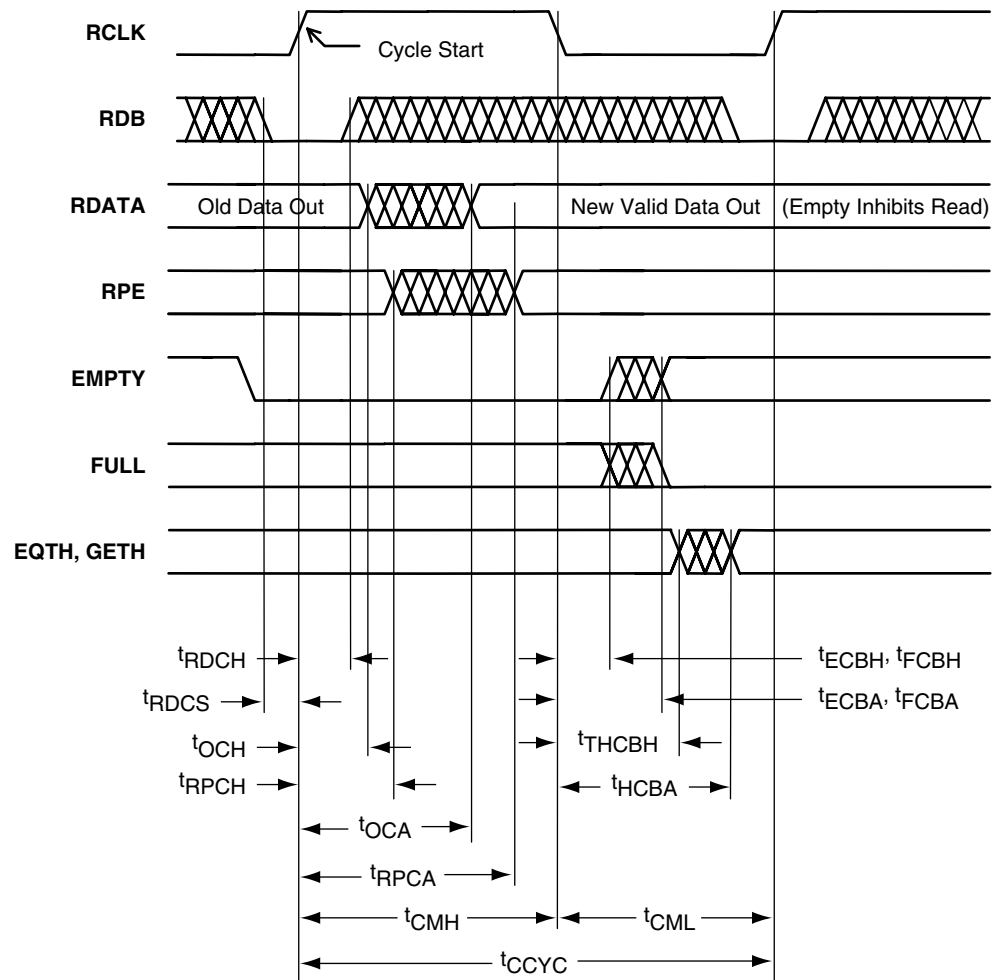
**T<sub>J</sub> = 0°C to 110°C; V<sub>DD</sub> = 2.3V to 2.7V**

**Notes:**

1. At fast cycles, EWRA, FWRA = MAX (7.5 ns - WRL), 3.0 ns.
2. At fast cycles, WRDLS (for enabling write) = MAX (7.5 ns - RDL), 3.0 ns.
3. -F speed grade devices are 20% slower than the standard numbers.



### Synchronous FIFO Read, Access Timed Output Strobe (Synchronous Transparent)



**Note:** *The plot shows the normal operation status.*

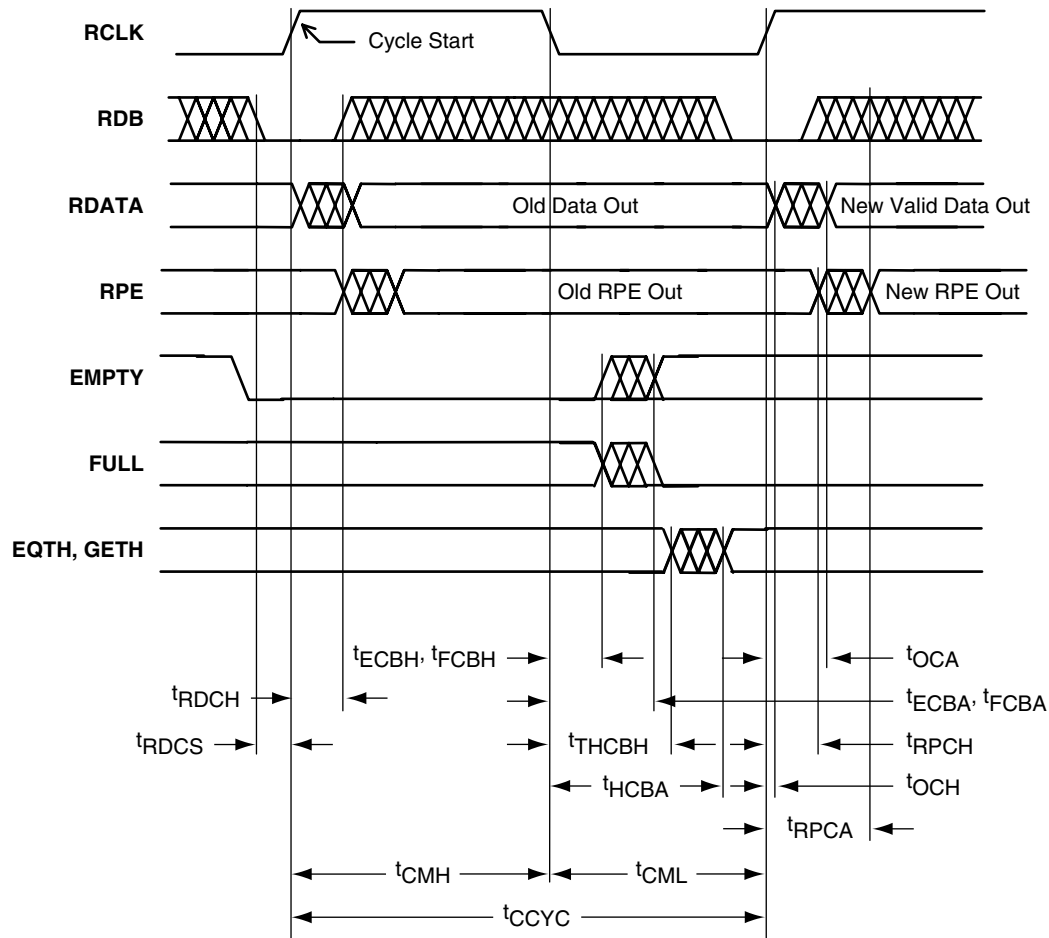
**$T_J = 0^{\circ}\text{C}$  to  $110^{\circ}\text{C}$ ;  $V_{DD} = 2.3\text{V}$  to  $2.7\text{V}$**

| Symbol t <sub>xxx</sub> | Description                                                | Min.             | Max. | Units | Notes                                                                               |
|-------------------------|------------------------------------------------------------|------------------|------|-------|-------------------------------------------------------------------------------------|
| CCYC                    | Cycle time                                                 | 7.5              |      | ns    |                                                                                     |
| CMH                     | Clock high phase                                           | 3.0              |      | ns    |                                                                                     |
| CML                     | Clock low phase                                            | 3.0              |      | ns    |                                                                                     |
| ECBA                    | New EMPTY access from RCLKS ↓                              | 3.0 <sup>1</sup> |      | ns    |                                                                                     |
| FCBA                    | FULL ↓ access from RCLKS ↓                                 | 3.0 <sup>1</sup> |      | ns    |                                                                                     |
| ECBH,<br>FCBH,<br>THCBH | Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓ |                  | 1.0  | ns    | Empty/full/thresh are invalid from the end of hold until the new access is complete |
| OCA                     | New DO access from RCLKS ↑                                 | 7.5              |      | ns    |                                                                                     |
| OCH                     | Old DO valid from RCLKS ↑                                  |                  | 3.0  | ns    |                                                                                     |
| RDCH                    | RDB hold from RCLKS ↑                                      | 0.5              |      | ns    |                                                                                     |
| RDCS                    | RDB setup to RCLKS ↑                                       | 1.0              |      | ns    |                                                                                     |
| RPCA                    | New RPE access from RCLKS ↑                                | 9.5              |      | ns    |                                                                                     |
| RPCH                    | Old RPE valid from RCLKS ↑                                 |                  | 3.0  | ns    |                                                                                     |
| HCBA                    | EQTH or GETH access from RCLKS ↓                           | 4.5              |      | ns    |                                                                                     |

**Notes:**

1. At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.
2. -F speed grade devices are 20% slower than the standard numbers.

# Synchronous FIFO Read, Pipeline Mode Outputs (Synchronous Pipelined)



**Note:** The plot shows the normal operation status.

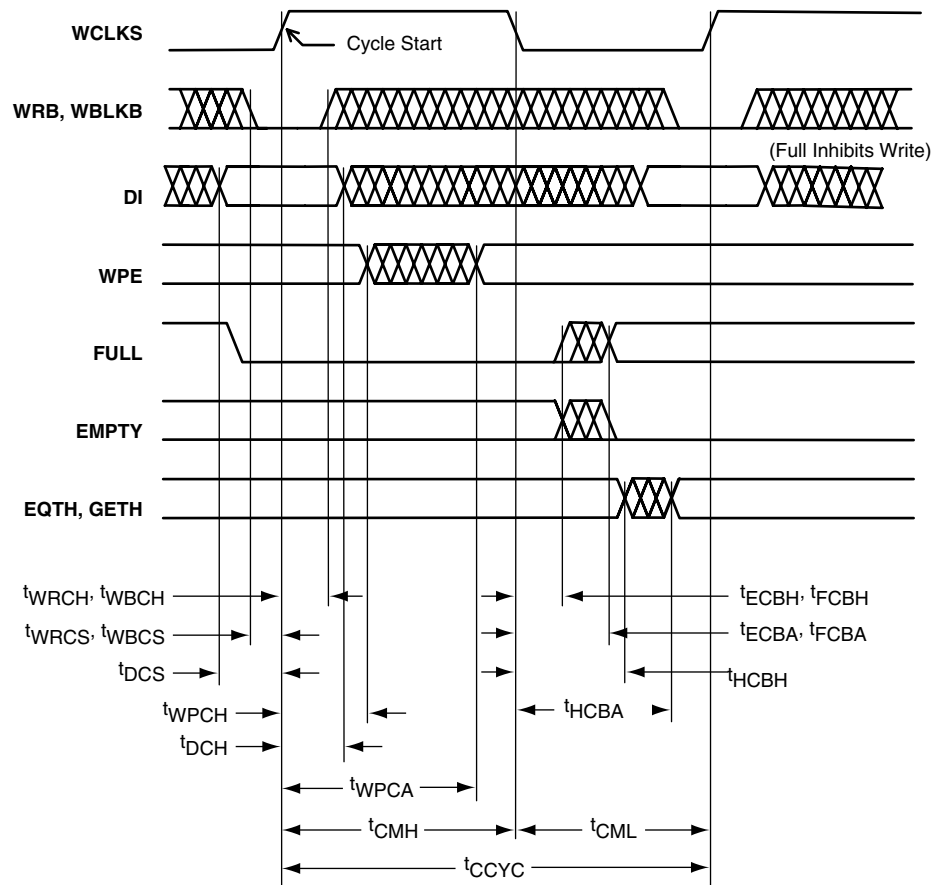
**T<sub>J</sub> = 0°C to 110°C; V<sub>DD</sub> = 2.3V to 2.7V**

| Symbol t <sub>xxx</sub> | Description                                                | Min.             | Max. | Units | Notes                                                                               |
|-------------------------|------------------------------------------------------------|------------------|------|-------|-------------------------------------------------------------------------------------|
| CCYC                    | Cycle time                                                 | 7.5              |      | ns    |                                                                                     |
| CMH                     | Clock high phase                                           | 3.0              |      | ns    |                                                                                     |
| CML                     | Clock low phase                                            | 3.0              |      | ns    |                                                                                     |
| ECBA                    | New EMPTY access from RCLKS ↓                              | 3.0 <sup>1</sup> |      | ns    |                                                                                     |
| FCBA                    | FULL ↓ access from RCLKS ↓                                 | 3.0 <sup>1</sup> |      | ns    |                                                                                     |
| ECBH, FCBH, THCBH       | Old EMPTY, FULL, EQTH, & GETH valid hold time from RCLKS ↓ |                  | 1.0  | ns    | Empty/full/thresh are invalid from the end of hold until the new access is complete |
| OCA                     | New DO access from RCLKS ↑                                 | 2.0              |      | ns    |                                                                                     |
| OCH                     | Old DO valid from RCLKS ↑                                  |                  | 0.75 | ns    |                                                                                     |
| RDCH                    | RDB hold from RCLKS ↑                                      | 0.5              |      | ns    |                                                                                     |
| RDCS                    | RDB setup to RCLKS ↑                                       | 1.0              |      | ns    |                                                                                     |
| RPCA                    | New RPE access from RCLKS ↑                                | 4.0              |      | ns    |                                                                                     |
| RPCH                    | Old RPE valid from RCLKS ↑                                 |                  | 1.0  | ns    |                                                                                     |
| HCBA                    | EQTH or GETH access from RCLKS ↓                           | 4.5              |      | ns    |                                                                                     |

## Notes:

- At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMS), 3.0 ns.
- F speed grade devices are 20% slower than the standard numbers.

## Synchronous FIFO Write



**Note:** The plot shows the normal operation status.

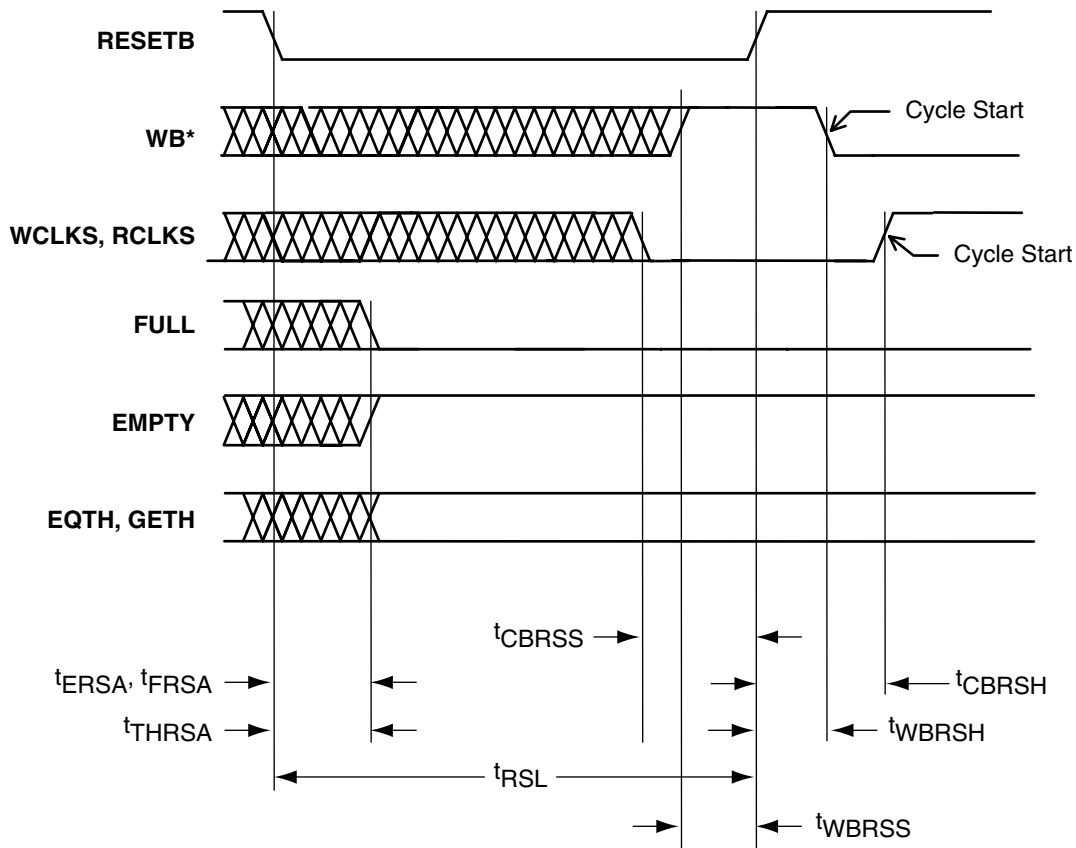
$T_J = 0^\circ\text{C to } 110^\circ\text{C}; V_{DD} = 2.3\text{V to } 2.7\text{V}$

| Symbol $t_{xxx}$ | Description                                                           | Min.             | Max. | Units | Notes                                                                               |
|------------------|-----------------------------------------------------------------------|------------------|------|-------|-------------------------------------------------------------------------------------|
| CCYC             | Cycle time                                                            | 7.5              |      | ns    |                                                                                     |
| CMH              | Clock high phase                                                      | 3.0              |      | ns    |                                                                                     |
| CML              | Clock low phase                                                       | 3.0              |      | ns    |                                                                                     |
| DCH              | DI hold from WCLKS $\uparrow$                                         | 0.5              |      | ns    |                                                                                     |
| DCS              | DI setup to WCLKS $\uparrow$                                          | 1.0              |      | ns    |                                                                                     |
| FCBA             | New FULL access from WCLKS $\downarrow$                               | 3.0 <sup>1</sup> |      | ns    |                                                                                     |
| ECBA             | EMPTY $\downarrow$ access from WCLKS $\downarrow$                     | 3.0 <sup>1</sup> |      | ns    |                                                                                     |
| ECBH, FCBH, HCBH | Old EMPTY, FULL, EQTH, & GETH valid hold time from WCLKS $\downarrow$ |                  | 1.0  | ns    | Empty/full/thresh are invalid from the end of hold until the new access is complete |
| HCBA             | EQTH or GETH access from WCLKS $\downarrow$                           | 4.5              |      | ns    |                                                                                     |
| WPCA             | New WPE access from WCLKS $\uparrow$                                  | 3.0              |      | ns    | WPE is invalid while PARGEN is active                                               |
| WPCH             | Old WPE valid from WCLKS $\uparrow$                                   |                  | 0.5  | ns    |                                                                                     |
| WRCH, WBCH       | WRB & WBLKB hold from WCLKS $\uparrow$                                | 0.5              |      | ns    |                                                                                     |
| WRCS, WBCS       | WRB & WBLKB setup to WCLKS $\uparrow$                                 | 1.0              |      | ns    |                                                                                     |

**Notes:**

- At fast cycles, ECBA and FCBA = MAX (7.5 ns – CMH), 3.0 ns.
- F speed grade devices are 20% slower than the standard numbers.

## FIFO Reset



**Note:** \*The plot shows the normal operation status.

$T_J = 0^{\circ}\text{C}$  to  $110^{\circ}\text{C}$ ;  $V_{DD} = 2.3\text{V}$  to  $2.7\text{V}$

| Symbol $t_{xxx}$ | Description                         | Min. | Max. | Units | Notes                  |
|------------------|-------------------------------------|------|------|-------|------------------------|
| CBRSH            | WCLKS or RCLKS ↑ hold from RESETB ↑ | 1.5  |      | ns    | Synchronous mode only  |
| CBRSS            | WCLKS or RCLKS ↓ setup to RESETB ↑  | 1.5  |      | ns    | Synchronous mode only  |
| ERSA             | New EMPTY ↑ access from RESETB ↓    | 3.0  |      | ns    |                        |
| FRSA             | FULL ↓ access from RESETB ↓         | 3.0  |      | ns    |                        |
| RSL              | RESETB low phase                    | 7.5  |      | ns    |                        |
| THRSA            | EQTH or GETH access from RESETB ↓   | 4.5  |      | ns    |                        |
| WBRSH            | WB ↓ hold from RESETB ↑             | 1.5  |      | ns    | Asynchronous mode only |
| WBRSS            | WB ↑ setup to RESETB ↑              | 1.5  |      | ns    | Asynchronous mode only |

**Note:** -F speed grade devices are 20% slower than the standard numbers.

## Pin Description

### I/O User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with standard LVTTTL and LVCMOS specifications. Unused I/O pins are configured as inputs with pull-up resistors.

### NC No Connect

To maintain compatibility with other Actel ProASIC<sup>PLUS</sup> products, it is recommended that this pin not be connected to the circuitry on the board.

### GL Global Pin

Low skew input pin for clock or other global signals. This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as a normal I/O.

### GLMX Global Multiplexing Pin

Low skew input pin for clock or other global signals. This pin can be used in one of two special ways: (Please see the *ProASIC<sup>PLUS</sup> Clock Conditioning Circuit* application note for details).

1. When the external feedback option is selected for the PLL block, this pin is routed as the external feedback source to the clock conditioning circuit.
2. In applications where two different signals access the same global net (but at different times) through the use of GLMXx and GLMXLx macros, this pin will be fixed as one of the source pins.

This pin can be configured with an internal pull-up resistor. When it is not connected to the global network or the clock conditioning circuit, it can be configured and used as any normal I/O.

### GND Ground

Common ground supply voltage.

### V<sub>DD</sub> Logic Array Power Supply Pin

2.5V supply voltage.

### V<sub>DDP</sub> I/O Pad Power Supply Pin

2.5V or 3.3V supply voltage.

### TMS Test Mode Select

The TMS pin controls the use of boundary-scan circuitry. This pin has an internal pull-up resistor.

### TCK Test Clock

Clock input pin for boundary scan (maximum 10 MHz).

### TDI Test Data In

Serial input for boundary scan. A dedicated pull-up resistor is included to pull this pin high when not being driven.

### TDO Test Data Out

Serial output for boundary scan.

### TRST Test Reset Input

Asynchronous, active low input pin for resetting boundary-scan circuitry. This pin has an internal pull-up resistor.

### RCK Running Clock

A free running clock is needed during programming if the programmer cannot guarantee that TCK will be uninterrupted.

### NPECL PECL Negative Input

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

### PPECL (I/P) PECL Positive input

Provides high speed clock or data signals to the PLL block. If unused, leave the pin unconnected.

### AVDD PLL Power Supply

Analog V<sub>DD</sub> should be V<sub>DD</sub> (core voltage) 2.5V (nominal) and be decoupled from GND with suitable decoupling capacitors to reduce noise. For more information, refer to Actel's *Using ProASIC<sup>PLUS</sup> Clock Conditioning Circuits* application note.

### AGND PLL Power Ground

Analog GND should be 0V and be decoupled from GND with suitable decoupling capacitors to reduce noise. For more information, refer to Actel's *Using ProASIC<sup>PLUS</sup> Clock Conditioning Circuits* application note.

### V<sub>PP</sub> Programming Supply Pin

This pin may be connected to any voltage between GND and 16.5V during normal operation, or it can be left unconnected.<sup>2</sup> For information on using this pin during programming, see the *Performing Internal In-System Programming Using Actel's ProASIC<sup>PLUS</sup> Devices* application note. Actel recommends floating the pin or connecting it to V<sub>DDP</sub>.

### V<sub>PN</sub> Programming Supply Pin

This pin may be connected to any voltage between GND and -13.8V during normal operation, or it can be left unconnected.<sup>3</sup> For information on using this pin during programming, see the *Performing Internal In-System Programming Using Actel's ProASIC<sup>PLUS</sup> Devices* application note. Actel recommends floating the pin or connecting it to GND.

<sup>2</sup> There is a nominal 40 kΩ pull-up resistor on V<sub>PP</sub>.

<sup>3</sup> There is a nominal 40 kΩ pull-down resistor on V<sub>PN</sub>.

## Power-up Sequencing

While ProASIC<sup>PLUS</sup> devices are live at power-up, the order of  $V_{DD}$  and  $V_{DDP}$  power-up is important during system start-up.  $V_{DD}$  should be powered up before (or coincident with)  $V_{DDP}$  on ProASIC<sup>PLUS</sup> devices. Failure to follow these guidelines may result in undesirable pin behavior during system start-up.

## Recommended Design Practice for $V_{PN}/V_{PP}$

Bypass capacitors **are required** from  $V_{PP}$  to GND and  $V_{PN}$  to GND for all ProASIC<sup>PLUS</sup> devices during programming.

During the erase cycle, ProASIC<sup>PLUS</sup> devices may have current surges on  $V_{PP}$  and  $V_{PN}$  power supplies. The only way to maintain the integrity of the power distribution to the ProASIC<sup>PLUS</sup> device during these current surges is to counteract the inductance of the finite length conductors that distribute the power to the device. This can be accomplished by providing a sufficient amount of bypass capacitance between the  $V_{PP}$  and  $V_{PN}$  pins and GND (using the shortest

paths possible). Without sufficient bypass capacitance to counteract the inductance, the  $V_{PP}$  and  $V_{PN}$  pins may incur a voltage spike beyond the voltage that the device can withstand. This issue applies to all programming configurations.

The power supply voltage limits are defined in the datasheet and application notes. The solution prevents spikes from damaging the ProASIC<sup>PLUS</sup> devices. Bypass capacitors are required for the  $V_{PP}$  and  $V_{PN}$  pads. The capacitors should be placed directly next to the device to be effective. To filter low frequency noise, use a 4.7 $\mu$ F (low ESR, <1 $\Omega$ , tantalum, 25V or greater rating) capacitor. To filter high frequency noise, use a 0.01 $\mu$ F to 0.1 $\mu$ F ceramic capacitor with a 25V or greater rating. The smaller high frequency capacitor should be placed closer to the device pins than the larger low frequency capacitor. The capacitors should be located as close to the device pins as possible (within 2.5cm, if possible). The same dual capacitor circuit should be used on both the  $V_{PP}$  and  $V_{PN}$  pins (Figure 27).

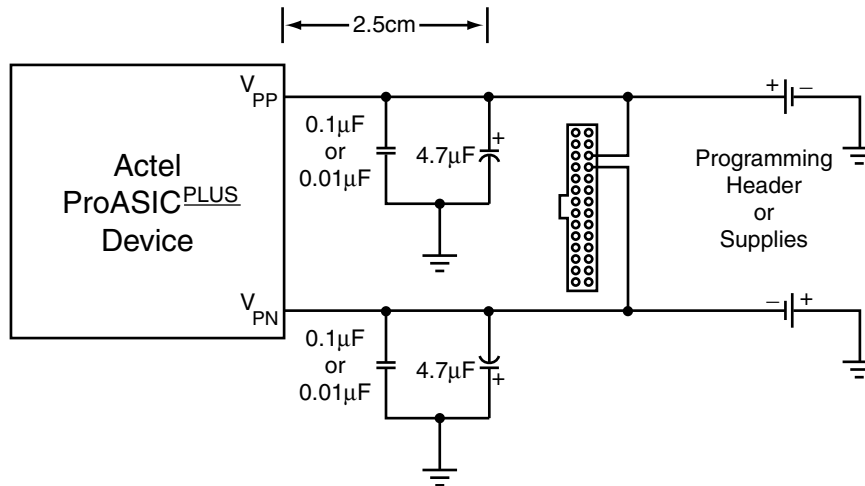
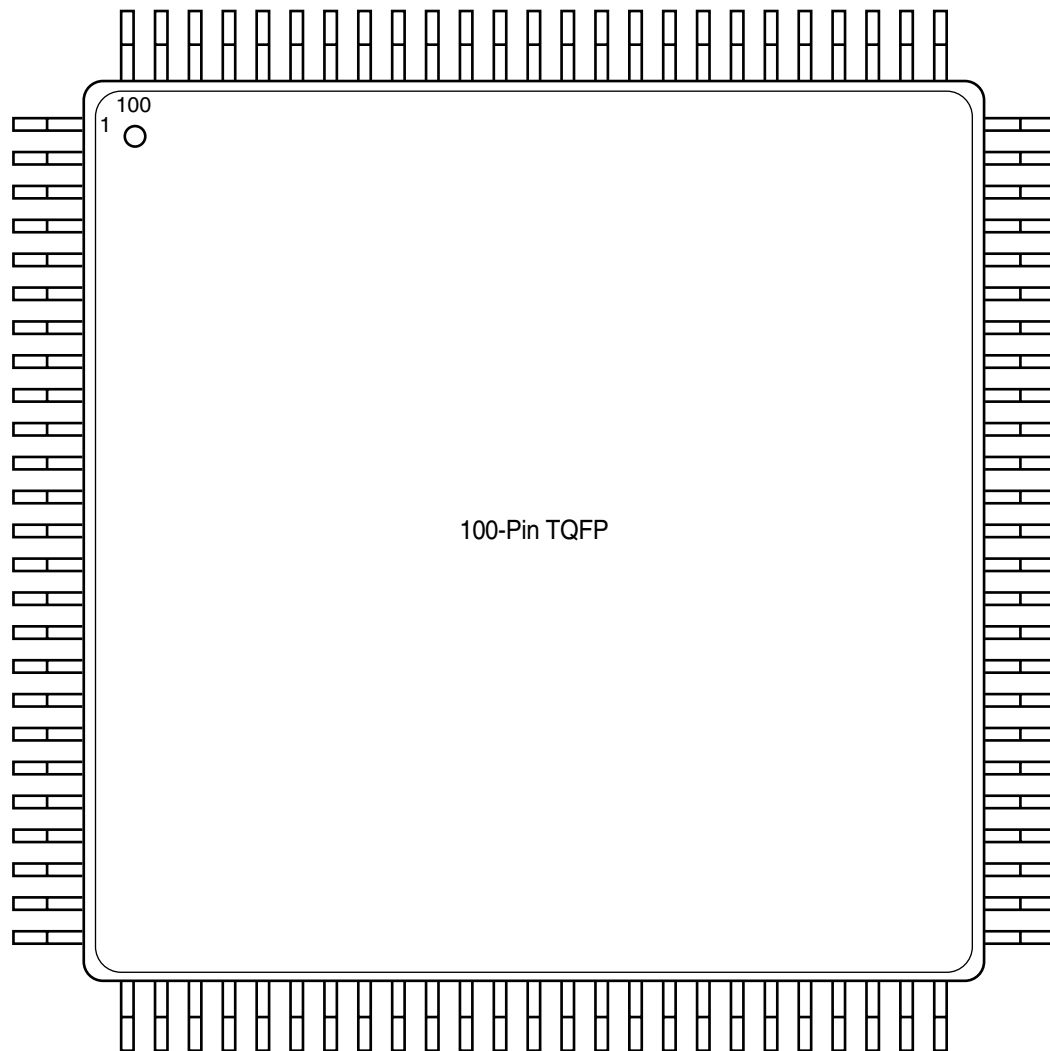


Figure 27 • ProASIC<sup>PLUS</sup>  $V_{PP}$  and  $V_{PN}$  Capacitor Requirements

## Package Pin Assignments

### 100-Pin TQFP



## 100-Pin TQFP

| Pin Number | APA075 Function  | APA150 Function  |
|------------|------------------|------------------|
| 1          | GND              | GND              |
| 2          | I/O              | I/O              |
| 3          | I/O              | I/O              |
| 4          | I/O              | I/O              |
| 5          | I/O              | I/O              |
| 6          | I/O              | I/O              |
| 7          | I/O              | I/O              |
| 8          | I/O              | I/O              |
| 9          | GND              | GND              |
| 10         | I/O (GLMX)       | I/O (GLMX)       |
| 11         | GL               | GL               |
| 12         | AGND             | AGND             |
| 13         | NPECL            | NPECL            |
| 14         | AVDD             | AVDD             |
| 15         | PPECL (I/P)      | PPECL (I/P)      |
| 16         | GL               | GL               |
| 17         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| 18         | I/O              | I/O              |
| 19         | I/O              | I/O              |
| 20         | I/O              | I/O              |
| 21         | I/O              | I/O              |
| 22         | I/O              | I/O              |
| 23         | I/O              | I/O              |
| 24         | I/O              | I/O              |
| 25         | GND              | GND              |
| 26         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 27         | I/O              | I/O              |
| 28         | I/O              | I/O              |
| 29         | I/O              | I/O              |
| 30         | I/O              | I/O              |
| 31         | I/O              | I/O              |
| 32         | I/O              | I/O              |
| 33         | I/O              | I/O              |
| 34         | I/O              | I/O              |
| 35         | I/O              | I/O              |
| 36         | I/O              | I/O              |
| 37         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| 38         | GND              | GND              |
| 39         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 40         | GND              | GND              |
| 41         | I/O              | I/O              |
| 42         | I/O              | I/O              |

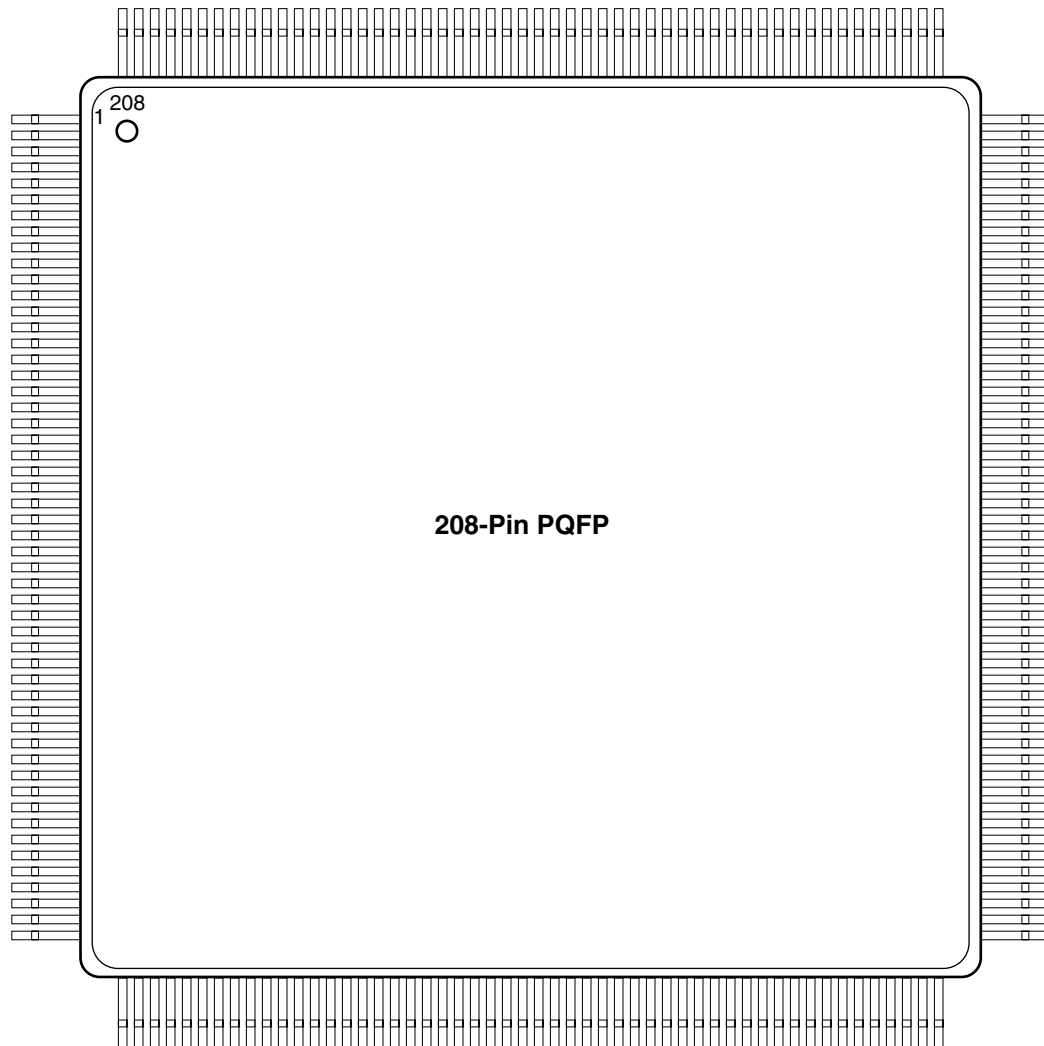
## 100-Pin TQFP (Continued)

| Pin Number | APA075 Function  | APA150 Function  |
|------------|------------------|------------------|
| 43         | I/O              | I/O              |
| 44         | I/O              | I/O              |
| 45         | I/O              | I/O              |
| 46         | I/O              | I/O              |
| 47         | TCK              | TCK              |
| 48         | TDI              | TDI              |
| 49         | TMS              | TMS              |
| 50         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 51         | GND              | GND              |
| 52         | V <sub>PP</sub>  | V <sub>PP</sub>  |
| 53         | V <sub>PN</sub>  | V <sub>PN</sub>  |
| 54         | TDO              | TDO              |
| 55         | TRST             | TRST             |
| 56         | RCK              | RCK              |
| 57         | I/O              | I/O              |
| 58         | I/O              | I/O              |
| 59         | I/O              | I/O              |
| 60         | GL               | GL               |
| 61         | PPECL (I/P)      | PPECL (I/P)      |
| 62         | AVDD             | AVDD             |
| 63         | NPECL            | NPECL            |
| 64         | AGND             | AGND             |
| 65         | GL               | GL               |
| 66         | I/O (GLMX)       | I/O (GLMX)       |
| 67         | GND              | GND              |
| 68         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| 69         | I/O              | I/O              |
| 70         | I/O              | I/O              |
| 71         | I/O              | I/O              |
| 72         | I/O              | I/O              |
| 73         | I/O              | I/O              |
| 74         | I/O              | I/O              |
| 75         | GND              | GND              |
| 76         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 77         | I/O              | I/O              |
| 78         | I/O              | I/O              |
| 79         | I/O              | I/O              |
| 80         | I/O              | I/O              |
| 81         | I/O              | I/O              |
| 82         | I/O              | I/O              |
| 83         | I/O              | I/O              |
| 84         | I/O              | I/O              |



**100-Pin TQFP (Continued)**

| Pin Number | APA075 Function  | APA150 Function  |
|------------|------------------|------------------|
| 85         | I/O              | I/O              |
| 86         | GND              | GND              |
| 87         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 88         | GND              | GND              |
| 89         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| 90         | I/O              | I/O              |
| 91         | I/O              | I/O              |
| 92         | I/O              | I/O              |
| 93         | I/O              | I/O              |
| 94         | I/O              | I/O              |
| 95         | I/O              | I/O              |
| 96         | I/O              | I/O              |
| 97         | I/O              | I/O              |
| 98         | I/O              | I/O              |
| 99         | I/O              | I/O              |
| 100        | V <sub>DDP</sub> | V <sub>DDP</sub> |

**Package Pin Assignments (Continued)****208-Pin PQFP**

## 208-Pin PQFP

| Pin Number | APA075 Function  | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| 1          | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 2          | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 3          | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 4          | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 5          | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 6          | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 7          | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 8          | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 9          | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 10         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 11         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 12         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 13         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 14         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 15         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 16         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| 17         | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 18         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 19         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 20         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 21         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 22         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 23         | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       |
| 24         | GL               | GL               | GL               | GL               | GL               | GL               | GL               |
| 25         | AGND             | AGND             | AGND             | AGND             | AGND             | AGND             | AGND             |
| 26         | NPECL            | NPECL            | NPECL            | NPECL            | NPECL            | NPECL            | NPECL            |
| 27         | AVDD             | AVDD             | AVDD             | AVDD             | AVDD             | AVDD             | AVDD             |
| 28         | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      |
| 29         | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 30         | GL               | GL               | GL               | GL               | GL               | GL               | GL               |
| 31         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 32         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 33         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 34         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 35         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 36         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| 37         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 38         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 39         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 40         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 41         | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 42         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |

## 208-Pin PQFP (Continued)

| Pin Number | APA075 Function  | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| 43         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 44         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 45         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 46         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 47         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 48         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 49         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 50         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 51         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 52         | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 53         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 54         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 55         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 56         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 57         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 58         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 59         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 60         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 61         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 62         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 63         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 64         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 65         | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 66         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 67         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 68         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 69         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 70         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 71         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| 72         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 73         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 74         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 75         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 76         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 77         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 78         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 79         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 80         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 81         | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 82         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 83         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 84         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |

## 208-Pin PQFP (Continued)

| Pin Number | APA075 Function  | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| 85         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 86         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 87         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 88         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| 89         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 90         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 91         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 92         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 93         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 94         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 95         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 96         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 97         | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 98         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 99         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 100        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 101        | TCK              | TCK              | TCK              | TCK              | TCK              | TCK              | TCK              |
| 102        | TDI              | TDI              | TDI              | TDI              | TDI              | TDI              | TDI              |
| 103        | TMS              | TMS              | TMS              | TMS              | TMS              | TMS              | TMS              |
| 104        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 105        | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 106        | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  |
| 107        | V <sub>PN</sub>  | V <sub>PN</sub>  | V <sub>PN</sub>  | V <sub>PN</sub>  | V <sub>PN</sub>  | V <sub>PN</sub>  | V <sub>PN</sub>  |
| 108        | TDO              | TDO              | TDO              | TDO              | TDO              | TDO              | TDO              |
| 109        | TRST             | TRST             | TRST             | TRST             | TRST             | TRST             | TRST             |
| 110        | RCK              | RCK              | RCK              | RCK              | RCK              | RCK              | RCK              |
| 111        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 112        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 113        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 114        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 115        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 116        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 117        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 118        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 119        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 120        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 121        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 122        | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 123        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 124        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 125        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 126        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |

## 208-Pin PQFP (Continued)

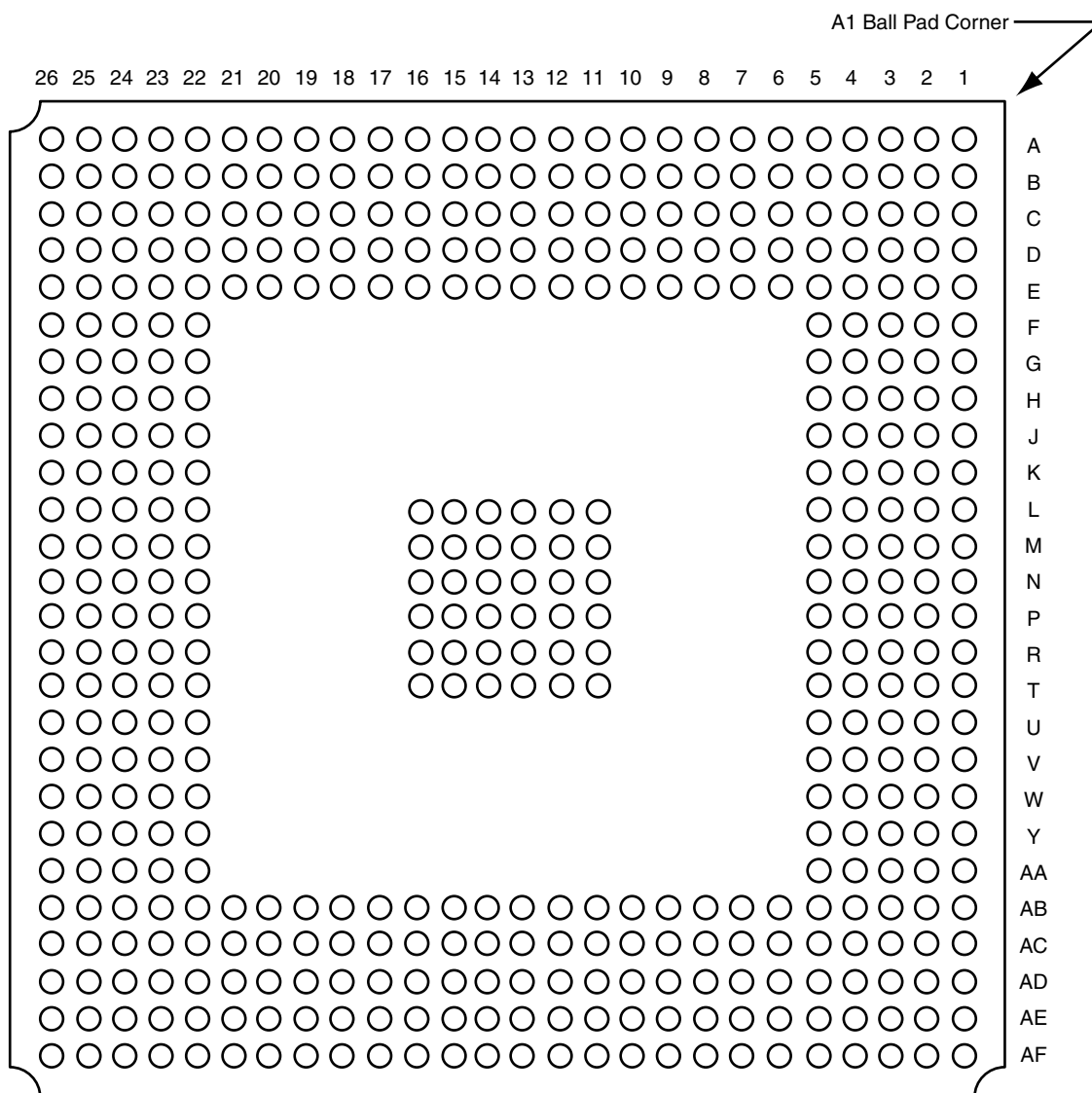
| Pin Number | APA075 Function  | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| 127        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 128        | GL               | GL               | GL               | GL               | GL               | GL               | GL               |
| 129        | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      |
| 130        | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 131        | AVDD             | AVDD             | AVDD             | AVDD             | AVDD             | AVDD             | AVDD             |
| 132        | NPECL            | NPECL            | NPECL            | NPECL            | NPECL            | NPECL            | NPECL            |
| 133        | AGND             | AGND             | AGND             | AGND             | AGND             | AGND             | AGND             |
| 134        | GL               | GL               | GL               | GL               | GL               | GL               | GL               |
| 135        | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       |
| 136        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 137        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 138        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 139        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 140        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 141        | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 142        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| 143        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 144        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 145        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 146        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 147        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 148        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 149        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 150        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 151        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 152        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 153        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 154        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 155        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 156        | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 157        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 158        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 159        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 160        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 161        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 162        | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 163        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 164        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 165        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 166        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 167        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 168        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |

## 208-Pin PQFP (Continued)

| Pin Number | APA075 Function  | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|
| 169        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 170        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 171        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| 172        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 173        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 174        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 175        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 176        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 177        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 178        | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 179        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 180        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 181        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 182        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 183        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 184        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 185        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 186        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| 187        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| 188        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 189        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 190        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 191        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 192        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 193        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 194        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 195        | GND              | GND              | GND              | GND              | GND              | GND              | GND              |
| 196        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 197        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 198        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 199        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 200        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 201        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 202        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 203        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 204        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 205        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 206        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 207        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| 208        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |

## Package Pin Assignments (Continued)

### 456-Pin PBGA (Bottom View)





## 456-Pin PBGA

| Pin Number | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|
| A1         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| A2         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| A3         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| A4         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| A5         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| A6         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| A7         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| A8         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| A9         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| A10        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| A11        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| A12        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| A13        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| A14        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| A15        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| A16        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| A17        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| A18        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| A19        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| A20        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| A21        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| A22        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| A23        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| A24        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| A25        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| A26        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| B1         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| B2         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| B3         | NC               | NC               | NC               | I/O              | I/O              | I/O              |
| B4         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| B5         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| B6         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| B7         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| B8         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| B9         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| B10        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| B11        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| B12        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| B13        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| B14        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| B15        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| B16        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |

## 456-Pin PBGA (Continued)

| Pin Number | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|
| B17        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| B18        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| B19        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| B20        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| B21        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| B22        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| B23        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| B24        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| B25        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| B26        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| C1         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| C2         | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| C3         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| C4         | NC               | NC               | NC               | I/O              | I/O              | I/O              |
| C5         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| C6         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| C7         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C8         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C9         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C10        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C11        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C12        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C13        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C14        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C15        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C16        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C17        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C18        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C19        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C20        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| C21        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| C22        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| C23        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| C24        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| C25        | NC               | NC               | NC               | I/O              | I/O              | I/O              |
| C26        | NC               | NC               | NC               | I/O              | I/O              | I/O              |
| D1         | NC               | NC               | NC               | I/O              | I/O              | I/O              |
| D2         | NC               | NC               | NC               | I/O              | I/O              | I/O              |
| D3         | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| D4         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| D5         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| D6         | NC               | NC               | I/O              | I/O              | I/O              | I/O              |

## 456-Pin PBGA (Continued)

| Pin Number | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|
| D7         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D8         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D9         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D10        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D11        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D12        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D13        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D14        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D15        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D16        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D17        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D18        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D19        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D20        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D21        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| D22        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| D23        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| D24        | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| D25        | NC               | NC               | NC               | I/O              | I/O              | I/O              |
| D26        | NC               | NC               | NC               | I/O              | I/O              | I/O              |
| E1         | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| E2         | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| E3         | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| E4         | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| E5         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| E6         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| E7         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| E8         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| E9         | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| E10        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| E11        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| E12        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| E13        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| E14        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| E15        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| E16        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| E17        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| E18        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| E19        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| E20        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| E21        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| E22        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |

## 456-Pin PBGA (Continued)

| Pin Number | APA150 Function | APA300 Function | APA450 Function | APA600 Function | APA750 Function | APA1000 Function |
|------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| E23        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| E24        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| E25        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| E26        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| F1         | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| F2         | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| F3         | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| F4         | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| F5         | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| F22        | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| F23        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| F24        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| F25        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| F26        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| G1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| G2         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| G3         | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| G4         | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| G5         | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| G22        | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| G23        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| G24        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| G25        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| G26        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| H1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| H2         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| H3         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| H4         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| H5         | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| H22        | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| H23        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| H24        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| H25        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| H26        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| J1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| J2         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| J3         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| J4         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| J5         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| J22        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| J23        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| J24        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |

## 456-Pin PBGA (Continued)

| Pin Number | APA150 Function | APA300 Function | APA450 Function | APA600 Function | APA750 Function | APA1000 Function |
|------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| J25        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| J26        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| K1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| K2         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| K3         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| K4         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| K5         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| K22        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| K23        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| K24        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| K25        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| K26        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| L1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| L2         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| L3         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| L4         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| L5         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| L11        | GND             | GND             | GND             | GND             | GND             | GND              |
| L12        | GND             | GND             | GND             | GND             | GND             | GND              |
| L13        | GND             | GND             | GND             | GND             | GND             | GND              |
| L14        | GND             | GND             | GND             | GND             | GND             | GND              |
| L15        | GND             | GND             | GND             | GND             | GND             | GND              |
| L16        | GND             | GND             | GND             | GND             | GND             | GND              |
| L22        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| L23        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| L24        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| L25        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| L26        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| M1         | GL              | GL              | GL              | GL              | GL              | GL               |
| M2         | GL              | GL              | GL              | GL              | GL              | GL               |
| M3         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| M4         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| M5         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| M11        | GND             | GND             | GND             | GND             | GND             | GND              |
| M12        | GND             | GND             | GND             | GND             | GND             | GND              |
| M13        | GND             | GND             | GND             | GND             | GND             | GND              |
| M14        | GND             | GND             | GND             | GND             | GND             | GND              |
| M15        | GND             | GND             | GND             | GND             | GND             | GND              |
| M16        | GND             | GND             | GND             | GND             | GND             | GND              |
| M22        | GL              | GL              | GL              | GL              | GL              | GL               |
| M23        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| M24        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |

**456-Pin PBGA (Continued)**

| Pin Number | APA150 Function | APA300 Function | APA450 Function | APA600 Function | APA750 Function | APA1000 Function |
|------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| M25        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| M26        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| N1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| N2         | I/O (GLMX)      | I/O (GLMX)      | I/O (GLMX)      | I/O (GLMX)      | I/O (GLMX)      | I/O (GLMX)       |
| N3         | AGND            | AGND            | AGND            | AGND            | AGND            | AGND             |
| N4         | PPECL (I/P)     | PPECL (I/P)     | PPECL (I/P)     | PPECL (I/P)     | PPECL (I/P)     | PPECL (I/P)      |
| N5         | AVDD            | AVDD            | AVDD            | AVDD            | AVDD            | AVDD             |
| N11        | GND             | GND             | GND             | GND             | GND             | GND              |
| N12        | GND             | GND             | GND             | GND             | GND             | GND              |
| N13        | GND             | GND             | GND             | GND             | GND             | GND              |
| N14        | GND             | GND             | GND             | GND             | GND             | GND              |
| N15        | GND             | GND             | GND             | GND             | GND             | GND              |
| N16        | GND             | GND             | GND             | GND             | GND             | GND              |
| N22        | NPECL           | NPECL           | NPECL           | NPECL           | NPECL           | NPECL            |
| N23        | GL              | GL              | GL              | GL              | GL              | GL               |
| N24        | AVDD            | AVDD            | AVDD            | AVDD            | AVDD            | AVDD             |
| N25        | I/O (GLMX)      | I/O (GLMX)      | I/O (GLMX)      | I/O (GLMX)      | I/O (GLMX)      | I/O (GLMX)       |
| N26        | AGND            | AGND            | AGND            | AGND            | AGND            | AGND             |
| P1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| P2         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| P3         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| P4         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| P5         | NPECL           | NPECL           | NPECL           | NPECL           | NPECL           | NPECL            |
| P11        | GND             | GND             | GND             | GND             | GND             | GND              |
| P12        | GND             | GND             | GND             | GND             | GND             | GND              |
| P13        | GND             | GND             | GND             | GND             | GND             | GND              |
| P14        | GND             | GND             | GND             | GND             | GND             | GND              |
| P15        | GND             | GND             | GND             | GND             | GND             | GND              |
| P16        | GND             | GND             | GND             | GND             | GND             | GND              |
| P22        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| P23        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| P24        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| P25        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| P26        | PPECL (I/P)     | PPECL (I/P)     | PPECL (I/P)     | PPECL (I/P)     | PPECL (I/P)     | PPECL (I/P)      |
| R1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| R2         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| R3         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| R4         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| R5         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| R11        | GND             | GND             | GND             | GND             | GND             | GND              |
| R12        | GND             | GND             | GND             | GND             | GND             | GND              |
| R13        | GND             | GND             | GND             | GND             | GND             | GND              |

## 456-Pin PBGA (Continued)

| Pin Number | APA150 Function | APA300 Function | APA450 Function | APA600 Function | APA750 Function | APA1000 Function |
|------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| R14        | GND             | GND             | GND             | GND             | GND             | GND              |
| R15        | GND             | GND             | GND             | GND             | GND             | GND              |
| R16        | GND             | GND             | GND             | GND             | GND             | GND              |
| R22        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| R23        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| R24        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| R25        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| R26        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| T1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| T2         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| T3         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| T4         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| T5         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| T11        | GND             | GND             | GND             | GND             | GND             | GND              |
| T12        | GND             | GND             | GND             | GND             | GND             | GND              |
| T13        | GND             | GND             | GND             | GND             | GND             | GND              |
| T14        | GND             | GND             | GND             | GND             | GND             | GND              |
| T15        | GND             | GND             | GND             | GND             | GND             | GND              |
| T16        | GND             | GND             | GND             | GND             | GND             | GND              |
| T22        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| T23        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| T24        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| T25        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| T26        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| U1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| U2         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| U3         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| U4         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| U5         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| U22        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| U23        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| U24        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| U25        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| U26        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| V1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| V2         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| V3         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| V4         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| V5         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| V22        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| V23        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| V24        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |

## 456-Pin PBGA (Continued)

| Pin Number | APA150 Function | APA300 Function | APA450 Function | APA600 Function | APA750 Function | APA1000 Function |
|------------|-----------------|-----------------|-----------------|-----------------|-----------------|------------------|
| V25        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| V26        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| W1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| W2         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| W3         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| W4         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| W5         | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| W22        | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| W23        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| W24        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| W25        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| W26        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| Y1         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| Y2         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| Y3         | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| Y4         | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| Y5         | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| Y22        | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| Y23        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| Y24        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| Y25        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| Y26        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| AA1        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| AA2        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| AA3        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| AA4        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| AA5        | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| AA22       | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| AA23       | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| AA24       | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| AA25       | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| AA26       | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| AB1        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| AB2        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| AB3        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| AB4        | NC              | I/O             | I/O             | I/O             | I/O             | I/O              |
| AB5        | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| AB6        | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| AB7        | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub>  |
| AB8        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| AB9        | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |
| AB10       | I/O             | I/O             | I/O             | I/O             | I/O             | I/O              |



## 456-Pin PBGA (Continued)

| Pin Number | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|
| AB11       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AB12       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AB13       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AB14       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AB15       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AB16       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AB17       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AB18       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AB19       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AB20       | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AB21       | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AB22       | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AB23       | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| AB24       | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| AB25       | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| AB26       | NC               | NC               | NC               | I/O              | I/O              | I/O              |
| AC1        | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC2        | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC3        | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC4        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AC5        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AC6        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC7        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC8        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC9        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC10       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC11       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC12       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC13       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC14       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC15       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC16       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC17       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC18       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC19       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC20       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AC21       | TMS              | TMS              | TMS              | TMS              | TMS              | TMS              |
| AC22       | TDO              | TDO              | TDO              | TDO              | TDO              | TDO              |
| AC23       | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AC24       | RCK              | RCK              | RCK              | RCK              | RCK              | RCK              |
| AC25       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AC26       | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |

**456-Pin PBGA (Continued)**

| Pin Number | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|
| AD1        | NC               | NC               | NC               | I/O              | I/O              | I/O              |
| AD2        | NC               | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD3        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AD4        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AD5        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AD6        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AD7        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD8        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD9        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD10       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD11       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD12       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD13       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD14       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD15       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD16       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD17       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD18       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD19       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AD20       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AD21       | TCK              | TCK              | TCK              | TCK              | TCK              | TCK              |
| AD22       | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  |
| AD23       | NC               | NC               | NC               | I/O              | I/O              | I/O              |
| AD24       | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AD25       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AD26       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AE1        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AE2        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AE3        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AE4        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AE5        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AE6        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AE7        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AE8        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AE9        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AE10       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AE11       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AE12       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AE13       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AE14       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AE15       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AE16       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |

## 456-Pin PBGA (Continued)

| Pin Number | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|------------------|------------------|------------------|------------------|
| AE17       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AE18       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AE19       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AE20       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AE21       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AE22       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AE23       | V <sub>PN</sub>  | V <sub>PN</sub>  | V <sub>PN</sub>  | V <sub>PN</sub>  | V <sub>PN</sub>  | V <sub>PN</sub>  |
| AE24       | TRST             | TRST             | TRST             | TRST             | TRST             | TRST             |
| AE25       | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AE26       | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AF1        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AF2        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AF3        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AF4        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AF5        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AF6        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AF7        | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AF8        | NC               | NC               | NC               | I/O              | I/O              | I/O              |
| AF9        | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AF10       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AF11       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AF12       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AF13       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AF14       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AF15       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AF16       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AF17       | I/O              | I/O              | I/O              | I/O              | I/O              | I/O              |
| AF18       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AF19       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AF20       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AF21       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AF22       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AF23       | TDI              | TDI              | TDI              | TDI              | TDI              | TDI              |
| AF24       | NC               | NC               | I/O              | I/O              | I/O              | I/O              |
| AF25       | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AF26       | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |

## Package Assignments (Continued)

### 144-FBGA (Bottom View)

|   | 12                                                                                  | 11                                                                                  | 10                                                                                  | 9                                                                                   | 8                                                                                   | 7                                                                                   | 6                                                                                   | 5                                                                                   | 4                                                                                   | 3                                                                                   | 2                                                                                     | 1                                                                                     |
|---|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| A |    |    |    |    |    |    |    |    |    |    |    |    |
| B |    |    |    |    |    |    |    |    |    |    |    |    |
| C |    |    |    |    |    |    |    |    |    |    |    |    |
| D |   |   |   |   |   |   |   |   |   |   |   |   |
| E |  |  |  |  |  |  |  |  |  |  |  |  |
| F |  |  |  |  |  |  |  |  |  |  |  |  |
| G |  |  |  |  |  |  |  |  |  |  |  |  |
| H |  |  |  |  |  |  |  |  |  |  |  |  |
| J |  |  |  |  |  |  |  |  |  |  |  |  |
| K |  |  |  |  |  |  |  |  |  |  |  |  |
| L |  |  |  |  |  |  |  |  |  |  |  |  |
| M |  |  |  |  |  |  |  |  |  |  |  |  |

144-FBGA Pin

| Pin Number | APA075 Function | APA150 Function | APA300 Function | APA450 Function |
|------------|-----------------|-----------------|-----------------|-----------------|
| A1         | I/O             | I/O             | I/O             | I/O             |
| A2         | I/O             | I/O             | I/O             | I/O             |
| A3         | I/O             | I/O             | I/O             | I/O             |
| A4         | I/O             | I/O             | I/O             | I/O             |
| A5         | I/O             | I/O             | I/O             | I/O             |
| A6         | GND             | GND             | GND             | GND             |
| A7         | I/O             | I/O             | I/O             | I/O             |
| A8         | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> |
| A9         | I/O             | I/O             | I/O             | I/O             |
| A10        | I/O             | I/O             | I/O             | I/O             |
| A11        | I/O             | I/O             | I/O             | I/O             |
| A12        | I/O             | I/O             | I/O             | I/O             |
| B1         | I/O             | I/O             | I/O             | I/O             |
| B2         | GND             | GND             | GND             | GND             |
| B3         | I/O             | I/O             | I/O             | I/O             |
| B4         | I/O             | I/O             | I/O             | I/O             |
| B5         | I/O             | I/O             | I/O             | I/O             |
| B6         | I/O             | I/O             | I/O             | I/O             |
| B7         | I/O             | I/O             | I/O             | I/O             |
| B8         | I/O             | I/O             | I/O             | I/O             |
| B9         | I/O             | I/O             | I/O             | I/O             |
| B10        | I/O             | I/O             | I/O             | I/O             |
| B11        | GND             | GND             | GND             | GND             |
| B12        | I/O             | I/O             | I/O             | I/O             |
| C1         | I/O             | I/O             | I/O             | I/O             |
| C2         | GL              | GL              | GL              | GL              |
| C3         | I/O             | I/O             | I/O             | I/O             |
| C4         | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> | V <sub>DD</sub> |
| C5         | I/O             | I/O             | I/O             | I/O             |
| C6         | I/O             | I/O             | I/O             | I/O             |
| C7         | I/O             | I/O             | I/O             | I/O             |
| C8         | I/O             | I/O             | I/O             | I/O             |
| C9         | I/O             | I/O             | I/O             | I/O             |
| C10        | I/O             | I/O             | I/O             | I/O             |
| C11        | I/O             | I/O             | I/O             | I/O             |
| C12        | I/O             | I/O             | I/O             | I/O             |
| D1         | I/O             | I/O             | I/O             | I/O             |
| D2         | I/O             | I/O             | I/O             | I/O             |
| D3         | I/O             | I/O             | I/O             | I/O             |
| D4         | I/O             | I/O             | I/O             | I/O             |
| D5         | I/O             | I/O             | I/O             | I/O             |
| D6         | I/O             | I/O             | I/O             | I/O             |

144-FBGA Pin (Continued)

| Pin Number | APA075 Function  | APA150 Function  | APA300 Function  | APA450 Function  |
|------------|------------------|------------------|------------------|------------------|
| D7         | I/O              | I/O              | I/O              | I/O              |
| D8         | I/O              | I/O              | I/O              | I/O              |
| D9         | I/O              | I/O              | I/O              | I/O              |
| D10        | I/O              | I/O              | I/O              | I/O              |
| D11        | I/O              | I/O              | I/O              | I/O              |
| D12        | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       |
| E1         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| E2         | I/O              | I/O              | I/O              | I/O              |
| E3         | I/O              | I/O              | I/O              | I/O              |
| E4         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| E5         | I/O              | I/O              | I/O              | I/O              |
| E6         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| E7         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| E8         | AVDD             | AVDD             | AVDD             | AVDD             |
| E9         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| E10        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| E11        | NPECL            | NPECL            | NPECL            | NPECL            |
| E12        | AGND             | AGND             | AGND             | AGND             |
| F1         | GL               | GL               | GL               | GL               |
| F2         | AGND             | AGND             | AGND             | AGND             |
| F3         | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       |
| F4         | I/O              | I/O              | I/O              | I/O              |
| F5         | GND              | GND              | GND              | GND              |
| F6         | GND              | GND              | GND              | GND              |
| F7         | GND              | GND              | GND              | GND              |
| F8         | I/O              | I/O              | I/O              | I/O              |
| F9         | GL               | GL               | GL               | GL               |
| F10        | GND              | GND              | GND              | GND              |
| F11        | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      |
| F12        | GL               | GL               | GL               | GL               |
| G1         | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      |
| G2         | GND              | GND              | GND              | GND              |
| G3         | AVDD             | AVDD             | AVDD             | AVDD             |
| G4         | NPECL            | NPECL            | NPECL            | NPECL            |
| G5         | GND              | GND              | GND              | GND              |
| G6         | GND              | GND              | GND              | GND              |
| G7         | GND              | GND              | GND              | GND              |
| G8         | I/O              | I/O              | I/O              | I/O              |
| G9         | I/O              | I/O              | I/O              | I/O              |
| G10        | I/O              | I/O              | I/O              | I/O              |
| G11        | I/O              | I/O              | I/O              | I/O              |
| G12        | I/O              | I/O              | I/O              | I/O              |

144-FBGA Pin (Continued)

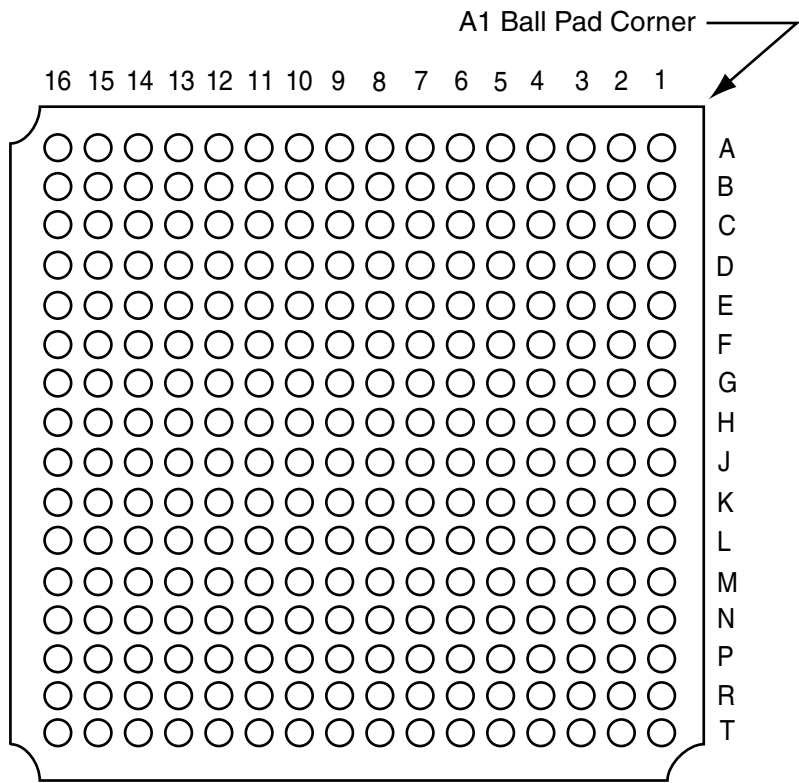
| Pin Number | APA075 Function  | APA150 Function  | APA300 Function  | APA450 Function  |
|------------|------------------|------------------|------------------|------------------|
| H1         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| H2         | I/O              | I/O              | I/O              | I/O              |
| H3         | I/O              | I/O              | I/O              | I/O              |
| H4         | I/O              | I/O              | I/O              | I/O              |
| H5         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| H6         | I/O              | I/O              | I/O              | I/O              |
| H7         | I/O              | I/O              | I/O              | I/O              |
| H8         | I/O              | I/O              | I/O              | I/O              |
| H9         | I/O              | I/O              | I/O              | I/O              |
| H10        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H11        | I/O              | I/O              | I/O              | I/O              |
| H12        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J1         | I/O              | I/O              | I/O              | I/O              |
| J2         | I/O              | I/O              | I/O              | I/O              |
| J3         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| J4         | I/O              | I/O              | I/O              | I/O              |
| J5         | I/O              | I/O              | I/O              | I/O              |
| J6         | I/O              | I/O              | I/O              | I/O              |
| J7         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J8         | TCK              | TCK              | TCK              | TCK              |
| J9         | I/O              | I/O              | I/O              | I/O              |
| J10        | TDO              | TDO              | TDO              | TDO              |
| J11        | I/O              | I/O              | I/O              | I/O              |
| J12        | I/O              | I/O              | I/O              | I/O              |
| K1         | I/O              | I/O              | I/O              | I/O              |
| K2         | I/O              | I/O              | I/O              | I/O              |
| K3         | I/O              | I/O              | I/O              | I/O              |
| K4         | I/O              | I/O              | I/O              | I/O              |
| K5         | I/O              | I/O              | I/O              | I/O              |
| K6         | I/O              | I/O              | I/O              | I/O              |
| K7         | GND              | GND              | GND              | GND              |
| K8         | I/O              | I/O              | I/O              | I/O              |
| K9         | I/O              | I/O              | I/O              | I/O              |
| K10        | GND              | GND              | GND              | GND              |
| K11        | I/O              | I/O              | I/O              | I/O              |
| K12        | I/O              | I/O              | I/O              | I/O              |
| L1         | GND              | GND              | GND              | GND              |
| L2         | I/O              | I/O              | I/O              | I/O              |
| L3         | I/O              | I/O              | I/O              | I/O              |
| L4         | I/O              | I/O              | I/O              | I/O              |
| L5         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| L6         | I/O              | I/O              | I/O              | I/O              |

144-FBGA Pin (Continued)

| Pin Number | APA075 Function  | APA150 Function  | APA300 Function  | APA450 Function  |
|------------|------------------|------------------|------------------|------------------|
| L7         | I/O              | I/O              | I/O              | I/O              |
| L8         | I/O              | I/O              | I/O              | I/O              |
| L9         | TMS              | TMS              | TMS              | TMS              |
| L10        | RCK              | RCK              | RCK              | RCK              |
| L11        | I/O              | I/O              | I/O              | I/O              |
| L12        | TRST             | TRST             | TRST             | TRST             |
| M1         | I/O              | I/O              | I/O              | I/O              |
| M2         | I/O              | I/O              | I/O              | I/O              |
| M3         | I/O              | I/O              | I/O              | I/O              |
| M4         | I/O              | I/O              | I/O              | I/O              |
| M5         | I/O              | I/O              | I/O              | I/O              |
| M6         | I/O              | I/O              | I/O              | I/O              |
| M7         | I/O              | I/O              | I/O              | I/O              |
| M8         | I/O              | I/O              | I/O              | I/O              |
| M9         | TDI              | TDI              | TDI              | TDI              |
| M10        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| M11        | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  |
| M12        | V <sub>PN</sub>  | V <sub>PN</sub>  | V <sub>PN</sub>  | V <sub>PN</sub>  |

Package Assignments (Continued)

256-FBGA (Bottom View)



## 256-Pin FBGA

| Pin Number | APA150 Function | APA300 Function | APA450 Function | APA600 Function |
|------------|-----------------|-----------------|-----------------|-----------------|
| A1         | GND             | GND             | GND             | GND             |
| A2         | I/O             | I/O             | I/O             | I/O             |
| A3         | I/O             | I/O             | I/O             | I/O             |
| A4         | I/O             | I/O             | I/O             | I/O             |
| A5         | I/O             | I/O             | I/O             | I/O             |
| A6         | I/O             | I/O             | I/O             | I/O             |
| A7         | I/O             | I/O             | I/O             | I/O             |
| A8         | I/O             | I/O             | I/O             | I/O             |
| A9         | I/O             | I/O             | I/O             | I/O             |
| A10        | I/O             | I/O             | I/O             | I/O             |
| A11        | I/O             | I/O             | I/O             | I/O             |
| A12        | I/O             | I/O             | I/O             | I/O             |
| A13        | I/O             | I/O             | I/O             | I/O             |
| A14        | I/O             | I/O             | I/O             | I/O             |
| A15        | I/O             | I/O             | I/O             | I/O             |
| A16        | GND             | GND             | GND             | GND             |
| B1         | I/O             | I/O             | I/O             | I/O             |
| B2         | I/O             | I/O             | I/O             | I/O             |
| B3         | I/O             | I/O             | I/O             | I/O             |
| B4         | I/O             | I/O             | I/O             | I/O             |
| B5         | I/O             | I/O             | I/O             | I/O             |
| B6         | I/O             | I/O             | I/O             | I/O             |
| B7         | I/O             | I/O             | I/O             | I/O             |
| B8         | I/O             | I/O             | I/O             | I/O             |
| B9         | I/O             | I/O             | I/O             | I/O             |
| B10        | I/O             | I/O             | I/O             | I/O             |
| B11        | I/O             | I/O             | I/O             | I/O             |
| B12        | I/O             | I/O             | I/O             | I/O             |
| B13        | I/O             | I/O             | I/O             | I/O             |
| B14        | I/O             | I/O             | I/O             | I/O             |
| B15        | I/O             | I/O             | I/O             | I/O             |
| B16        | I/O             | I/O             | I/O             | I/O             |
| C1         | I/O             | I/O             | I/O             | I/O             |
| C2         | I/O             | I/O             | I/O             | I/O             |
| C3         | I/O             | I/O             | I/O             | I/O             |
| C4         | I/O             | I/O             | I/O             | I/O             |
| C5         | I/O             | I/O             | I/O             | I/O             |
| C6         | I/O             | I/O             | I/O             | I/O             |
| C7         | I/O             | I/O             | I/O             | I/O             |
| C8         | I/O             | I/O             | I/O             | I/O             |
| C9         | I/O             | I/O             | I/O             | I/O             |
| C10        | I/O             | I/O             | I/O             | I/O             |
| C11        | I/O             | I/O             | I/O             | I/O             |
| C12        | I/O             | I/O             | I/O             | I/O             |
| C13        | I/O             | I/O             | I/O             | I/O             |



## 256-Pin FBGA (Continued)

| Pin Number | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|------------------|------------------|
| C14        | I/O              | I/O              | I/O              | I/O              |
| C15        | I/O              | I/O              | I/O              | I/O              |
| C16        | I/O              | I/O              | I/O              | I/O              |
| D1         | I/O              | I/O              | I/O              | I/O              |
| D2         | I/O              | I/O              | I/O              | I/O              |
| D3         | I/O              | I/O              | I/O              | I/O              |
| D4         | I/O              | I/O              | I/O              | I/O              |
| D5         | I/O              | I/O              | I/O              | I/O              |
| D6         | I/O              | I/O              | I/O              | I/O              |
| D7         | I/O              | I/O              | I/O              | I/O              |
| D8         | I/O              | I/O              | I/O              | I/O              |
| D9         | I/O              | I/O              | I/O              | I/O              |
| D10        | I/O              | I/O              | I/O              | I/O              |
| D11        | I/O              | I/O              | I/O              | I/O              |
| D12        | I/O              | I/O              | I/O              | I/O              |
| D13        | I/O              | I/O              | I/O              | I/O              |
| D14        | I/O              | I/O              | I/O              | I/O              |
| D15        | I/O              | I/O              | I/O              | I/O              |
| D16        | I/O              | I/O              | I/O              | I/O              |
| E1         | I/O              | I/O              | I/O              | I/O              |
| E2         | I/O              | I/O              | I/O              | I/O              |
| E3         | I/O              | I/O              | I/O              | I/O              |
| E4         | I/O              | I/O              | I/O              | I/O              |
| E5         | I/O              | I/O              | I/O              | I/O              |
| E6         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| E7         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| E8         | I/O              | I/O              | I/O              | I/O              |
| E9         | I/O              | I/O              | I/O              | I/O              |
| E10        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| E11        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| E12        | I/O              | I/O              | I/O              | I/O              |
| E13        | I/O              | I/O              | I/O              | I/O              |
| E14        | I/O              | I/O              | I/O              | I/O              |
| E15        | I/O              | I/O              | I/O              | I/O              |
| E16        | I/O              | I/O              | I/O              | I/O              |
| F1         | I/O              | I/O              | I/O              | I/O              |
| F2         | I/O              | I/O              | I/O              | I/O              |
| F3         | I/O              | I/O              | I/O              | I/O              |
| F4         | I/O              | I/O              | I/O              | I/O              |
| F5         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| F6         | GND              | GND              | GND              | GND              |
| F7         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| F8         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| F9         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| F10        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |

## 256-Pin FBGA (Continued)

| Pin Number | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|------------------|------------------|
| F11        | GND              | GND              | GND              | GND              |
| F12        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| F13        | I/O              | I/O              | I/O              | I/O              |
| F14        | I/O              | I/O              | I/O              | I/O              |
| F15        | I/O              | I/O              | I/O              | I/O              |
| F16        | I/O              | I/O              | I/O              | I/O              |
| G1         | I/O              | I/O              | I/O              | I/O              |
| G2         | I/O              | I/O              | I/O              | I/O              |
| G3         | I/O              | I/O              | I/O              | I/O              |
| G4         | I/O              | I/O              | I/O              | I/O              |
| G5         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| G6         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| G7         | GND              | GND              | GND              | GND              |
| G8         | GND              | GND              | GND              | GND              |
| G9         | GND              | GND              | GND              | GND              |
| G10        | GND              | GND              | GND              | GND              |
| G11        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| G12        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| G13        | I/O              | I/O              | I/O              | I/O              |
| G14        | I/O              | I/O              | I/O              | I/O              |
| G15        | I/O              | I/O              | I/O              | I/O              |
| G16        | I/O              | I/O              | I/O              | I/O              |
| H1         | GL               | GL               | GL               | GL               |
| H2         | NPECL            | NPECL            | NPECL            | NPECL            |
| H3         | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       |
| H4         | AGND             | AGND             | AGND             | AGND             |
| H5         | I/O              | I/O              | I/O              | I/O              |
| H6         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| H7         | GND              | GND              | GND              | GND              |
| H8         | GND              | GND              | GND              | GND              |
| H9         | GND              | GND              | GND              | GND              |
| H10        | GND              | GND              | GND              | GND              |
| H11        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| H12        | I/O              | I/O              | I/O              | I/O              |
| H13        | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       | I/O (GLMX)       |
| H14        | NPECL            | NPECL            | NPECL            | NPECL            |
| H15        | AGND             | AGND             | AGND             | AGND             |
| H16        | GL               | GL               | GL               | GL               |
| J1         | GL               | GL               | GL               | GL               |
| J2         | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      |
| J3         | AVDD             | AVDD             | AVDD             | AVDD             |
| J4         | I/O              | I/O              | I/O              | I/O              |
| J5         | I/O              | I/O              | I/O              | I/O              |
| J6         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J7         | GND              | GND              | GND              | GND              |

## 256-Pin FBGA (Continued)

| Pin Number | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|------------------|------------------|
| J8         | GND              | GND              | GND              | GND              |
| J9         | GND              | GND              | GND              | GND              |
| J10        | GND              | GND              | GND              | GND              |
| J11        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J12        | I/O              | I/O              | I/O              | I/O              |
| J13        | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      | PPECL (I/P)      |
| J14        | I/O              | I/O              | I/O              | I/O              |
| J15        | AVDD             | AVDD             | AVDD             | AVDD             |
| J16        | GL               | GL               | GL               | GL               |
| K1         | I/O              | I/O              | I/O              | I/O              |
| K2         | I/O              | I/O              | I/O              | I/O              |
| K3         | I/O              | I/O              | I/O              | I/O              |
| K4         | I/O              | I/O              | I/O              | I/O              |
| K5         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K6         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| K7         | GND              | GND              | GND              | GND              |
| K8         | GND              | GND              | GND              | GND              |
| K9         | GND              | GND              | GND              | GND              |
| K10        | GND              | GND              | GND              | GND              |
| K11        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| K12        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K13        | I/O              | I/O              | I/O              | I/O              |
| K14        | I/O              | I/O              | I/O              | I/O              |
| K15        | I/O              | I/O              | I/O              | I/O              |
| K16        | I/O              | I/O              | I/O              | I/O              |
| L1         | I/O              | I/O              | I/O              | I/O              |
| L2         | I/O              | I/O              | I/O              | I/O              |
| L3         | I/O              | I/O              | I/O              | I/O              |
| L4         | I/O              | I/O              | I/O              | I/O              |
| L5         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| L6         | GND              | GND              | GND              | GND              |
| L7         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| L8         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| L9         | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| L10        | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  | V <sub>DD</sub>  |
| L11        | GND              | GND              | GND              | GND              |
| L12        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| L13        | I/O              | I/O              | I/O              | I/O              |
| L14        | I/O              | I/O              | I/O              | I/O              |
| L15        | I/O              | I/O              | I/O              | I/O              |
| L16        | I/O              | I/O              | I/O              | I/O              |
| M1         | I/O              | I/O              | I/O              | I/O              |
| M2         | I/O              | I/O              | I/O              | I/O              |
| M3         | I/O              | I/O              | I/O              | I/O              |
| M4         | I/O              | I/O              | I/O              | I/O              |

## 256-Pin FBGA (Continued)

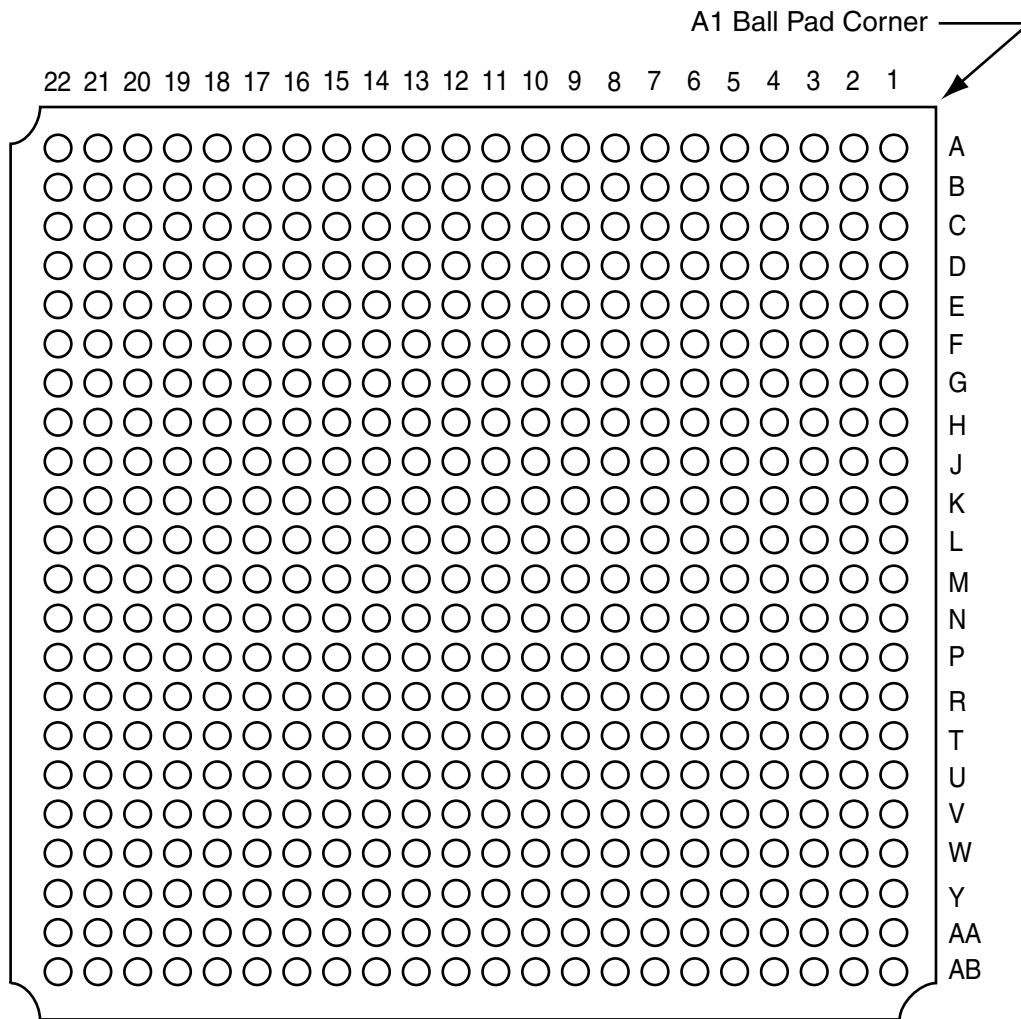
| Pin Number | APA150 Function  | APA300 Function  | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|------------------|------------------|
| M5         | I/O              | I/O              | I/O              | I/O              |
| M6         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| M7         | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| M8         | I/O              | I/O              | I/O              | I/O              |
| M9         | I/O              | I/O              | I/O              | I/O              |
| M10        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| M11        | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> | V <sub>DDP</sub> |
| M12        | I/O              | I/O              | I/O              | I/O              |
| M13        | I/O              | I/O              | I/O              | I/O              |
| M14        | I/O              | I/O              | I/O              | I/O              |
| M15        | I/O              | I/O              | I/O              | I/O              |
| M16        | I/O              | I/O              | I/O              | I/O              |
| N1         | I/O              | I/O              | I/O              | I/O              |
| N2         | I/O              | I/O              | I/O              | I/O              |
| N3         | I/O              | I/O              | I/O              | I/O              |
| N4         | I/O              | I/O              | I/O              | I/O              |
| N5         | I/O              | I/O              | I/O              | I/O              |
| N6         | I/O              | I/O              | I/O              | I/O              |
| N7         | I/O              | I/O              | I/O              | I/O              |
| N8         | I/O              | I/O              | I/O              | I/O              |
| N9         | I/O              | I/O              | I/O              | I/O              |
| N10        | I/O              | I/O              | I/O              | I/O              |
| N11        | I/O              | I/O              | I/O              | I/O              |
| N12        | I/O              | I/O              | I/O              | I/O              |
| N13        | I/O              | I/O              | I/O              | I/O              |
| N14        | RCK              | RCK              | RCK              | RCK              |
| N15        | I/O              | I/O              | I/O              | I/O              |
| N16        | I/O              | I/O              | I/O              | I/O              |
| P1         | I/O              | I/O              | I/O              | I/O              |
| P2         | I/O              | I/O              | I/O              | I/O              |
| P3         | I/O              | I/O              | I/O              | I/O              |
| P4         | I/O              | I/O              | I/O              | I/O              |
| P5         | I/O              | I/O              | I/O              | I/O              |
| P6         | I/O              | I/O              | I/O              | I/O              |
| P7         | I/O              | I/O              | I/O              | I/O              |
| P8         | I/O              | I/O              | I/O              | I/O              |
| P9         | I/O              | I/O              | I/O              | I/O              |
| P10        | I/O              | I/O              | I/O              | I/O              |
| P11        | I/O              | I/O              | I/O              | I/O              |
| P12        | I/O              | I/O              | I/O              | I/O              |
| P13        | TCK              | TCK              | TCK              | TCK              |
| P14        | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  | V <sub>PP</sub>  |
| P15        | TRST             | TRST             | TRST             | TRST             |
| P16        | I/O              | I/O              | I/O              | I/O              |
| R1         | I/O              | I/O              | I/O              | I/O              |

## 256-Pin FBGA (Continued)

| Pin Number | APA150 Function | APA300 Function | APA450 Function | APA600 Function |
|------------|-----------------|-----------------|-----------------|-----------------|
| R2         | I/O             | I/O             | I/O             | I/O             |
| R3         | I/O             | I/O             | I/O             | I/O             |
| R4         | I/O             | I/O             | I/O             | I/O             |
| R5         | I/O             | I/O             | I/O             | I/O             |
| R6         | I/O             | I/O             | I/O             | I/O             |
| R7         | I/O             | I/O             | I/O             | I/O             |
| R8         | I/O             | I/O             | I/O             | I/O             |
| R9         | I/O             | I/O             | I/O             | I/O             |
| R10        | I/O             | I/O             | I/O             | I/O             |
| R11        | I/O             | I/O             | I/O             | I/O             |
| R12        | I/O             | I/O             | I/O             | I/O             |
| R13        | I/O             | I/O             | I/O             | I/O             |
| R14        | TDI             | TDI             | TDI             | TDI             |
| R15        | V <sub>PN</sub> | V <sub>PN</sub> | V <sub>PN</sub> | V <sub>PN</sub> |
| R16        | TDO             | TDO             | TDO             | TDO             |
| T1         | GND             | GND             | GND             | GND             |
| T2         | I/O             | I/O             | I/O             | I/O             |
| T3         | I/O             | I/O             | I/O             | I/O             |
| T4         | I/O             | I/O             | I/O             | I/O             |
| T5         | I/O             | I/O             | I/O             | I/O             |
| T6         | I/O             | I/O             | I/O             | I/O             |
| T7         | I/O             | I/O             | I/O             | I/O             |
| T8         | I/O             | I/O             | I/O             | I/O             |
| T9         | I/O             | I/O             | I/O             | I/O             |
| T10        | I/O             | I/O             | I/O             | I/O             |
| T11        | I/O             | I/O             | I/O             | I/O             |
| T12        | I/O             | I/O             | I/O             | I/O             |
| T13        | I/O             | I/O             | I/O             | I/O             |
| T14        | I/O             | I/O             | I/O             | I/O             |
| T15        | TMS             | TMS             | TMS             | TMS             |
| T16        | GND             | GND             | GND             | GND             |

## Package Assignments (Continued)

### 484-Pin FBGA (Bottom View)



484-Pin FBGA

| Pin Number | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|
| A1         | GND              | GND              |
| A2         | GND              | GND              |
| A3         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| A4         | I/O              | I/O              |
| A5         | I/O              | I/O              |
| A6         | I/O              | I/O              |
| A7         | I/O              | I/O              |
| A8         | I/O              | I/O              |
| A9         | I/O              | I/O              |
| A10        | I/O              | I/O              |
| A11        | I/O              | I/O              |
| A12        | I/O              | I/O              |
| A13        | I/O              | I/O              |
| A14        | I/O              | I/O              |
| A15        | I/O              | I/O              |
| A16        | I/O              | I/O              |
| A17        | I/O              | I/O              |
| A18        | I/O              | I/O              |
| A19        | I/O              | I/O              |
| A20        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| A21        | GND              | GND              |
| A22        | GND              | GND              |
| B1         | GND              | GND              |
| B2         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| B3         | I/O              | I/O              |
| B4         | I/O              | I/O              |
| B5         | I/O              | I/O              |
| B6         | I/O              | I/O              |
| B7         | I/O              | I/O              |
| B8         | I/O              | I/O              |
| B9         | I/O              | I/O              |
| B10        | I/O              | I/O              |
| B11        | I/O              | I/O              |
| B12        | I/O              | I/O              |
| B13        | I/O              | I/O              |
| B14        | I/O              | I/O              |
| B15        | I/O              | I/O              |
| B16        | I/O              | I/O              |
| B17        | I/O              | I/O              |
| B18        | I/O              | I/O              |
| B19        | I/O              | I/O              |
| B20        | I/O              | I/O              |

484-Pin FBGA (Continued)

| Pin Number | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|
| B21        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| B22        | GND              | GND              |
| C1         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| C2         | NC               | I/O              |
| C3         | I/O              | I/O              |
| C4         | I/O              | I/O              |
| C5         | GND              | GND              |
| C6         | I/O              | I/O              |
| C7         | I/O              | I/O              |
| C8         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| C9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| C10        | I/O              | I/O              |
| C11        | I/O              | I/O              |
| C12        | NC               | I/O              |
| C13        | NC               | I/O              |
| C14        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| C15        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| C16        | NC               | I/O              |
| C17        | I/O              | I/O              |
| C18        | GND              | GND              |
| C19        | I/O              | I/O              |
| C20        | I/O              | I/O              |
| C21        | I/O              | I/O              |
| C22        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| D1         | I/O              | I/O              |
| D2         | I/O              | I/O              |
| D3         | NC               | I/O              |
| D4         | GND              | GND              |
| D5         | I/O              | I/O              |
| D6         | I/O              | I/O              |
| D7         | I/O              | I/O              |
| D8         | I/O              | I/O              |
| D9         | I/O              | I/O              |
| D10        | I/O              | I/O              |
| D11        | I/O              | I/O              |
| D12        | I/O              | I/O              |
| D13        | I/O              | I/O              |
| D14        | I/O              | I/O              |
| D15        | I/O              | I/O              |
| D16        | I/O              | I/O              |
| D17        | I/O              | I/O              |
| D18        | I/O              | I/O              |

484-Pin FBGA (Continued)

| Pin Number | APA450 Function | APA600 Function |
|------------|-----------------|-----------------|
| D19        | GND             | GND             |
| D20        | I/O             | I/O             |
| D21        | I/O             | I/O             |
| D22        | I/O             | I/O             |
| E1         | I/O             | I/O             |
| E2         | NC              | I/O             |
| E3         | GND             | GND             |
| E4         | I/O             | I/O             |
| E5         | I/O             | I/O             |
| E6         | I/O             | I/O             |
| E7         | I/O             | I/O             |
| E8         | I/O             | I/O             |
| E9         | I/O             | I/O             |
| E10        | I/O             | I/O             |
| E11        | I/O             | I/O             |
| E12        | I/O             | I/O             |
| E13        | I/O             | I/O             |
| E14        | I/O             | I/O             |
| E15        | I/O             | I/O             |
| E16        | I/O             | I/O             |
| E17        | I/O             | I/O             |
| E18        | I/O             | I/O             |
| E19        | I/O             | I/O             |
| E20        | GND             | GND             |
| E21        | I/O             | I/O             |
| E22        | I/O             | I/O             |
| F1         | I/O             | I/O             |
| F2         | I/O             | I/O             |
| F3         | I/O             | I/O             |
| F4         | I/O             | I/O             |
| F5         | I/O             | I/O             |
| F6         | I/O             | I/O             |
| F7         | I/O             | I/O             |
| F8         | I/O             | I/O             |
| F9         | I/O             | I/O             |
| F10        | I/O             | I/O             |
| F11        | I/O             | I/O             |
| F12        | I/O             | I/O             |
| F13        | I/O             | I/O             |
| F14        | I/O             | I/O             |
| F15        | I/O             | I/O             |
| F16        | I/O             | I/O             |

484-Pin FBGA (Continued)

| Pin Number | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|
| F17        | I/O              | I/O              |
| F18        | I/O              | I/O              |
| F19        | I/O              | I/O              |
| F20        | I/O              | I/O              |
| F21        | I/O              | I/O              |
| F22        | NC               | I/O              |
| G1         | I/O              | I/O              |
| G2         | I/O              | I/O              |
| G3         | NC               | I/O              |
| G4         | I/O              | I/O              |
| G5         | I/O              | I/O              |
| G6         | I/O              | I/O              |
| G7         | I/O              | I/O              |
| G8         | I/O              | I/O              |
| G9         | I/O              | I/O              |
| G10        | I/O              | I/O              |
| G11        | I/O              | I/O              |
| G12        | I/O              | I/O              |
| G13        | I/O              | I/O              |
| G14        | I/O              | I/O              |
| G15        | I/O              | I/O              |
| G16        | I/O              | I/O              |
| G17        | I/O              | I/O              |
| G18        | I/O              | I/O              |
| G19        | I/O              | I/O              |
| G20        | I/O              | I/O              |
| G21        | I/O              | I/O              |
| G22        | I/O              | I/O              |
| H1         | I/O              | I/O              |
| H2         | I/O              | I/O              |
| H3         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| H4         | I/O              | I/O              |
| H5         | I/O              | I/O              |
| H6         | I/O              | I/O              |
| H7         | I/O              | I/O              |
| H8         | I/O              | I/O              |
| H9         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H10        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H11        | I/O              | I/O              |
| H12        | I/O              | I/O              |
| H13        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H14        | V <sub>DDP</sub> | V <sub>DDP</sub> |



484-Pin FBGA (Continued)

| Pin Number | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|
| H15        | I/O              | I/O              |
| H16        | I/O              | I/O              |
| H17        | I/O              | I/O              |
| H18        | I/O              | I/O              |
| H19        | I/O              | I/O              |
| H20        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| H21        | I/O              | I/O              |
| H22        | I/O              | I/O              |
| J1         | I/O              | I/O              |
| J2         | I/O              | I/O              |
| J3         | NC               | I/O              |
| J4         | I/O              | I/O              |
| J5         | I/O              | I/O              |
| J6         | I/O              | I/O              |
| J7         | I/O              | I/O              |
| J8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| J9         | GND              | GND              |
| J10        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J12        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J13        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J14        | GND              | GND              |
| J15        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| J16        | I/O              | I/O              |
| J17        | I/O              | I/O              |
| J18        | I/O              | I/O              |
| J19        | I/O              | I/O              |
| J20        | NC               | I/O              |
| J21        | I/O              | I/O              |
| J22        | I/O              | I/O              |
| K1         | I/O              | I/O              |
| K2         | I/O              | I/O              |
| K3         | NC               | I/O              |
| K4         | I/O              | I/O              |
| K5         | I/O              | I/O              |
| K6         | I/O              | I/O              |
| K7         | I/O              | I/O              |
| K8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| K10        | GND              | GND              |
| K11        | GND              | GND              |
| K12        | GND              | GND              |

484-Pin FBGA (Continued)

| Pin Number | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|
| K13        | GND              | GND              |
| K14        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| K15        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K16        | I/O              | I/O              |
| K17        | I/O              | I/O              |
| K18        | I/O              | I/O              |
| K19        | I/O              | I/O              |
| K20        | I/O              | I/O              |
| K21        | I/O              | I/O              |
| K22        | I/O              | I/O              |
| L1         | NC               | I/O              |
| L2         | I/O              | I/O              |
| L3         | I/O              | I/O              |
| L4         | GL               | GL               |
| L5         | NPECL            | NPECL            |
| L6         | I/O (GLMX)       | I/O (GLMX)       |
| L7         | AGND             | AGND             |
| L8         | I/O              | I/O              |
| L9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| L10        | GND              | GND              |
| L11        | GND              | GND              |
| L12        | GND              | GND              |
| L13        | GND              | GND              |
| L14        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| L15        | I/O              | I/O              |
| L16        | I/O (GLMX)       | I/O (GLMX)       |
| L17        | NPECL            | NPECL            |
| L18        | AGND             | AGND             |
| L19        | GL               | GL               |
| L20        | I/O              | I/O              |
| L21        | I/O              | I/O              |
| L22        | I/O              | I/O              |
| M1         | I/O              | I/O              |
| M2         | I/O              | I/O              |
| M3         | I/O              | I/O              |
| M4         | GL               | GL               |
| M5         | PPECL (I/P)      | PPECL (I/P)      |
| M6         | AVDD             | AVDD             |
| M7         | I/O              | I/O              |
| M8         | I/O              | I/O              |
| M9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| M10        | GND              | GND              |

484-Pin FBGA (Continued)

| Pin Number | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|
| M11        | GND              | GND              |
| M12        | GND              | GND              |
| M13        | GND              | GND              |
| M14        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| M15        | I/O              | I/O              |
| M16        | PPECL (I/P)      | PPECL (I/P)      |
| M17        | I/O              | I/O              |
| M18        | AVDD             | AVDD             |
| M19        | GL               | GL               |
| M20        | I/O              | I/O              |
| M21        | I/O              | I/O              |
| M22        | I/O              | I/O              |
| N1         | I/O              | I/O              |
| N2         | I/O              | I/O              |
| N3         | NC               | I/O              |
| N4         | I/O              | I/O              |
| N5         | I/O              | I/O              |
| N6         | I/O              | I/O              |
| N7         | I/O              | I/O              |
| N8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| N9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| N10        | GND              | GND              |
| N11        | GND              | GND              |
| N12        | GND              | GND              |
| N13        | GND              | GND              |
| N14        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| N15        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| N16        | I/O              | I/O              |
| N17        | I/O              | I/O              |
| N18        | I/O              | I/O              |
| N19        | I/O              | I/O              |
| N20        | NC               | I/O              |
| N21        | I/O              | I/O              |
| N22        | I/O              | I/O              |
| P1         | I/O              | I/O              |
| P2         | I/O              | I/O              |
| P3         | I/O              | I/O              |
| P4         | I/O              | I/O              |
| P5         | I/O              | I/O              |
| P6         | I/O              | I/O              |
| P7         | I/O              | I/O              |
| P8         | V <sub>DDP</sub> | V <sub>DDP</sub> |

484-Pin FBGA (Continued)

| Pin Number | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|
| P9         | GND              | GND              |
| P10        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| P11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| P12        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| P13        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| P14        | GND              | GND              |
| P15        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| P16        | I/O              | I/O              |
| P17        | I/O              | I/O              |
| P18        | I/O              | I/O              |
| P19        | I/O              | I/O              |
| P20        | NC               | I/O              |
| P21        | I/O              | I/O              |
| P22        | I/O              | I/O              |
| R1         | I/O              | I/O              |
| R2         | I/O              | I/O              |
| R3         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| R4         | I/O              | I/O              |
| R5         | I/O              | I/O              |
| R6         | I/O              | I/O              |
| R7         | I/O              | I/O              |
| R8         | I/O              | I/O              |
| R9         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| R10        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| R11        | I/O              | I/O              |
| R12        | I/O              | I/O              |
| R13        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| R14        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| R15        | I/O              | I/O              |
| R16        | I/O              | I/O              |
| R17        | I/O              | I/O              |
| R18        | I/O              | I/O              |
| R19        | I/O              | I/O              |
| R20        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| R21        | I/O              | I/O              |
| R22        | I/O              | I/O              |
| T1         | I/O              | I/O              |
| T2         | I/O              | I/O              |
| T3         | NC               | I/O              |
| T4         | I/O              | I/O              |
| T5         | I/O              | I/O              |
| T6         | I/O              | I/O              |

484-Pin FBGA (Continued)

| Pin Number | APA450 Function | APA600 Function |
|------------|-----------------|-----------------|
| T7         | I/O             | I/O             |
| T8         | I/O             | I/O             |
| T9         | I/O             | I/O             |
| T10        | I/O             | I/O             |
| T11        | I/O             | I/O             |
| T12        | I/O             | I/O             |
| T13        | I/O             | I/O             |
| T14        | I/O             | I/O             |
| T15        | I/O             | I/O             |
| T16        | I/O             | I/O             |
| T17        | RCK             | RCK             |
| T18        | I/O             | I/O             |
| T19        | I/O             | I/O             |
| T20        | NC              | I/O             |
| T21        | I/O             | I/O             |
| T22        | I/O             | I/O             |
| U1         | I/O             | I/O             |
| U2         | I/O             | I/O             |
| U3         | I/O             | I/O             |
| U4         | I/O             | I/O             |
| U5         | I/O             | I/O             |
| U6         | I/O             | I/O             |
| U7         | I/O             | I/O             |
| U8         | I/O             | I/O             |
| U9         | I/O             | I/O             |
| U10        | I/O             | I/O             |
| U11        | I/O             | I/O             |
| U12        | I/O             | I/O             |
| U13        | I/O             | I/O             |
| U14        | I/O             | I/O             |
| U15        | I/O             | I/O             |
| U16        | TCK             | TCK             |
| U17        | V <sub>PP</sub> | V <sub>PP</sub> |
| U18        | TRST            | TRST            |
| U19        | I/O             | I/O             |
| U20        | NC              | I/O             |
| U21        | I/O             | I/O             |
| U22        | I/O             | I/O             |
| V1         | I/O             | I/O             |
| V2         | I/O             | I/O             |
| V3         | GND             | GND             |
| V4         | I/O             | I/O             |

484-Pin FBGA (Continued)

| Pin Number | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|
| V5         | I/O              | I/O              |
| V6         | I/O              | I/O              |
| V7         | I/O              | I/O              |
| V8         | I/O              | I/O              |
| V9         | I/O              | I/O              |
| V10        | I/O              | I/O              |
| V11        | I/O              | I/O              |
| V12        | I/O              | I/O              |
| V13        | I/O              | I/O              |
| V14        | I/O              | I/O              |
| V15        | I/O              | I/O              |
| V16        | I/O              | I/O              |
| V17        | TDI              | TDI              |
| V18        | V <sub>PN</sub>  | V <sub>PN</sub>  |
| V19        | TDO              | TDO              |
| V20        | GND              | GND              |
| V21        | NC               | I/O              |
| V22        | I/O              | I/O              |
| W1         | NC               | I/O              |
| W2         | I/O              | I/O              |
| W3         | I/O              | I/O              |
| W4         | GND              | GND              |
| W5         | I/O              | I/O              |
| W6         | I/O              | I/O              |
| W7         | I/O              | I/O              |
| W8         | I/O              | I/O              |
| W9         | I/O              | I/O              |
| W10        | I/O              | I/O              |
| W11        | I/O              | I/O              |
| W12        | I/O              | I/O              |
| W13        | I/O              | I/O              |
| W14        | I/O              | I/O              |
| W15        | I/O              | I/O              |
| W16        | I/O              | I/O              |
| W17        | I/O              | I/O              |
| W18        | TMS              | TMS              |
| W19        | GND              | GND              |
| W20        | NC               | I/O              |
| W21        | NC               | I/O              |
| W22        | I/O              | I/O              |
| Y1         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| Y2         | I/O              | I/O              |

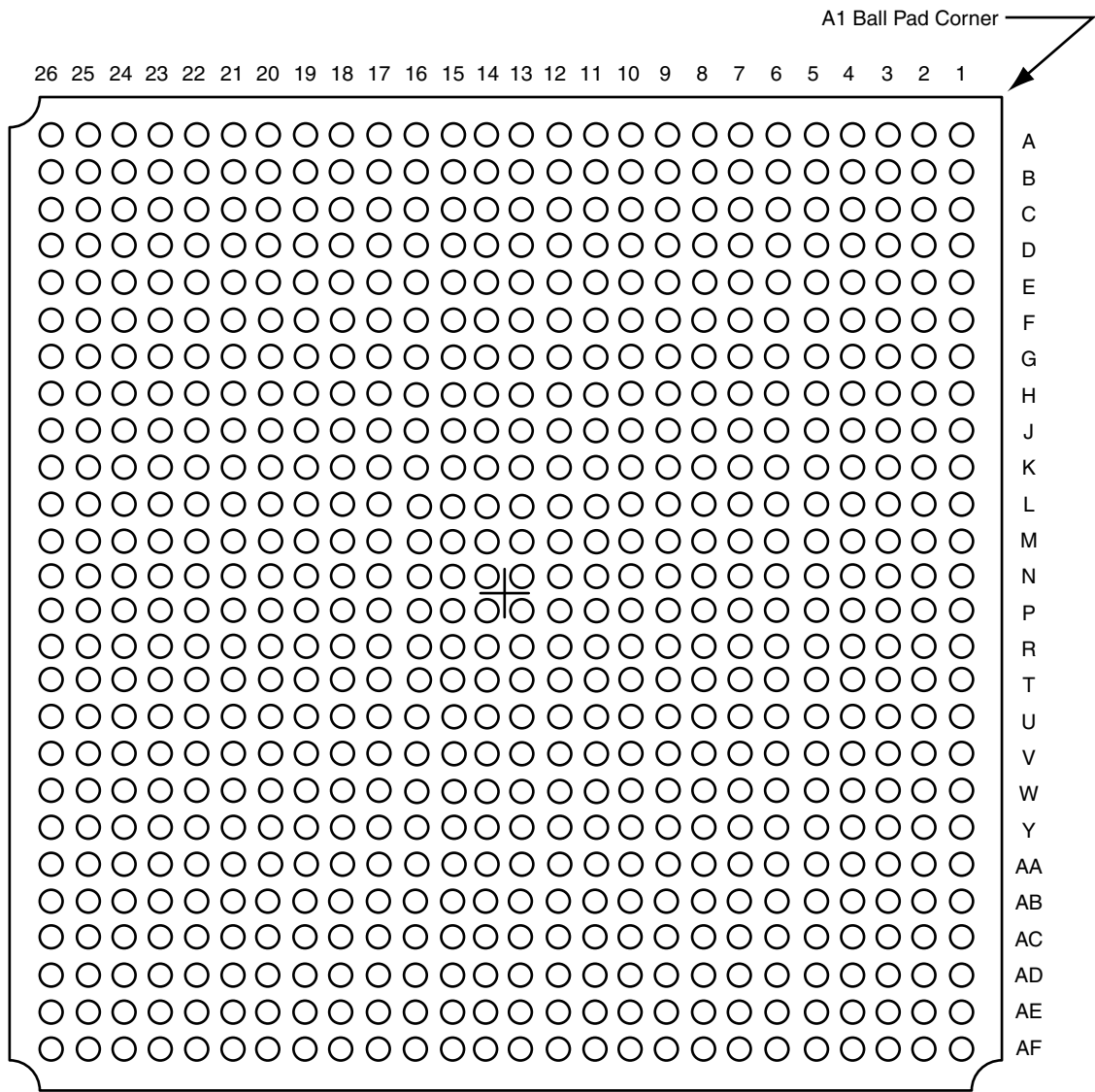
484-Pin FBGA (Continued)

| Pin Number | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|
| Y3         | I/O              | I/O              |
| Y4         | I/O              | I/O              |
| Y5         | GND              | GND              |
| Y6         | I/O              | I/O              |
| Y7         | I/O              | I/O              |
| Y8         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y10        | I/O              | I/O              |
| Y11        | I/O              | I/O              |
| Y12        | I/O              | I/O              |
| Y13        | I/O              | I/O              |
| Y14        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y15        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y16        | I/O              | I/O              |
| Y17        | I/O              | I/O              |
| Y18        | GND              | GND              |
| Y19        | I/O              | I/O              |
| Y20        | I/O              | I/O              |
| Y21        | NC               | I/O              |
| Y22        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AA1        | GND              | GND              |
| AA2        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AA3        | I/O              | I/O              |
| AA4        | I/O              | I/O              |
| AA5        | I/O              | I/O              |
| AA6        | I/O              | I/O              |
| AA7        | I/O              | I/O              |
| AA8        | I/O              | I/O              |
| AA9        | I/O              | I/O              |
| AA10       | I/O              | I/O              |
| AA11       | I/O              | I/O              |
| AA12       | I/O              | I/O              |
| AA13       | I/O              | I/O              |
| AA14       | I/O              | I/O              |
| AA15       | I/O              | I/O              |
| AA16       | I/O              | I/O              |
| AA17       | I/O              | I/O              |
| AA18       | NC               | I/O              |
| AA19       | NC               | I/O              |
| AA20       | I/O              | I/O              |
| AA21       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AA22       | GND              | GND              |

484-Pin FBGA (Continued)

| Pin Number | APA450 Function  | APA600 Function  |
|------------|------------------|------------------|
| AB1        | GND              | GND              |
| AB2        | GND              | GND              |
| AB3        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AB4        | I/O              | I/O              |
| AB5        | I/O              | I/O              |
| AB6        | I/O              | I/O              |
| AB7        | I/O              | I/O              |
| AB8        | I/O              | I/O              |
| AB9        | I/O              | I/O              |
| AB10       | I/O              | I/O              |
| AB11       | I/O              | I/O              |
| AB12       | I/O              | I/O              |
| AB13       | I/O              | I/O              |
| AB14       | I/O              | I/O              |
| AB15       | I/O              | I/O              |
| AB16       | I/O              | I/O              |
| AB17       | I/O              | I/O              |
| AB18       | NC               | I/O              |
| AB19       | I/O              | I/O              |
| AB20       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AB21       | GND              | GND              |
| AB22       | GND              | GND              |

Package Pin Assignments (Continued)  
676-Pin FBGA (Bottom View)



676-FBGA Pin

| Pin Number | APA600 Function | APA750 Function |
|------------|-----------------|-----------------|
| A1         | GND             | GND             |
| A2         | GND             | GND             |
| A3         | I/O             | I/O             |
| A4         | I/O             | I/O             |
| A5         | I/O             | I/O             |
| A6         | I/O             | I/O             |
| A7         | I/O             | I/O             |
| A8         | I/O             | I/O             |
| A9         | I/O             | I/O             |
| A10        | I/O             | I/O             |
| A11        | I/O             | I/O             |
| A12        | I/O             | I/O             |
| A13        | I/O             | I/O             |
| A14        | I/O             | I/O             |
| A15        | I/O             | I/O             |
| A16        | I/O             | I/O             |
| A17        | I/O             | I/O             |
| A18        | I/O             | I/O             |
| A19        | I/O             | I/O             |
| A20        | I/O             | I/O             |
| A21        | I/O             | I/O             |
| A22        | I/O             | I/O             |
| A23        | I/O             | I/O             |
| A24        | I/O             | I/O             |
| A25        | GND             | GND             |
| A26        | GND             | GND             |
| B1         | GND             | GND             |
| B2         | GND             | GND             |
| B3         | GND             | GND             |
| B4         | GND             | GND             |
| B5         | I/O             | I/O             |
| B6         | I/O             | I/O             |
| B7         | I/O             | I/O             |
| B8         | I/O             | I/O             |
| B9         | I/O             | I/O             |
| B10        | I/O             | I/O             |
| B11        | I/O             | I/O             |
| B12        | I/O             | I/O             |
| B13        | I/O             | I/O             |
| B14        | I/O             | I/O             |
| B15        | I/O             | I/O             |
| B16        | I/O             | I/O             |
| B17        | I/O             | I/O             |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function | APA750 Function |
|------------|-----------------|-----------------|
| B18        | I/O             | I/O             |
| B19        | I/O             | I/O             |
| B20        | I/O             | I/O             |
| B21        | I/O             | I/O             |
| B22        | I/O             | I/O             |
| B23        | I/O             | I/O             |
| B24        | I/O             | I/O             |
| B25        | GND             | GND             |
| B26        | GND             | GND             |
| C1         | GND             | GND             |
| C2         | GND             | GND             |
| C3         | GND             | GND             |
| C4         | GND             | GND             |
| C5         | I/O             | I/O             |
| C6         | I/O             | I/O             |
| C7         | I/O             | I/O             |
| C8         | I/O             | I/O             |
| C9         | I/O             | I/O             |
| C10        | I/O             | I/O             |
| C11        | I/O             | I/O             |
| C12        | I/O             | I/O             |
| C13        | I/O             | I/O             |
| C14        | I/O             | I/O             |
| C15        | I/O             | I/O             |
| C16        | I/O             | I/O             |
| C17        | I/O             | I/O             |
| C18        | I/O             | I/O             |
| C19        | I/O             | I/O             |
| C20        | I/O             | I/O             |
| C21        | I/O             | I/O             |
| C22        | I/O             | I/O             |
| C23        | I/O             | I/O             |
| C24        | I/O             | I/O             |
| C25        | I/O             | I/O             |
| C26        | I/O             | I/O             |
| D1         | I/O             | I/O             |
| D2         | I/O             | I/O             |
| D3         | GND             | GND             |
| D4         | I/O             | I/O             |
| D5         | I/O             | I/O             |
| D6         | I/O             | I/O             |
| D7         | I/O             | I/O             |
| D8         | I/O             | I/O             |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function | APA750 Function |
|------------|-----------------|-----------------|
| D9         | I/O             | I/O             |
| D10        | I/O             | I/O             |
| D11        | I/O             | I/O             |
| D12        | I/O             | I/O             |
| D13        | I/O             | I/O             |
| D14        | I/O             | I/O             |
| D15        | I/O             | I/O             |
| D16        | I/O             | I/O             |
| D17        | I/O             | I/O             |
| D18        | I/O             | I/O             |
| D19        | I/O             | I/O             |
| D20        | I/O             | I/O             |
| D21        | I/O             | I/O             |
| D22        | I/O             | I/O             |
| D23        | I/O             | I/O             |
| D24        | I/O             | I/O             |
| D25        | I/O             | I/O             |
| D26        | I/O             | I/O             |
| E1         | I/O             | I/O             |
| E2         | I/O             | I/O             |
| E3         | I/O             | I/O             |
| E4         | I/O             | I/O             |
| E5         | I/O             | I/O             |
| E6         | I/O             | I/O             |
| E7         | I/O             | I/O             |
| E8         | I/O             | I/O             |
| E9         | I/O             | I/O             |
| E10        | I/O             | I/O             |
| E11        | I/O             | I/O             |
| E12        | I/O             | I/O             |
| E13        | I/O             | I/O             |
| E14        | I/O             | I/O             |
| E15        | I/O             | I/O             |
| E16        | I/O             | I/O             |
| E17        | I/O             | I/O             |
| E18        | I/O             | I/O             |
| E19        | I/O             | I/O             |
| E20        | I/O             | I/O             |
| E21        | I/O             | I/O             |
| E22        | I/O             | I/O             |
| E23        | I/O             | I/O             |
| E24        | I/O             | I/O             |
| E25        | I/O             | I/O             |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function | APA750 Function |
|------------|-----------------|-----------------|
| E26        | I/O             | I/O             |
| F1         | I/O             | I/O             |
| F2         | I/O             | I/O             |
| F3         | I/O             | I/O             |
| F4         | I/O             | I/O             |
| F5         | GND             | GND             |
| F6         | I/O             | I/O             |
| F7         | NC              | NC              |
| F8         | I/O             | I/O             |
| F9         | I/O             | I/O             |
| F10        | I/O             | I/O             |
| F11        | I/O             | I/O             |
| F12        | I/O             | I/O             |
| F13        | I/O             | I/O             |
| F14        | I/O             | I/O             |
| F15        | I/O             | I/O             |
| F16        | I/O             | I/O             |
| F17        | I/O             | I/O             |
| F18        | I/O             | I/O             |
| F19        | I/O             | I/O             |
| F20        | I/O             | I/O             |
| F21        | I/O             | I/O             |
| F22        | I/O             | I/O             |
| F23        | I/O             | I/O             |
| F24        | I/O             | I/O             |
| F25        | I/O             | I/O             |
| F26        | I/O             | I/O             |
| G1         | I/O             | I/O             |
| G2         | I/O             | I/O             |
| G3         | I/O             | I/O             |
| G4         | I/O             | I/O             |
| G5         | I/O             | I/O             |
| G6         | I/O             | I/O             |
| G7         | I/O             | I/O             |
| G8         | V <sub>DD</sub> | V <sub>DD</sub> |
| G9         | NC              | NC              |
| G10        | I/O             | I/O             |
| G11        | NC              | NC              |
| G12        | I/O             | I/O             |
| G13        | NC              | NC              |
| G14        | I/O             | I/O             |
| G15        | NC              | NC              |
| G16        | I/O             | I/O             |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function  | APA750 Function  |
|------------|------------------|------------------|
| G17        | NC               | NC               |
| G18        | I/O              | I/O              |
| G19        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| G20        | NC               | NC               |
| G21        | I/O              | I/O              |
| G22        | I/O              | I/O              |
| G23        | I/O              | I/O              |
| G24        | I/O              | I/O              |
| G25        | I/O              | I/O              |
| G26        | I/O              | I/O              |
| H1         | I/O              | I/O              |
| H2         | I/O              | I/O              |
| H3         | I/O              | I/O              |
| H4         | I/O              | I/O              |
| H5         | I/O              | I/O              |
| H6         | I/O              | I/O              |
| H7         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H8         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| H9         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H10        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H11        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H12        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H13        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H14        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H15        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H16        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H17        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H18        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| H19        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| H20        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| H21        | I/O              | I/O              |
| H22        | I/O              | I/O              |
| H23        | I/O              | I/O              |
| H24        | I/O              | I/O              |
| H25        | I/O              | I/O              |
| H26        | I/O              | I/O              |
| J1         | I/O              | I/O              |
| J2         | I/O              | I/O              |
| J3         | I/O              | I/O              |
| J4         | I/O              | I/O              |
| J5         | I/O              | I/O              |
| J6         | I/O              | I/O              |
| J7         | NC               | NC               |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function  | APA750 Function  |
|------------|------------------|------------------|
| J8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| J9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J10        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J12        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J13        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J14        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J15        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J16        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J17        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J18        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J19        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| J20        | NC               | NC               |
| J21        | I/O              | I/O              |
| J22        | I/O              | I/O              |
| J23        | I/O              | I/O              |
| J24        | I/O              | I/O              |
| J25        | I/O              | I/O              |
| J26        | I/O              | I/O              |
| K1         | I/O              | I/O              |
| K2         | I/O              | I/O              |
| K3         | I/O              | I/O              |
| K4         | I/O              | I/O              |
| K5         | I/O              | I/O              |
| K6         | I/O              | I/O              |
| K7         | I/O              | I/O              |
| K8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| K10        | GND              | GND              |
| K11        | GND              | GND              |
| K12        | GND              | GND              |
| K13        | GND              | GND              |
| K14        | GND              | GND              |
| K15        | GND              | GND              |
| K16        | GND              | GND              |
| K17        | GND              | GND              |
| K18        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| K19        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K20        | I/O              | I/O              |
| K21        | I/O              | I/O              |
| K22        | I/O              | I/O              |
| K23        | I/O              | I/O              |
| K24        | I/O              | I/O              |



676-FBGA Pin (Continued)

| Pin Number | APA600 Function  | APA750 Function  |
|------------|------------------|------------------|
| K25        | I/O              | I/O              |
| K26        | I/O              | I/O              |
| L1         | I/O              | I/O              |
| L2         | I/O              | I/O              |
| L3         | I/O              | I/O              |
| L4         | I/O              | I/O              |
| L5         | I/O              | I/O              |
| L6         | I/O              | I/O              |
| L7         | NC               | NC               |
| L8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| L9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| L10        | GND              | GND              |
| L11        | GND              | GND              |
| L12        | GND              | GND              |
| L13        | GND              | GND              |
| L14        | GND              | GND              |
| L15        | GND              | GND              |
| L16        | GND              | GND              |
| L17        | GND              | GND              |
| L18        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| L19        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| L20        | NC               | NC               |
| L21        | I/O              | I/O              |
| L22        | I/O              | I/O              |
| L23        | I/O              | I/O              |
| L24        | I/O              | I/O              |
| L25        | I/O              | I/O              |
| L26        | I/O              | I/O              |
| M1         | I/O              | I/O              |
| M2         | I/O              | I/O              |
| M3         | I/O              | I/O              |
| M4         | I/O              | I/O              |
| M5         | I/O              | I/O              |
| M6         | I/O              | I/O              |
| M7         | I/O              | I/O              |
| M8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| M9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| M10        | GND              | GND              |
| M11        | GND              | GND              |
| M12        | GND              | GND              |
| M13        | GND              | GND              |
| M14        | GND              | GND              |
| M15        | GND              | GND              |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function  | APA750 Function  |
|------------|------------------|------------------|
| M16        | GND              | GND              |
| M17        | GND              | GND              |
| M18        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| M19        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| M20        | I/O              | I/O              |
| M21        | I/O              | I/O              |
| M22        | I/O              | I/O              |
| M23        | I/O              | I/O              |
| M24        | I/O              | I/O              |
| M25        | I/O              | I/O              |
| M26        | I/O              | I/O              |
| N1         | GL               | GL               |
| N2         | AGND             | AGND             |
| N3         | I/O (GLMX)       | I/O (GLMX)       |
| N4         | I/O              | I/O              |
| N5         | NPECL            | NPECL            |
| N6         | I/O              | I/O              |
| N7         | NC               | NC               |
| N8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| N9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| N10        | GND              | GND              |
| N11        | GND              | GND              |
| N12        | GND              | GND              |
| N13        | GND              | GND              |
| N14        | GND              | GND              |
| N15        | GND              | GND              |
| N16        | GND              | GND              |
| N17        | GND              | GND              |
| N18        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| N19        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| N20        | NC               | NC               |
| N21        | I/O              | I/O              |
| N22        | GL               | GL               |
| N23        | I/O              | I/O              |
| N24        | NPECL            | NPECL            |
| N25        | GL               | GL               |
| N26        | I/O              | I/O              |
| P1         | GL               | GL               |
| P2         | AVDD             | AVDD             |
| P3         | I/O              | I/O              |
| P4         | I/O              | I/O              |
| P5         | PPECL (I/P)      | PPECL (I/P)      |
| P6         | I/O              | I/O              |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function  | APA750 Function  |
|------------|------------------|------------------|
| P7         | I/O              | I/O              |
| P8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| P9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| P10        | GND              | GND              |
| P11        | GND              | GND              |
| P12        | GND              | GND              |
| P13        | GND              | GND              |
| P14        | GND              | GND              |
| P15        | GND              | GND              |
| P16        | GND              | GND              |
| P17        | GND              | GND              |
| P18        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| P19        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| P20        | I/O              | I/O              |
| P21        | I/O              | I/O              |
| P22        | I/O (GLMX)       | I/O (GLMX)       |
| P23        | I/O              | I/O              |
| P24        | PPECL (I/P)      | PPECL (I/P)      |
| P25        | AVDD             | AVDD             |
| P26        | AGND             | AGND             |
| R1         | I/O              | I/O              |
| R2         | I/O              | I/O              |
| R3         | I/O              | I/O              |
| R4         | I/O              | I/O              |
| R5         | I/O              | I/O              |
| R6         | I/O              | I/O              |
| R7         | NC               | NC               |
| R8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| R9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| R10        | GND              | GND              |
| R11        | GND              | GND              |
| R12        | GND              | GND              |
| R13        | GND              | GND              |
| R14        | GND              | GND              |
| R15        | GND              | GND              |
| R16        | GND              | GND              |
| R17        | GND              | GND              |
| R18        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| R19        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| R20        | NC               | NC               |
| R21        | I/O              | I/O              |
| R22        | I/O              | I/O              |
| R23        | I/O              | I/O              |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function  | APA750 Function  |
|------------|------------------|------------------|
| R24        | I/O              | I/O              |
| R25        | I/O              | I/O              |
| R26        | I/O              | I/O              |
| T1         | I/O              | I/O              |
| T2         | I/O              | I/O              |
| T3         | I/O              | I/O              |
| T4         | I/O              | I/O              |
| T5         | I/O              | I/O              |
| T6         | I/O              | I/O              |
| T7         | I/O              | I/O              |
| T8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| T9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| T10        | GND              | GND              |
| T11        | GND              | GND              |
| T12        | GND              | GND              |
| T13        | GND              | GND              |
| T14        | GND              | GND              |
| T15        | GND              | GND              |
| T16        | GND              | GND              |
| T17        | GND              | GND              |
| T18        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| T19        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| T20        | I/O              | I/O              |
| T21        | I/O              | I/O              |
| T22        | I/O              | I/O              |
| T23        | I/O              | I/O              |
| T24        | I/O              | I/O              |
| T25        | I/O              | I/O              |
| T26        | I/O              | I/O              |
| U1         | I/O              | I/O              |
| U2         | I/O              | I/O              |
| U3         | I/O              | I/O              |
| U4         | I/O              | I/O              |
| U5         | I/O              | I/O              |
| U6         | I/O              | I/O              |
| U7         | NC               | NC               |
| U8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| U9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| U10        | GND              | GND              |
| U11        | GND              | GND              |
| U12        | GND              | GND              |
| U13        | GND              | GND              |
| U14        | GND              | GND              |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function  | APA750 Function  |
|------------|------------------|------------------|
| U15        | GND              | GND              |
| U16        | GND              | GND              |
| U17        | GND              | GND              |
| U18        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| U19        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| U20        | NC               | NC               |
| U21        | I/O              | I/O              |
| U22        | I/O              | I/O              |
| U23        | I/O              | I/O              |
| U24        | I/O              | I/O              |
| U25        | I/O              | I/O              |
| U26        | I/O              | I/O              |
| V1         | I/O              | I/O              |
| V2         | I/O              | I/O              |
| V3         | I/O              | I/O              |
| V4         | I/O              | I/O              |
| V5         | I/O              | I/O              |
| V6         | I/O              | I/O              |
| V7         | I/O              | I/O              |
| V8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| V9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| V10        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| V11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| V12        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| V13        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| V14        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| V15        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| V16        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| V17        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| V18        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| V19        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| V20        | I/O              | I/O              |
| V21        | I/O              | I/O              |
| V22        | I/O              | I/O              |
| V23        | I/O              | I/O              |
| V24        | I/O              | I/O              |
| V25        | I/O              | I/O              |
| V26        | I/O              | I/O              |
| W1         | I/O              | I/O              |
| W2         | I/O              | I/O              |
| W3         | I/O              | I/O              |
| W4         | I/O              | I/O              |
| W5         | I/O              | I/O              |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function  | APA750 Function  |
|------------|------------------|------------------|
| W6         | I/O              | I/O              |
| W7         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| W8         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| W9         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W10        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W11        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W12        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W13        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W14        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W15        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W16        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W17        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W18        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W19        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| W20        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W21        | I/O              | I/O              |
| W22        | I/O              | I/O              |
| W23        | I/O              | I/O              |
| W24        | I/O              | I/O              |
| W25        | I/O              | I/O              |
| W26        | I/O              | I/O              |
| Y1         | I/O              | I/O              |
| Y2         | I/O              | I/O              |
| Y3         | I/O              | I/O              |
| Y4         | I/O              | I/O              |
| Y5         | I/O              | I/O              |
| Y6         | I/O              | I/O              |
| Y7         | I/O              | I/O              |
| Y8         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| Y9         | NC               | NC               |
| Y10        | I/O              | I/O              |
| Y11        | NC               | NC               |
| Y12        | I/O              | I/O              |
| Y13        | NC               | NC               |
| Y14        | I/O              | I/O              |
| Y15        | NC               | NC               |
| Y16        | I/O              | I/O              |
| Y17        | NC               | NC               |
| Y18        | I/O              | I/O              |
| Y19        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y20        | V <sub>PP</sub>  | V <sub>PP</sub>  |
| Y21        | I/O              | I/O              |
| Y22        | I/O              | I/O              |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function | APA750 Function |
|------------|-----------------|-----------------|
| Y23        | I/O             | I/O             |
| Y24        | I/O             | I/O             |
| Y25        | I/O             | I/O             |
| Y26        | I/O             | I/O             |
| AA1        | I/O             | I/O             |
| AA2        | I/O             | I/O             |
| AA3        | I/O             | I/O             |
| AA4        | I/O             | I/O             |
| AA5        | I/O             | I/O             |
| AA6        | GND             | GND             |
| AA7        | I/O             | I/O             |
| AA8        | I/O             | I/O             |
| AA9        | I/O             | I/O             |
| AA10       | I/O             | I/O             |
| AA11       | I/O             | I/O             |
| AA12       | I/O             | I/O             |
| AA13       | I/O             | I/O             |
| AA14       | I/O             | I/O             |
| AA15       | I/O             | I/O             |
| AA16       | I/O             | I/O             |
| AA17       | I/O             | I/O             |
| AA18       | I/O             | I/O             |
| AA19       | I/O             | I/O             |
| AA20       | I/O             | I/O             |
| AA21       | TDO             | TDO             |
| AA22       | GND             | GND             |
| AA23       | GND             | GND             |
| AA24       | I/O             | I/O             |
| AA25       | I/O             | I/O             |
| AA26       | I/O             | I/O             |
| AB1        | I/O             | I/O             |
| AB2        | I/O             | I/O             |
| AB3        | I/O             | I/O             |
| AB4        | I/O             | I/O             |
| AB5        | I/O             | I/O             |
| AB6        | GND             | GND             |
| AB7        | GND             | GND             |
| AB8        | I/O             | I/O             |
| AB9        | I/O             | I/O             |
| AB10       | I/O             | I/O             |
| AB11       | I/O             | I/O             |
| AB12       | I/O             | I/O             |
| AB13       | I/O             | I/O             |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function | APA750 Function |
|------------|-----------------|-----------------|
| AB14       | I/O             | I/O             |
| AB15       | I/O             | I/O             |
| AB16       | I/O             | I/O             |
| AB17       | I/O             | I/O             |
| AB18       | I/O             | I/O             |
| AB19       | I/O             | I/O             |
| AB20       | I/O             | I/O             |
| AB21       | TCK             | TCK             |
| AB22       | TRST            | TRST            |
| AB23       | I/O             | I/O             |
| AB24       | I/O             | I/O             |
| AB25       | I/O             | I/O             |
| AB26       | I/O             | I/O             |
| AC1        | I/O             | I/O             |
| AC2        | I/O             | I/O             |
| AC3        | I/O             | I/O             |
| AC4        | I/O             | I/O             |
| AC5        | GND             | GND             |
| AC6        | I/O             | I/O             |
| AC7        | I/O             | I/O             |
| AC8        | I/O             | I/O             |
| AC9        | GND             | GND             |
| AC10       | I/O             | I/O             |
| AC11       | I/O             | I/O             |
| AC12       | I/O             | I/O             |
| AC13       | I/O             | I/O             |
| AC14       | I/O             | I/O             |
| AC15       | I/O             | I/O             |
| AC16       | I/O             | I/O             |
| AC17       | I/O             | I/O             |
| AC18       | I/O             | I/O             |
| AC19       | I/O             | I/O             |
| AC20       | I/O             | I/O             |
| AC21       | I/O             | I/O             |
| AC22       | TMS             | TMS             |
| AC23       | RCK             | RCK             |
| AC24       | I/O             | I/O             |
| AC25       | I/O             | I/O             |
| AC26       | I/O             | I/O             |
| AD1        | I/O             | I/O             |
| AD2        | I/O             | I/O             |
| AD3        | I/O             | I/O             |
| AD4        | I/O             | I/O             |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function | APA750 Function |
|------------|-----------------|-----------------|
| AD5        | I/O             | I/O             |
| AD6        | I/O             | I/O             |
| AD7        | I/O             | I/O             |
| AD8        | I/O             | I/O             |
| AD9        | I/O             | I/O             |
| AD10       | I/O             | I/O             |
| AD11       | I/O             | I/O             |
| AD12       | I/O             | I/O             |
| AD13       | I/O             | I/O             |
| AD14       | I/O             | I/O             |
| AD15       | I/O             | I/O             |
| AD16       | I/O             | I/O             |
| AD17       | I/O             | I/O             |
| AD18       | I/O             | I/O             |
| AD19       | I/O             | I/O             |
| AD20       | I/O             | I/O             |
| AD21       | I/O             | I/O             |
| AD22       | I/O             | I/O             |
| AD23       | TDI             | TDI             |
| AD24       | V <sub>PN</sub> | V <sub>PN</sub> |
| AD25       | I/O             | I/O             |
| AD26       | I/O             | I/O             |
| AE1        | GND             | GND             |
| AE2        | GND             | GND             |
| AE3        | GND             | GND             |
| AE4        | I/O             | I/O             |
| AE5        | I/O             | I/O             |
| AE6        | I/O             | I/O             |
| AE7        | I/O             | I/O             |
| AE8        | I/O             | I/O             |
| AE9        | I/O             | I/O             |
| AE10       | I/O             | I/O             |
| AE11       | I/O             | I/O             |
| AE12       | I/O             | I/O             |
| AE13       | I/O             | I/O             |
| AE14       | I/O             | I/O             |
| AE15       | I/O             | I/O             |
| AE16       | I/O             | I/O             |
| AE17       | I/O             | I/O             |
| AE18       | I/O             | I/O             |
| AE19       | I/O             | I/O             |
| AE20       | I/O             | I/O             |
| AE21       | I/O             | I/O             |

676-FBGA Pin (Continued)

| Pin Number | APA600 Function | APA750 Function |
|------------|-----------------|-----------------|
| AE22       | I/O             | I/O             |
| AE23       | I/O             | I/O             |
| AE24       | I/O             | I/O             |
| AE25       | GND             | GND             |
| AE26       | GND             | GND             |
| AF1        | GND             | GND             |
| AF2        | GND             | GND             |
| AF3        | GND             | GND             |
| AF4        | GND             | GND             |
| AF5        | I/O             | I/O             |
| AF6        | I/O             | I/O             |
| AF7        | I/O             | I/O             |
| AF8        | I/O             | I/O             |
| AF9        | I/O             | I/O             |
| AF10       | I/O             | I/O             |
| AF11       | I/O             | I/O             |
| AF12       | I/O             | I/O             |
| AF13       | I/O             | I/O             |
| AF14       | I/O             | I/O             |
| AF15       | I/O             | I/O             |
| AF16       | I/O             | I/O             |
| AF17       | I/O             | I/O             |
| AF18       | I/O             | I/O             |
| AF19       | I/O             | I/O             |
| AF20       | I/O             | I/O             |
| AF21       | I/O             | I/O             |
| AF22       | I/O             | I/O             |
| AF23       | I/O             | I/O             |
| AF24       | I/O             | I/O             |
| AF25       | GND             | GND             |
| AF26       | GND             | GND             |

### 896-Pin FBGA (Bottom View)

896 FBGA Pin

| Pin Number | APA750 Function | APA1000 Function |
|------------|-----------------|------------------|
| A2         | GND             | GND              |
| A3         | GND             | GND              |
| A4         | I/O             | I/O              |
| A5         | GND             | GND              |
| A6         | I/O             | I/O              |
| A7         | GND             | GND              |
| A8         | I/O             | I/O              |
| A9         | I/O             | I/O              |
| A10        | I/O             | I/O              |
| A11        | I/O             | I/O              |
| A12        | I/O             | I/O              |
| A13        | I/O             | I/O              |
| A14        | I/O             | I/O              |
| A15        | I/O             | I/O              |
| A16        | I/O             | I/O              |
| A17        | I/O             | I/O              |
| A18        | I/O             | I/O              |
| A19        | I/O             | I/O              |
| A20        | I/O             | I/O              |
| A21        | I/O             | I/O              |
| A22        | I/O             | I/O              |
| A23        | I/O             | I/O              |
| A24        | GND             | GND              |
| A25        | I/O             | I/O              |
| A26        | GND             | GND              |
| A27        | I/O             | I/O              |
| A28        | GND             | GND              |
| A29        | GND             | GND              |
| B1         | GND             | GND              |
| B2         | GND             | GND              |
| B3         | I/O             | I/O              |
| B4         | V <sub>DD</sub> | V <sub>DD</sub>  |
| B5         | I/O             | I/O              |
| B6         | V <sub>DD</sub> | V <sub>DD</sub>  |
| B7         | I/O             | I/O              |
| B8         | I/O             | I/O              |
| B9         | I/O             | I/O              |
| B10        | I/O             | I/O              |
| B11        | I/O             | I/O              |
| B12        | I/O             | I/O              |
| B13        | I/O             | I/O              |
| B14        | I/O             | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| B15        | I/O              | I/O              |
| B16        | I/O              | I/O              |
| B17        | I/O              | I/O              |
| B18        | I/O              | I/O              |
| B19        | I/O              | I/O              |
| B20        | I/O              | I/O              |
| B21        | I/O              | I/O              |
| B22        | I/O              | I/O              |
| B23        | I/O              | I/O              |
| B24        | I/O              | I/O              |
| B25        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| B26        | I/O              | I/O              |
| B27        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| B28        | I/O              | I/O              |
| B29        | GND              | GND              |
| B30        | GND              | GND              |
| C1         | GND              | GND              |
| C2         | I/O              | I/O              |
| C3         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| C4         | I/O              | I/O              |
| C5         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| C6         | I/O              | I/O              |
| C7         | I/O              | I/O              |
| C8         | I/O              | I/O              |
| C9         | I/O              | I/O              |
| C10        | I/O              | I/O              |
| C11        | I/O              | I/O              |
| C12        | I/O              | I/O              |
| C13        | I/O              | I/O              |
| C14        | I/O              | I/O              |
| C15        | I/O              | I/O              |
| C16        | I/O              | I/O              |
| C17        | I/O              | I/O              |
| C18        | I/O              | I/O              |
| C19        | I/O              | I/O              |
| C20        | I/O              | I/O              |
| C21        | I/O              | I/O              |
| C22        | I/O              | I/O              |
| C23        | I/O              | I/O              |
| C24        | I/O              | I/O              |
| C25        | I/O              | I/O              |
| C26        | V <sub>DDP</sub> | V <sub>DDP</sub> |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| C27        | I/O              | I/O              |
| C28        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| C29        | NC               | I/O              |
| C30        | GND              | GND              |
| D1         | I/O              | I/O              |
| D2         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| D3         | I/O              | I/O              |
| D4         | GND              | GND              |
| D5         | I/O              | I/O              |
| D6         | I/O              | I/O              |
| D7         | I/O              | I/O              |
| D8         | I/O              | I/O              |
| D9         | I/O              | I/O              |
| D10        | I/O              | I/O              |
| D11        | I/O              | I/O              |
| D12        | I/O              | I/O              |
| D13        | I/O              | I/O              |
| D14        | I/O              | I/O              |
| D15        | I/O              | I/O              |
| D16        | I/O              | I/O              |
| D17        | I/O              | I/O              |
| D18        | I/O              | I/O              |
| D19        | I/O              | I/O              |
| D20        | I/O              | I/O              |
| D21        | I/O              | I/O              |
| D22        | I/O              | I/O              |
| D23        | I/O              | I/O              |
| D24        | I/O              | I/O              |
| D25        | I/O              | I/O              |
| D26        | I/O              | I/O              |
| D27        | GND              | GND              |
| D28        | I/O              | I/O              |
| D29        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| D30        | I/O              | I/O              |
| E1         | GND              | GND              |
| E2         | I/O              | I/O              |
| E3         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| E4         | I/O              | I/O              |
| E5         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| E6         | I/O              | I/O              |
| E7         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| E8         | I/O              | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| E9         | I/O              | I/O              |
| E10        | I/O              | I/O              |
| E11        | I/O              | I/O              |
| E12        | I/O              | I/O              |
| E13        | I/O              | I/O              |
| E14        | I/O              | I/O              |
| E15        | I/O              | I/O              |
| E16        | I/O              | I/O              |
| E17        | I/O              | I/O              |
| E18        | I/O              | I/O              |
| E19        | I/O              | I/O              |
| E20        | I/O              | I/O              |
| E21        | I/O              | I/O              |
| E22        | I/O              | I/O              |
| E23        | I/O              | I/O              |
| E24        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| E25        | I/O              | I/O              |
| E26        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| E27        | I/O              | I/O              |
| E28        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| E29        | I/O              | I/O              |
| E30        | GND              | GND              |
| F1         | I/O              | I/O              |
| F2         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| F3         | I/O              | I/O              |
| F4         | I/O              | I/O              |
| F5         | I/O              | I/O              |
| F6         | GND              | GND              |
| F7         | I/O              | I/O              |
| F8         | I/O              | I/O              |
| F9         | I/O              | I/O              |
| F10        | I/O              | I/O              |
| F11        | I/O              | I/O              |
| F12        | I/O              | I/O              |
| F13        | I/O              | I/O              |
| F14        | I/O              | I/O              |
| F15        | I/O              | I/O              |
| F16        | I/O              | I/O              |
| F17        | I/O              | I/O              |
| F18        | I/O              | I/O              |
| F19        | I/O              | I/O              |
| F20        | I/O              | I/O              |



896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| F21        | I/O              | I/O              |
| F22        | I/O              | I/O              |
| F23        | I/O              | I/O              |
| F24        | I/O              | I/O              |
| F25        | GND              | GND              |
| F26        | I/O              | I/O              |
| F27        | I/O              | I/O              |
| F28        | I/O              | I/O              |
| F29        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| F30        | I/O              | I/O              |
| G1         | GND              | GND              |
| G2         | I/O              | I/O              |
| G3         | I/O              | I/O              |
| G4         | I/O              | I/O              |
| G5         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| G6         | I/O              | I/O              |
| G7         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| G8         | I/O              | I/O              |
| G9         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| G10        | I/O              | I/O              |
| G11        | I/O              | I/O              |
| G12        | I/O              | I/O              |
| G13        | I/O              | I/O              |
| G14        | I/O              | I/O              |
| G15        | I/O              | I/O              |
| G16        | I/O              | I/O              |
| G17        | I/O              | I/O              |
| G18        | I/O              | I/O              |
| G19        | I/O              | I/O              |
| G20        | I/O              | I/O              |
| G21        | I/O              | I/O              |
| G22        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| G23        | I/O              | I/O              |
| G24        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| G25        | I/O              | I/O              |
| G26        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| G27        | I/O              | I/O              |
| G28        | I/O              | I/O              |
| G29        | I/O              | I/O              |
| G30        | GND              | GND              |
| H1         | I/O              | I/O              |
| H2         | I/O              | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| H3         | I/O              | I/O              |
| H4         | I/O              | I/O              |
| H5         | I/O              | I/O              |
| H6         | I/O              | I/O              |
| H7         | I/O              | I/O              |
| H8         | GND              | GND              |
| H9         | NC               | I/O              |
| H10        | NC               | I/O              |
| H11        | NC               | I/O              |
| H12        | NC               | I/O              |
| H13        | NC               | I/O              |
| H14        | NC               | I/O              |
| H15        | NC               | I/O              |
| H16        | NC               | I/O              |
| H17        | NC               | I/O              |
| H18        | NC               | I/O              |
| H19        | NC               | I/O              |
| H20        | NC               | I/O              |
| H21        | NC               | I/O              |
| H22        | NC               | I/O              |
| H23        | GND              | GND              |
| H24        | I/O              | I/O              |
| H25        | I/O              | I/O              |
| H26        | I/O              | I/O              |
| H27        | I/O              | I/O              |
| H28        | I/O              | I/O              |
| H29        | I/O              | I/O              |
| H30        | I/O              | I/O              |
| J1         | I/O              | I/O              |
| J2         | I/O              | I/O              |
| J3         | I/O              | I/O              |
| J4         | I/O              | I/O              |
| J5         | I/O              | I/O              |
| J6         | I/O              | I/O              |
| J7         | V <sub>DDP</sub> | V <sub>DDP</sub> |
| J8         | I/O              | I/O              |
| J9         | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J10        | NC               | I/O              |
| J11        | NC               | I/O              |
| J12        | NC               | I/O              |
| J13        | NC               | I/O              |
| J14        | NC               | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| J15        | NC               | I/O              |
| J16        | NC               | I/O              |
| J17        | NC               | I/O              |
| J18        | NC               | I/O              |
| J19        | NC               | I/O              |
| J20        | NC               | I/O              |
| J21        | NC               | I/O              |
| J22        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| J23        | I/O              | I/O              |
| J24        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| J25        | I/O              | I/O              |
| J26        | I/O              | I/O              |
| J27        | I/O              | I/O              |
| J28        | I/O              | I/O              |
| J29        | I/O              | I/O              |
| J30        | I/O              | I/O              |
| K1         | I/O              | I/O              |
| K2         | I/O              | I/O              |
| K3         | I/O              | I/O              |
| K4         | I/O              | I/O              |
| K5         | I/O              | I/O              |
| K6         | I/O              | I/O              |
| K7         | I/O              | I/O              |
| K8         | I/O              | I/O              |
| K9         | NC               | I/O              |
| K10        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| K11        | NC               | I/O              |
| K12        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K13        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K14        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K15        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K16        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K17        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K18        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K19        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| K20        | NC               | I/O              |
| K21        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| K22        | NC               | I/O              |
| K23        | I/O              | I/O              |
| K24        | I/O              | I/O              |
| K25        | I/O              | I/O              |
| K26        | I/O              | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function | APA1000 Function |
|------------|-----------------|------------------|
| K27        | I/O             | I/O              |
| K28        | I/O             | I/O              |
| K29        | I/O             | I/O              |
| K30        | I/O             | I/O              |
| L1         | I/O             | I/O              |
| L2         | I/O             | I/O              |
| L3         | I/O             | I/O              |
| L4         | I/O             | I/O              |
| L5         | I/O             | I/O              |
| L6         | I/O             | I/O              |
| L7         | I/O             | I/O              |
| L8         | I/O             | I/O              |
| L9         | NC              | I/O              |
| L10        | NC              | I/O              |
| L11        | V <sub>DD</sub> | V <sub>DD</sub>  |
| L12        | V <sub>DD</sub> | V <sub>DD</sub>  |
| L13        | V <sub>DD</sub> | V <sub>DD</sub>  |
| L14        | V <sub>DD</sub> | V <sub>DD</sub>  |
| L15        | V <sub>DD</sub> | V <sub>DD</sub>  |
| L16        | V <sub>DD</sub> | V <sub>DD</sub>  |
| L17        | V <sub>DD</sub> | V <sub>DD</sub>  |
| L18        | V <sub>DD</sub> | V <sub>DD</sub>  |
| L19        | V <sub>DD</sub> | V <sub>DD</sub>  |
| L20        | V <sub>DD</sub> | V <sub>DD</sub>  |
| L21        | NC              | I/O              |
| L22        | NC              | I/O              |
| L23        | I/O             | I/O              |
| L24        | I/O             | I/O              |
| L25        | I/O             | I/O              |
| L26        | I/O             | I/O              |
| L27        | I/O             | I/O              |
| L28        | I/O             | I/O              |
| L29        | I/O             | I/O              |
| L30        | I/O             | I/O              |
| M1         | I/O             | I/O              |
| M2         | I/O             | I/O              |
| M3         | I/O             | I/O              |
| M4         | I/O             | I/O              |
| M5         | I/O             | I/O              |
| M6         | I/O             | I/O              |
| M7         | I/O             | I/O              |
| M8         | I/O             | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| M9         | NC               | I/O              |
| M10        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| M11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| M12        | GND              | GND              |
| M13        | GND              | GND              |
| M14        | GND              | GND              |
| M15        | GND              | GND              |
| M16        | GND              | GND              |
| M17        | GND              | GND              |
| M18        | GND              | GND              |
| M19        | GND              | GND              |
| M20        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| M21        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| M22        | NC               | I/O              |
| M23        | I/O              | I/O              |
| M24        | I/O              | I/O              |
| M25        | I/O              | I/O              |
| M26        | I/O              | I/O              |
| M27        | I/O              | I/O              |
| M28        | I/O              | I/O              |
| M29        | I/O              | I/O              |
| M30        | I/O              | I/O              |
| N1         | I/O              | I/O              |
| N2         | I/O              | I/O              |
| N3         | I/O              | I/O              |
| N4         | I/O              | I/O              |
| N5         | I/O              | I/O              |
| N6         | I/O              | I/O              |
| N7         | I/O              | I/O              |
| N8         | I/O              | I/O              |
| N9         | NC               | I/O              |
| N10        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| N11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| N12        | GND              | GND              |
| N13        | GND              | GND              |
| N14        | GND              | GND              |
| N15        | GND              | GND              |
| N16        | GND              | GND              |
| N17        | GND              | GND              |
| N18        | GND              | GND              |
| N19        | GND              | GND              |
| N20        | V <sub>DD</sub>  | V <sub>DD</sub>  |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| N21        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| N22        | NC               | I/O              |
| N23        | I/O              | I/O              |
| N24        | I/O              | I/O              |
| N25        | I/O              | I/O              |
| N26        | I/O              | I/O              |
| N27        | I/O              | I/O              |
| N28        | I/O              | I/O              |
| N29        | I/O              | I/O              |
| N30        | I/O              | I/O              |
| P1         | I/O              | I/O              |
| P2         | I/O              | I/O              |
| P3         | I/O              | I/O              |
| P4         | I/O              | I/O              |
| P5         | I/O              | I/O              |
| P6         | I/O              | I/O              |
| P7         | I/O              | I/O              |
| P8         | I/O              | I/O              |
| P9         | I/O              | I/O              |
| P10        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| P11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| P12        | GND              | GND              |
| P13        | GND              | GND              |
| P14        | GND              | GND              |
| P15        | GND              | GND              |
| P16        | GND              | GND              |
| P17        | GND              | GND              |
| P18        | GND              | GND              |
| P19        | GND              | GND              |
| P20        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| P21        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| P22        | I/O              | I/O              |
| P23        | I/O              | I/O              |
| P24        | I/O              | I/O              |
| P25        | I/O              | I/O              |
| P26        | I/O              | I/O              |
| P27        | I/O              | I/O              |
| P28        | I/O              | I/O              |
| P29        | I/O              | I/O              |
| P30        | I/O              | I/O              |
| R1         | I/O              | I/O              |
| R2         | I/O (GLMX)       | I/O (GLMX)       |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| R3         | AGND             | AGND             |
| R4         | NPECL            | NPECL            |
| R5         | GL               | GL               |
| R6         | I/O              | I/O              |
| R7         | I/O              | I/O              |
| R8         | I/O              | I/O              |
| R9         | NC               | I/O              |
| R10        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| R11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| R12        | GND              | GND              |
| R13        | GND              | GND              |
| R14        | GND              | GND              |
| R15        | GND              | GND              |
| R16        | GND              | GND              |
| R17        | GND              | GND              |
| R18        | GND              | GND              |
| R19        | GND              | GND              |
| R20        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| R21        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| R22        | I/O              | I/O              |
| R23        | I/O              | I/O              |
| R24        | I/O              | I/O              |
| R25        | I/O              | I/O              |
| R26        | I/O              | I/O              |
| R27        | NPECL            | NPECL            |
| R28        | AGND             | AGND             |
| R29        | I/O (GLMX)       | I/O (GLMX)       |
| R30        | I/O              | I/O              |
| T1         | I/O              | I/O              |
| T2         | AVDD             | AVDD             |
| T3         | GL               | GL               |
| T4         | PPECL (I/P)      | PPECL (I/P)      |
| T5         | I/O              | I/O              |
| T6         | I/O              | I/O              |
| T7         | I/O              | I/O              |
| T8         | I/O              | I/O              |
| T9         | I/O              | I/O              |
| T10        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| T11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| T12        | GND              | GND              |
| T13        | GND              | GND              |
| T14        | GND              | GND              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| T15        | GND              | GND              |
| T16        | GND              | GND              |
| T17        | GND              | GND              |
| T18        | GND              | GND              |
| T19        | GND              | GND              |
| T20        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| T21        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| T22        | I/O              | I/O              |
| T23        | I/O              | I/O              |
| T24        | I/O              | I/O              |
| T25        | I/O              | I/O              |
| T26        | PPECL (I/P)      | PPECL (I/P)      |
| T27        | GL               | GL               |
| T28        | GL               | GL               |
| T29        | AVDD             | AVDD             |
| T30        | I/O              | I/O              |
| U1         | I/O              | I/O              |
| U2         | I/O              | I/O              |
| U3         | I/O              | I/O              |
| U4         | I/O              | I/O              |
| U5         | I/O              | I/O              |
| U6         | I/O              | I/O              |
| U7         | I/O              | I/O              |
| U8         | I/O              | I/O              |
| U9         | NC               | I/O              |
| U10        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| U11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| U12        | GND              | GND              |
| U13        | GND              | GND              |
| U14        | GND              | GND              |
| U15        | GND              | GND              |
| U16        | GND              | GND              |
| U17        | GND              | GND              |
| U18        | GND              | GND              |
| U19        | GND              | GND              |
| U20        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| U21        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| U22        | NC               | I/O              |
| U23        | I/O              | I/O              |
| U24        | I/O              | I/O              |
| U25        | I/O              | I/O              |
| U26        | I/O              | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| U27        | I/O              | I/O              |
| U28        | I/O              | I/O              |
| U29        | I/O              | I/O              |
| U30        | I/O              | I/O              |
| V1         | I/O              | I/O              |
| V2         | I/O              | I/O              |
| V3         | I/O              | I/O              |
| V4         | I/O              | I/O              |
| V5         | I/O              | I/O              |
| V6         | I/O              | I/O              |
| V7         | I/O              | I/O              |
| V8         | I/O              | I/O              |
| V9         | NC               | I/O              |
| V10        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| V11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| V12        | GND              | GND              |
| V13        | GND              | GND              |
| V14        | GND              | GND              |
| V15        | GND              | GND              |
| V16        | GND              | GND              |
| V17        | GND              | GND              |
| V18        | GND              | GND              |
| V19        | GND              | GND              |
| V20        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| V21        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| V22        | NC               | I/O              |
| V23        | I/O              | I/O              |
| V24        | I/O              | I/O              |
| V25        | I/O              | I/O              |
| V26        | I/O              | I/O              |
| V27        | I/O              | I/O              |
| V28        | I/O              | I/O              |
| V29        | I/O              | I/O              |
| V30        | I/O              | I/O              |
| W1         | I/O              | I/O              |
| W2         | I/O              | I/O              |
| W3         | I/O              | I/O              |
| W4         | I/O              | I/O              |
| W5         | I/O              | I/O              |
| W6         | I/O              | I/O              |
| W7         | I/O              | I/O              |
| W8         | I/O              | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| W9         | NC               | I/O              |
| W10        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| W12        | GND              | GND              |
| W13        | GND              | GND              |
| W14        | GND              | GND              |
| W15        | GND              | GND              |
| W16        | GND              | GND              |
| W17        | GND              | GND              |
| W18        | GND              | GND              |
| W19        | GND              | GND              |
| W20        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| W21        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| W22        | NC               | I/O              |
| W23        | I/O              | I/O              |
| W24        | I/O              | I/O              |
| W25        | I/O              | I/O              |
| W26        | I/O              | I/O              |
| W27        | I/O              | I/O              |
| W28        | I/O              | I/O              |
| W29        | I/O              | I/O              |
| W30        | I/O              | I/O              |
| Y1         | I/O              | I/O              |
| Y2         | I/O              | I/O              |
| Y3         | I/O              | I/O              |
| Y4         | I/O              | I/O              |
| Y5         | I/O              | I/O              |
| Y6         | I/O              | I/O              |
| Y7         | I/O              | I/O              |
| Y8         | I/O              | I/O              |
| Y9         | NC               | I/O              |
| Y10        | NC               | I/O              |
| Y11        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y12        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y13        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y14        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y15        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y16        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y17        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y18        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y19        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| Y20        | V <sub>DD</sub>  | V <sub>DD</sub>  |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| Y21        | NC               | I/O              |
| Y22        | NC               | I/O              |
| Y23        | I/O              | I/O              |
| Y24        | I/O              | I/O              |
| Y25        | I/O              | I/O              |
| Y26        | I/O              | I/O              |
| Y27        | I/O              | I/O              |
| Y28        | I/O              | I/O              |
| Y29        | I/O              | I/O              |
| Y30        | I/O              | I/O              |
| AA1        | I/O              | I/O              |
| AA2        | I/O              | I/O              |
| AA3        | I/O              | I/O              |
| AA4        | I/O              | I/O              |
| AA5        | I/O              | I/O              |
| AA6        | I/O              | I/O              |
| AA7        | I/O              | I/O              |
| AA8        | I/O              | I/O              |
| AA9        | NC               | I/O              |
| AA10       | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AA11       | NC               | I/O              |
| AA12       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AA13       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AA14       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AA15       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AA16       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AA17       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AA18       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AA19       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AA20       | NC               | I/O              |
| AA21       | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AA22       | NC               | I/O              |
| AA23       | I/O              | I/O              |
| AA24       | I/O              | I/O              |
| AA25       | I/O              | I/O              |
| AA26       | I/O              | I/O              |
| AA27       | I/O              | I/O              |
| AA28       | I/O              | I/O              |
| AA29       | I/O              | I/O              |
| AA30       | I/O              | I/O              |
| AB1        | I/O              | I/O              |
| AB2        | I/O              | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| AB3        | I/O              | I/O              |
| AB4        | I/O              | I/O              |
| AB5        | I/O              | I/O              |
| AB6        | I/O              | I/O              |
| AB7        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AB8        | I/O              | I/O              |
| AB9        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AB10       | NC               | I/O              |
| AB11       | NC               | I/O              |
| AB12       | NC               | I/O              |
| AB13       | NC               | I/O              |
| AB14       | NC               | I/O              |
| AB15       | NC               | I/O              |
| AB16       | NC               | I/O              |
| AB17       | NC               | I/O              |
| AB18       | NC               | I/O              |
| AB19       | NC               | I/O              |
| AB20       | NC               | I/O              |
| AB21       | NC               | I/O              |
| AB22       | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AB23       | I/O              | I/O              |
| AB24       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AB25       | I/O              | I/O              |
| AB26       | I/O              | I/O              |
| AB27       | I/O              | I/O              |
| AB28       | I/O              | I/O              |
| AB29       | I/O              | I/O              |
| AB30       | I/O              | I/O              |
| AC1        | I/O              | I/O              |
| AC2        | I/O              | I/O              |
| AC3        | I/O              | I/O              |
| AC4        | I/O              | I/O              |
| AC5        | I/O              | I/O              |
| AC6        | I/O              | I/O              |
| AC7        | I/O              | I/O              |
| AC8        | GND              | GND              |
| AC9        | NC               | I/O              |
| AC10       | NC               | I/O              |
| AC11       | NC               | I/O              |
| AC12       | NC               | I/O              |
| AC13       | NC               | I/O              |
| AC14       | NC               | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| AC15       | NC               | I/O              |
| AC16       | NC               | I/O              |
| AC17       | NC               | I/O              |
| AC18       | NC               | I/O              |
| AC19       | NC               | I/O              |
| AC20       | NC               | I/O              |
| AC21       | NC               | I/O              |
| AC22       | NC               | I/O              |
| AC23       | GND              | GND              |
| AC24       | I/O              | I/O              |
| AC25       | I/O              | I/O              |
| AC26       | I/O              | I/O              |
| AC27       | I/O              | I/O              |
| AC28       | I/O              | I/O              |
| AC29       | I/O              | I/O              |
| AC30       | I/O              | I/O              |
| AD1        | GND              | GND              |
| AD2        | I/O              | I/O              |
| AD3        | I/O              | I/O              |
| AD4        | I/O              | I/O              |
| AD5        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AD6        | I/O              | I/O              |
| AD7        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AD8        | I/O              | I/O              |
| AD9        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AD10       | I/O              | I/O              |
| AD11       | I/O              | I/O              |
| AD12       | I/O              | I/O              |
| AD13       | I/O              | I/O              |
| AD14       | I/O              | I/O              |
| AD15       | I/O              | I/O              |
| AD16       | I/O              | I/O              |
| AD17       | I/O              | I/O              |
| AD18       | I/O              | I/O              |
| AD19       | I/O              | I/O              |
| AD20       | I/O              | I/O              |
| AD21       | I/O              | I/O              |
| AD22       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AD23       | TCK              | TCK              |
| AD24       | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AD25       | TRST             | TRST             |
| AD26       | V <sub>DDP</sub> | V <sub>DDP</sub> |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| AD27       | I/O              | I/O              |
| AD28       | I/O              | I/O              |
| AD29       | I/O              | I/O              |
| AD30       | GND              | GND              |
| AE1        | I/O              | I/O              |
| AE2        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AE3        | I/O              | I/O              |
| AE4        | I/O              | I/O              |
| AE5        | I/O              | I/O              |
| AE6        | GND              | GND              |
| AE7        | I/O              | I/O              |
| AE8        | I/O              | I/O              |
| AE9        | I/O              | I/O              |
| AE10       | I/O              | I/O              |
| AE11       | I/O              | I/O              |
| AE12       | I/O              | I/O              |
| AE13       | I/O              | I/O              |
| AE14       | I/O              | I/O              |
| AE15       | I/O              | I/O              |
| AE16       | I/O              | I/O              |
| AE17       | I/O              | I/O              |
| AE18       | I/O              | I/O              |
| AE19       | I/O              | I/O              |
| AE20       | I/O              | I/O              |
| AE21       | I/O              | I/O              |
| AE22       | I/O              | I/O              |
| AE23       | I/O              | I/O              |
| AE24       | I/O              | I/O              |
| AE25       | GND              | GND              |
| AE26       | I/O              | I/O              |
| AE27       | I/O              | I/O              |
| AE28       | I/O              | I/O              |
| AE29       | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AE30       | I/O              | I/O              |
| AF1        | GND              | GND              |
| AF2        | I/O              | I/O              |
| AF3        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AF4        | I/O              | I/O              |
| AF5        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AF6        | I/O              | I/O              |
| AF7        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AF8        | I/O              | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| AF9        | I/O              | I/O              |
| AF10       | I/O              | I/O              |
| AF11       | I/O              | I/O              |
| AF12       | I/O              | I/O              |
| AF13       | I/O              | I/O              |
| AF14       | I/O              | I/O              |
| AF15       | I/O              | I/O              |
| AF16       | I/O              | I/O              |
| AF17       | I/O              | I/O              |
| AF18       | I/O              | I/O              |
| AF19       | I/O              | I/O              |
| AF20       | I/O              | I/O              |
| AF21       | I/O              | I/O              |
| AF22       | I/O              | I/O              |
| AF23       | I/O              | I/O              |
| AF24       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AF25       | I/O              | I/O              |
| AF26       | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AF27       | TDO              | TDO              |
| AF28       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AF29       | V <sub>PN</sub>  | V <sub>PN</sub>  |
| AF30       | GND              | GND              |
| AG1        | I/O              | I/O              |
| AG2        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AG3        | I/O              | I/O              |
| AG4        | GND              | GND              |
| AG5        | I/O              | I/O              |
| AG6        | I/O              | I/O              |
| AG7        | I/O              | I/O              |
| AG8        | I/O              | I/O              |
| AG9        | I/O              | I/O              |
| AG10       | I/O              | I/O              |
| AG11       | I/O              | I/O              |
| AG12       | I/O              | I/O              |
| AG13       | I/O              | I/O              |
| AG14       | I/O              | I/O              |
| AG15       | I/O              | I/O              |
| AG16       | I/O              | I/O              |
| AG17       | I/O              | I/O              |
| AG18       | I/O              | I/O              |
| AG19       | I/O              | I/O              |
| AG20       | I/O              | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function  | APA1000 Function |
|------------|------------------|------------------|
| AG21       | I/O              | I/O              |
| AG22       | I/O              | I/O              |
| AG23       | I/O              | I/O              |
| AG24       | I/O              | I/O              |
| AG25       | I/O              | I/O              |
| AG26       | I/O              | I/O              |
| AG27       | GND              | GND              |
| AG28       | RCK              | RCK              |
| AG29       | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AG30       | I/O              | I/O              |
| AH1        | GND              | GND              |
| AH2        | I/O              | I/O              |
| AH3        | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AH4        | I/O              | I/O              |
| AH5        | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AH6        | I/O              | I/O              |
| AH7        | I/O              | I/O              |
| AH8        | I/O              | I/O              |
| AH9        | I/O              | I/O              |
| AH10       | I/O              | I/O              |
| AH11       | I/O              | I/O              |
| AH12       | I/O              | I/O              |
| AH13       | I/O              | I/O              |
| AH14       | I/O              | I/O              |
| AH15       | I/O              | I/O              |
| AH16       | I/O              | I/O              |
| AH17       | I/O              | I/O              |
| AH18       | I/O              | I/O              |
| AH19       | I/O              | I/O              |
| AH20       | I/O              | I/O              |
| AH21       | I/O              | I/O              |
| AH22       | I/O              | I/O              |
| AH23       | I/O              | I/O              |
| AH24       | I/O              | I/O              |
| AH25       | I/O              | I/O              |
| AH26       | V <sub>DDP</sub> | V <sub>DDP</sub> |
| AH27       | TDI              | TDI              |
| AH28       | V <sub>DD</sub>  | V <sub>DD</sub>  |
| AH29       | V <sub>PP</sub>  | V <sub>PP</sub>  |
| AH30       | GND              | GND              |
| AJ1        | GND              | GND              |
| AJ2        | GND              | GND              |



896 FBGA Pin (Continued)

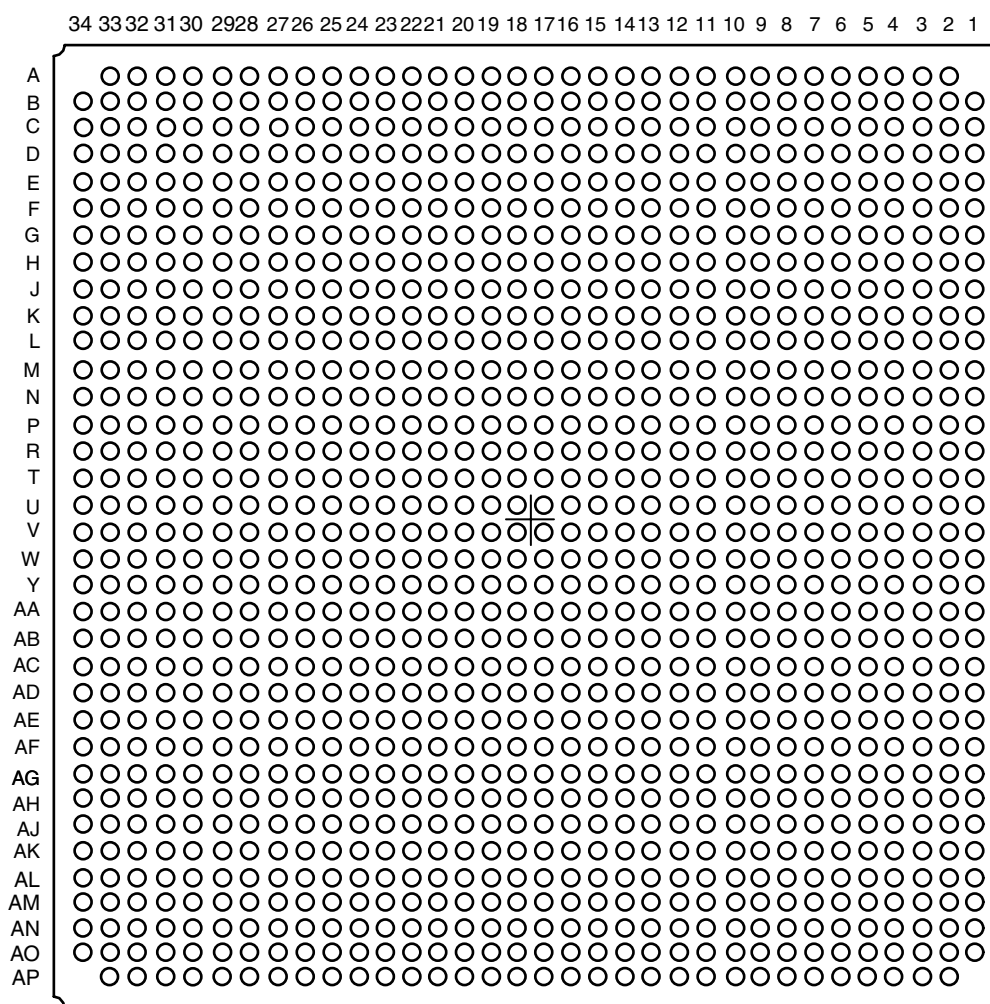
| Pin Number | APA750 Function | APA1000 Function |
|------------|-----------------|------------------|
| AJ3        | I/O             | I/O              |
| AJ4        | V <sub>DD</sub> | V <sub>DD</sub>  |
| AJ5        | I/O             | I/O              |
| AJ6        | V <sub>DD</sub> | V <sub>DD</sub>  |
| AJ7        | I/O             | I/O              |
| AJ8        | I/O             | I/O              |
| AJ9        | I/O             | I/O              |
| AJ10       | I/O             | I/O              |
| AJ11       | I/O             | I/O              |
| AJ12       | I/O             | I/O              |
| AJ13       | I/O             | I/O              |
| AJ14       | I/O             | I/O              |
| AJ15       | I/O             | I/O              |
| AJ16       | I/O             | I/O              |
| AJ17       | I/O             | I/O              |
| AJ18       | I/O             | I/O              |
| AJ19       | I/O             | I/O              |
| AJ20       | I/O             | I/O              |
| AJ21       | I/O             | I/O              |
| AJ22       | I/O             | I/O              |
| AJ23       | I/O             | I/O              |
| AJ24       | I/O             | I/O              |
| AJ25       | V <sub>DD</sub> | V <sub>DD</sub>  |
| AJ26       | I/O             | I/O              |
| AJ27       | V <sub>DD</sub> | V <sub>DD</sub>  |
| AJ28       | TMS             | TMS              |
| AJ29       | GND             | GND              |
| AJ30       | GND             | GND              |
| AK2        | GND             | GND              |
| AK3        | GND             | GND              |
| AK4        | I/O             | I/O              |
| AK5        | GND             | GND              |
| AK6        | I/O             | I/O              |
| AK7        | GND             | GND              |
| AK8        | I/O             | I/O              |
| AK9        | I/O             | I/O              |
| AK10       | I/O             | I/O              |
| AK11       | I/O             | I/O              |
| AK12       | I/O             | I/O              |
| AK13       | I/O             | I/O              |
| AK14       | I/O             | I/O              |
| AK15       | I/O             | I/O              |

896 FBGA Pin (Continued)

| Pin Number | APA750 Function | APA1000 Function |
|------------|-----------------|------------------|
| AK16       | I/O             | I/O              |
| AK17       | I/O             | I/O              |
| AK18       | I/O             | I/O              |
| AK19       | I/O             | I/O              |
| AK20       | I/O             | I/O              |
| AK21       | I/O             | I/O              |
| AK22       | I/O             | I/O              |
| AK23       | I/O             | I/O              |
| AK24       | GND             | GND              |
| AK25       | I/O             | I/O              |
| AK26       | GND             | GND              |
| AK27       | I/O             | I/O              |
| AK28       | GND             | GND              |
| AK29       | GND             | GND              |

## Package Pin Assignments (Continued)

### 1152-Pin FBGA (Bottom View)



1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| A2         | NC               |
| A3         | GND              |
| A4         | GND              |
| A5         | GND              |
| A6         | I/O              |
| A7         | V <sub>DD</sub>  |
| A8         | V <sub>DD</sub>  |
| A9         | V <sub>DD</sub>  |
| A10        | V <sub>DD</sub>  |
| A11        | I/O              |
| A12        | GND              |
| A13        | I/O              |
| A14        | V <sub>DDP</sub> |
| A15        | V <sub>DDP</sub> |
| A16        | I/O              |
| A17        | GND              |
| A18        | GND              |
| A19        | I/O              |
| A20        | V <sub>DDP</sub> |
| A21        | V <sub>DDP</sub> |
| A22        | I/O              |
| A23        | GND              |
| A24        | I/O              |
| A25        | V <sub>DD</sub>  |
| A26        | V <sub>DD</sub>  |
| A27        | V <sub>DD</sub>  |
| A28        | V <sub>DD</sub>  |
| A29        | I/O              |
| A30        | GND              |
| A31        | GND              |
| A32        | GND              |
| A33        | NC               |
| B1         | NC               |
| B2         | NC               |
| B3         | GND              |
| B4         | GND              |
| B5         | GND              |
| B6         | NC               |
| B7         | I/O              |
| B8         | NC               |
| B9         | I/O              |
| B10        | NC               |
| B11        | I/O              |
| B12        | GND              |
| B13        | I/O              |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| B14        | V <sub>DDP</sub> |
| B15        | V <sub>DDP</sub> |
| B16        | I/O              |
| B17        | GND              |
| B18        | GND              |
| B19        | I/O              |
| B20        | V <sub>DDP</sub> |
| B21        | V <sub>DDP</sub> |
| B22        | I/O              |
| B23        | GND              |
| B24        | I/O              |
| B25        | NC               |
| B26        | I/O              |
| B27        | NC               |
| B28        | I/O              |
| B29        | NC               |
| B30        | GND              |
| B31        | GND              |
| B32        | GND              |
| B33        | NC               |
| B34        | NC               |
| C1         | GND              |
| C2         | GND              |
| C3         | NC               |
| C4         | GND              |
| C5         | GND              |
| C6         | I/O              |
| C7         | GND              |
| C8         | I/O              |
| C9         | GND              |
| C10        | I/O              |
| C11        | I/O              |
| C12        | I/O              |
| C13        | I/O              |
| C14        | I/O              |
| C15        | I/O              |
| C16        | I/O              |
| C17        | I/O              |
| C18        | I/O              |
| C19        | I/O              |
| C20        | I/O              |
| C21        | I/O              |
| C22        | I/O              |
| C23        | I/O              |
| C24        | I/O              |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| C25        | I/O              |
| C26        | GND              |
| C27        | I/O              |
| C28        | GND              |
| C29        | I/O              |
| C30        | GND              |
| C31        | GND              |
| C32        | NC               |
| C33        | GND              |
| C34        | GND              |
| D1         | GND              |
| D2         | GND              |
| D3         | GND              |
| D4         | GND              |
| D5         | I/O              |
| D6         | V <sub>DD</sub>  |
| D7         | I/O              |
| D8         | V <sub>DD</sub>  |
| D9         | I/O              |
| D10        | I/O              |
| D11        | I/O              |
| D12        | I/O              |
| D13        | I/O              |
| D14        | I/O              |
| D15        | I/O              |
| D16        | I/O              |
| D17        | I/O              |
| D18        | I/O              |
| D19        | I/O              |
| D20        | I/O              |
| D21        | I/O              |
| D22        | I/O              |
| D23        | I/O              |
| D24        | I/O              |
| D25        | I/O              |
| D26        | I/O              |
| D27        | V <sub>DD</sub>  |
| D28        | I/O              |
| D29        | V <sub>DD</sub>  |
| D30        | I/O              |
| D31        | GND              |
| D32        | GND              |
| D33        | GND              |
| D34        | GND              |
| E1         | GND              |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| E2         | GND              |
| E3         | GND              |
| E4         | I/O              |
| E5         | V <sub>DD</sub>  |
| E6         | I/O              |
| E7         | V <sub>DDP</sub> |
| E8         | I/O              |
| E9         | I/O              |
| E10        | I/O              |
| E11        | I/O              |
| E12        | I/O              |
| E13        | I/O              |
| E14        | I/O              |
| E15        | I/O              |
| E16        | I/O              |
| E17        | I/O              |
| E18        | I/O              |
| E19        | I/O              |
| E20        | I/O              |
| E21        | I/O              |
| E22        | I/O              |
| E23        | I/O              |
| E24        | I/O              |
| E25        | I/O              |
| E26        | I/O              |
| E27        | I/O              |
| E28        | V <sub>DDP</sub> |
| E29        | I/O              |
| E30        | V <sub>DD</sub>  |
| E31        | I/O              |
| E32        | GND              |
| E33        | GND              |
| E34        | GND              |
| F1         | I/O              |
| F2         | NC               |
| F3         | I/O              |
| F4         | V <sub>DD</sub>  |
| F5         | I/O              |
| F6         | GND              |
| F7         | I/O              |
| F8         | I/O              |
| F9         | I/O              |
| F10        | I/O              |
| F11        | I/O              |
| F12        | I/O              |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| F13        | I/O              |
| F14        | I/O              |
| F15        | I/O              |
| F16        | I/O              |
| F17        | I/O              |
| F18        | I/O              |
| F19        | I/O              |
| F20        | I/O              |
| F21        | I/O              |
| F22        | I/O              |
| F23        | I/O              |
| F24        | I/O              |
| F25        | I/O              |
| F26        | I/O              |
| F27        | I/O              |
| F28        | I/O              |
| F29        | GND              |
| F30        | I/O              |
| F31        | V <sub>DD</sub>  |
| F32        | I/O              |
| F33        | NC               |
| F34        | NC               |
| G1         | V <sub>DD</sub>  |
| G2         | I/O              |
| G3         | GND              |
| G4         | I/O              |
| G5         | V <sub>DDP</sub> |
| G6         | I/O              |
| G7         | V <sub>DD</sub>  |
| G8         | I/O              |
| G9         | V <sub>DDP</sub> |
| G10        | I/O              |
| G11        | I/O              |
| G12        | I/O              |
| G13        | I/O              |
| G14        | I/O              |
| G15        | I/O              |
| G16        | I/O              |
| G17        | I/O              |
| G18        | I/O              |
| G19        | I/O              |
| G20        | I/O              |
| G21        | I/O              |
| G22        | I/O              |
| G23        | I/O              |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| G24        | I/O              |
| G25        | I/O              |
| G26        | V <sub>DDP</sub> |
| G27        | I/O              |
| G28        | V <sub>DD</sub>  |
| G29        | I/O              |
| G30        | V <sub>DDP</sub> |
| G31        | I/O              |
| G32        | GND              |
| G33        | I/O              |
| G34        | V <sub>DD</sub>  |
| H1         | V <sub>DD</sub>  |
| H2         | NC               |
| H3         | I/O              |
| H4         | V <sub>DD</sub>  |
| H5         | I/O              |
| H6         | I/O              |
| H7         | I/O              |
| H8         | GND              |
| H9         | I/O              |
| H10        | I/O              |
| H11        | I/O              |
| H12        | I/O              |
| H13        | I/O              |
| H14        | I/O              |
| H15        | I/O              |
| H16        | I/O              |
| H17        | I/O              |
| H18        | I/O              |
| H19        | I/O              |
| H20        | I/O              |
| H21        | I/O              |
| H22        | I/O              |
| H23        | I/O              |
| H24        | I/O              |
| H25        | I/O              |
| H26        | I/O              |
| H27        | GND              |
| H28        | I/O              |
| H29        | I/O              |
| H30        | I/O              |
| H31        | V <sub>DD</sub>  |
| H32        | I/O              |
| H33        | NC               |
| H34        | V <sub>DD</sub>  |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| J1         | V <sub>DD</sub>  |
| J2         | I/O              |
| J3         | GND              |
| J4         | I/O              |
| J5         | I/O              |
| J6         | I/O              |
| J7         | V <sub>DDP</sub> |
| J8         | I/O              |
| J9         | V <sub>DD</sub>  |
| J10        | I/O              |
| J11        | V <sub>DDP</sub> |
| J12        | I/O              |
| J13        | I/O              |
| J14        | I/O              |
| J15        | I/O              |
| J16        | I/O              |
| J17        | I/O              |
| J18        | I/O              |
| J19        | I/O              |
| J20        | I/O              |
| J21        | I/O              |
| J22        | I/O              |
| J23        | I/O              |
| J24        | V <sub>DDP</sub> |
| J25        | I/O              |
| J26        | V <sub>DD</sub>  |
| J27        | I/O              |
| J28        | V <sub>DDP</sub> |
| J29        | I/O              |
| J30        | I/O              |
| J31        | I/O              |
| J32        | GND              |
| J33        | I/O              |
| J34        | V <sub>DD</sub>  |
| K1         | V <sub>DD</sub>  |
| K2         | NC               |
| K3         | I/O              |
| K4         | I/O              |
| K5         | I/O              |
| K6         | I/O              |
| K7         | I/O              |
| K8         | I/O              |
| K9         | I/O              |
| K10        | GND              |
| K11        | I/O              |

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| Pin Number | APA1000 Function |
|------------|------------------|
| K12        | I/O              |
| K13        | I/O              |
| K14        | I/O              |
| K15        | I/O              |
| K16        | I/O              |
| K17        | I/O              |
| K18        | I/O              |
| K19        | I/O              |
| K20        | I/O              |
| K21        | I/O              |
| K22        | I/O              |
| K23        | I/O              |
| K24        | I/O              |
| K25        | GND              |
| K26        | I/O              |
| K27        | I/O              |
| K28        | I/O              |
| K29        | I/O              |
| K30        | I/O              |
| K31        | I/O              |
| K32        | I/O              |
| K33        | NC               |
| K34        | V <sub>DD</sub>  |
| L1         | I/O              |
| L2         | I/O              |
| L3         | I/O              |
| L4         | I/O              |
| L5         | I/O              |
| L6         | I/O              |
| L7         | I/O              |
| L8         | I/O              |
| L9         | V <sub>DDP</sub> |
| L10        | I/O              |
| L11        | V <sub>DD</sub>  |
| L12        | I/O              |
| L13        | I/O              |
| L14        | I/O              |
| L15        | I/O              |
| L16        | I/O              |
| L17        | I/O              |
| L18        | I/O              |
| L19        | I/O              |
| L20        | I/O              |
| L21        | I/O              |
| L22        | I/O              |

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| Pin Number | APA1000 Function |
|------------|------------------|
| L23        | I/O              |
| L24        | V <sub>DD</sub>  |
| L25        | I/O              |
| L26        | V <sub>DDP</sub> |
| L27        | I/O              |
| L28        | I/O              |
| L29        | I/O              |
| L30        | I/O              |
| L31        | I/O              |
| L32        | I/O              |
| L33        | I/O              |
| L34        | I/O              |
| M1         | GND              |
| M2         | GND              |
| M3         | I/O              |
| M4         | I/O              |
| M5         | I/O              |
| M6         | I/O              |
| M7         | I/O              |
| M8         | I/O              |
| M9         | I/O              |
| M10        | I/O              |
| M11        | I/O              |
| M12        | V <sub>DD</sub>  |
| M13        | I/O              |
| M14        | V <sub>DDP</sub> |
| M15        | V <sub>DDP</sub> |
| M16        | V <sub>DDP</sub> |
| M17        | V <sub>DDP</sub> |
| M18        | V <sub>DDP</sub> |
| M19        | V <sub>DDP</sub> |
| M20        | V <sub>DDP</sub> |
| M21        | V <sub>DDP</sub> |
| M22        | I/O              |
| M23        | V <sub>DD</sub>  |
| M24        | I/O              |
| M25        | I/O              |
| M26        | I/O              |
| M27        | I/O              |
| M28        | I/O              |
| M29        | I/O              |
| M30        | I/O              |
| M31        | I/O              |
| M32        | I/O              |
| M33        | GND              |

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| Pin Number | APA1000 Function |
|------------|------------------|
| M34        | GND              |
| N1         | I/O              |
| N2         | I/O              |
| N3         | I/O              |
| N4         | I/O              |
| N5         | I/O              |
| N6         | I/O              |
| N7         | I/O              |
| N8         | I/O              |
| N9         | I/O              |
| N10        | I/O              |
| N11        | I/O              |
| N12        | I/O              |
| N13        | V <sub>DD</sub>  |
| N14        | V <sub>DD</sub>  |
| N15        | V <sub>DD</sub>  |
| N16        | V <sub>DD</sub>  |
| N17        | V <sub>DD</sub>  |
| N18        | V <sub>DD</sub>  |
| N19        | V <sub>DD</sub>  |
| N20        | V <sub>DD</sub>  |
| N21        | V <sub>DD</sub>  |
| N22        | V <sub>DD</sub>  |
| N23        | I/O              |
| N24        | I/O              |
| N25        | I/O              |
| N26        | I/O              |
| N27        | I/O              |
| N28        | I/O              |
| N29        | I/O              |
| N30        | I/O              |
| N31        | I/O              |
| N32        | I/O              |
| N33        | I/O              |
| N34        | I/O              |
| P1         | V <sub>DDP</sub> |
| P2         | V <sub>DDP</sub> |
| P3         | I/O              |
| P4         | I/O              |
| P5         | I/O              |
| P6         | I/O              |
| P7         | I/O              |
| P8         | I/O              |
| P9         | I/O              |
| P10        | I/O              |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| P11        | I/O              |
| P12        | V <sub>DDP</sub> |
| P13        | V <sub>DD</sub>  |
| P14        | GND              |
| P15        | GND              |
| P16        | GND              |
| P17        | GND              |
| P18        | GND              |
| P19        | GND              |
| P20        | GND              |
| P21        | GND              |
| P22        | V <sub>DD</sub>  |
| P23        | V <sub>DDP</sub> |
| P24        | I/O              |
| P25        | I/O              |
| P26        | I/O              |
| P27        | I/O              |
| P28        | I/O              |
| P29        | I/O              |
| P30        | I/O              |
| P31        | I/O              |
| P32        | I/O              |
| P33        | V <sub>DDP</sub> |
| P34        | V <sub>DDP</sub> |
| R1         | V <sub>DDP</sub> |
| R2         | V <sub>DDP</sub> |
| R3         | I/O              |
| R4         | I/O              |
| R5         | I/O              |
| R6         | I/O              |
| R7         | I/O              |
| R8         | I/O              |
| R9         | I/O              |
| R10        | I/O              |
| R11        | I/O              |
| R12        | V <sub>DDP</sub> |
| R13        | V <sub>DD</sub>  |
| R14        | GND              |
| R15        | GND              |
| R16        | GND              |
| R17        | GND              |
| R18        | GND              |
| R19        | GND              |
| R20        | GND              |
| R21        | GND              |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| R22        | V <sub>DD</sub>  |
| R23        | V <sub>DDP</sub> |
| R24        | I/O              |
| R25        | I/O              |
| R26        | I/O              |
| R27        | I/O              |
| R28        | I/O              |
| R29        | I/O              |
| R30        | I/O              |
| R31        | I/O              |
| R32        | I/O              |
| R33        | V <sub>DDP</sub> |
| R34        | V <sub>DDP</sub> |
| T1         | I/O              |
| T2         | I/O              |
| T3         | I/O              |
| T4         | I/O              |
| T5         | I/O              |
| T6         | I/O              |
| T7         | I/O              |
| T8         | I/O              |
| T9         | I/O              |
| T10        | I/O              |
| T11        | I/O              |
| T12        | V <sub>DDP</sub> |
| T13        | V <sub>DD</sub>  |
| T14        | GND              |
| T15        | GND              |
| T16        | GND              |
| T17        | GND              |
| T18        | GND              |
| T19        | GND              |
| T20        | GND              |
| T21        | GND              |
| T22        | V <sub>DD</sub>  |
| T23        | V <sub>DDP</sub> |
| T24        | I/O              |
| T25        | I/O              |
| T26        | I/O              |
| T27        | I/O              |
| T28        | I/O              |
| T29        | I/O              |
| T30        | I/O              |
| T31        | I/O              |
| T32        | I/O              |

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| Pin Number | APA1000 Function |
|------------|------------------|
| T33        | I/O              |
| T34        | I/O              |
| U1         | GND              |
| U2         | GND              |
| U3         | I/O              |
| U4         | I/O              |
| U5         | AGND             |
| U6         | NPECL            |
| U7         | GL               |
| U8         | I/O              |
| U9         | I/O              |
| U10        | I/O              |
| U11        | I/O              |
| U12        | V <sub>DDP</sub> |
| U13        | V <sub>DD</sub>  |
| U14        | GND              |
| U15        | GND              |
| U16        | GND              |
| U17        | GND              |
| U18        | GND              |
| U19        | GND              |
| U20        | GND              |
| U21        | GND              |
| U22        | V <sub>DD</sub>  |
| U23        | V <sub>DDP</sub> |
| U24        | I/O              |
| U25        | I/O              |
| U26        | I/O              |
| U27        | I/O              |
| U28        | I/O              |
| U29        | NPECL            |
| U30        | AGND             |
| U31        | I/O              |
| U32        | I/O              |
| U33        | GND              |
| U34        | GND              |
| V1         | GND              |
| V2         | GND              |
| V3         | I/O              |
| V4         | AVDD             |
| V5         | GL               |
| V6         | PPECL (I/P)      |
| V7         | I/O              |
| V8         | I/O              |
| V9         | I/O              |

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| Pin Number | APA1000 Function |
|------------|------------------|
| V10        | I/O              |
| V11        | I/O              |
| V12        | V <sub>DDP</sub> |
| V13        | V <sub>DD</sub>  |
| V14        | GND              |
| V15        | GND              |
| V16        | GND              |
| V17        | GND              |
| V18        | GND              |
| V19        | GND              |
| V20        | GND              |
| V21        | GND              |
| V22        | V <sub>DD</sub>  |
| V23        | V <sub>DDP</sub> |
| V24        | I/O              |
| V25        | I/O              |
| V26        | I/O              |
| V27        | I/O              |
| V28        | PPECL (I/P)      |
| V29        | GL               |
| V30        | GL               |
| V31        | AVDD             |
| V32        | I/O              |
| V33        | GND              |
| V34        | GND              |
| W1         | I/O              |
| W2         | I/O              |
| W3         | I/O              |
| W4         | I/O              |
| W5         | I/O              |
| W6         | I/O              |
| W7         | I/O              |
| W8         | I/O              |
| W9         | I/O              |
| W10        | I/O              |
| W11        | I/O              |
| W12        | V <sub>DDP</sub> |
| W13        | V <sub>DD</sub>  |
| W14        | GND              |
| W15        | GND              |
| W16        | GND              |
| W17        | GND              |
| W18        | GND              |
| W19        | GND              |
| W20        | GND              |

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| Pin Number | APA1000 Function |
|------------|------------------|
| W21        | GND              |
| W22        | V <sub>DD</sub>  |
| W23        | V <sub>DDP</sub> |
| W24        | I/O              |
| W25        | I/O              |
| W26        | I/O              |
| W27        | I/O              |
| W28        | I/O              |
| W29        | I/O              |
| W30        | I/O              |
| W31        | I/O              |
| W32        | I/O              |
| W33        | I/O              |
| W34        | I/O              |
| Y1         | V <sub>DDP</sub> |
| Y2         | V <sub>DDP</sub> |
| Y3         | I/O              |
| Y4         | I/O              |
| Y5         | I/O              |
| Y6         | I/O              |
| Y7         | I/O              |
| Y8         | I/O              |
| Y9         | I/O              |
| Y10        | I/O              |
| Y11        | I/O              |
| Y12        | V <sub>DDP</sub> |
| Y13        | V <sub>DD</sub>  |
| Y14        | GND              |
| Y15        | GND              |
| Y16        | GND              |
| Y17        | GND              |
| Y18        | GND              |
| Y19        | GND              |
| Y20        | GND              |
| Y21        | GND              |
| Y22        | V <sub>DD</sub>  |
| Y23        | V <sub>DDP</sub> |
| Y24        | I/O              |
| Y25        | I/O              |
| Y26        | I/O              |
| Y27        | I/O              |
| Y28        | I/O              |
| Y29        | I/O              |
| Y30        | I/O              |
| Y31        | I/O              |

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| Pin Number | APA1000 Function |
|------------|------------------|
| Y32        | I/O              |
| Y33        | V <sub>DDP</sub> |
| Y34        | V <sub>DDP</sub> |
| AA1        | V <sub>DDP</sub> |
| AA2        | V <sub>DDP</sub> |
| AA3        | I/O              |
| AA4        | I/O              |
| AA5        | I/O              |
| AA6        | I/O              |
| AA7        | I/O              |
| AA8        | I/O              |
| AA9        | I/O              |
| AA10       | I/O              |
| AA11       | I/O              |
| AA12       | V <sub>DDP</sub> |
| AA13       | V <sub>DD</sub>  |
| AA14       | GND              |
| AA15       | GND              |
| AA16       | GND              |
| AA17       | GND              |
| AA18       | GND              |
| AA19       | GND              |
| AA20       | GND              |
| AA21       | GND              |
| AA22       | V <sub>DD</sub>  |
| AA23       | V <sub>DDP</sub> |
| AA24       | I/O              |
| AA25       | I/O              |
| AA26       | I/O              |
| AA27       | I/O              |
| AA28       | I/O              |
| AA29       | I/O              |
| AA30       | I/O              |
| AA31       | I/O              |
| AA32       | I/O              |
| AA33       | V <sub>DDP</sub> |
| AA34       | V <sub>DDP</sub> |
| AB1        | I/O              |
| AB2        | I/O              |
| AB3        | I/O              |
| AB4        | I/O              |
| AB5        | I/O              |
| AB6        | I/O              |
| AB7        | I/O              |
| AB8        | I/O              |

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| Pin Number | APA1000 Function |
|------------|------------------|
| AB9        | I/O              |
| AB10       | I/O              |
| AB11       | I/O              |
| AB12       | I/O              |
| AB13       | V <sub>DD</sub>  |
| AB14       | V <sub>DD</sub>  |
| AB15       | V <sub>DD</sub>  |
| AB16       | V <sub>DD</sub>  |
| AB17       | V <sub>DD</sub>  |
| AB18       | V <sub>DD</sub>  |
| AB19       | V <sub>DD</sub>  |
| AB20       | V <sub>DD</sub>  |
| AB21       | V <sub>DD</sub>  |
| AB22       | V <sub>DD</sub>  |
| AB23       | I/O              |
| AB24       | I/O              |
| AB25       | I/O              |
| AB26       | I/O              |
| AB27       | I/O              |
| AB28       | I/O              |
| AB29       | I/O              |
| AB30       | I/O              |
| AB31       | I/O              |
| AB32       | I/O              |
| AB33       | I/O              |
| AB34       | I/O              |
| AC1        | GND              |
| AC2        | GND              |
| AC3        | I/O              |
| AC4        | I/O              |
| AC5        | I/O              |
| AC6        | I/O              |
| AC7        | I/O              |
| AC8        | I/O              |
| AC9        | I/O              |
| AC10       | I/O              |
| AC11       | I/O              |
| AC12       | V <sub>DD</sub>  |
| AC13       | I/O              |
| AC14       | V <sub>DDP</sub> |
| AC15       | V <sub>DDP</sub> |
| AC16       | V <sub>DDP</sub> |
| AC17       | V <sub>DDP</sub> |
| AC18       | V <sub>DDP</sub> |
| AC19       | V <sub>DDP</sub> |

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| Pin Number | APA1000 Function |
|------------|------------------|
| AC20       | V <sub>DDP</sub> |
| AC21       | V <sub>DDP</sub> |
| AC22       | I/O              |
| AC23       | V <sub>DD</sub>  |
| AC24       | I/O              |
| AC25       | I/O              |
| AC26       | I/O              |
| AC27       | I/O              |
| AC28       | I/O              |
| AC29       | I/O              |
| AC30       | I/O              |
| AC31       | I/O              |
| AC32       | I/O              |
| AC33       | GND              |
| AC34       | GND              |
| AD1        | I/O              |
| AD2        | I/O              |
| AD3        | I/O              |
| AD4        | I/O              |
| AD5        | I/O              |
| AD6        | I/O              |
| AD7        | I/O              |
| AD8        | I/O              |
| AD9        | V <sub>DDP</sub> |
| AD10       | I/O              |
| AD11       | V <sub>DD</sub>  |
| AD12       | I/O              |
| AD13       | I/O              |
| AD14       | I/O              |
| AD15       | I/O              |
| AD16       | I/O              |
| AD17       | I/O              |
| AD18       | I/O              |
| AD19       | I/O              |
| AD20       | I/O              |
| AD21       | I/O              |
| AD22       | I/O              |
| AD23       | I/O              |
| AD24       | V <sub>DD</sub>  |
| AD25       | I/O              |
| AD26       | V <sub>DDP</sub> |
| AD27       | I/O              |
| AD28       | I/O              |
| AD29       | I/O              |
| AD30       | I/O              |

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| Pin Number | APA1000 Function |
|------------|------------------|
| AD31       | I/O              |
| AD32       | I/O              |
| AD33       | I/O              |
| AD34       | I/O              |
| AE1        | V <sub>DD</sub>  |
| AE2        | NC               |
| AE3        | I/O              |
| AE4        | I/O              |
| AE5        | I/O              |
| AE6        | I/O              |
| AE7        | I/O              |
| AE8        | I/O              |
| AE9        | I/O              |
| AE10       | GND              |
| AE11       | I/O              |
| AE12       | I/O              |
| AE13       | I/O              |
| AE14       | I/O              |
| AE15       | I/O              |
| AE16       | I/O              |
| AE17       | I/O              |
| AE18       | I/O              |
| AE19       | I/O              |
| AE20       | I/O              |
| AE21       | I/O              |
| AE22       | I/O              |
| AE23       | I/O              |
| AE24       | I/O              |
| AE25       | GND              |
| AE26       | I/O              |
| AE27       | I/O              |
| AE28       | I/O              |
| AE29       | I/O              |
| AE30       | I/O              |
| AE31       | I/O              |
| AE32       | I/O              |
| AE33       | NC               |
| AE34       | V <sub>DD</sub>  |
| AF1        | V <sub>DD</sub>  |
| AF2        | I/O              |
| AF3        | GND              |
| AF4        | I/O              |
| AF5        | I/O              |
| AF6        | I/O              |
| AF7        | V <sub>DDP</sub> |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| AF8        | I/O              |
| AF9        | V <sub>DD</sub>  |
| AF10       | I/O              |
| AF11       | V <sub>DDP</sub> |
| AF12       | I/O              |
| AF13       | I/O              |
| AF14       | I/O              |
| AF15       | I/O              |
| AF16       | I/O              |
| AF17       | I/O              |
| AF18       | I/O              |
| AF19       | I/O              |
| AF20       | I/O              |
| AF21       | I/O              |
| AF22       | I/O              |
| AF23       | I/O              |
| AF24       | V <sub>DDP</sub> |
| AF25       | TCK              |
| AF26       | V <sub>DD</sub>  |
| AF27       | TRST             |
| AF28       | V <sub>DDP</sub> |
| AF29       | I/O              |
| AF30       | I/O              |
| AF31       | I/O              |
| AF32       | GND              |
| AF33       | I/O              |
| AF34       | V <sub>DD</sub>  |
| AG1        | V <sub>DD</sub>  |
| AG2        | NC               |
| AG3        | I/O              |
| AG4        | V <sub>DD</sub>  |
| AG5        | I/O              |
| AG6        | I/O              |
| AG7        | I/O              |
| AG8        | GND              |
| AG9        | I/O              |
| AG10       | I/O              |
| AG11       | I/O              |
| AG12       | I/O              |
| AG13       | I/O              |
| AG14       | I/O              |
| AG15       | I/O              |
| AG16       | I/O              |
| AG17       | I/O              |
| AG18       | I/O              |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| AG19       | I/O              |
| AG20       | I/O              |
| AG21       | I/O              |
| AG22       | I/O              |
| AG23       | I/O              |
| AG24       | I/O              |
| AG25       | I/O              |
| AG26       | I/O              |
| AG27       | GND              |
| AG28       | I/O              |
| AG29       | I/O              |
| AG30       | I/O              |
| AG31       | V <sub>DD</sub>  |
| AG32       | I/O              |
| AG33       | NC               |
| AG34       | V <sub>DD</sub>  |
| AH1        | V <sub>DD</sub>  |
| AH2        | I/O              |
| AH3        | GND              |
| AH4        | I/O              |
| AH5        | V <sub>DDP</sub> |
| AH6        | I/O              |
| AH7        | V <sub>DD</sub>  |
| AH8        | I/O              |
| AH9        | V <sub>DDP</sub> |
| AH10       | I/O              |
| AH11       | I/O              |
| AH12       | I/O              |
| AH13       | I/O              |
| AH14       | I/O              |
| AH15       | I/O              |
| AH16       | I/O              |
| AH17       | I/O              |
| AH18       | I/O              |
| AH19       | I/O              |
| AH20       | I/O              |
| AH21       | I/O              |
| AH22       | I/O              |
| AH23       | I/O              |
| AH24       | I/O              |
| AH25       | I/O              |
| AH26       | V <sub>DDP</sub> |
| AH27       | I/O              |
| AH28       | V <sub>DD</sub>  |
| AH29       | TDO              |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| AH30       | V <sub>DDP</sub> |
| AH31       | V <sub>PN</sub>  |
| AH32       | GND              |
| AH33       | I/O              |
| AH34       | V <sub>DD</sub>  |
| AJ1        | I/O              |
| AJ2        | NC               |
| AJ3        | I/O              |
| AJ4        | V <sub>DD</sub>  |
| AJ5        | I/O              |
| AJ6        | GND              |
| AJ7        | I/O              |
| AJ8        | I/O              |
| AJ9        | I/O              |
| AJ10       | I/O              |
| AJ11       | I/O              |
| AJ12       | I/O              |
| AJ13       | I/O              |
| AJ14       | I/O              |
| AJ15       | I/O              |
| AJ16       | I/O              |
| AJ17       | I/O              |
| AJ18       | I/O              |
| AJ19       | I/O              |
| AJ20       | I/O              |
| AJ21       | I/O              |
| AJ22       | I/O              |
| AJ23       | I/O              |
| AJ24       | I/O              |
| AJ25       | I/O              |
| AJ26       | I/O              |
| AJ27       | I/O              |
| AJ28       | I/O              |
| AJ29       | GND              |
| AJ30       | RCK              |
| AJ31       | V <sub>DD</sub>  |
| AJ32       | I/O              |
| AJ33       | NC               |
| AJ34       | NC               |
| AK1        | GND              |
| AK2        | GND              |
| AK3        | GND              |
| AK4        | I/O              |
| AK5        | V <sub>DD</sub>  |
| AK6        | I/O              |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| AK7        | V <sub>DDP</sub> |
| AK8        | I/O              |
| AK9        | I/O              |
| AK10       | I/O              |
| AK11       | I/O              |
| AK12       | I/O              |
| AK13       | I/O              |
| AK14       | I/O              |
| AK15       | I/O              |
| AK16       | I/O              |
| AK17       | I/O              |
| AK18       | I/O              |
| AK19       | I/O              |
| AK20       | I/O              |
| AK21       | I/O              |
| AK22       | I/O              |
| AK23       | I/O              |
| AK24       | I/O              |
| AK25       | I/O              |
| AK26       | I/O              |
| AK27       | I/O              |
| AK28       | V <sub>DDP</sub> |
| AK29       | TDI              |
| AK30       | V <sub>DD</sub>  |
| AK31       | V <sub>PN</sub>  |
| AK32       | GND              |
| AK33       | GND              |
| AK34       | GND              |
| AL1        | GND              |
| AL2        | GND              |
| AL3        | GND              |
| AL4        | GND              |
| AL5        | I/O              |
| AL6        | V <sub>DD</sub>  |
| AL7        | I/O              |
| AL8        | V <sub>DD</sub>  |
| AL9        | I/O              |
| AL10       | I/O              |
| AL11       | I/O              |
| AL12       | I/O              |
| AL13       | I/O              |
| AL14       | I/O              |
| AL15       | I/O              |
| AL16       | I/O              |
| AL17       | I/O              |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| AL18       | I/O              |
| AL19       | I/O              |
| AL20       | I/O              |
| AL21       | I/O              |
| AL22       | I/O              |
| AL23       | I/O              |
| AL24       | I/O              |
| AL25       | I/O              |
| AL26       | I/O              |
| AL27       | V <sub>DD</sub>  |
| AL28       | I/O              |
| AL29       | V <sub>DD</sub>  |
| AL30       | TMS              |
| AL31       | GND              |
| AL32       | GND              |
| AL33       | GND              |
| AL34       | GND              |
| AM1        | GND              |
| AM2        | GND              |
| AM3        | NC               |
| AM4        | GND              |
| AM5        | GND              |
| AM6        | I/O              |
| AM7        | GND              |
| AM8        | I/O              |
| AM9        | GND              |
| AM10       | I/O              |
| AM11       | I/O              |
| AM12       | I/O              |
| AM13       | I/O              |
| AM14       | I/O              |
| AM15       | I/O              |
| AM16       | I/O              |
| AM17       | I/O              |
| AM18       | I/O              |
| AM19       | I/O              |
| AM20       | I/O              |
| AM21       | I/O              |
| AM22       | I/O              |
| AM23       | I/O              |
| AM24       | I/O              |
| AM25       | I/O              |
| AM26       | GND              |
| AM27       | I/O              |
| AM28       | GND              |



1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| AM29       | I/O              |
| AM30       | GND              |
| AM31       | GND              |
| AM32       | NC               |
| AM33       | GND              |
| AM34       | GND              |
| AN1        | NC               |
| AN2        | NC               |
| AN3        | GND              |
| AN4        | GND              |
| AN5        | GND              |
| AN6        | NC               |
| AN7        | I/O              |
| AN8        | NC               |
| AN9        | I/O              |
| AN10       | NC               |
| AN11       | I/O              |
| AN12       | GND              |
| AN13       | I/O              |
| AN14       | V <sub>DDP</sub> |
| AN15       | V <sub>DDP</sub> |
| AN16       | I/O              |
| AN17       | GND              |
| AN18       | GND              |
| AN19       | I/O              |
| AN20       | V <sub>DDP</sub> |
| AN21       | V <sub>DDP</sub> |
| AN22       | I/O              |
| AN23       | GND              |
| AN24       | I/O              |
| AN25       | NC               |
| AN26       | I/O              |
| AN27       | NC               |
| AN28       | I/O              |
| AN29       | NC               |
| AN30       | GND              |
| AN31       | GND              |
| AN32       | GND              |
| AN33       | NC               |
| AN34       | NC               |
| AP2        | NC               |
| AP3        | GND              |
| AP4        | GND              |
| AP5        | GND              |
| AP6        | I/O              |

1152 FBGA Pin

| Pin Number | APA1000 Function |
|------------|------------------|
| AP7        | V <sub>DD</sub>  |
| AP8        | V <sub>DD</sub>  |
| AP9        | V <sub>DD</sub>  |
| AP10       | V <sub>DD</sub>  |
| AP11       | I/O              |
| AP12       | GND              |
| AP13       | I/O              |
| AP14       | V <sub>DDP</sub> |
| AP15       | V <sub>DDP</sub> |
| AP16       | I/O              |
| AP17       | GND              |
| AP18       | GND              |
| AP19       | I/O              |
| AP20       | V <sub>DDP</sub> |
| AP21       | V <sub>DDP</sub> |
| AP22       | I/O              |
| AP23       | GND              |
| AP24       | I/O              |
| AP25       | V <sub>DD</sub>  |
| AP26       | V <sub>DD</sub>  |
| AP27       | V <sub>DD</sub>  |
| AP28       | V <sub>DD</sub>  |
| AP29       | I/O              |
| AP30       | GND              |
| AP31       | GND              |
| AP32       | GND              |
| AP33       | NC               |

## List of Changes

The following table lists critical changes that were made in the current version of the document.

| Previous version | Changes in current version (Advanced v2.0)                                                                                                                                    | Page               |
|------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| Advanced v0.7    | The "Product Availability" table on page 4 was updated.                                                                                                                       | page 4             |
|                  | The "Array Coordinates" section on page 10 and Table 2 are new.                                                                                                               | page 10            |
|                  | The "Power-up Sequencing" section on page 11 is new.                                                                                                                          | page 11            |
|                  | Table 4 on page 12 was updated.                                                                                                                                               | page 12            |
|                  | The "Timing Control and Characteristics" section on page 15 was updated. Physical Implementation, Functional Description, Lock Signal, and PLL Configuration Options are new. | page 15 to page 16 |
|                  | Figure 12 on page 16 was updated.                                                                                                                                             | page 16            |
|                  | Figure 13 on page 17 was updated.                                                                                                                                             | page 17            |
|                  | Sample Implementations, Adjustable Clock Delay, and the "Clock Skew Minimization" section on page 17 are new.                                                                 | page 17            |
|                  | Figure 14, Figure 15, Figure 16, Figure 17, and Figure 18 are new.                                                                                                            | page 18 to page 20 |
|                  | The "PLL Electrical Specifications" table on page 21 is new.                                                                                                                  | page 21            |
|                  | The "Design Environment" section on page 26 was updated.                                                                                                                      | page 26            |
|                  | Figure 24 on page 27 was updated.                                                                                                                                             | page 27            |
|                  | The "Calculating Power Dissipation" section on page 29 was updated.                                                                                                           | page 29            |
|                  | The "DC Electrical Specifications (VDDP = 2.5V ±0.2V) <sup>1</sup> " table on page 32 was updated.                                                                            | page 32            |
|                  | The "DC Electrical Specifications (VDDP = 3.3V ±0.3V and VDD 2.5V ±0.2V) <sup>1</sup> " table on page 33 was updated.                                                         | page 33            |
|                  | The "DC Specifications (3.3V PCI Operation) <sup>1</sup> " table on page 34 was updated.                                                                                      | page 34            |
|                  | The "Tristate Buffer Delays" section on page 36 (the figure and table) have been updated.                                                                                     | page 36            |
|                  | The "Output Buffer Delays" section on page 37 (the figure and table) have been updated.                                                                                       | page 37            |
|                  | The "Input Buffer Delays" table on page 38 was updated.                                                                                                                       | page 38            |
|                  | The "Global Input Buffer Delays" table on page 38 was updated.                                                                                                                | page 38            |
|                  | The "Predicted Global Routing Delay <sup>*</sup> " table on page 39 was updated.                                                                                              | page 39            |
|                  | The "Global Routing Skew" table on page 39 was updated.                                                                                                                       | page 39            |
|                  | The "Sample Macrocell Library Listing <sup>*</sup> " table on page 40 was updated.                                                                                            | page 40            |
|                  | The "Pin Description" section on page 61 was updated. GLMX is new.                                                                                                            | page 61            |
|                  | The "Power-up Sequencing" section on page 62 was updated.                                                                                                                     | page 62            |
|                  | Pin AK31 of FG1152 for the APA1000 changed to V <sub>PP</sub>                                                                                                                 | page 128           |

|                 |                                                                                                                            |          |
|-----------------|----------------------------------------------------------------------------------------------------------------------------|----------|
| (Advanced v0.6) | The "Features and Benefits" section on page 1 were updated.                                                                | page 1   |
|                 | The "ProASICPLUS Product Profile" table on page 1 was updated.                                                             | page 1   |
|                 | The "Ordering Information" section on page 3 was updated.                                                                  | page 3   |
|                 | The "Plastic Device Resources" table on page 3 was updated.                                                                | page 3   |
|                 | The "Product Plan" table on page 4 was updated.                                                                            | page 4   |
|                 | Table 1 on page 10 was updated.                                                                                            | page 10  |
|                 | Figure 12 on page 15 was updated.                                                                                          | page 15  |
|                 | The "Design Environment" section on page 23 was updated.                                                                   | page 23  |
|                 | The "Package Thermal Characteristics" table on page 24 was updated.                                                        | page 24  |
|                 | The "Calculating Power Dissipation" section on page 25 was updated.                                                        | page 25  |
|                 | The "Absolute Maximum Ratings*" table on page 26 was updated.                                                              | page 26  |
|                 | The "Programming and Storage and Operating Temperature Limits" table on page 26 was updated.                               | page 26  |
|                 | The "Supply Voltages" table on page 26 was updated.                                                                        | page 26  |
|                 | The "Recommended Operating Conditions" table on page 26 was updated.                                                       | page 26  |
|                 | The "DC Electrical Specifications ( $V_{DDP} = 2.5V \pm 0.2V$ )1" table on page 27 was updated.                            | page 27  |
|                 | The "DC Electrical Specifications ( $V_{DDP} = 3.3V \pm 0.3V$ and $V_{DD} 2.5V \pm 0.2V$ )1" table on page 28 was updated. | page 28  |
|                 | The "Synchronous Write and Read to the Same Location" figure on page 44 was updated.                                       | page 44  |
|                 | The "Asynchronous Write and Synchronous Read to the Same Location" figure on page 45 was updated.                          | page 45  |
|                 | The "Asynchronous FIFO Read" figure on page 50 was updated.                                                                | page 50  |
|                 | The "Pin Description" section on page 57 has been updated.                                                                 | page 57  |
| Advanced v0.5   | The "Recommended Design Practice for VPN/VPP" section on page 57 is new.                                                   | page 57  |
|                 | The "100-Pin TQFP" figure on page 63 is new.                                                                               | page 63  |
| Advanced v0.4   | The "484-Pin FBGA" figure on page 95 is new.                                                                               | page 95  |
|                 | The description for the $V_{PN}$ pin has changed.                                                                          | page 57  |
|                 | The "Plastic Device Resources" table on page 3 has been updated.                                                           | page 3   |
|                 | Figure 12 and Figure 13 on page 15 have been updated.                                                                      | page 15  |
|                 | The "Tristate Buffer Delays" table on page 31 has been updated.                                                            | page 31  |
|                 | The "Output Buffer Delays" table on page 32 has been updated.                                                              | page 32  |
|                 | The "Input Buffer Delays" table on page 33 has been updated.                                                               | page 33  |
|                 | The "Global Input Buffer Delays" table on page 34 has been updated.                                                        | page 34  |
|                 | The "456-Pin PBGA" table on page 73 has been updated.                                                                      | page 73  |
|                 | The "676-FBGA Pin" table on page 102 has been updated.                                                                     | page 102 |

|               |                                                                                                                                                                                                                                                                                         |                     |
|---------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------|
| Advanced v0.3 | The “ProASIC <sup>PLUS</sup> Product Profile” figure on page 1 has been changed.                                                                                                                                                                                                        | page 1              |
|               | The “Plastic Device Resources” figure on page 3 has been updated.                                                                                                                                                                                                                       | page 3              |
|               | The Supply Voltages table on page 10 has been updated.                                                                                                                                                                                                                                  | page 10             |
|               | WDATA has been changed to DI, and RDATA has been changed to DO to make them consistent with the signal names found in the <i>Macro Library Guide</i> .                                                                                                                                  |                     |
|               | Figure 13 on page 19 and Figure 14 on page 20 have been updated.                                                                                                                                                                                                                        | page 19 and page 20 |
|               | The “Design Environment” figure on page 23 and Figure 18 on page 23 have been updated.                                                                                                                                                                                                  | page 23 and page 23 |
|               | The table in the “Package Thermal Characteristics” section on page 24 has been updated.                                                                                                                                                                                                 | page 24             |
|               | The “Calculating Power Dissipation” section on page 25 is new.                                                                                                                                                                                                                          | page 25             |
|               | The “Programming and Storage and Operating Temperature Limits” section on page 26 is new.                                                                                                                                                                                               | page 26             |
|               | The “Supply Voltages” section on page 26 has been updated.                                                                                                                                                                                                                              | page 26             |
|               | The “DC Electrical Specifications ( $V_{DDP} = 2.5V \pm 0.2V$ )” table on page 27 was updated.                                                                                                                                                                                          | page 27             |
|               | The “DC Electrical Specifications ( $V_{DDP} = 3.3V \pm 0.3V$ and $V_{DD} 2.5V \pm 0.2V$ )” table on page 28 was updated.                                                                                                                                                               | page 28             |
|               | The “AC Specifications (3.3V PCI Revision 2.2 Operation)” table on page 30 was updated.                                                                                                                                                                                                 | page 30             |
|               | The “Clock Conditioning Circuit” section on page 14 was updated.                                                                                                                                                                                                                        | page 14             |
|               | Figure 12 on page 15 was updated.                                                                                                                                                                                                                                                       | page 15             |
|               | Figure 13 on page 15 is new.                                                                                                                                                                                                                                                            | page 15             |
|               | Tables 5, 6, and 7 from Advanced v0.3 were removed.                                                                                                                                                                                                                                     |                     |
|               | The “Memory Block SRAM Interface Signals” figure on page 19 was updated.                                                                                                                                                                                                                | page 19             |
|               | The “Memory Block FIFO Interface Signals” figure on page 48 was updated.                                                                                                                                                                                                                | page 48             |
|               | All pinout tables have been updated, and several packages are new:<br>208-Pin PQFP – APA150, APA300, APA450, APA600<br>456-Pin PBGA – APA150, APA300, APA450, APA600<br>144-Pin FBGA – APA150, APA300, APA450<br>256-Pin FBGA – APA150, APA300, APA450, APA600<br>676-Pin FBGA – APA600 |                     |
| Advanced v0.1 | Figure 15 on page 21 has been updated                                                                                                                                                                                                                                                   | page 21             |

## Datasheet Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as “Product Brief,” “Advanced,” “Production.” The definition of these categories are as follows:

### Product Brief

The product brief is a modified version of an advanced datasheet containing general product information. This brief summarizes specific device and family information for unreleased products.

### Advanced

This datasheet version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production.

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<http://www.actel.com>

**Actel Europe Ltd.**

Maxfli Court, Riverside Way  
Camberley, Surrey GU15 3YL  
United Kingdom

**Tel:** +44-(0)1276 401450

**Fax:** +44-(0)1276 401490

**Actel Corporation**

955 East Arques Avenue  
Sunnyvale, California 94086  
USA

**Tel:** (408) 739-1010

**Fax:** (408) 739-1540

**Actel Asia-Pacific**

EXOS Ebisu Bldg. 4F  
1-24-14 Ebisu Shibuya-ku  
Tokyo 150 Japan

**Tel:** +81-(0)3-3445-7671

**Fax:** +81-(0)3-3445-7668