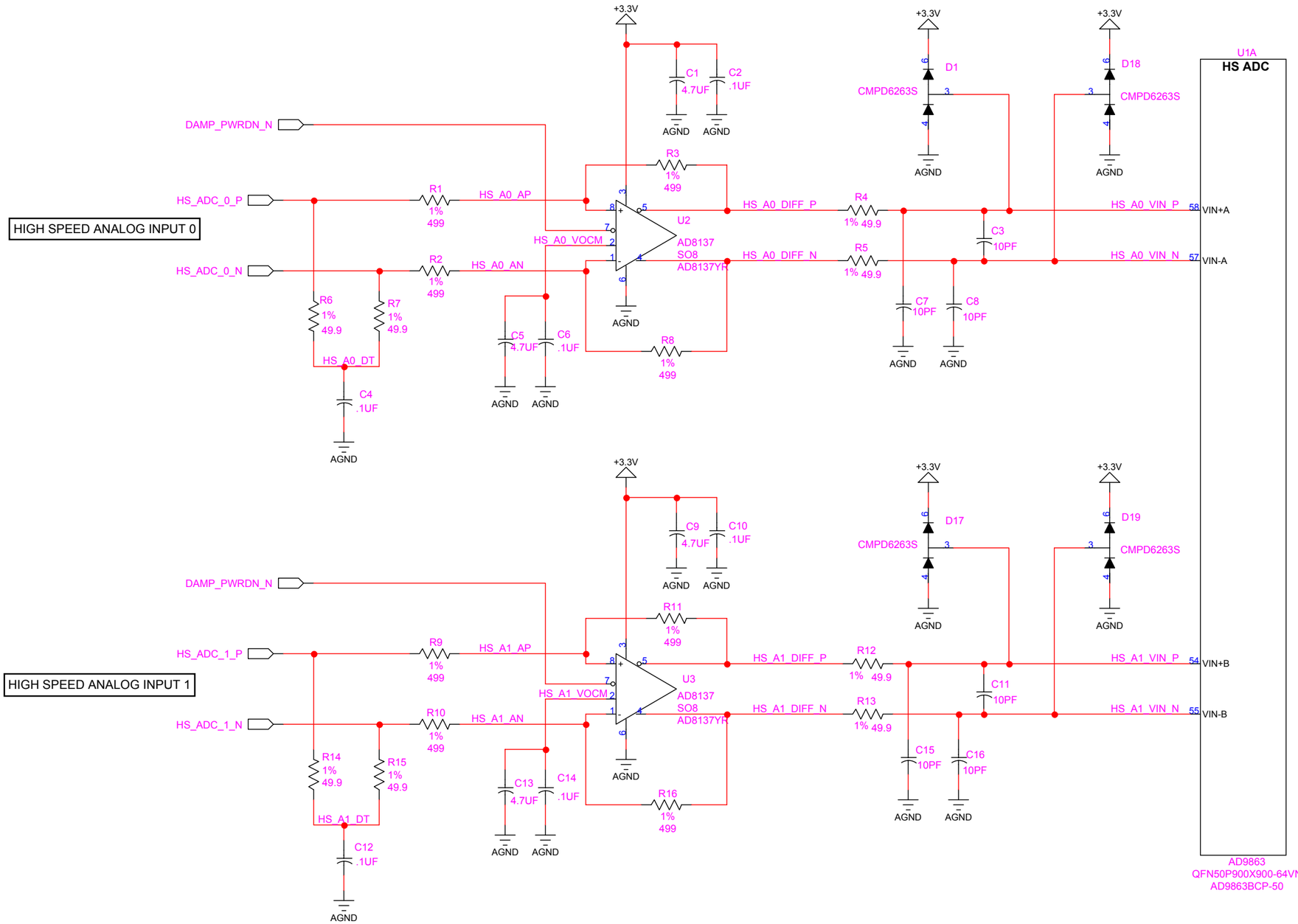
# HIGH SPEED ADC 0 & 1

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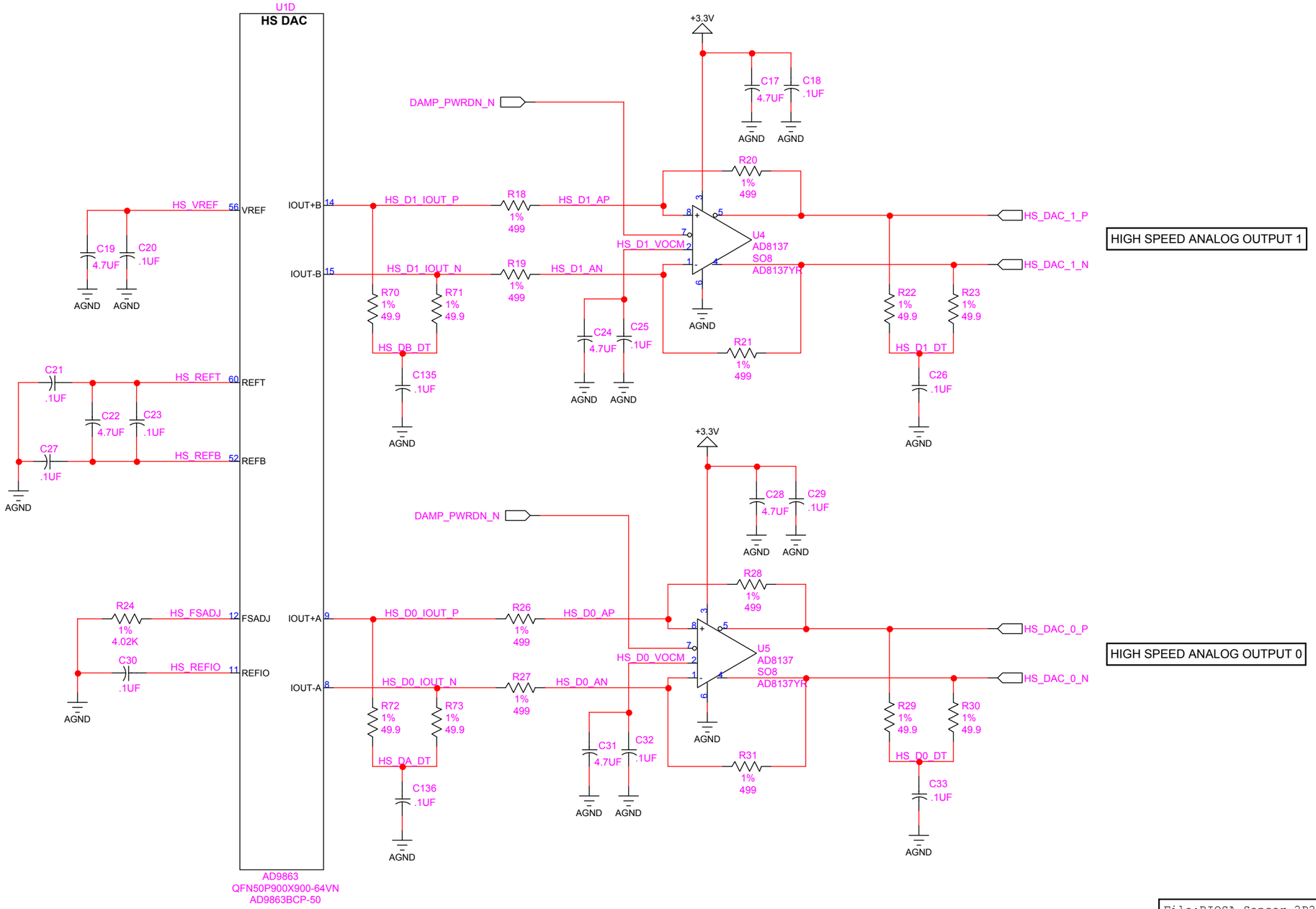
# HIGH SPEED DAC 0 & 1




HIGH SPEED ANALOG OUTPUT 1

HIGH SPEED ANALOG OUTPUT 0

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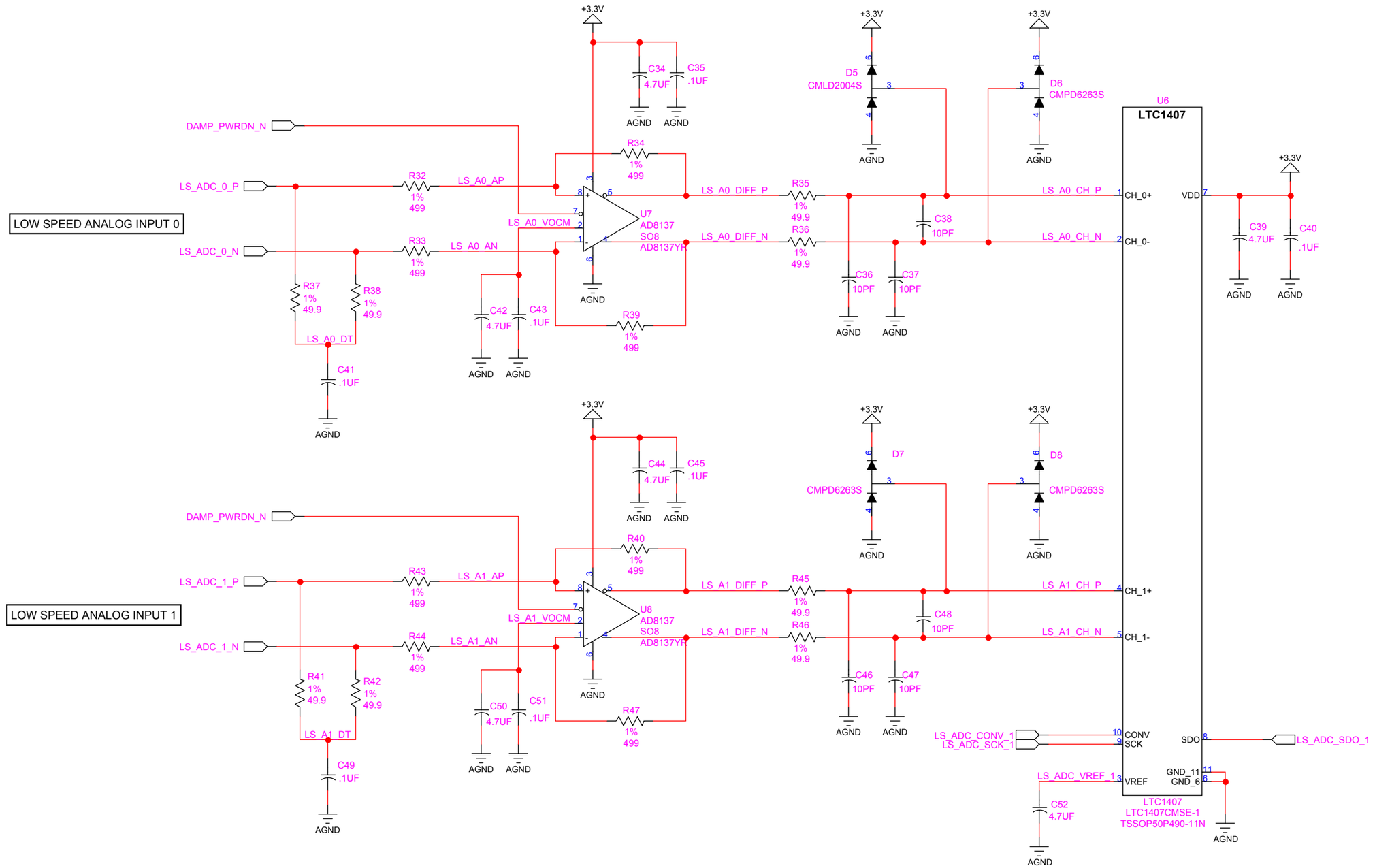
# LOW SPEED ADC 0 & 1

LOW SPEED ANALOG INPUT 0

LOW SPEED ANALOG INPUT 1

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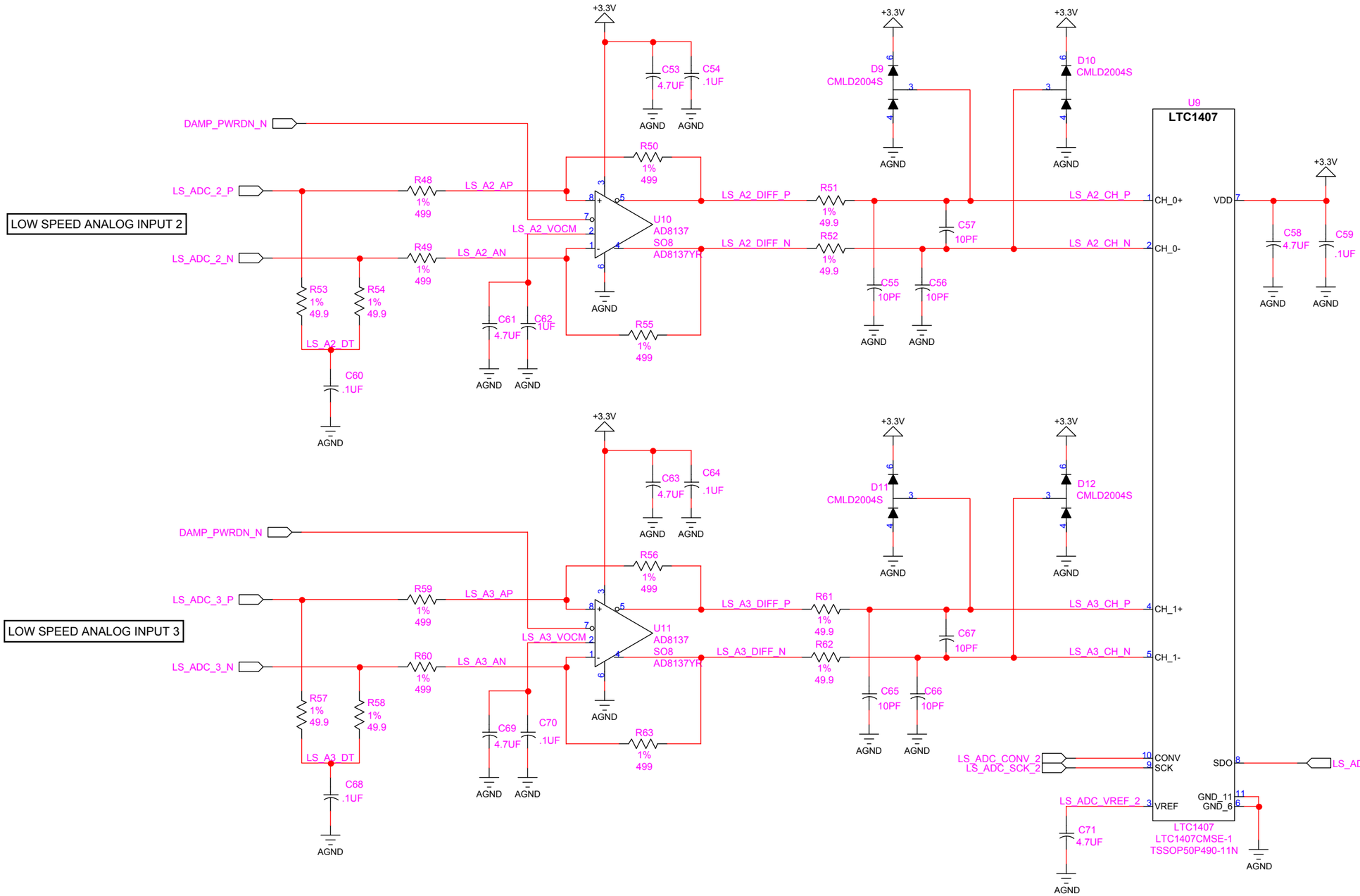
# LOW SPEED ADC 2 & 3

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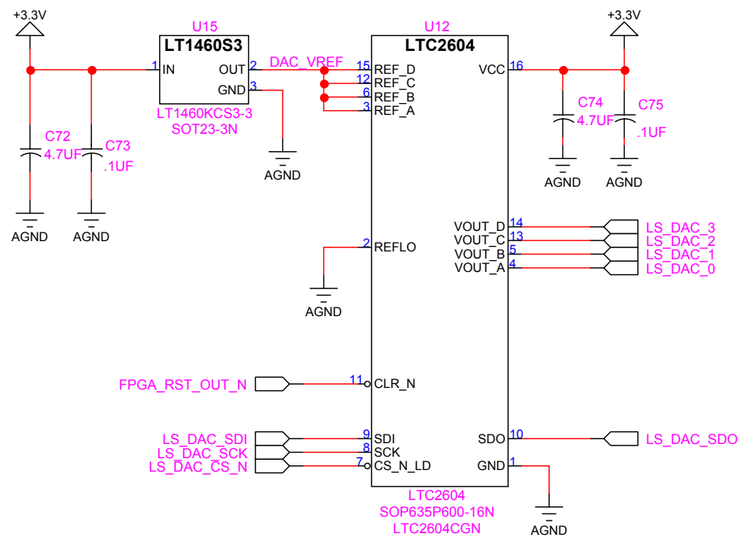
# LOW SPEED DAC 0,1,2,3(OPTIONAL)

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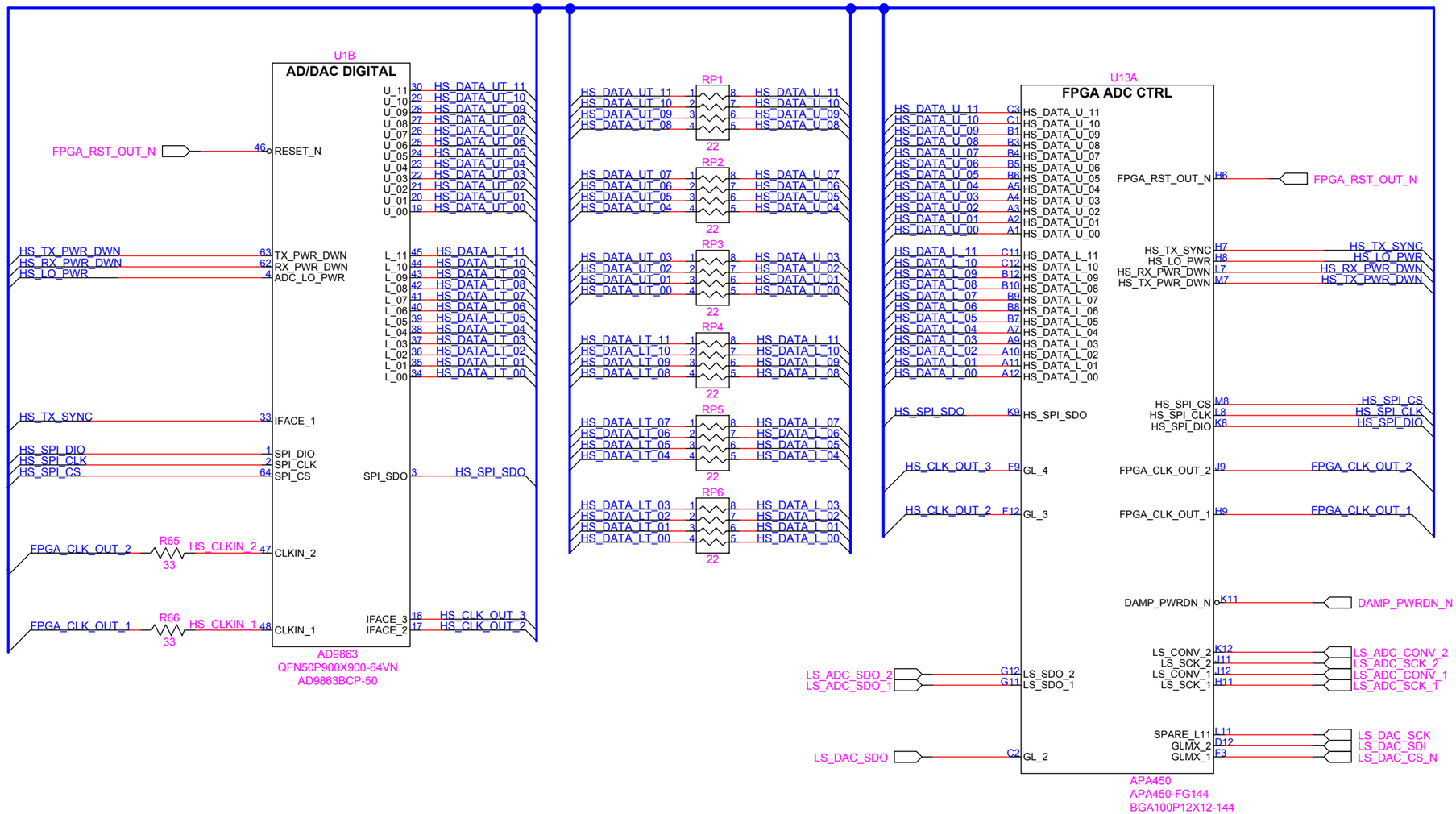
# AD/DAC FPGA INTERFACE

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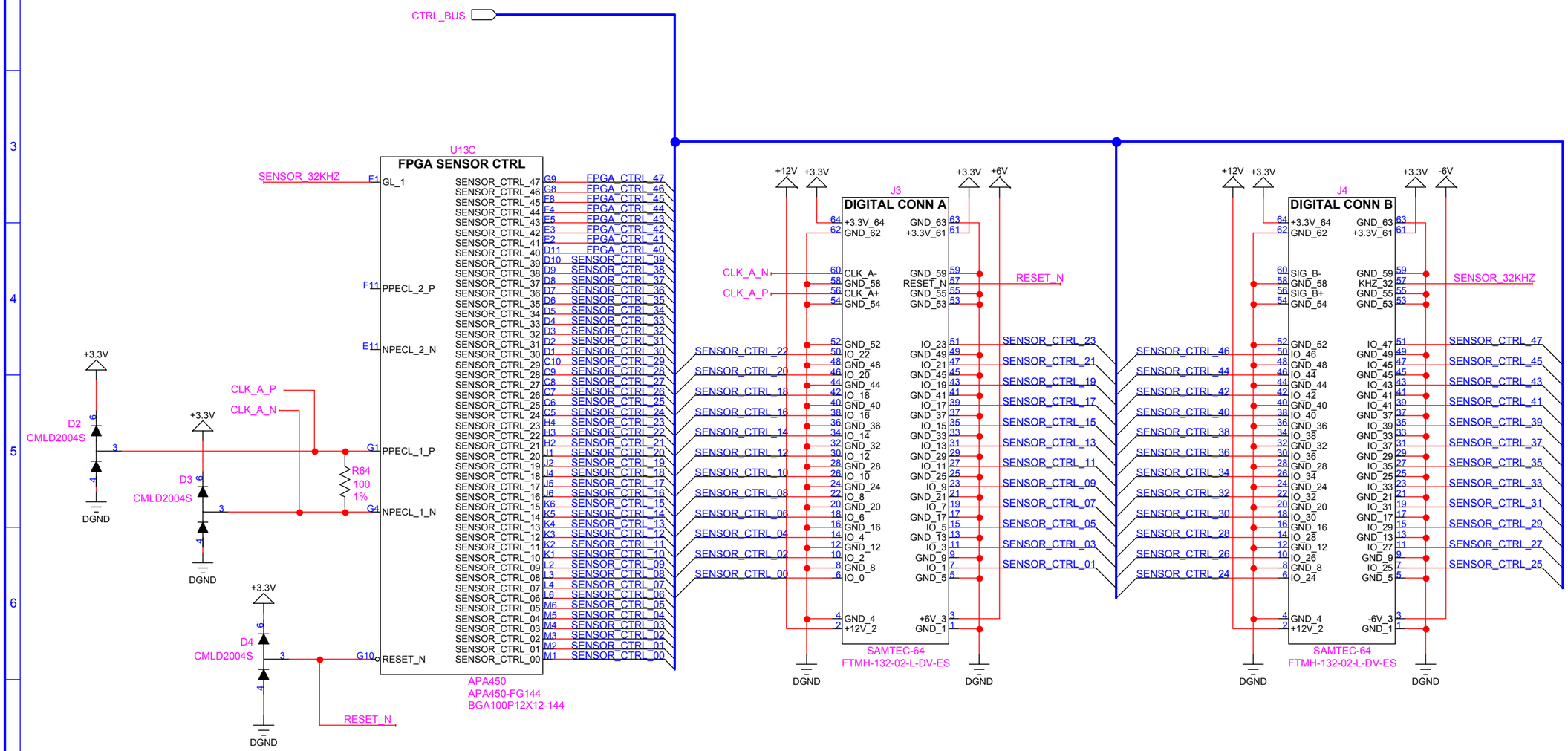
# FINGERBOARD INTERFACE

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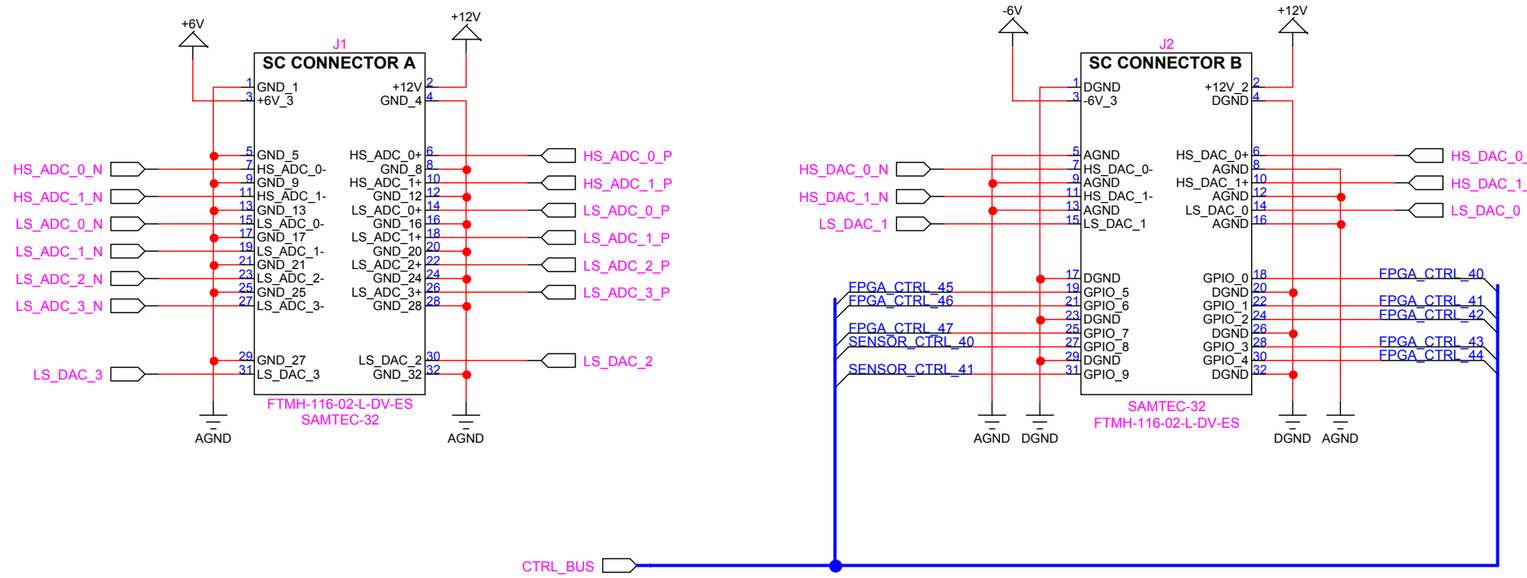
# SENSOR INTERFACE

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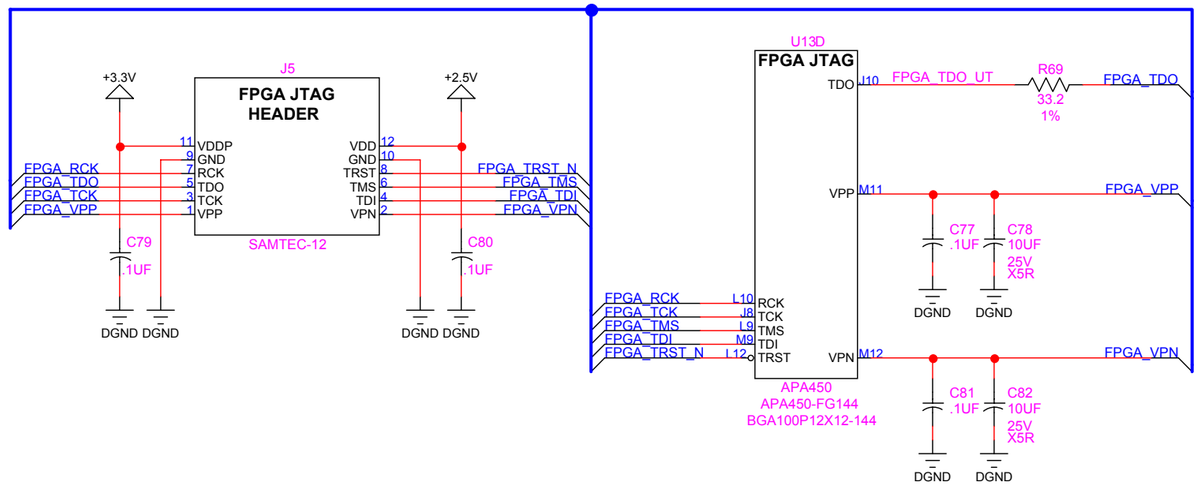
# FPGA PROGRAMMING

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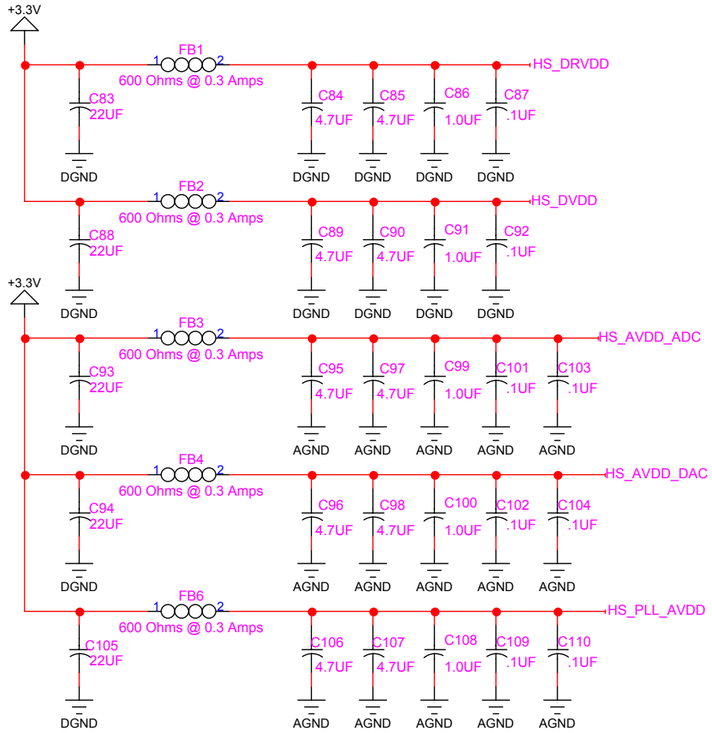
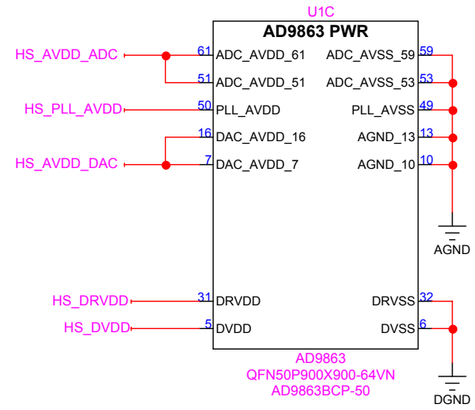
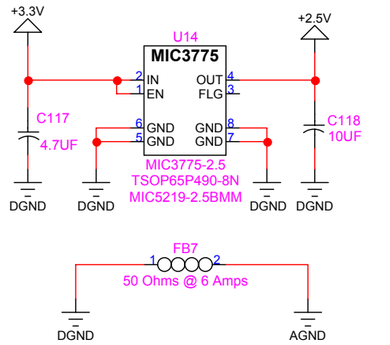
# POWER DISTRIBUTION







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