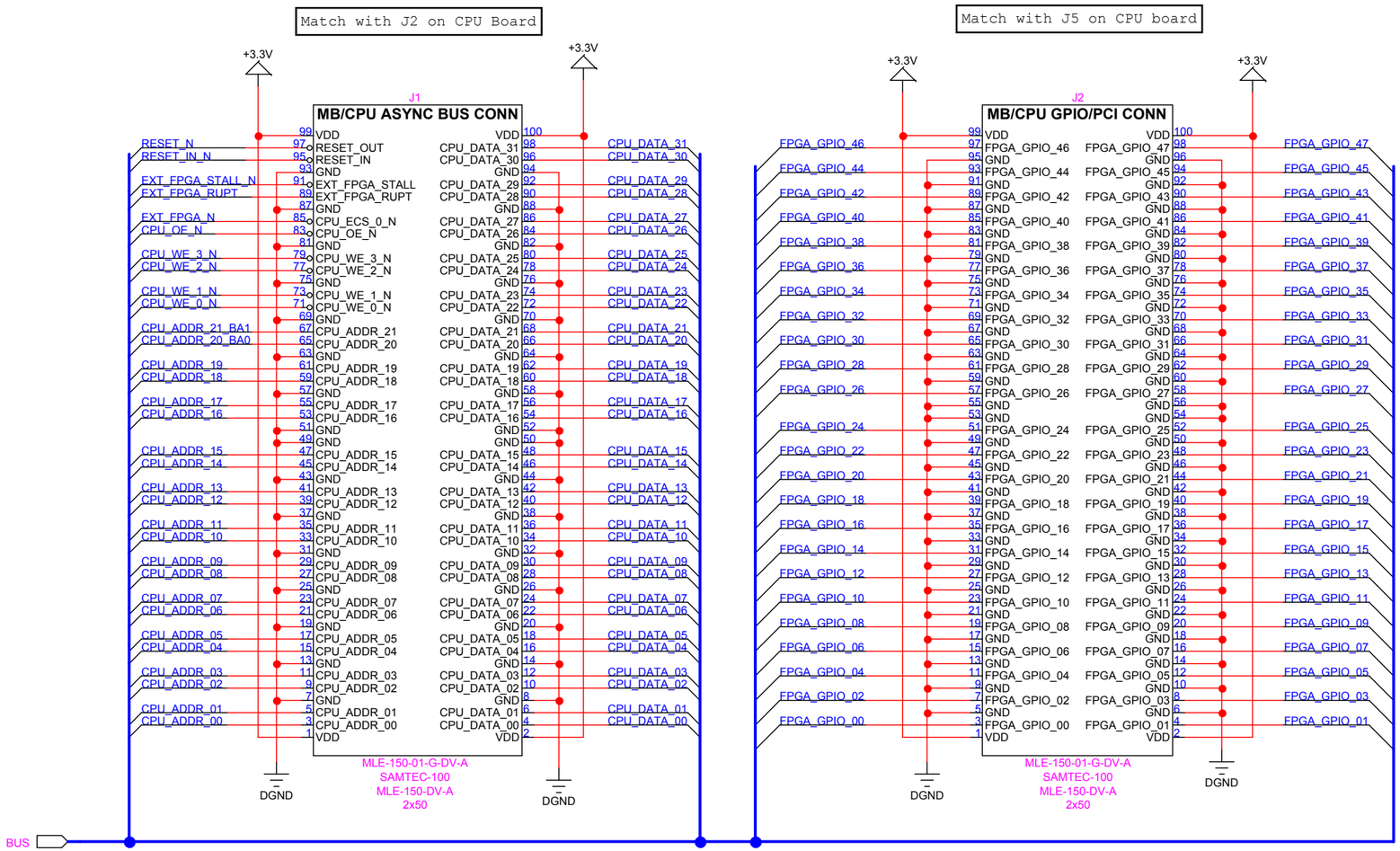
CPU BOARD INTERFACE



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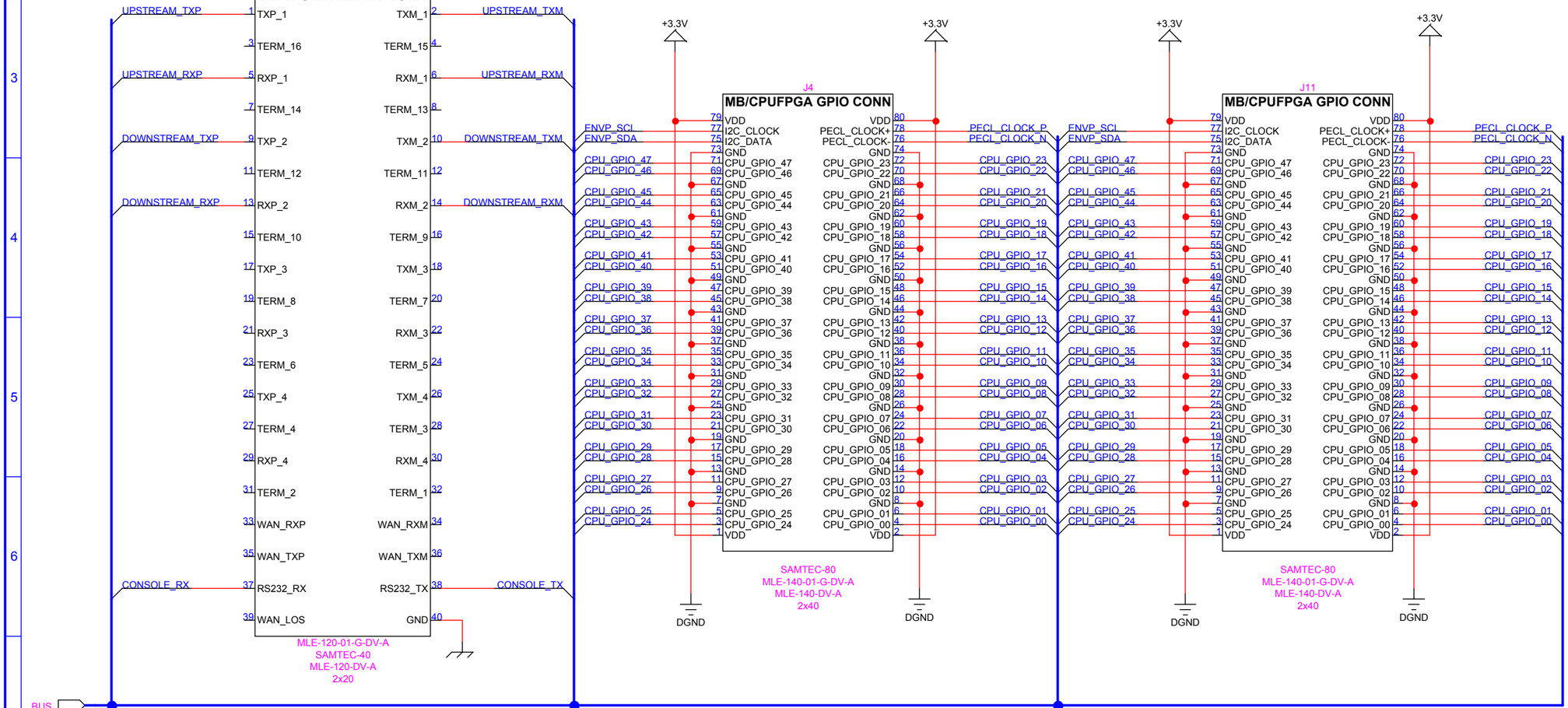
CPU ETHERNET AND GPIO

4 RJ45 Compatible ports
Match with J6 on CPU board

Match with J4 on CPU board



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FINGERBOARD INTERFACE

Match with J1 on Fingerboard

U1G
MB/FPGA SENSOR CTRL

SI_47	M15	SENSOR_CTRL_47	D14	IO_47
SI_46	M8	SENSOR_CTRL_46	B14	IO_46
SI_45	M7	SENSOR_CTRL_45	A14	IO_45
SI_44	M3	SENSOR_CTRL_44	F13	IO_44
SI_43	M2	SENSOR_CTRL_43	C13	IO_43
SI_42	M1	SENSOR_CTRL_42	A13	IO_42
SI_41	L22	SENSOR_CTRL_41	E12	IO_41
SI_40	L21	SENSOR_CTRL_40	D12	IO_40
SI_39	L20	SENSOR_CTRL_39	B12	IO_39
SI_38	L15	SENSOR_CTRL_38	A12	IO_38
SI_37	L8	SENSOR_CTRL_37	E11	IO_37
SI_36	L3	SENSOR_CTRL_36	C11	IO_36
SI_35	L2	SENSOR_CTRL_35	A11	IO_35
SI_34	L1	SENSOR_CTRL_34	E10	IO_34
SI_33	K22	SENSOR_CTRL_33	D10	IO_33
SI_32	K21	SENSOR_CTRL_32	B10	IO_32
SI_31	K20	SENSOR_CTRL_31	A10	IO_31
SI_30	K19	SENSOR_CTRL_30	E9	IO_30
SI_29	K18	SENSOR_CTRL_29	C9	IO_29
SI_28	K17	SENSOR_CTRL_28	A9	IO_28
SI_27	K16	SENSOR_CTRL_27	E8	IO_27
SI_26	K7	SENSOR_CTRL_26	D8	IO_26
SI_25	K6	SENSOR_CTRL_25	B8	IO_25
SI_24	K5	SENSOR_CTRL_24	A8	IO_24
SI_23	K4	SENSOR_CTRL_23	E7	IO_23
SI_22	K3	SENSOR_CTRL_22	C7	IO_22
SI_21	K2	SENSOR_CTRL_21	A7	IO_21
SI_20	K1	SENSOR_CTRL_20	F6	IO_20
SI_19	J22	SENSOR_CTRL_19	D6	IO_19
SI_18	J21	SENSOR_CTRL_18	B6	IO_18
SI_17	J20	SENSOR_CTRL_17	A6	IO_17
SI_16	J19	SENSOR_CTRL_16	E5	IO_16
SI_15	J18	SENSOR_CTRL_15	C5	IO_15
SI_14	J17	SENSOR_CTRL_14	A5	IO_14
SI_13	J16	SENSOR_CTRL_13	E4	IO_13
SI_12	J7	SENSOR_CTRL_12	D4	IO_12
SI_11	J6	SENSOR_CTRL_11	B4	IO_11
SI_10	J5	SENSOR_CTRL_10	A4	IO_10
SI_09	J4	SENSOR_CTRL_09	E3	IO_09
SI_08	J3	SENSOR_CTRL_08	C3	IO_08
SI_07	J2	SENSOR_CTRL_07	A3	IO_07
SI_06	J1	SENSOR_CTRL_06	E2	IO_06
SI_05	H22	SENSOR_CTRL_05	D2	IO_05
SI_04	H21	SENSOR_CTRL_04	B2	IO_04
SI_03	H19	SENSOR_CTRL_03	A2	IO_03
SI_02	H18	SENSOR_CTRL_02	E1	IO_02
SI_01	H17	SENSOR_CTRL_01	C1	IO_01
SI_00	H16	SENSOR_CTRL_00	A1	IO_00

APA600
BGA100P22X22-484

J5A
MB/FINGERBOARD CONN

	C14	GND_20	
	D13	GND_19	
	B13	GND_18	
	C12	GND_17	
	D11	GND_16	
	B11	GND_15	
	C10	GND_14	
	D9	GND_13	
	B9	GND_12	
	C8	GND_11	
	D7	GND_10	
	B7	GND_09	
	C6	GND_08	
	D5	GND_07	
	B5	GND_06	
	C4	GND_05	
	D3	GND_04	
	B3	GND_03	
	C2	GND_02	
	D1	GND_01	
	B1	GND_00	
RESET_IN_N	C18	RESET_IN_N	
	C15	PWR_RET	
RESET_N	A19	RESET_N	
ENVP_SCL	B16	ENVP_SCL	
ENVP_SDA	A16	ENVP_SDA	
KHZ_32	E14	KHZ_32_IN	
CONSOLE_RX	E19	CONSOLE_RX	
CONSOLE_TX	D19	CONSOLE_TX	
+12V	C19		
+6V	C16		
+3.3V	B19		
-6V	C17		
UP_TX-	E18	UPSTREAM_TXM	
UP_TX+	D18	UPSTREAM_TXP	
UP_RX-	B18	UPSTREAM_RXM	
UP_RX+	A18	UPSTREAM_RXP	
DOWN_TX-	E17	DOWNSTREAM_TXM	
DOWN_TX+	D17	DOWNSTREAM_TXP	
DOWN_RX-	B17	DOWNSTREAM_RXM	
DOWN_RX+	A17	DOWNSTREAM_RXP	
CLK3-	E16	SLOT_3_CLOCK_N	
CLK3+	D16	SLOT_3_CLOCK_P	
CLK2-	E15	SLOT_2_CLOCK_N	
CLK2+	D15	SLOT_2_CLOCK_P	
CLK1-	B15	SLOT_1_CLOCK_N	
CLK1+	A15	SLOT_1_CLOCK_P	

AVX-95
5x19

DGND

+12V
+6V
+3.3V
-6V

ENVP_SCL — R36 10K — +3.3V
ENVP_SDA — R39 10K — +3.3V

J5B
MB/FINGERBOARD CONN SHRD

F19	SHRD_19	
F18	SHRD_18	
F17	SHRD_17	
F16	SHRD_16	
F15	SHRD_15	
F14	SHRD_14	
F13	SHRD_13	
F12	SHRD_12	
F11	SHRD_11	
F10	SHRD_10	
F9	SHRD_09	
F8	SHRD_08	
F7	SHRD_07	
F6	SHRD_06	
F5	SHRD_05	
F4	SHRD_04	
F3	SHRD_03	
F2	SHRD_02	
F1	SHRD_01	

AVX-95
5x19
CON_HM_064784-95

DGND

FB1
100 Ohms @ 3 Amps

DGND

BUS

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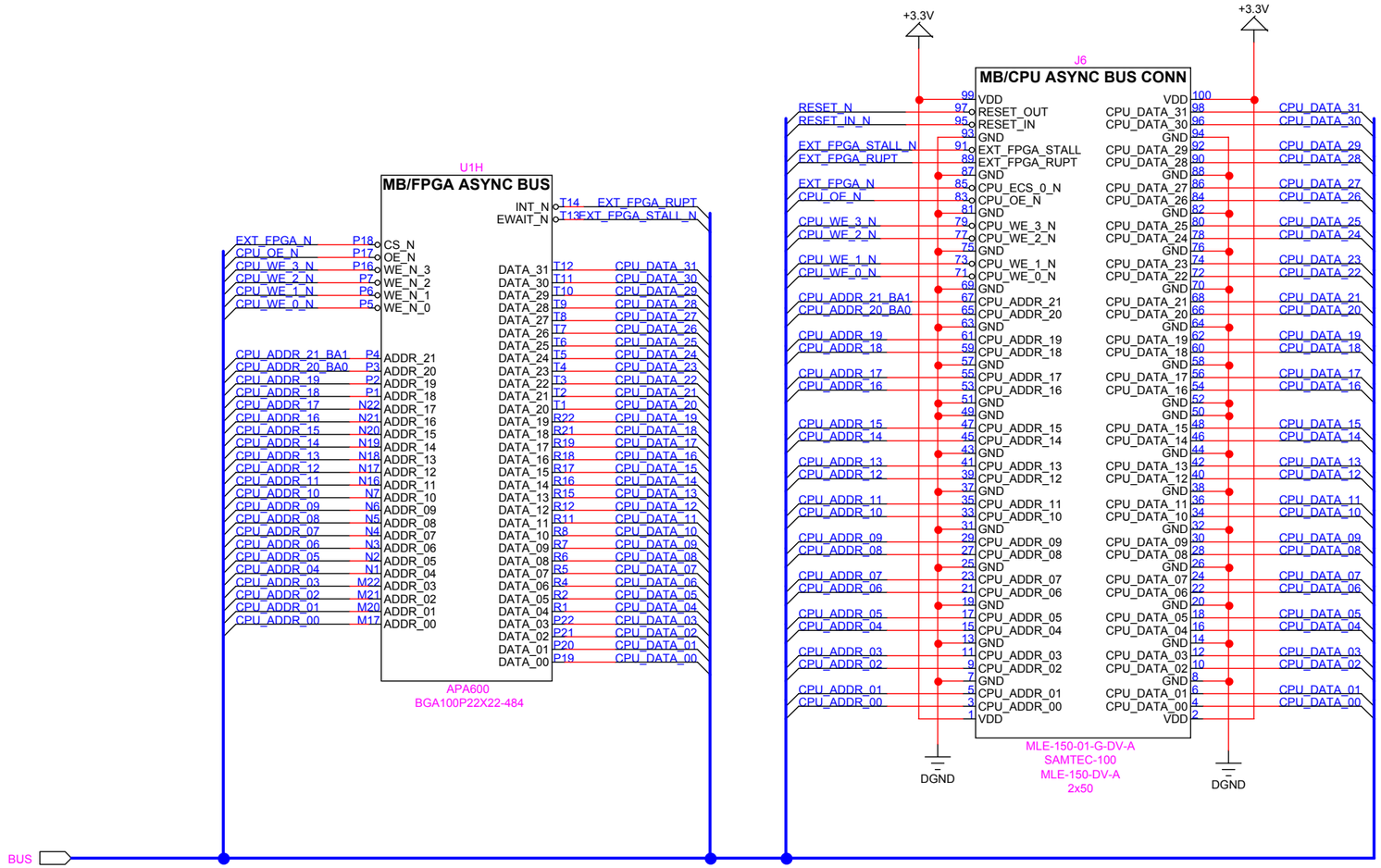
FPGA ASYNC INTERFACE



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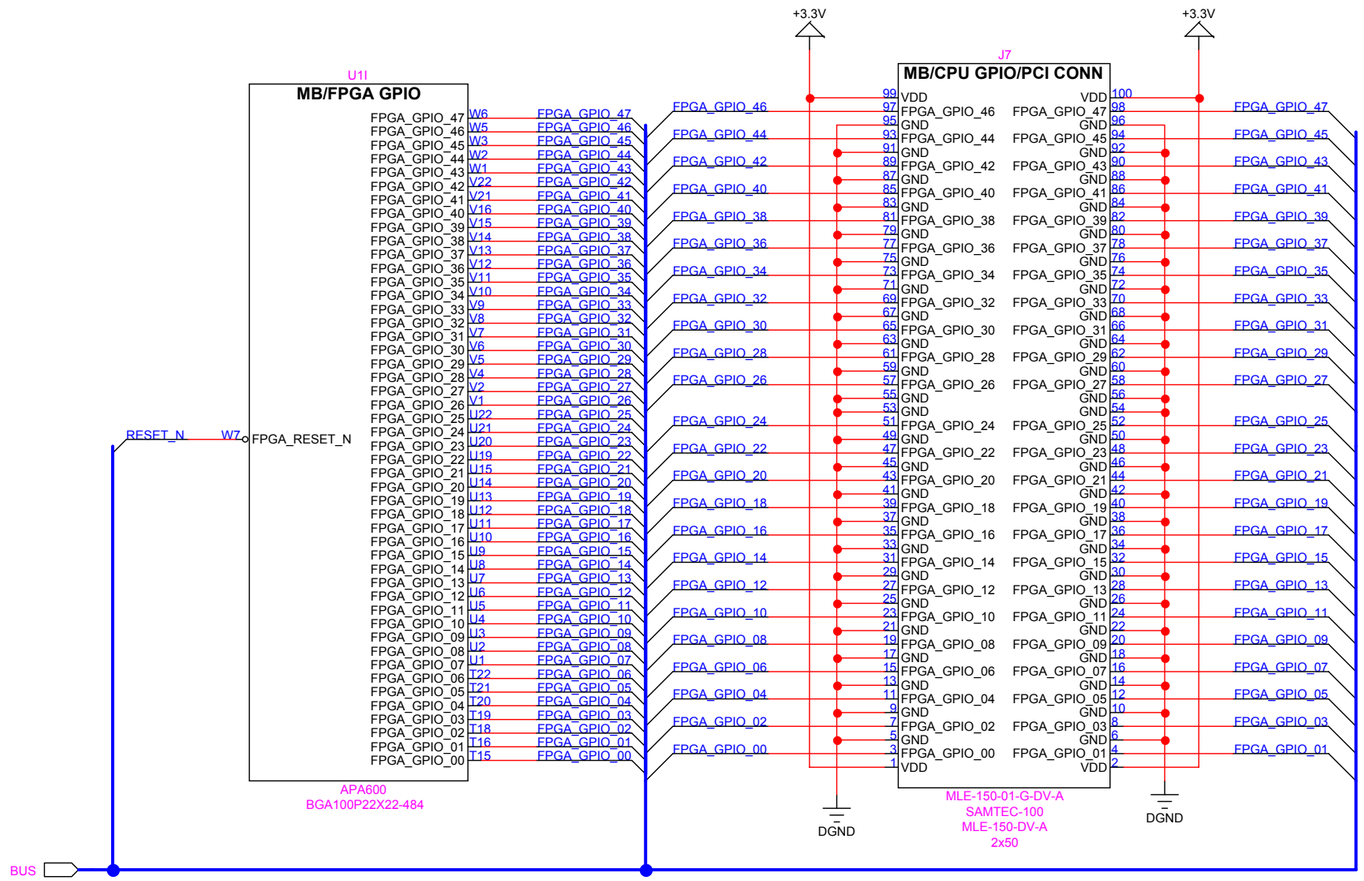
FPGA GPIO INTERFACE



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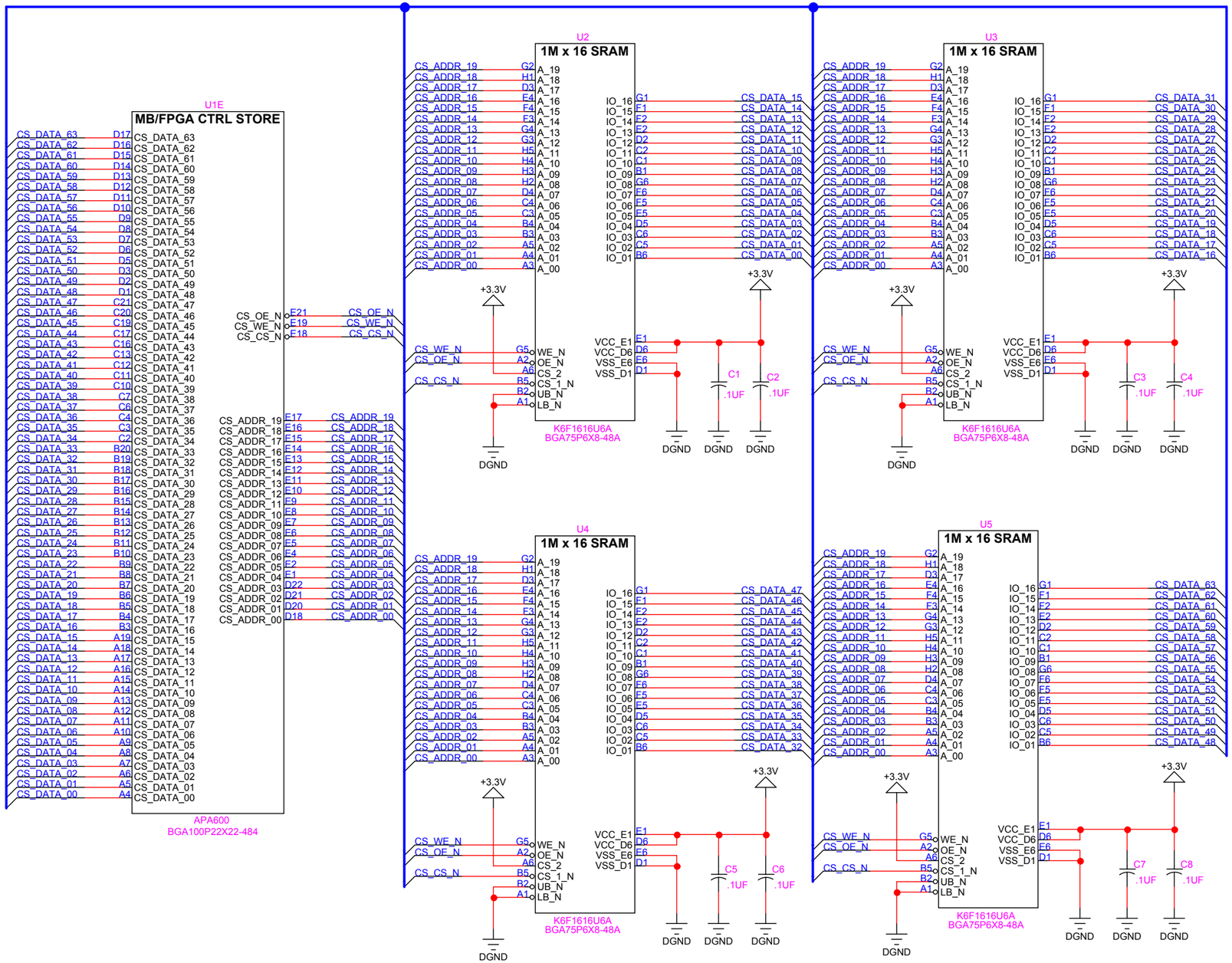
CONTROL STORE



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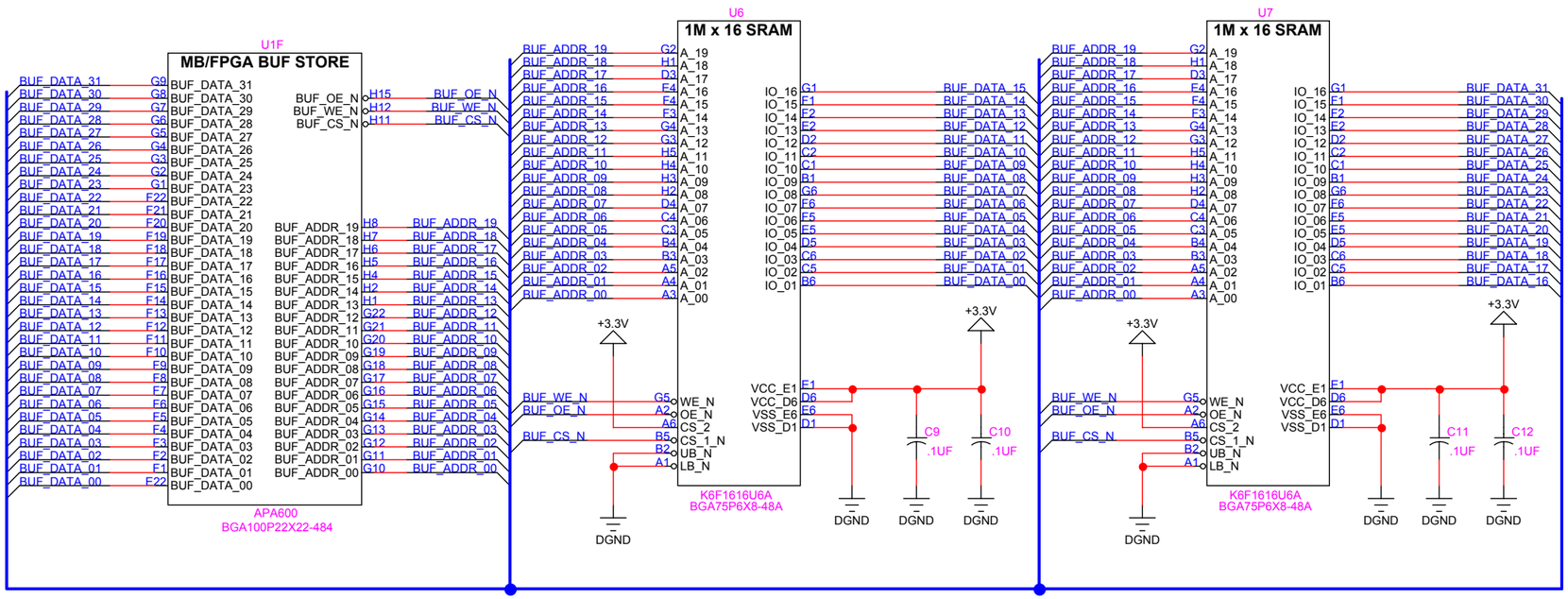
BUFFER MEMORY



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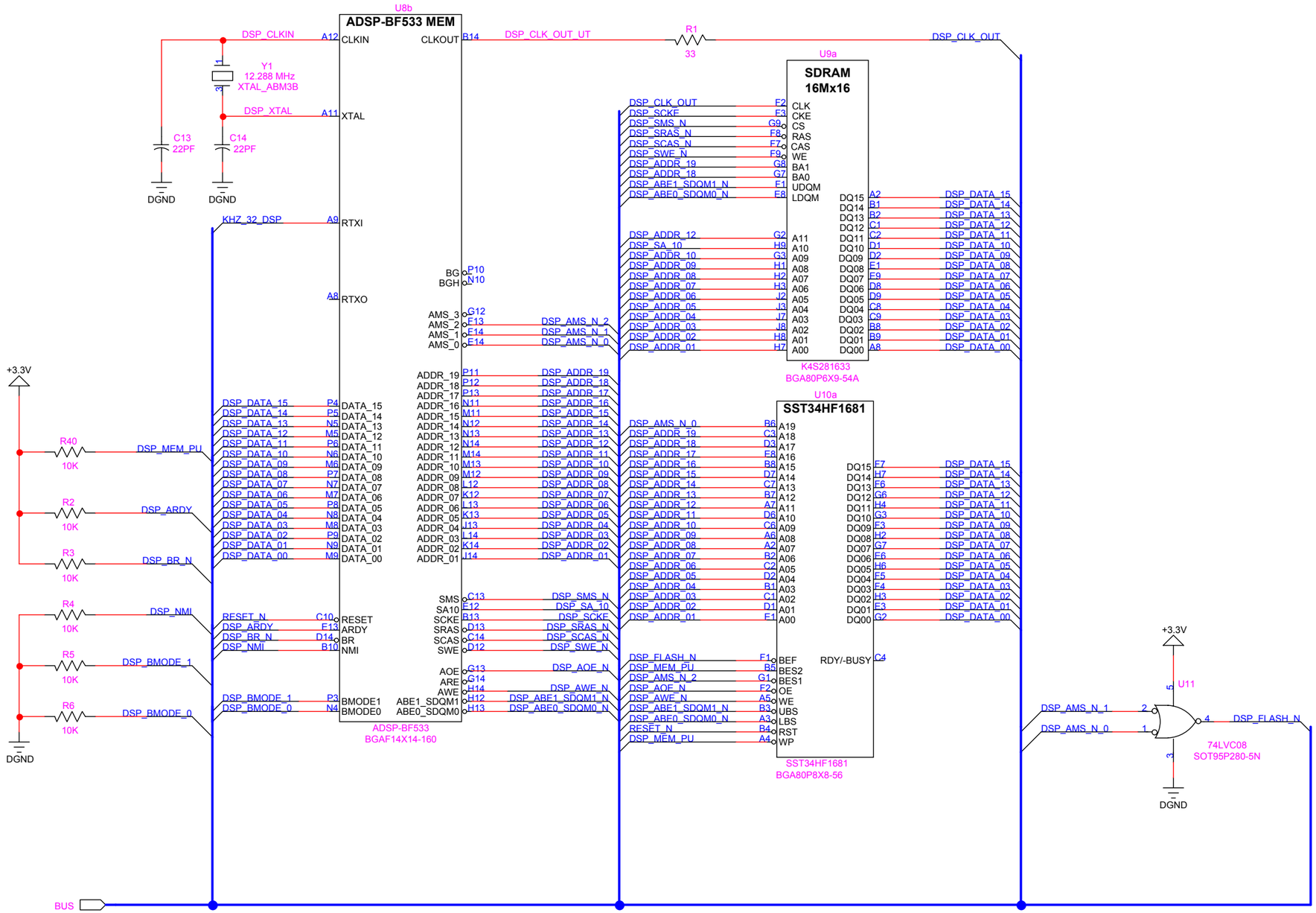
DSP AND STORAGE



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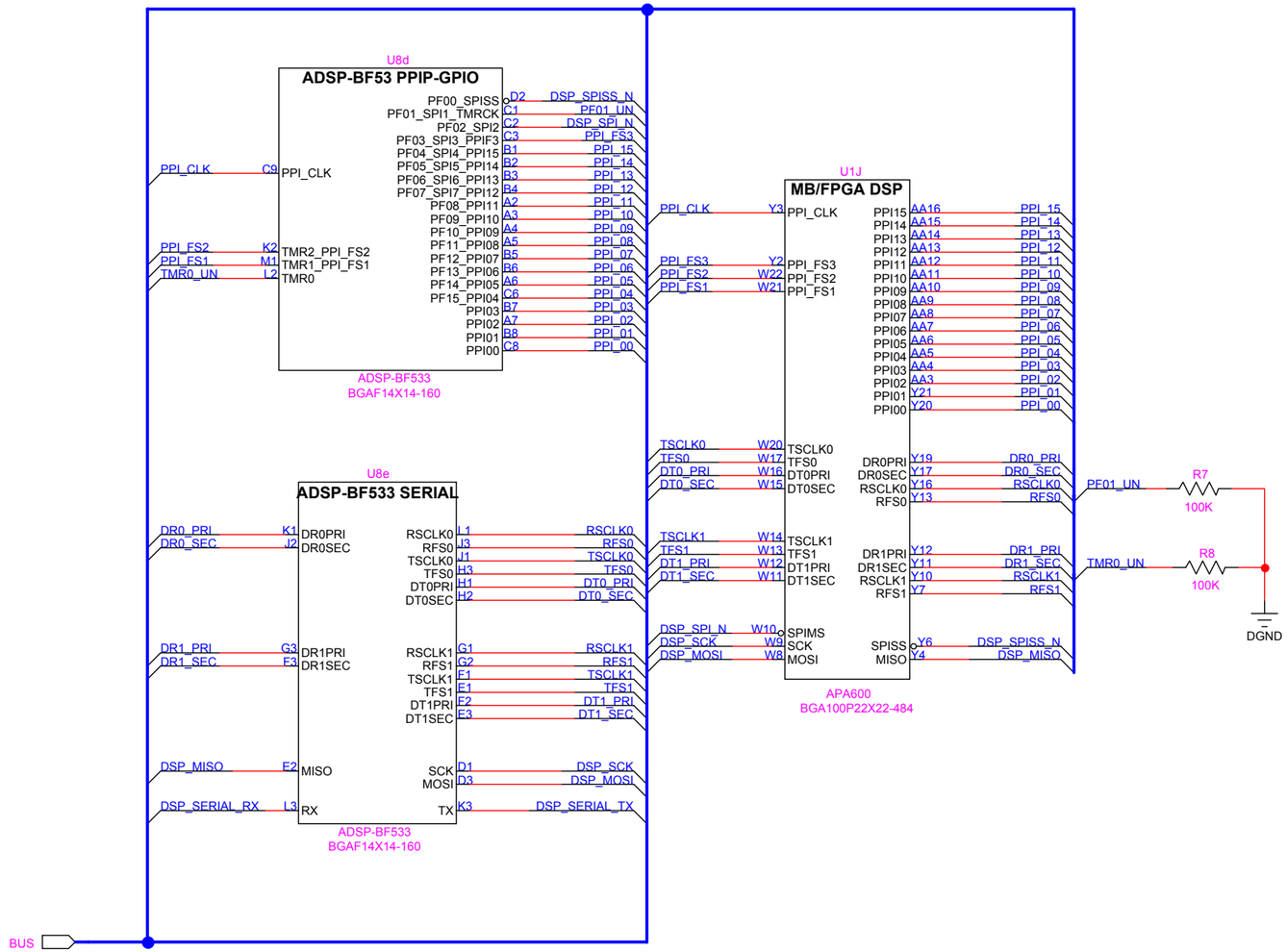
DSP TO FPGA INTERFACE



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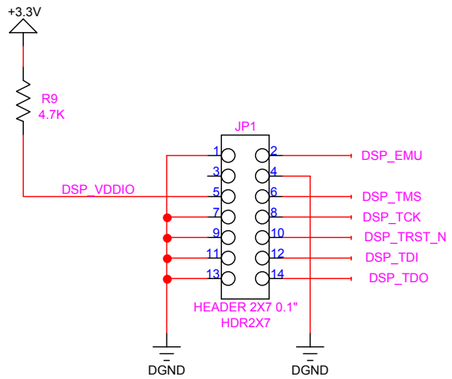
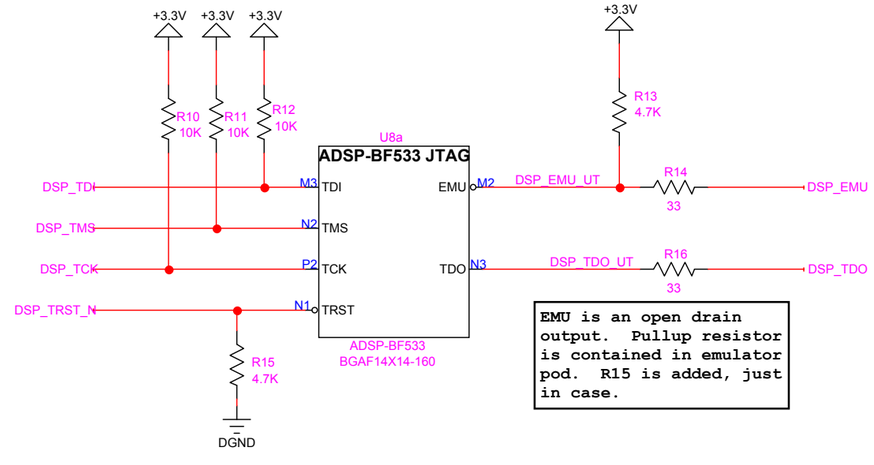
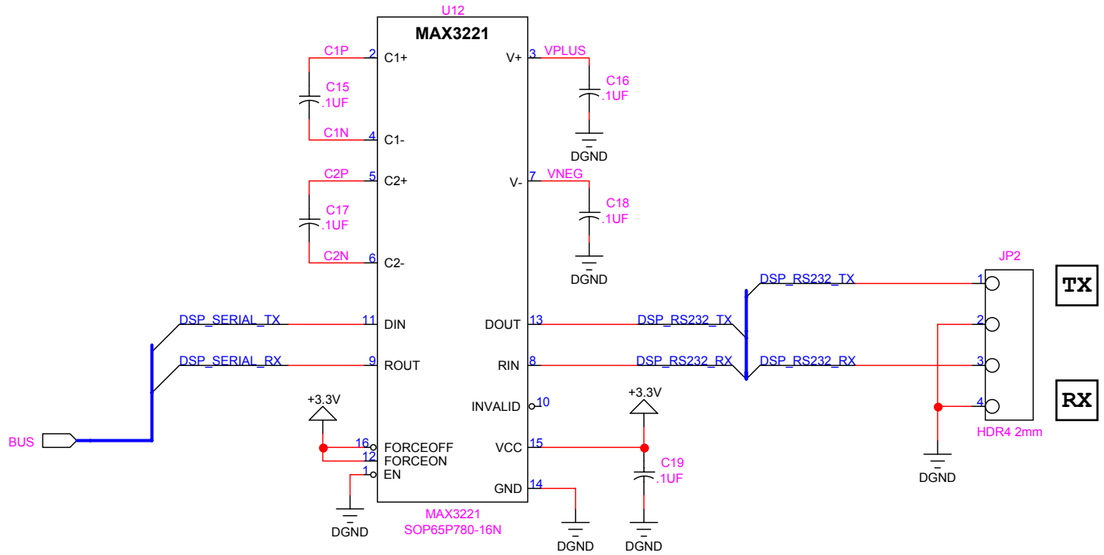
DSP JTAG DEBUG



Pin 3 of JP3 must be clipped off prior to using an emulator.



EMU is an open drain output. Pullup resistor is contained in emulator pod. R15 is added, just in case.



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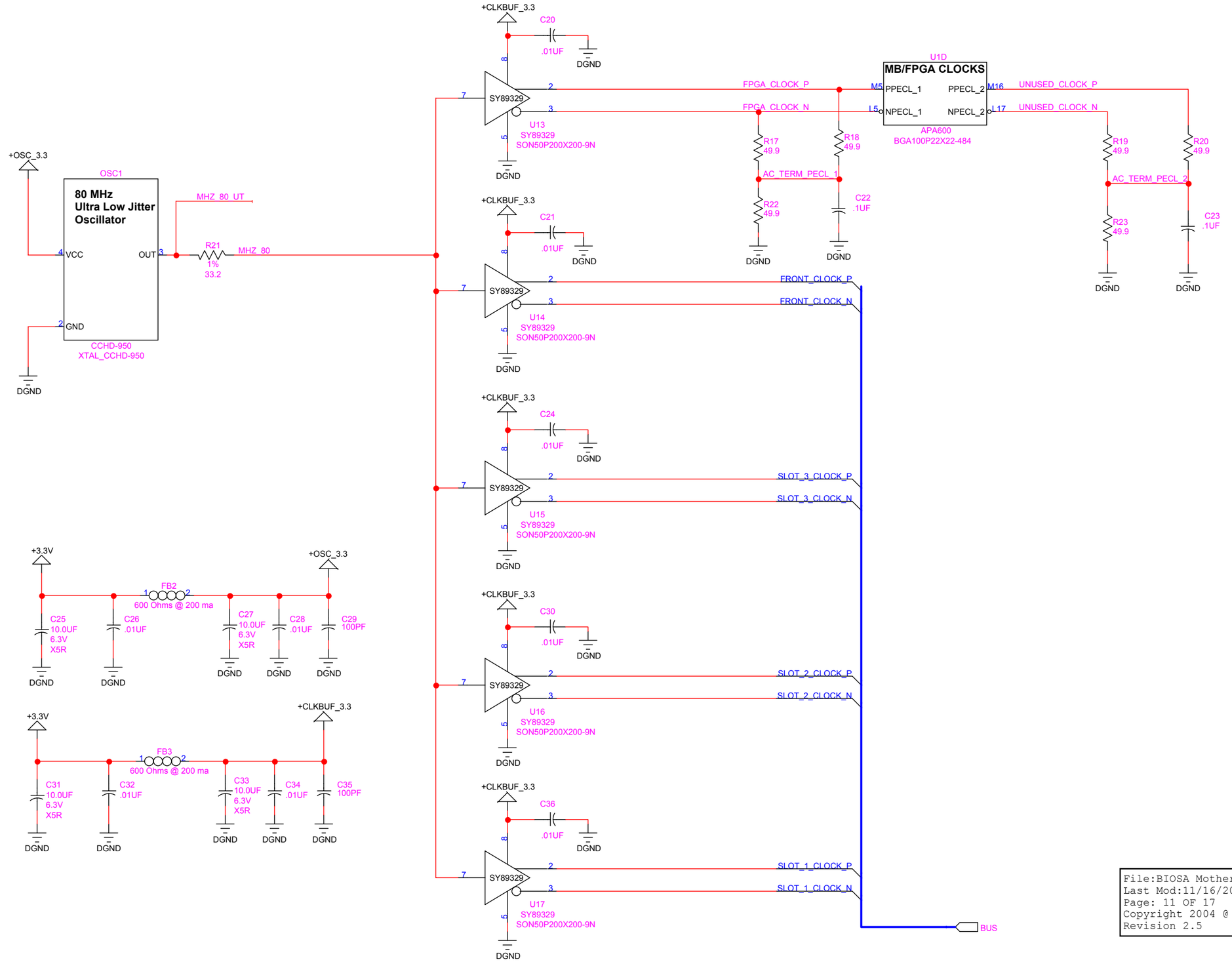
FINGERBOARD CLOCK GENERATOR



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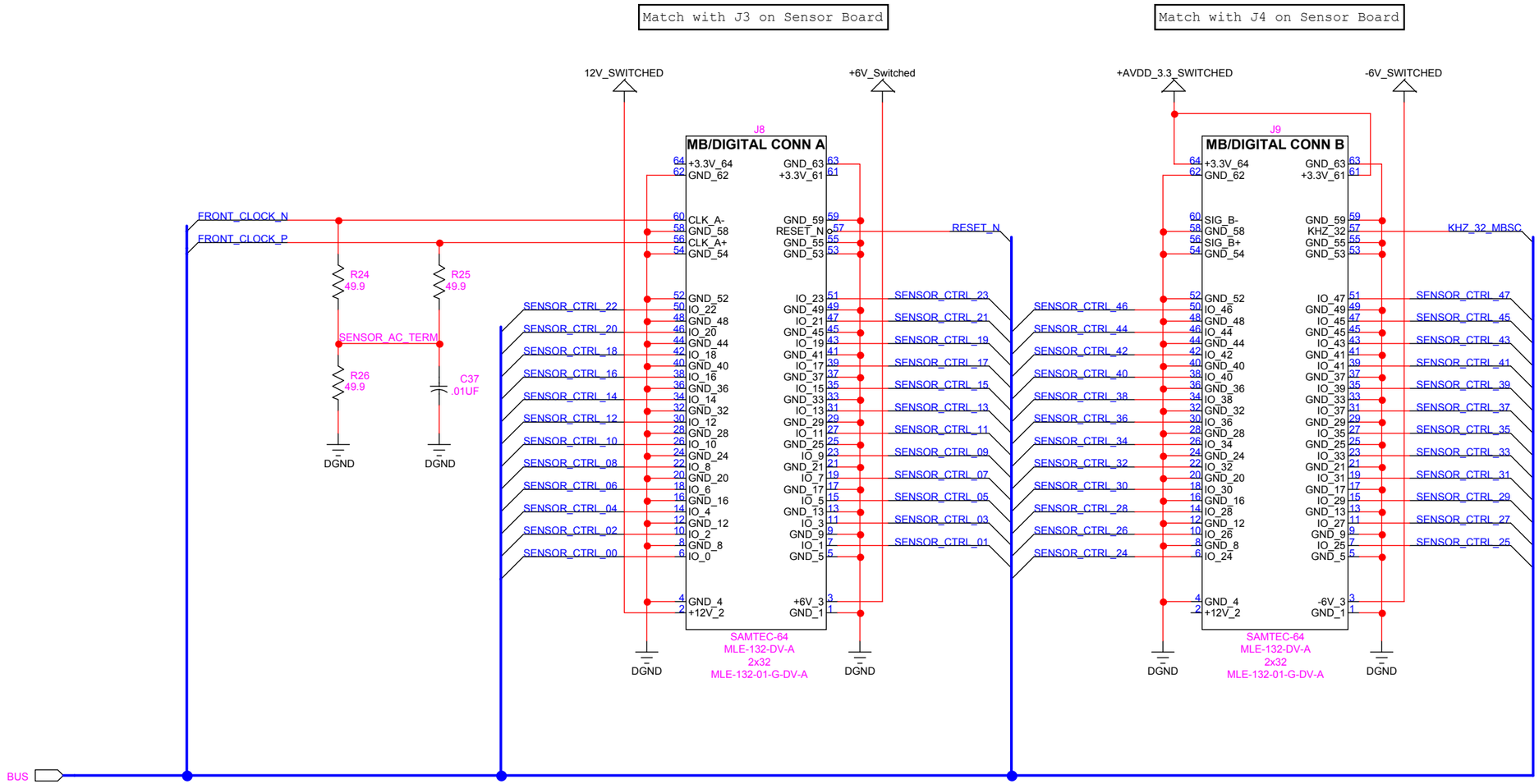
SENSOR CONTROL CONNECTOR



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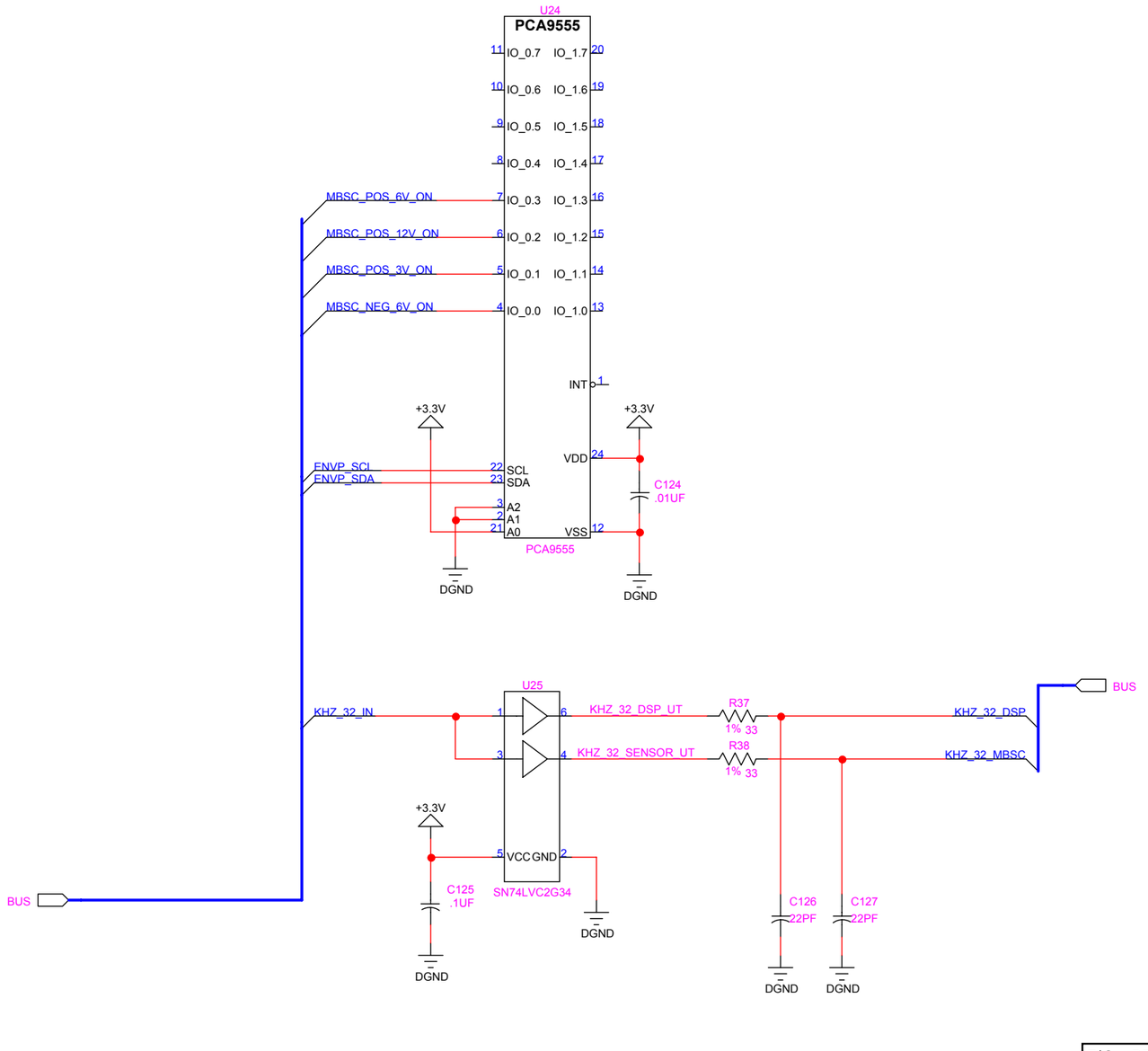
I2C POWER CONTROL AND 32KHZ DISTRIBUTION

I2C Address = "0100001R"



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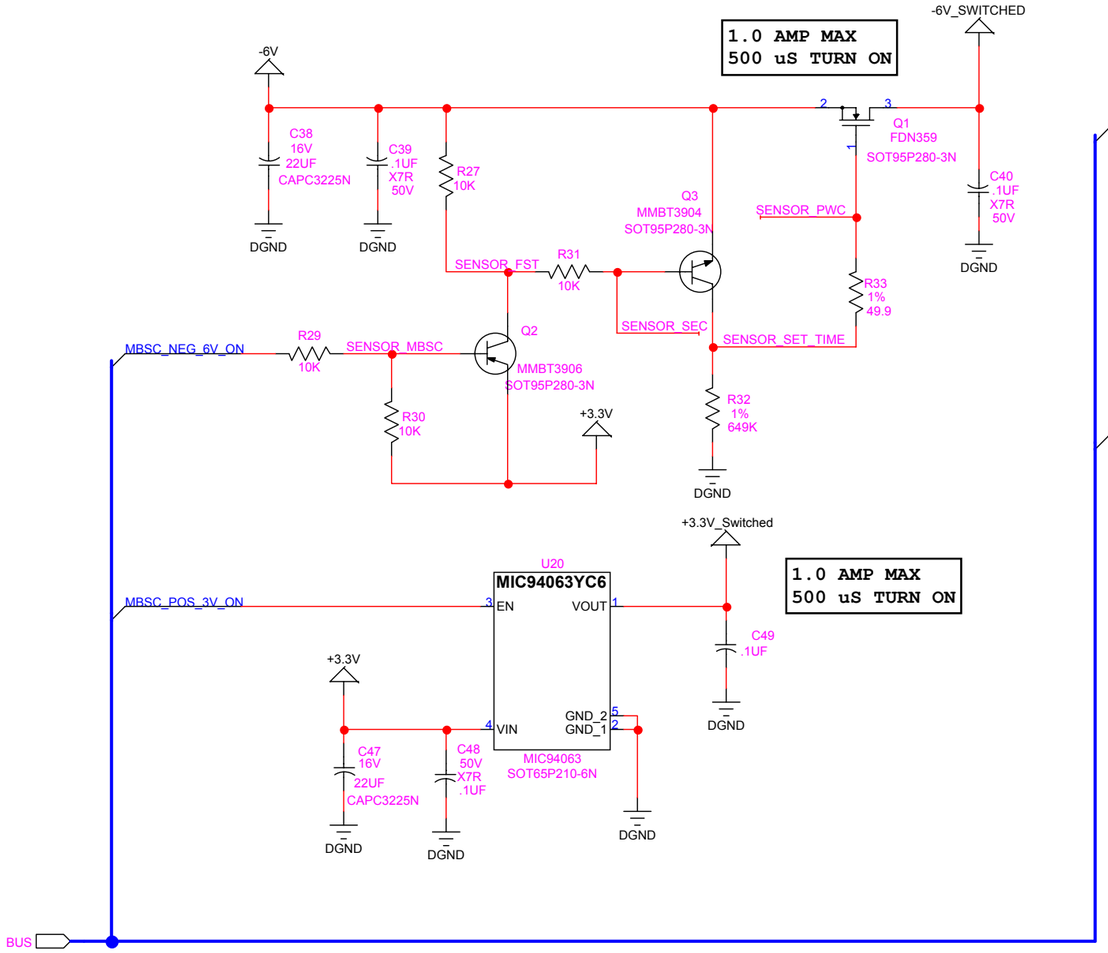
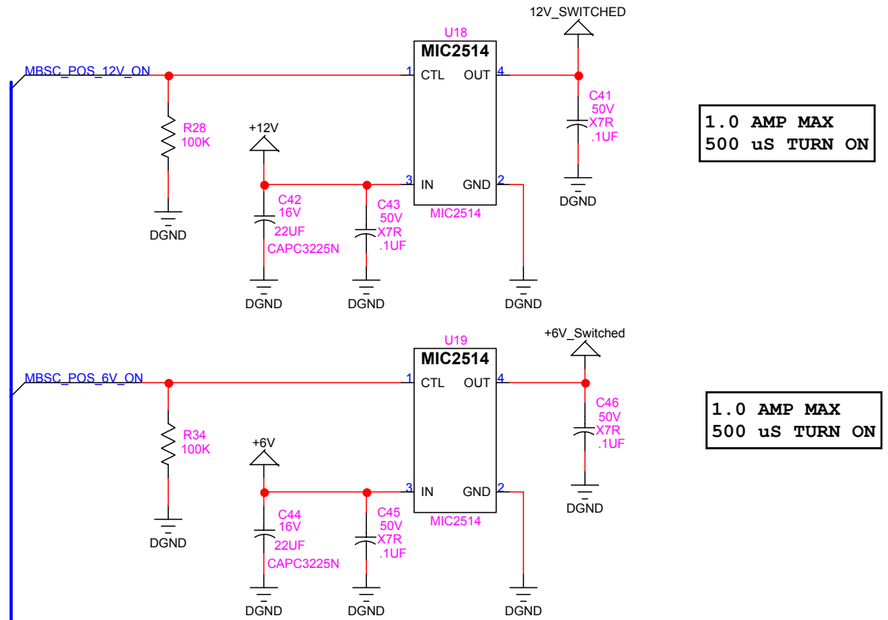
INSTRUMENT POWER CONTROL





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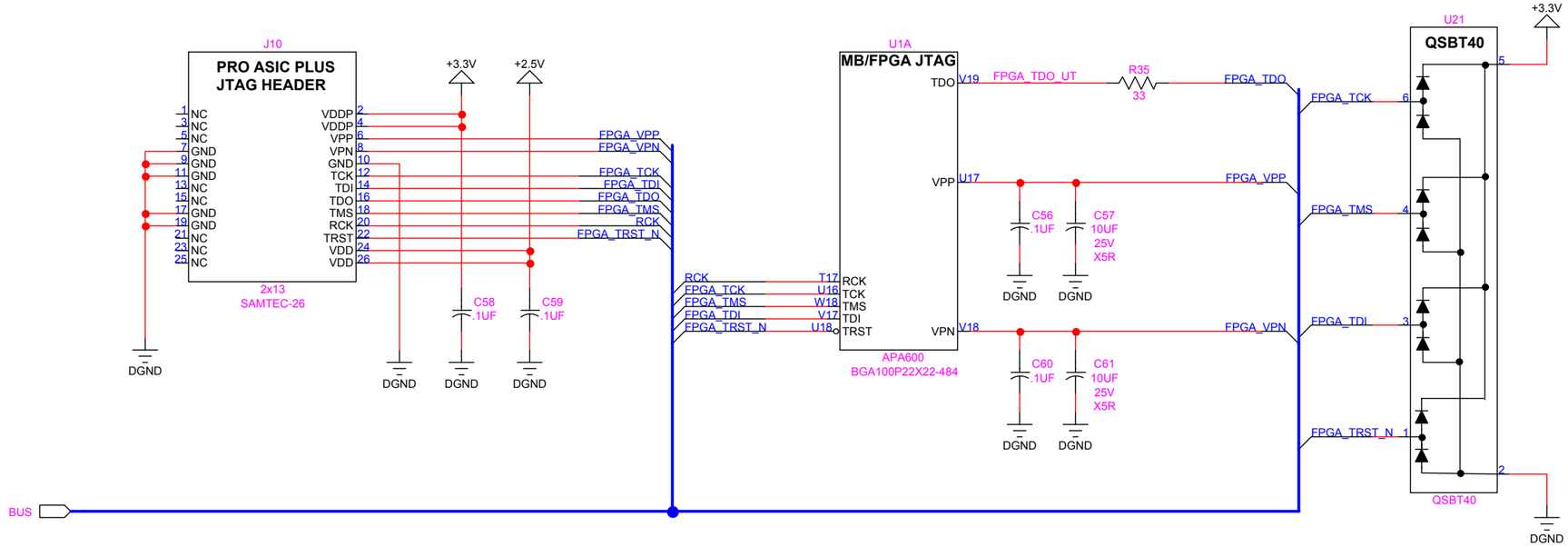
FPGA PROGRAMMING INTERFACE



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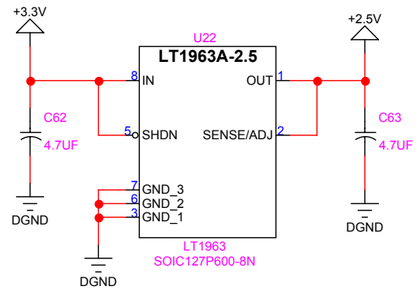
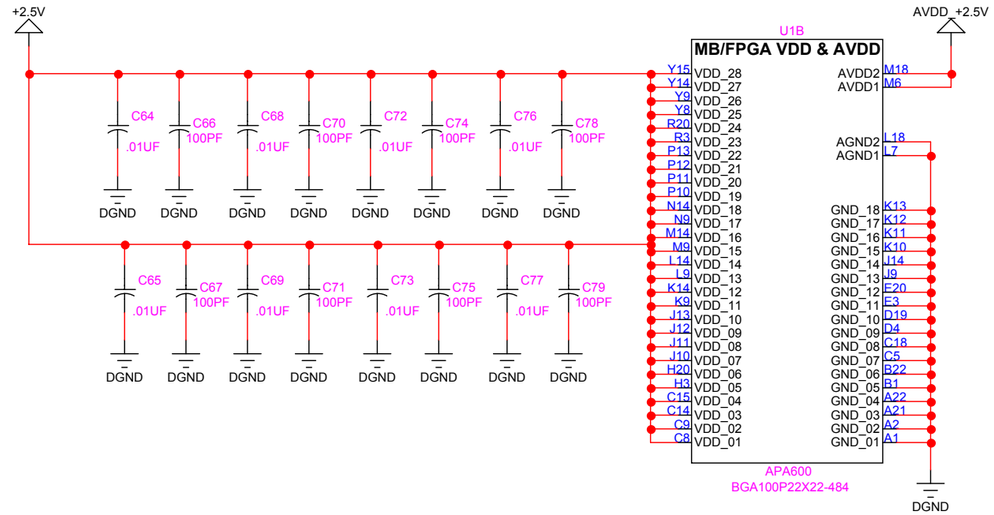
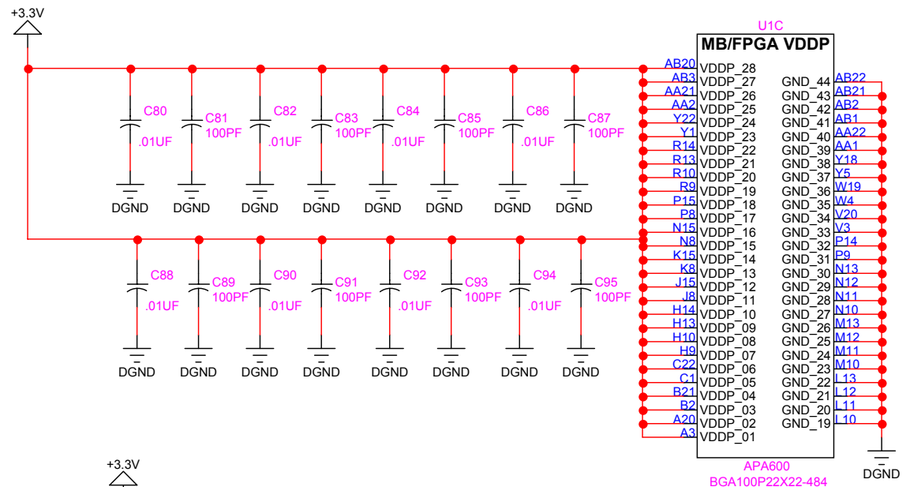
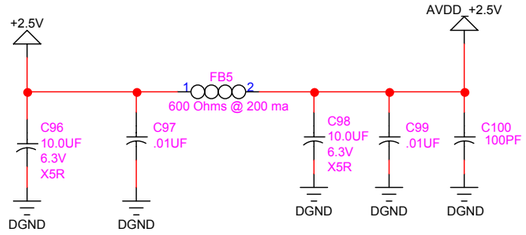
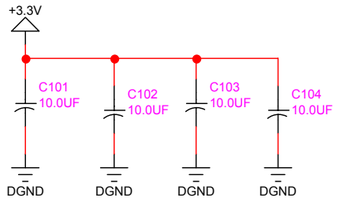
FPGA POWER DISTRIBUTION











BULK BYPASS FOR APA400
PLACE ONE 10UF CAP ON
EACH SIDE OF APA400 PKG.

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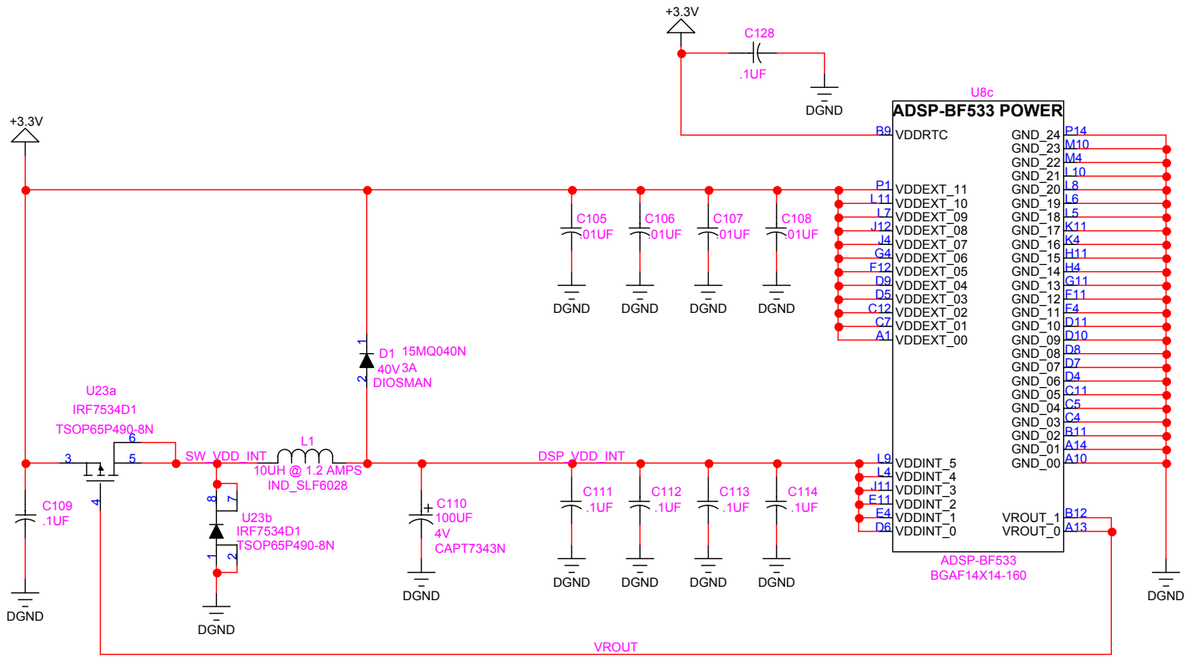
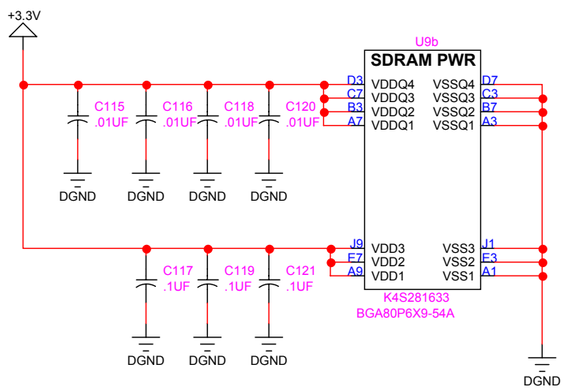
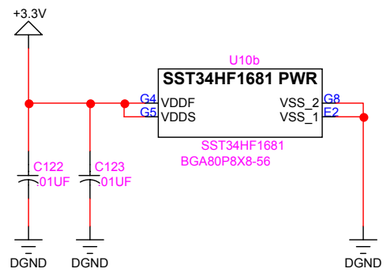
DSP POWER DISTRIBUTION







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