Physics of Failure
As an Integrated Part of Design for Reliability

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SUMMARY & CONCLUSIONS

As part of a UK DTI collaborative funded project developing a holistic methodology and assessment model for the enhancement of electronics reliability, a study into the use of Physics of Failure (PoF) methods was undertaken. It was conducted by reviewing the use made of PoF techniques by the partners and specifically by undertaking a of a number of case studies. It is concluded that PoF methods, and particularly life modelling, are an essential tool in design for reliability. PoF analysis can also be used in establishing reliability enhancement testing (RET) and environmental stress screening (ESS) conditions. A guide for the effective use and inclusion of the PoF methods into product design and development process has been developed and described. The techniques offer benefits in getting a design right first time, thereby avoiding redesign and retest cycles, with consequent cost savings and reduced product development times. The PoF method has limitations associated with the fact that it is essentially a bottom up approach assessing time to failure due to known failure mechanisms. It is consequently difficult to apply to full systems, has limitations in assessing failure rate prior to the onset of life limiting wear out, and is dependent on identifying, and having a validated model, for all potential failure mechanisms.

1. INTRODUCTION

Traditionally all high reliability electronics was designed and developed to a methodology prescribed by Military Specifications that was not firmly scientifically based and has been increasingly questioned. The standard reliability improvement approach of test, fail, analyse, and fix is no longer affordable and the use of handbook part count methods for predicting service reliability has been largely discredited. More scientific based reliability practices were demanded and the methods propounded are generally referred to as Physics of Failure. Among the leading protagonists of the "new" methods is CALCE EPSC, at the University of Maryland, and they have developed methodologies and software models to support the approach. A number of leading electronics manufacturers and users have been involved in a UK DTI funded project, named REMM, with the object of developing a holistic methodology to enhance product reliability, and a model to assess the service reliability of a product at various stages of its life cycle. As part of this collaborative project a study was undertaken into the part Physics of Failure methods can play in the overall design for reliability process. This included the conducting and review of a number of case studies using the CALCE PWA life predicting software. The results of these case studies and the overall conclusions of the whole study are reported in this paper.

2. ACRONYMS AND ABBREVIATIONS

UK DTI UK: Government Department of Industry.
REMM: Reliability Enhancement Methodology and Modelling.
CALCE EPSC: Computer Aided Life Cycle Engineering Electronic Products and Systems Consortium (University of Maryland).
SEU: Single Event Upset.
EOS: Electrical Overstress.
ESD: Electrostatic Damage.
CTE: Coefficient of Thermal Expansion.
CCA: Circuit Card Assembly.

3. THE PHYSICS OF FAILURE METHOD

What is meant by Physics of Failure in reliability?

- It is a methodology that enhances reliability by addressing the root cause mechanisms and driving forces responsible for equipment failures.
- In particular, modelling failure mechanisms and understanding the application environment so failures that will occur within the required service life can be predicted and eliminated from the design.

Excepting software and system design faults all equipment failures are due to the physical failure of an element of the system and should be capable of being explained by a physical or chemical process or combination thereof. Understanding each individual physical process, and the environmental and operating loads that drive the process, it should be possible to develop a model based on the physics of the phenomenon.

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For electronics this requires a detailed knowledge of the structure and materials of the devices, board, module and unit assemblies. The task is greatly extended by the complexity of modern day electronics, and the large number of different parts used, which are largely proprietary to different manufacturers.

4. HISTORY OF PoF MODELS

In the past the Defence and Aircraft Electronics industries have relied on military standardisation when acquiring systems and equipment, prescribing the use of military specifications and components rather than best commercial practices. These design and reliability practices were often not firmly based on engineering science or physics, created a need for costly test, analyse and fix programmes to ensure improve reliability, and inhibited the use of state-of-the-art, low-cost components. They were best practice when they were developed, but today the methodology and practices are outmatched by the rate at which product technology, together with modelling and simulation, is advancing. Additionally, the declining proportion of the market dedicated to high value electronics and the project demands for reduced product development periods, means that the emphasis on prescriptive testing programmes is no longer affordable. Modern reliability technologies use modelling and simulation techniques and are based upon engineering science.

The current interest in a 'Physics of Failure' approach to electronic reliability is not a new phenomena, rather it is simply, the next logical step in an orderly progression delineated years ago. The PoF approach to electronic reliability actually has a long and colourful history.

An early major contributor to this effort was the Electronic Component Reliability Centre (ECRC) at Battelle Memorial Institute in Columbus, one of their principle contributions was the Reliability Physics Notebook written under contract to Rome Air Defence Centre (RADC) and published as RADC-TR-65-330. It described "Results of physical and chemical investigations of processes in materials which cause or contribute to degradation, ageing and failure of electronic devices." The 1965 document outlined three stages of model evolution:

"Early Models - empirically based, derived from experimental data according to statistically defined goodness-of-fit criteria. An example is the stress-strength interference model. Reliability in this model is defined as the probability, 'P', that no stress will be encountered that exceeds the device's strength. The models are generally not used to determine how long a device will operate satisfactorily."

"Current Models - permit at least a partial theoretical interpretation of the physical process, even though these models are generally derived empirically. The form of the mathematical models not only includes operating time but also the environmental stresses as parameters."

"Future Models - will be based upon physical theories of rate processes. The important expected advantage of future models over existing models will be their utility in the initial device-development stages in generating 'optimum' designs as a function of reliability, desired input-output characteristics, material properties, design configuration, manufacturing processes, etc."

From this brief historical sketch it would appear that the "Physics of Failure" models currently being advanced, are simply the third generation models delineated back in 1965. The early focus of the physics of failure studies tended to be static models of electro-chemical failure modes based upon material and process device defects and accelerated by temperature. They did not include mechanical wearout failure modes of components or the interconnection technology, specifically solder joints. Part screening to precipitate out these device defects was one of the major tools utilised to deal with such defects. With the vastly improved manufacturing processes and the successful resolution of the majority of these early solid state circuit reliability limitations, orders of magnitude improvement in device reliability and life have been achieved over the intervening years. Thus, it is only natural then that we now move into the third generation, dynamic, 'rate of process', Physics of Failure models.

5. STEPS TO MEETING PRODUCT RELIABILITY REQUIREMENTS

The process to achieve reliability requirements can be divided into four fundamental steps.

(1) Understand the application environmental extremes, life cycle environment and life and reliability requirements.

(2) Ensure each component part and assembly can survive and function over the whole application environment.

(3) Ensure every part's construction and assembly technology has the capability to meet the life requirement subjected to the life cycle environment.

(4) Assess probability of failure within the desired life and review and amend design and manufacturing methods to minimise this probability

Step 1. If any analysis is to be undertaken it is essential to obtain from the customer the life required of the product, both in terms of operating hours and storage or elapsed time and any combination thereof. The failure rate that can be tolerated during this life must also be known and may be specified by the customer or calculated from a warranty cost calculation. It is also essential to agree with the customer the whole life cycle environment for which the product will be designed. This will be substantially different from the operating environment limits as for most applications the extremes are rare occurrences in the product life cycle. The number and rate of thermal cycles is as or more important than the typical range of temperature experienced.

Steps 2 and 3 Having agreed the requirements, testing and or analysis can be used to ensure that the equipment fully operates at the extremes of the environmental range and will not degrade to the point of failure during the operating and or storage life under the life cycle conditions. It is at this stage that PoF modelling offers great benefit. Note, that environmental conditions cover all stress conditions, including more obscure parameters such as atmospheric radiation.

Step 4 The last step is the most difficult, requiring a process for assessing the probability of failure within the service life, in which the equipment supplier and the customer has confidence. The assessed failure rate can then be

compared with the specified or calculated required rate and if needed steps can then be taken to minimise the probability of failure. Except for design faults, failures in this category are due to errors or defects, which constitute latent faults built in during some stage of manufacture, either at part suppliers, sub-contractors or during assembly and test.

6. FAILURE MECHANISMS OF ELECTRONIC ASSEMBLIES

Although frequently not followed, the steps described in section 4 appear obvious, but a difficulty with electronics is the multitude of mechanisms by which electronic assemblies can fail.

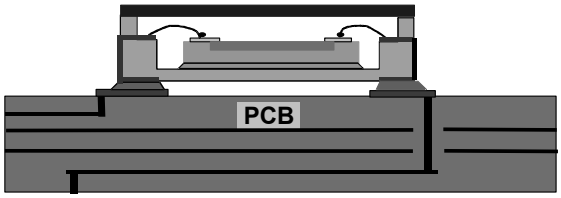

Figure 1 Schematic cross section drawing of device mounted on PCB

Figure 1 shows a schematic of a device mounted on a printed circuit board, showing die attach, the wire bond between die and internal package metallisation, the cavity package with hermetic seal, solder joints between the external metallisation of the package and board and interconnecting tracks within the board itself. Any of the above mentioned can degrade and cause a failure. Add to this the many ways in which the device itself can fail, the failures associated with interconnections from board to board within the unit, and external input and output connections and the extent of the problem becomes apparent.

However excepting design faults of some sort there are only two ways in which an element in a product can fail,

(1) due to overstress and (2) by wearing out.

Overstress is related to design marginality at the environmental extremes, or operation outside those extremes, while wear out is a life degradation effect. Extended exposure to a stress reduces the strength of an equipment element to a level below the stress seen in normal operation with cresultant failure. Examples of both failure types for electronic assemblies are given in Table 1.

Failure Mechanism			
Overstress (Environ. Extreme)		Wear out (life)	
Mechanical	Yield, Fracture, Delamination	Mechanical	Fatigue, Creep
Thermal	Glass transition	Thermal	Diffusion voiding
Electrical	EOS, ESD, Dielectric breakdown	Electrical	Electro-migration, Conductive filament
Radiation	SEU	Radiation	Embittlement Charge tapping
Chemical		Chemical	Corrosion, Dendrites, Intermetallic growth

Table 1 Examples of Overstress and Wear out failure mechanisms

Handbook part count reliability prediction methods were accepted for so long because, up to fifteen years ago, the predominant cause of equipment faults was device failure, and this masked other mechanisms. The explosion in the use of electronics, and the volume in which devices are now manufactured, necessitated a much better process control, and as a result devices have not been the major cause of failure for some years. The major cause has now become interconnects, in particular solder joints and other assembly defects. Despite this, to fully analyse the reliability and life of an electronics design, all the possible failure mechanisms and their driving forces have to be identified and considered. Models for time or cycles to failure have been developed for many mechanisms both at the device (Ref 1) and assembly levels (Ref 2).

7. CASE STUDIES

In order to demonstrate how the PoF modelling technique can help in reliability assessment of electronic assemblies, specific case studies involving the simulation of thermo-mechanical properties, failure mechanisms and life prediction of a real electronic board assemblies has been undertaken by REMM partners. The results of three such case studies are summarised in this section. The simulation models are based on PoF deterministic models.

7.1 TRW Loughborough University Case study

The PCB assembly used for the first case study was a digital electronic board assembly provided by TRW and the analysis was conducted by Loughborough University, (Ref. 3), using an early version of the CALCE PWA software. The processor board assembly was sandwiched between an analogue and a power supply board, mounted inside the electronics module of a civil flight systems actuator. The CCA consisted of a 7 layer, 1 oz copper, FR4 board with devices mounted on one side; some of which were lead-less ceramic chip carriers. The assembly had a known service solder fatigue failure mode.
Thermal analysis, Vibration analysis and Fatigue life modelling were conducted for the purposes of assessing the reliability of the assembly.

Prior to any analysis a model of the board construction must be created, requiring knowledge of the materials, layer thickness and material properties. The early version of CALCE PWA used in this study required all components to be added by hand. Component materials thermo-mechanical properties and power levels are also required. The software provides a database that contains the physical properties of many common electronic materials.

Thermal simulation was conducted to determine the temperature distribution over the board, and a vibration analysis, using application input levels, was conducted to provide an input to the fatigue model. The reasonableness of the thermal and vibration assessments was confirmed by measurements of board temperatures and resonant frequencies during development testing.

The solder-joint fatigue assessment was conducted using the software fatigue assessment module. The aim was to predict the time to failure for specific components subjected to thermal and vibration loads experienced during service life and compare to the known failure mode.

Fatigue Analysis Results

Computations of the life of the board, its components and interconnects were made for both the thermal and vibration fatigue failures, and the combined effects of the two were assessed. The operational ambient temperature variation was significantly higher than that predicted from the board power dissipation but the effects were added to get the overall thermal cycle range. Two different ambient variations were assessed. The first temperature range of –20°C to 60°C represented the operating condition of the board assembly, while the second represented the qualification condition having a temperature range of –20°C to 120°C.

The results from the solder-joint fatigue simulation are presented in cycles to failure for corner solder joints, as these experience the highest fatigue stresses. The predicted cycles to failure were very dependent on an empirical factor but the software correctly indicated the failure sites observed in service. Taking CALCE advice on the empirical factor to use, the cycles to failure predicted were of the right order of magnitude. In this application the predicted vibration fatigue life-time was orders of magnitude higher than the thermal fatigue, indicating that thermal fatigue is the primary loading. As a result of the considerable mismatch between the CTE of the ceramic leadless component and the board materials, thermally induced displacements at the solder joints produce a complex cyclic stress and strain distribution at the solder joint, resulting in crack initiation and propagation.

The first-order fatigue models predicted very low fatigue life cycles for the leadless device compared to the leaded components. Adding leads to the LCC device was predicted to give large increase in cycles to failure, from less than 100 to more than a million under the test condition and the service issue was resolved using this solution.

A comparison of the fatigue results with the field failures (not shown for confidentiality reasons) of the board assembly shows that the first-order fatigue simulation models predicted ultra conservative life cycles for leadless devices, while over predicting life cycles for the leaded device. However the fatigue simulation models accurately predict the failure sites and the trend of failures as observed in the field.

7.2 BAE SYSTEMS Case Study

As with any new software an initial 'learning' period is required before productive use can commence. A case study was undertaken to compare the vibration characteristic predictions of CalcePWA, manual calculation and actual results to validate the software.

The board chosen was a prototype production board (Fig 2). The main criterion for selection of the PCB was that it should be of a regular shape and average complexity avoiding the excess time needed to enter an extremely complicated board.

Due to the complex modelling performed by the software, a large amount of information was required to gain accurate predictions. The gathering of the individual component information from manufacturers web sites had to be searched, datasheets read and data entered into the software component database. Each modelling parameter (vibration and temperature) also required entry to reproduce the load that the board is expected to see in its working life. This information is used to predict the failure modes of the physical board.

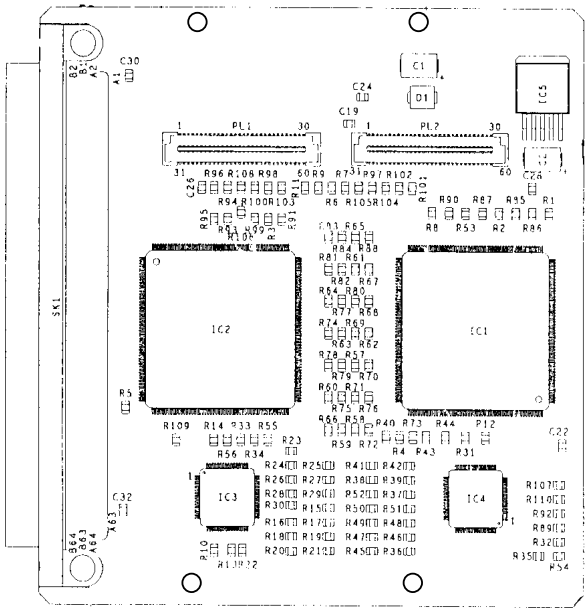

Figure 2 BAE SYSTEMS Board used for vibration analysis

Finding and loading the data required can take considerable time dependent on the operator and skill level. It is expected that as 'educated' guesses and judgement are required throughout the process, the operator should be of a competent level, either through education or experience.

The next step was to accurately select the fixing conditions that would remain constant throughout simulation and test. As can be seen from Figure 2 the board is to be fixed by 4 single point clamps on the top and bottom edges, spaced approximately at the ¼ and ¾ points.

Two versions of the CALCE PWA software were used in the trial but both require the masses of the components to be inputted, but only the masses for the two largest IC's i.e. IC1 and IC2 could be located. However the later version of the software used in this study has the ability to use component volume and material density to calculate a value so this was used for the remaining component weights.

Initially problems were encountered using the advanced vibration engine. The auto-mesh facility generated errors, so a uniform grid was selected. This affected the Finite Element Mode (FEM) generation, which in turn generated results which were not even half of the frequency value expected when analysed. The uniform grid was cleared and the error caused removed so that the auto-mesh command could execute properly. The resulting values were closer to what was expected. To increase the accuracy of the results the exact X-Y co-ordinates of the point clamps were measured and entered to ±1mm. Other factors that affect the results are; solder joint height, lead geometry and lead material. If the predicted results are not as expected the aforementioned values should be checked.

An empirical damping factor, specific to board type, also had to be entered and using the value recommended by CALCE resulted in fairly accurate predictions.

The actual test was executed and compared to the predictions from both versions of the PWA software and the manual calculation using the % error formula as given below:

$$\%\,error = \frac{actual - calculated}{actual} \times 100\%$$

	PWA2std	%error	PWA3std	%error	Manual	%error
1st harm	284	5.5	256	5.5	330	22
2nd harm	360	10	312	5.5	n/a	n/a
3rd harm	663	50	329	25	n/a	n/a

Table 2 Comparison of resonant frequencies predictions

The results from the software and the manual calculation and are shown in the table 2. As the first natural frequency is usually the only one required, the manual calculation was only performed for the first natural frequency.

The worst case displacement is approximately 3 thousandths of an inch. It can be seen from the above table that the greatest % error for the most important natural frequency (1st) arises from the manual calculation. This is to be expected, as the engineer would have made some assumptions when performing the calculations.

It can also be seen that the greatest % error between the actual and the CalcePWA software occurs at the 3rd natural frequency (50% PWA2, 25% PWA3). A possible reason for this could be a rounding error, as the displacement being dealt with is so small any rounding taking place within the software could have dramatic effects. This is viewed to be satisfactory if the effects from the 1st and 3rd harmonics are not cumulative.

It can also be seen that an awareness of the expected answer is required, as several factors that seem insignificant at the time have a drastic impact upon the final result. Therefore it is beneficial to know when the answers are in the right area.

It was concluded that the PWA software prediction of the prototype production board is approximately accurate to the actual results produced (5.5%) and considerably better than the manual calculation (22%).

It was also concluded that there was a significant inaccuracy at the 3rd natural frequency, however, this is not thought as important as the 1st natural frequency (see discussion).

It can finally be concluded that the PWA software performs accurate predictions, when it is given accurate information.

7.3 TRW Aeronautical Systems Case study

Over the last few years TRW Aeronautical Systems, UK, has made increasing use of the CALCE PWA (1) circuit card assembly (CCA) analysis software in their design and development process. Board layouts can be directly loaded from CAD design files and after adding device power levels and material data, an analysis of the thermal and vibrational performance of the boards can then be quickly generated, many times faster than by conventional FE analysis. This allows device positioning, board stiffening and supports, and thermal management features to be amended or added manually. Using the life cycle thermal and vibrational environment the software can then be used to predict the life of the various solder joints.

In order to provide confidence in the output from the models embodied in the software a number of validation exercises have been conducted and two are described here.

Vibration Analysis

The vibration performance of the multi-layer through-hole power conversion card shown in Fig 4, was analysed. The CCA had a copper heat plate on the device side, surface mount chip devices on the solder side of the board and was supported on two sides by edge clamps. The two flying lead connectors offer little support, but the handle provides some stiffness to that edge.

A major difficulty when analysing such a board is to select the most representative boundary conditions, as this has a major effect on the resonant frequencies and displacement predicted. Edge clamps are classed as fixed supports and the best results were found taking the board edge as the line of overlap of the clamp. Representing the handle as a stiffening fixed or simple support gave a less accurate result than simply representing it as a component mass.

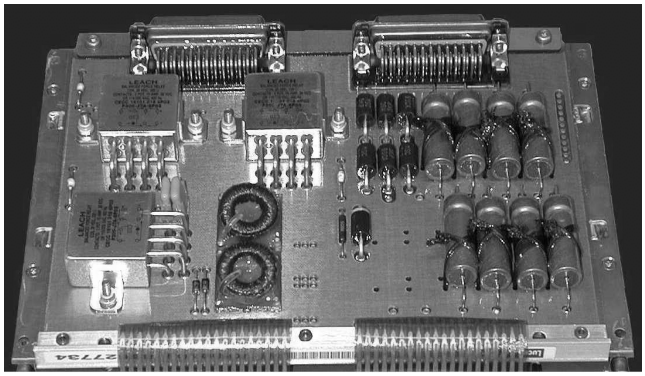

Figure 4 Power conversion card

The results of the analysis are shown in Table 3, which compares the frequency and displacement predicted and measured and Figure 5, which shows the first order resonant mode shape.

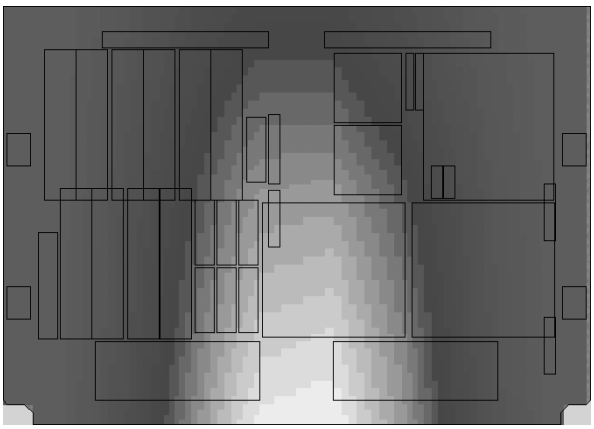

Figure 5 Predicted primary vibration mode shape

After using the boundary conditions, as discussed above, the correlation of predicted to actual resonant frequency was good. The displacement was found to be more difficult and very dependent on the empirical board-damping factor that has to be arbitrarily fixed, based on experience and testing. Experience has shown that for this type of board a factor of 0.05 gives a close correlation, as indicated in Table 3.

	CALCE PWA Prediction	Measured Value
Resonant Frequency (Hz)	160	158
Displacement (thou)	10	11

Table 3 Comparison of predicted and measured primary vibration resonance mode

Solder Joint Fatigue

TRW has a long history of using surface mount technology in the harsh environment of engine controls. Over that period it has amassed a lot of test results and service history on the life of solder joints made to a range of devices, but in particular to leadless chip carriers. These results have been used to validate the latest CalcePWA joint fatigue model. The boards evaluated were two standards of double sided surface mount boards designed for ceramic leadless chip carriers. Both included dual copper clad invar constraining cores, resulting in a CTE of between 6.0 and 6.5ppm/°C (matched to alumina) for one board, and 10.5 to 11.5 ppm/°C for the other.

Test results available are for a one hour temperature cycle ranging from –45°C to 100°C, which it has been found can be correlated to the number of flight cycles seen by a civil engine control. A factor that has to be considered in joint life prediction is the height of the solder joint. A solder joint fatigue analysis was conducted for a 44 lead chip carrier on both standards of board and compared to the known test values of cycles to failure. Another empirical fatigue factor has to be used in the model dependent upon the package type.

Solder joint height (mil)	Predicted cycles to failure
2	3687
3	4195
4	4414

Table 4 Effect of solder joint height

The effect of solder joint height on the prediction was computed for an 11ppm/°C board and the results are shown in Table 4. As expected the joint height has a marked effect on cycles to failure with increased height giving longer life. The sensitivity of the prediction to board CTE was investigated and the results are given in Table 5, for CTE between 10.5 to 11.5 ppm/°C, indicating the necessity to control the manufacture of the boards tightly.

Board CTE ppm/^{o}C	10.5	11	11.5
Predicted cycles to failure	4936	3687	2840

Table 5 Effect of board CTE

Table 6 compares the predicted cycles to failure with the number of cycles found on test. Test failure was determined both visually and by continuity measurement. Testing of the well-matched board was stopped at 7,500 cycles with no sign of impending failure. Inspection of very old boards from service confirm that the solder joint life for well matched boards, (within 1ppm), is well beyond 15,000 cycles, but nothing like the near to infinite cycles prediction produced by the model, when the board and component CTE are set equal.

	Predicted cycles to failure	Test cycles to failure
10.5 to 11.5 ppm/^{o}C	2840 - 3687	1600 - 2200
6.0 to 6.5 ppm/^{o}C	850,000 – 10,000,000,000	>15,000

Table 6 Comparison of predicted and test cycles to failure

These latest results for fatigue life predictions using the recommended empirical factor are somewhat optimistic for the higher CTE board using actual values of the solder joint height. This suggests that we should contemplate adjusting the factor to give a more accurate answer in future analyses. However TRW believe with careful interpretation, that the prediction for the leadless joints can now be relied on, and the model definitely indicates the areas of concern. The model is still very optimistic for assemblies where the CTE matching is very good.

8. PoF IN THE DESIGN PROCESS

8.1 As a Design Tool

The objective is to improve the reliability of a component, module or Line Replaceable Unit by understanding and analysing the physical phenomena and mechanisms by which products fail. As a design tool it can be used for identifying and mitigating risk to reliable operation or life enabling engineering based design options and for design justification.

Up front failure analysis of products such as CCAs, Modules, and Components can dramatically reduce cost of ownership, increase product reliability and thus reduce risks.

To fit into the design process, the failure assessment software must have a high level of information sharing between electrical and mechanical design tools. This process can be used for initial design and redesign of products, following the flow diagram below illustrates the paths which have to be considered when applying the PoF process. This leads to a better understanding of failure mechanisms by using PoF modelling techniques, applies virtual qualification, and reduces levels of reliability testing, test time and development costs. This process enhances the chance of the product design being right first time, (passes qualification testing), and enables a mature and reliable design at entry into service.

This PoF technique has been included within the REMM process and includes a flow diagram, Figure 6, and guidance for effective use described in Section 9 of this paper.

8.2 Reliability Enhancement Testing (RET)

Failure assessment models are used during virtual qualification studies to determine how the product will react under high load conditions, and to map the outcome of the test conditions to product performance in the actual use condition. Failure models can be used to help determine conditions and product fixturing necessary to excite only the relevant failures. It can ensure overstress conditions are avoided and indicate sensible test times. It can also be used to warn of failures that may occur only as a result of the accelerated test conditions.

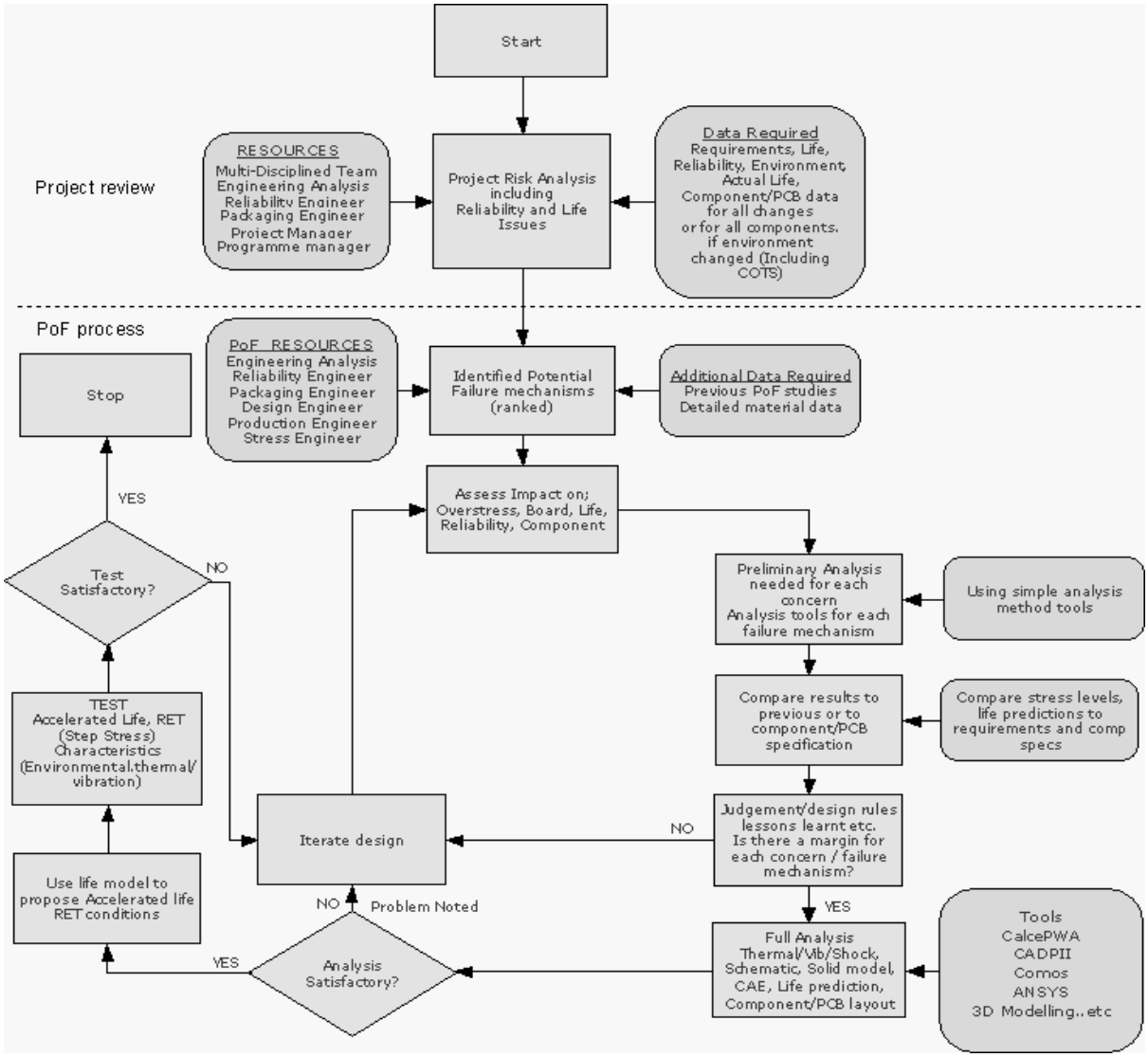

Figure 6 PoF Technique

8.3 Environmental Stress Screening (ESS) Testing

The use of failure assessment models is critical to product screening. Screens are used to remove products that would fail earlier than expected due to manufacturing defects. Screening involves examining the product during or after manufacture to find the types, locations and severity of flaws introduced from the manufacturing process. Screens can be carried out by product inspection and/or stress based screening methods. To apply a stress screening, it is necessary to know what failures result from defects in the product and how the application of external loads can precipitate failure of flawed products. Failure models help in this area by providing time to failure estimates based on material, geometry and load conditions. A manufacturing flaw may be represented in an inappropriate geometry and/or a changed material property. Applying this information to the failure assessment process allows us to determine if a stress-based screen is viable.

8.4 Life Consumption Monitoring (LCM)

The use of failure assessment models allows for the development of guidelines for equipment monitoring (LCM) and devices to provide early warning for imminent equipment

failure. By understanding, the type, location and severity of the failures in the electronic product, stress may be monitored allowing for estimates of useful remaining life.

9. GUIDANCE FOR THE USE OF POF IN DESIGN FOR RELIABILITY

REMM concluded that PoF methodology is an essential part of design for reliability and developed a guide summarised below for its effective use, supporting Figure 6.

- Programme manager buy in is essential to establish a multi-disciplined PoF team, including part time specialists. All should attend a project reliability risk assessment at an early stage of the project. A structured brain storm approach can initially be used followed by a more detailed elicitation with individual designers and specialists. Concerns are targeted at new design aspects or changed environment.
- Data on the reliability performance of previous similar designs and material data, particularly on the new aspects of the current project, must be available.
- Tools and expert practitioners must be made available and these include standard tools, such as Finite Element thermal and stress analysis, as well as PoF specific failure modelling software.
- System and installation impacts must be considered as these can greatly influence the reliability and life of a line replaceable unit or equipment.
- The PoF team should collectively assess the impact of the identified risks and prioritise the preliminary mitigating actions. These may involve accessing existing data from various sources, undertaking preliminary analysis or modelling, preliminary testing or a combination of these.
- The team using comparisons to previous experience and the expertise available reviews the preliminary results. A judgement must be made to decide if the element of the design is acceptable, a full assessment is required, or the reliability risk is unacceptable.
- If the conclusion above or from the full assessment is unacceptable then design iteration is recommended and the whole assessment process repeated.

10. EFFECTIVENESS AND LIMITATIONS

This paper has shown how the use of PoF techniques is an essential element of a design for reliability methodology. It is applicable specifically to the features of a design from components to assembly methods and technology that are new to the to equipment supplier or when understood features are being used in an environment outside that for which previous service history or data is available. Effective use of the methodology will yield many benefits including.

- Getting the design right first time, eliminating redesign and re -test cycles.
- Identifying more effective accelerated life and RET test regimes
- Yielding significant cost and development cycle time reductions
- More effective Environmental Stress Screening (ESS) regimes targeting known causes of failure will reduce infant mortality and life time failure rates.

However the methodology has limitations that should be recognised.

- Essentially a “Bottom Up” approach and therefore difficult to apply to systems.
- Obtaining all the material physical properties data required and the life cycle environmental conditions is not easy.
- Dependent on identifying all risks and failure mechanisms and any risks identified with no known life model or algorithm can not be analysed.
- Modelling assesses time or cycles to failure and can not easily provide a failure rate prior to the onset of normal wear out.

Failure prior to normal wear out are driven by manufacturing defect or error rate at some stage in component or board manufacture, assembly, or test.

The case studies have shown the modelling software has reached the state of development that it can be very effectively used in standard design processes to provide the benefits identified.

ACKNOWLEDGEMENTS

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Jane Marshall has been employed at TRW since 1991 as a reliability statistician. Before joining Lucas she was a lecturer in statistics at Nottingham Trent University where she was involved in external reliability courses and consultancy. At TRW she has been involved in many aspects of reliability including; Prediction; FMECA; FTA; reliability testing and data analysis on aerospace and automotive products. She was project leader of a jointly funded research project with the University of Strathclyde investigating reliability Growth Modelling. She has a Ph.D. from Loughborough University entitled 'The organisation and statistical analysis of an electronic component field failure database' and is a British expert on IEC TC56: WG2. She was project manager of REMM.

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Ian Snook is currently employed at BAE SYSTEMS, Waterlooville, as ARM and TLC Group Manager. He has been employed at BAE Systems since 1977 as a engineer and as a Reliability Engineer from 1982 to present as group manager, during this time he studied at Nottingham Trent University to obtain a Master of Philosophy in Reliability Engineering.
At BAE he has been involved in many aspects of reliability including; Feasibility, Definition, Development and In-Service phases, Prediction; FMECA; FTA; reliability growth, R&M Demonstration, ESS testing and data analysis on Underwater systems products both in-house and Off-site for other sites.

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Bob Newman graduated with a 1st Class honours degree and has a doctorate on Dielectric Thin films (1971). Held a number of positions in the Microelectronics Hybrid Circuits group at TRW having responsibility for electronic packaging for harsh environment and led an MOD funded programme into the use of surface mount technology in engine controls. He became Process Engineering Manager in 1984 and continued in similar positions until 1995 when he was appointed Technology Consultant Electronic Packaging reporting to the Chief Engineer Electronics TRW Aeronautical Systems.