A Low Power Imaging and Obstacle Avoidance Sonar for Small UUVs

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Abstract-Teratech Corporation is developing an electronic-sonar system for imaging and obstacle avoidance to be integrated into a low power, compact marine vehicles. This sonar system will switch between 2D imaging and 3D obstacle avoidance using a dual purpose planar array. The system incorporates a low power design to preserve the vehicle's ability to conduct extended range missions. The capability of the sonar is a result of the development of application specific integrated circuits based on Teratech's proprietary Charge Domain Processing (CDP) technology. The intended application is for reconnaissance in shallow and very-shallow waters.

I. INTRODUCTION

As smaller and more maneuverable UUV's are developed, the demands on forward looking sonars are increasing at a pace that is more exponential than proportional to the size reduction. The smaller UUV offers less space for acoustic arrays, less room for electronics, requires the sonar to use less power, and demands higher resolution and frame rate to avoid obstacles with the smaller, more maneuverable vehicles. The smaller sonar arrays are operating at frequencies ten times higher than the larger UUV. Because of the increased absorption losses at higher frequencies, detection ranges are shortened and vehicles are operating closer to the bottom to find and classify targets of interest. Teratech has been addressing these needs by extending the application specific integrated circuit (ASIC) developed for medical ultrasound to the high resolution sonar problem of small UUVs and handheld sonars. While medical ultrasound is short range (1-15 cm) and low power, small UUVs and handheld sonars are required to be effective between 1 and 50 m while maintaining reasonable frame rates when round-trip travel times have increased a hundredfold. Also larger aperture arrays are required to maintain reasonable resolution at longer ranges. These requirements have lead to the development of the multi-purpose, dual frequency bistatic sonar system reported here.

II. MULTI-PURPOSE SONAR SYSTEM

Teratech Corporation has been developing a dual-frequency, multi-purpose sonar for use as a handheld diver sonar and also as a forward-looking sonar for small UUV's. This sonar used a curvilinear array for hydrodynamic shaping. The design of this array focuses on broadband characteristics to provide the system with a long range detection mode at 750 kHz and a shorter range high resolution mode at 1500 kHz. The curvilinear array is a half-wavelength design centered at 1 MHz. This allows the sonar to operate simultaneously with an AUV side-looking sonar also operating in the 1 MHz range without interference from grating lobes. The total power requirements of the sonar preamp/beamformer and transmitter electronics is 10 watts. A 6"x 4"x 2.6" dry space (L x W x H) is required directly behind the array. In the divers' handheld sonar, an additional seven watts is required for the PIII computer, which provides system control and data recording functions and four watts of power is required for the diver's head-mounted display. The system's field of view is approximately 50 degrees, consisting of a 64 beam image in the detection mode at 750 kHz and a 128 beam image in the high resolution mode at 1500 kHz. The 64 beam image is formed in two pings and the 128 beam image is formed in four pings.

III. HANDHELD SONAR DESIGN

The primary objective of this research is to design and develop a handheld sonar system that produces high-resolution, two-dimensional images of the region directly in front of the diver. The specifications of this system are detailed in [1].

With this goal, a diver handheld sonar system will be demonstrated in 2003. The system will consist of a 1D curved-linear, 192-element array with beamforming electronics, a PC host controller and a display system, all packaged in a watertight

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housing unit. Prevco Subsea Housing, Palm City, FL will provide mechanical design and construction of a watertight housing. Critical components being developed are: a 64-channel CDP beamformer with apodization and real-time dynamic-focusing coprocessor, and a bank of low-noise amplifiers with programmable gain. The beamforming electronics are being developed based on Teratech's proprietary low-power, high-throughput CDP technology [2, 3]. The CDP architecture enables the development of a powerful and efficient beamformer. The electronic-beamforming output will be connected to the PC through a high-speed IEEE 1394 bus. Due to the fact that this “All-In-One” approach is based on a commercially available PC, it offers the potential of a low-cost, high-performance, compact implementation that is easily upgradeable. Consequently, it also offers a much better potential for an eventual commercial product.

IV. ELECTRONICS SYSTEM

A. Low-Power Electronics

The beamformer electronics will use Teratech Corporation’s patented charge-domain-processing (CDP) technology. The chip set allows all of the front-end electronics through the beamformer to be mounted on modest-sized printed circuit boards that can be completely housed in the nose of the AUV. Because these parts can be produced cheaply and quickly, this approach dramatically increases the reliability of the product and reduces the maintenance cost.

In a CDP circuit, sampled data are represented by analog charge packets; if the information is accurate to 10-bit words, instead of representing it by 10 separate digital bits, each charge packet will represent a 10-bit value, and these charge packets can be manipulated at a high speed with a high accuracy (~9 bit) in a very small chip area. It is well known that a conventional digital implementation offers flexibility and relatively unlimited accuracy. However, the state-of-the-art DSPs offer less than 2000 MOPs/chip and each chip requires two Watts of electric power. An electronic-beamformer with conventional digital signal processors would still require six chips and 12 Watts to perform identical computations as a single CDP beamformer.

As mentioned, charge-coupled devices, CCDs, require less chip area and power. However, in a conventional CCD, signals are nondestructively sensed as current. Clock feed-through associated with this current mode sensing techniques is so large that a high-common-mode rejection amplifier is needed to extract a signal from the presence of clock noise. This limits the dynamic range of conventional CCDs to less than 40dB. Consequently, throughout the past decade, the lack of accuracy, flexibility and programmability of conventional CCDs has turned system developers away from CCD implementations. At Teratech, a proprietary charge sensing technique, which eliminates clock feed-through completely, has been developed. Furthermore, a charge domain multiplier that maintains the output accuracy to more than 8-bits has been invented. As a result, CCD signal processors with more than 60dB output dynamic range have been routinely demonstrated at Teratech.

Furthermore, an extensive CCD cell library including A/D, D/A, multipliers, adders, and comparators has been developed. By combining these high-speed, low-power charge-domain units with conventional CMOS digital control and memory circuits, a new charge-domain processing, CDP, technology has been created. This CDP technique provides programming flexibility similar to the conventional all-digital implementation. This design tool allows rapid implementation of application-specific hybrid CCD/CMOS electronics into operational systems with reduced cycle time and cost. The advantages offered by the CDP technology are summarized as follows:

- Revolutionary, proprietary technology--long product lifetime
- CDP cell library--fast product cycle, Low NRE for ASICs
- Foundry compatible process--low production cost
- Single chip solution eases system integration.

A technology comparison of the proposed beamforming device and the state-of-the art digital

DSPs reveals that the CDP beamformer implementation provides significant advantages in power, weight, and cost [7].

B. Beamforming Electronics

The objective of a beamforming system is to focus signals received from an image point onto a transducer array. By inserting proper delays in a beamformer in order to align wavefronts that are propagating in a particular direction, signals arriving from the direction of interest are added coherently, while those from other directions do not add coherently or cancel. However, as the array is scanning through the imaging plane, there are three difficult implementation issues: first, each delay line has to be long enough to compensate for the path differences of a large linear array; second, the delay value has to be adjusted periodically for proper beam steering; and finally, the long round-trip delays, when performing long-range imaging, must be processed in parallel to provide reasonable display update rates. Ideally, the time-of-flight from the radiation source to the focal point could be calculated at every clock cycle for every channel from multiple directions of arrival in parallel. In a conventional implementation, separate electronic circuitry is necessary for each beam. For a multi-beam system, the resulting electronics rapidly become both bulky and costly as the number of beams increases. A single-chip multiple beamforming processor based on a time-multiplexed delay generation architecture is proposed. The chip combines programmable delays with a sequentially addressable digital delay selection resulting in a compact, low-power implementation of a multiple beamforming processor.

A delay-and-sum beamformer allows a transducer array to "look" for signals propagating from a particular direction. By adjusting the delays associated with each element of the array, the array's look direction can be electronically steered toward the source of radiation. As shown in Fig. 1, the multiple beamforming chip consists of N parallel beamforming modules, a summing circuit and a Finite-Impulse-Response (FIR) filter. Within each module, there is a sampling circuit, a programmable delay line, an apodization multiplier and a bank of delay controls that are sequentially addressable.

In this implementation, the delay control unit within each module consists of a storage buffer containing the differential delays for that channel. The device operates as follows: once a set of sampled returned-echoes are loaded in the N delay lines, at time t_1, the delays required for forming beam 1 are computed within each module and applied in parallel to all delay lines. The sampled return-echoes with proper delays are coherently summed to form the first beam. At time t_2, the delays required for forming beam 2 are computed within each module and applied in parallel to all delay lines. The sampled return-echoes with proper delays are coherently summed to form the second beam. The procedure repeats until the k^{th} beam is coherently formed using the architecture depicted in Fig. 1.

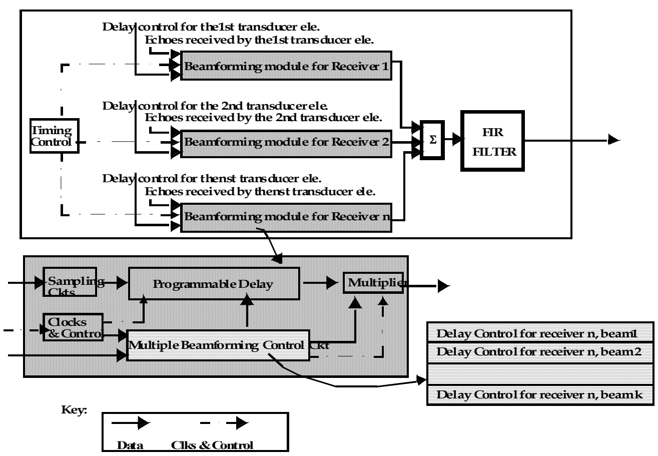

Fig. 1. A block diagram of a single-chip multiple beamforming chip architecture.

V. SYSTEM IMPLEMENTATION

A. Differential Delay

For the 1D curved-linear array, the delays implemented in tapped-delay lines are programmed based on the differential delay relative to the center of the array. For a given image location, the differential delay to any array element, (x_m), is given by (1).

$$f(r,\theta)=\frac{r}{c_o}\left(1-\sqrt{1+\frac{x_m^2}{r^2}-\frac{2x_m\sin\theta}{r}}\right),(1)$$

Here, the average propagation velocity is defined to be c_o. As depicted in Fig. 2, the angular offset is described by the angle θ.

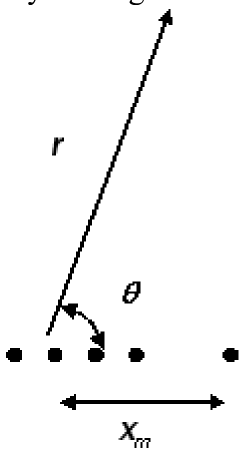

Fig. 2. Steered-linear array geometry.

B. Array Calibration

The final array to be used in the handheld sonar system is being designed and constructed by Material Systems, Inc. (MSI), Littleton, MA, as part of a small-business innovative research (SBIR) program. In the interim, a 64-element linear array, constructed by MSI is being evaluated. This array was chosen because it represents one-third of the final 192-element array that will be used in the final system. The prototype array contains 64 elements. The element-to-element pitch is 0.5 lambda at 1 MHz (0.75 mm); thereby, allowing the array to be steered without introducing significant grating lobes in the received beam pattern. The elements are 9 mm tall with –200 dB//V/μPa sensitivity. The projector elements are capable of 165 dB/V//μPa.

To calibrate the prototype array, the precise time-of-flight from a single-element transmitter to each receive element was determined. By measuring the physical distance from the source to the center of the 1D array, the distance from the transmitter to each element was computed based on the expected element location. In turn, the expected distance was compared to the distance as computed, based on the time of arrival of the transmitted waveform, multiplied by the estimated velocity in water, c_o. The velocity was estimated using the distance measured from the source to the center of the array divided by the time-of-arrival of the transmitted waveform. As a reference, usable estimates of sound velocity based on the temperature of the water were also available.

The single-element transmitter, manufactured by MSI, was placed approximately 3 meters from the front face of the receiving array. A high-voltage, 3-cycle burst was used to drive the immersed transducer. Signals received at each of the 64 array elements were time gated and digitized at 5 Msamples/second. Based on the measured distance from the source to the center element in the array, the water velocity was determined to be 1474.4 m/s. At this data acquisition rate and acoustic propagation velocity, one sample in time corresponds to 294 μm.

Care was taken to position the transmitter directly in front of the center element of the array. In addition, the offset of the transmitter relative to the center element must also be taken into account mathematically. Fig. 3 summarizes the calibration results. The upper pane plots the theoretical (solid line) and measured time-of-flight (+) from the source to each of the 64 array elements in digital samples at the 5 MHz acquisition rate. The lower pane depicts the difference between the theoretical and measured time-of-flight in digital samples. These errors are then used as corrections to the differential delays computed using (1). Although the error correction is most useful for aligning wavefronts in coherent imaging, it is also beneficial to the relative image quality of incoherent imaging where the phase information of the waveforms is lost.

Preliminary results of tests performed on the prototype array from MSI indicate that the physical location of each element was equal to the minimum granularity of the measurement system (+/- 200 ns). The final 192-element array will be comprised of three, 64-element segments that are similar to the prototype. The transmitter will be comprised of 2 elements (one left and one right of center) with overlapping coverage similar to headlights on a car.

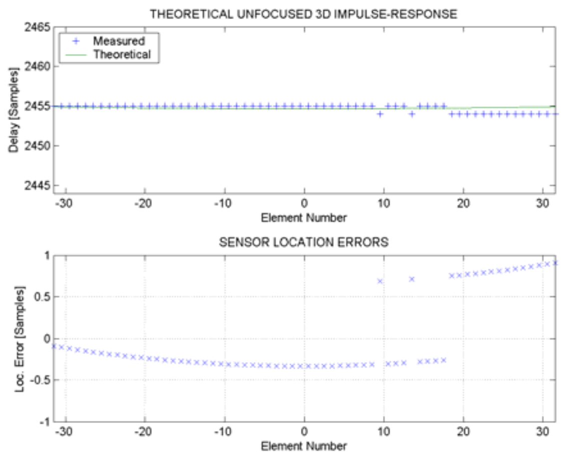

Fig. 3. Theoretical and measured time-of-flight delay for each of the 64 array elements (top), and corresponding errors (bottom) where one sample corresponds to 200 ns delay error.

C. Prototype System using 1D Linear Array

A preliminary design of the diver-held sonar system has been successfully completed. This design includes the overall system block diagram, system packaging, the choice of commercial-off-the-shelf (COTS) single-board computer, system-performance optimization (including the analyses of apodization, or shading, functions and necessary precision) and the characterization of the array response. The IEEE-1394 interface was chosen to connect the COTS computer system to the custom signal-conditioning/beamforming hardware designed and implemented by Teratech. A one-dimensional partial array was evaluated and calibrated at Teratech Corporation.

This real-time sonar image system has been developed using Teratech's proprietary CDP technology to implement electronic-focusing beamformers. The first prototype implements three 64-channel beamformers operating in parallel. Prior to beamforming, each transducer output is amplified using a low-noise amplifier with programmable gain that can be set from 0 to 60 dB. A single, digitally beamformed output is available from the system.

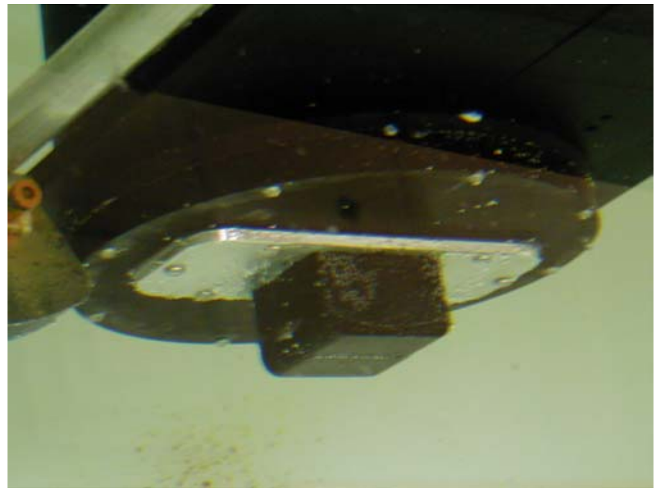

Fig. 4. 2D sparse array sonar board with 128-channel input and 4 parallel CDP beamformers.

To improve the signal response, a wide-bandwidth frequency-modulated (FM) chirp transmit waveform was chosen. The chirp signal is linearly swept in frequency from 1.25 to 1.75 MHz. The duration of the chirp is 50 µs. Acoustic echoes from the target are electronically-beamformed in parallel using each of the 64 array elements to create two-dimensional images in azimuth and range. Data are digitized and then downloaded from the sonar board via a high-speed, IEEE 1394, serial bus. The computer renders the image to the user and provides a real-time display of the image area.

Various test objects have been used to evaluate the system performance. Given the intended application of the sonar system, cinder-block and tire targets were chosen to evaluate image performance. The targets were placed approximately 1-3 meters from the face of the 1D array.

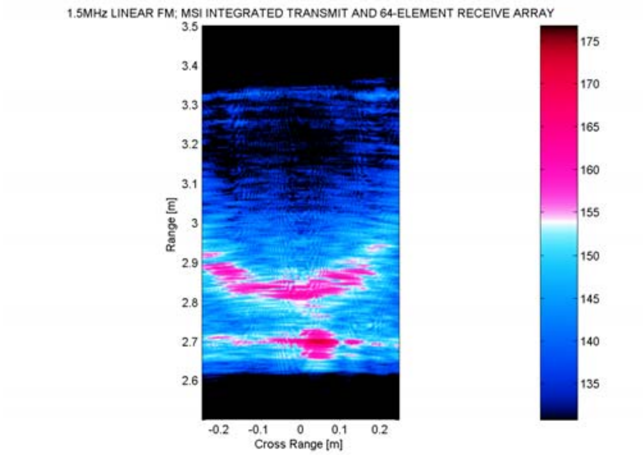

Fig. 5. Acoustic image of a tire sitting on top of chain-linked fence using a red-white-blue pseudo-color map.

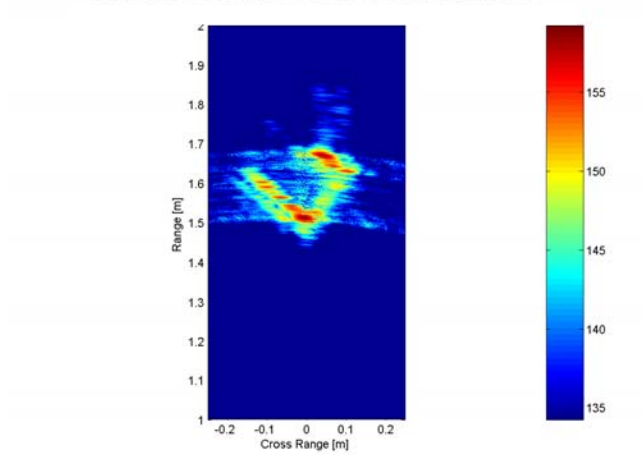

Fig. 6. Acoustic, cross-section image of cinder block using a rainbow pseudo-color map.

Fig. 4 depicts the integrated transmit and 64 element receive array manufactured by MSI. To validate the imaging capabilities of the prototype array, a rubber tire sitting on top of a chain-linked fence were placed on the floor of a water tank at a range of 3 meters. The depression angle was approximately 10 degrees down. At 0.75 mm inter-element spacing, the narrowband angular resolution of the receive array is approximately 1.2 degrees. The angular extent of the targets was approximately 1 meter, thereby allowing at least 15 independent beams to illuminate the targets. An image was generated (see Fig. 5), using a pseudo-color map that was chosen to be similar to that used by Ed Belcher, APL, in the LIMIS [5]. The images, obtained using the 1.5 MHz identification mode, show the front edge of the fence (horizontal line image bottom) and the leading edge of the tire (image middle).

Fig. 6 is the acoustic image cross-section of a cinder block that is rotated 45 degrees relative to boresight. The openings into the cinder block are toward the right-hand side of the image. As with the previous image, the linear FM chirp was used as the transmitted waveform.

VI. CONCLUSION

The current sonar design has focused on imaging with a curvilinear one dimensional array. This system has the highest channel count developed to date with Teratech's Charge Domain Processing technology and has been able to accomplish this with a power budget close to the much smaller medical systems. Because the time-delay beamforming is totally under software control, the same card set for the bistatic 192 element curvilinear sonar could also be used for a 192 element planar array designed for 3D obstacle avoidance. The new generation beamformer ASIC developed for this project increased the number of beams formed by the system from 16 to 32 per ping. It can also accommodate larger steering angles accomplished by increasing the individual beamformer pipelines from 128 samples to 200 samples per channel. This allows the more maneuverable UUV's to lead the FOV and avoid obstacles at higher turn rates in restricted spaces.

Future plans are under development to integrate and test this sonar into a small Remus vehicle and extend the obstacle avoidance capability to 3D.

Acknowledgments

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