A High-Speed Acoustic Data Acquisition System Using Mostly COTS Components

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Abstract - **A data acquisition system has been developed at the Marine Physical Laboratory for recording digitized and multiplexed data from a variety of acoustic arrays and sampling systems. This system is composed of an industrial Pentium III CPU, a GPS time/frequency processor, a gigabit Ethernet interface, a high-speed parallel interface and a custom telemetry interface in a Compact-PCI chassis. A reconfigured version of this system could potentially fit into an eight inch diameter pressure case for autonomous deployment at sea. Control and programmability are provided by LabVIEW running under Windows NT or XP. The combination of the custom telemetry interface and high speed parallel interface provides a flexible, bi-directional channel for multiplexed serial data through coax or fiber at telemetry rates up to 200 MBaud. The custom telemetry interface can be reconfigured for a variety of existing and future telemetry systems utilizing coax and single or multimode fiber. The design of this interface exploits recent transceiver technology that exists for high bandwidth communication applications such as Fibre-Channel and ATM. This commercial technology provides the serializing/deserializing, coding/decoding, bit synchronization and byte framing required for the high-speed fiber link and can be operated synchronously or asynchronously using on-chip FIFOs. Data is recorded by the acquisition system in a standard format that does not require the translation usually required with proprietary data recording systems. Tests have shown that continuous data recording rates as high as 20 Mbytes/sec would be possible using high performance disk arrays. During a recent acoustic experiment off the coast of San Diego, data was recorded from a 128 element transducer array at a rate of 6.5 MBytes/sec. The data was simultaneously moved via FTP over gigabit Ethernet to a UNIX workstation for archiving to DLT tape, allowing the acquisition system to record continuously for several days. The configuration of this system and performance during the recent experiment will be described, as well as other current and potential future applications.**

INTRODUCTION

The MPL Mid-Frequency Array (MFA) consists of 128 hydrophones in a two-dimensional, 4 by 32 element pattern and a pressure case containing sampling and telemetry electronics. Data from all 128 channels is simultaneously sampled at 24 kHz, time division multiplexed, and telemetered to the surface on single-mode fiber. In the past, telemetered data from the MFA was received at the surface and recorded using a custom VME acquisition system running VxWorks. However, these VME-based telemetry and recording systems are now obsolete and are difficult and expensive to modify, operate and maintain. The MFA and other similar hydrophone arrays continue to be used for acoustic experiments, but a new telemetry and data acquisition system was necessary.

A new, Compact PCI based telemetry and acquisition system was developed that utilized newer and more reliable technology. The new systems are capable of bi-directional telemetry over coax or fiber and of recording data continuously at higher data rates. These systems are also significantly less expensive, smaller, and easier to duplicate. As a by-product of this development, a custom telemetry interface was designed with the flexibility to be used with a variety of existing and future arrays and sampling systems.

SYSTEM OVERVIEW

Fig. 1 shows a photograph of the data acquisition system, excluding the external SCSI disk array. The system is composed of a PEP CP302 Pentium III CPU (F), A Datum/Bancomm BC637CPCI Time Frequency Processor (D), A National Instruments PXI-6534 High-Speed Parallel Interface (C), A Custom Telemetry Interface (B), A PEP CP360 Ultra2 SCSI Interface (A), A Ramix PMC671TX Gigabit Ethernet Interface (E), 4 IDE disk drives (G), a CPCI power supply (H) and a 1U fan tray (I). The entire system occupies approximately half of the space in a 4U 19" rackmount Compact PCI enclosure, with the Compact PCI components populating an 8-slot, 3U backplane on the left and the 4 IDE disk drives and the power supply in the available space to the right of the backplane. The remaining space on and beside the backplane is available for future expansion. This system usually operates stand-alone without a monitor or keyboard. Access to the data on the SCSI disk array is available via FTP over gigabit Ethernet, and start-up and control of the system is accomplished by remote control from another machine on the network via the 100baseT Ethernet. The rackmount Compact PCI chassis is mounted in a small enclosure for easy transport and to allow stacking with the SCSI disk array and other identical acquisition systems when multiple arrays are used on an experiment.

The PEP CP302 is a complete mobile Pentium III CPU on a ruggedized, single slot, 3U Compact PCI circuit board. Due to the small size, relatively low power and high reliability, the CP302 has been used in several at-sea deployable acquisition systems. Although size and power consumption are not critical for this system, the CP302 was used to maintain compatibility with other existing systems. Four 48GB IDE disks are installed in the enclosure to provide the system partition on which Windows NT and LabVIEW are installed and data storage for lower rate telemetry systems. The version of CP302 CPU used in this system has one of the Compact PCI connectors dedicated to a rear I/O module that provides a second IDE interface and allows for the connection of 4 IDE disks. As a tradeoff for the rear I/O capability, only one connector remains for the PCI interface, which limits the throughput to 32 bits at 33 MHz. Without the rear I/O, the CP302 is capable of interfacing to a 64-bit backplane.

Although the CP302 has on-board 100baseT Ethernet, a separate, dedicated gigabit Ethernet interface was used to maximize the data rate between the acquisition system and a UNIX workstation. The Ramix PMC672TX is a full-duplex gigabit Ethernet interface on a single PMC card, and can be installed on the CP302 PMC site or on a separate Compact PCI PMC carrier (as shown in Fig. 1). The PMC672TX interfaces to twisted pair Ethernet cabling using a front-panel RJ-45 receptacle and has on-board buffers and DMA capability for minimal CPU overhead. Data can be moved from the acquisition system to the UNIX workstation via FTP and archived to DLT tape while the acquisition system continues to record, allowing continuous data acquisition and archiving at the MFA data rate of 6.5 MB/sec.

Fig. 1. Photograph of Acquisition System
- A. PEP CP360 Ultra2 SCSI Interface
- B. Custom Telemetry Interface
- C. PXI6534 High-Speed Parallel Interface
- D. BC637CPCI Time/Frequency Processor
- E. PMC671TX Gigabit Ethernet Interface
- F. PEP CP302 CPU
- G. 2.5" IDE Disk Drives (4)
- H. CPCI Power Supply
- I. 1U Fan Tray

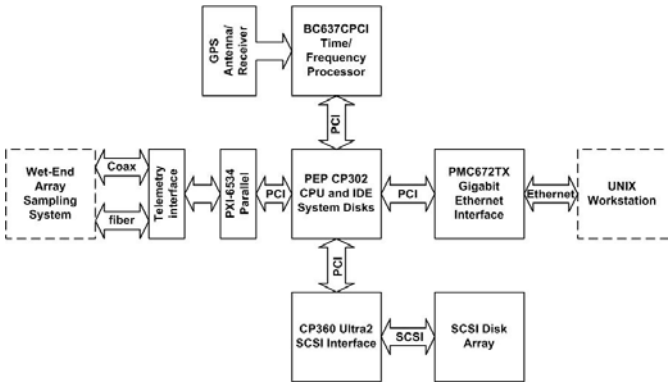

Fig. 2. General Block Diagram of Acquisition System

The Datum/Bancomm BC637CPCI time frequency processor provides GPS synchronized time stamping of the data and is readily interfaced to LabVIEW. The telemetry interface generates a single TTL strobe per second that is synchronized with the uplink telemetry data. Upon detection of this strobe, the BC637CPCI stores a timestamp that is synchronized to GPS time and accurate to the nearest hundred nanoseconds. The timestamp register is then read once per second by the LabVIEW program running on the CPU and written to the data file.

The block diagram in Fig. 2 shows the major components and the data flow through the acquisition system.

TELEMETRY INTERFACE

The remaining two major components of the acquisition system are the National Instruments PXI-6534 and the custom telemetry interface. The combination of these two components forms a flexible, bi-directional, high-data rate telemetry channel for this system that can be interfaced to coax or single-mode or multi-mode fiber.

The PXI-6534 is a high-speed, 32-bit parallel interface that is readily interfaced to LabVIEW. To accommodate the high data rates, the PXI-6534 has a large on-board memory buffer (64 Mbytes of SRAM) and is capable of bus-mastering scatter-gather DMA transfers to CPU system memory with minimal CPU overhead. Continuous transfers up to 20 MWord/s by 8, 16 or 32 bit words are possible. For this application, the PXI-6534 was configured to provide two 8-bit ports for uplink and downlink telemetry channels with bi-direction rates up to 20 MByte/sec. The remaining 16 bits are used for peripheral functions such as driving LED indicators and channel selection for the single channel DAC output.

The custom telemetry interface (Figs. 3 and 4) has a 68-pin connector that matches the PXI-6534 and interfaces to it through a short ribbon cable (visible in Fig. 1). The custom telemetry interface contains all of the electronic components necessary to interface the PXI-6534 to our different serial telemetry systems using coaxial cable or fiber, as shown in the block diagram in Fig. 5. These components include a

programmable logic device (PLD), the fiber optic transceiver chip, media transceivers for coax and fiber, a 12-bit DAC, oscillators and assorted support electronics.

The Altera EPM7512AEQC208 PLD (A in Fig. 3) was selected as the programmable logic device, which is a 512 macrocell EEPROM-based programmable logic chip in a 208-pin Plastic Quad Flat Pack [4]. This chip provides more than enough programmable resources and I/O for all of our current and future applications and is in-circuit programmable via an on-board JTAG connector. The PLD can be programmed using schematic entry or a hardware description language (Verilog was used for the MFA acquisition system). The in-circuit programmability allows for the interface to be conveniently reprogrammed for each application without requiring the replacement of a socketed chip, as was done with earlier PLD technologies.

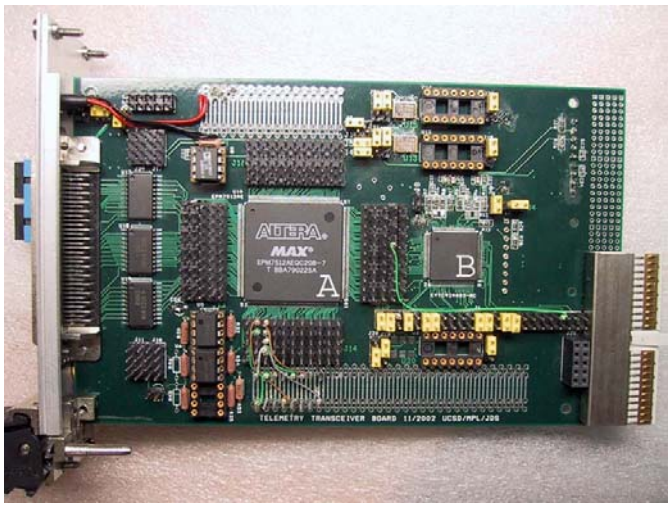

Fig. 3. Telemetry Interface, Component Side

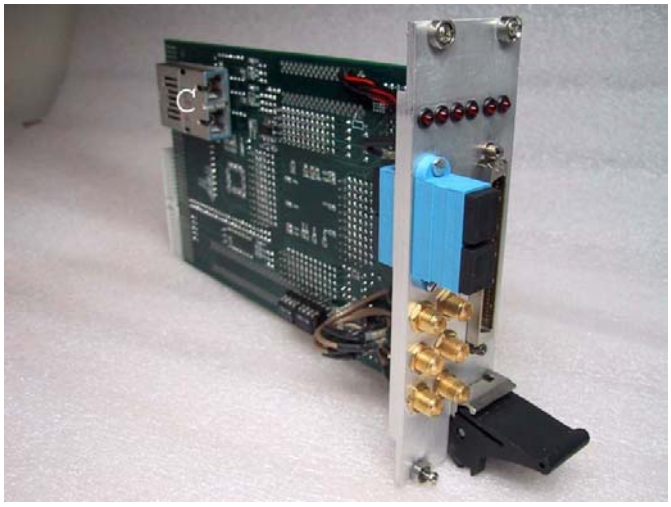

Fig. 4. Telemetry interface, Front Panel and Solder Side

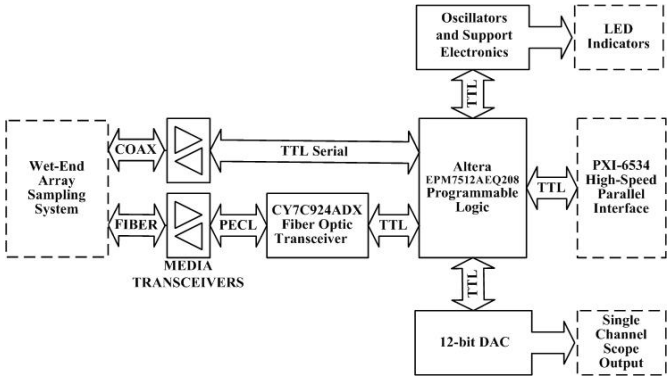

Fig. 5. Block Diagram of Telemetry Interface

The Cypress CY7C924ADX fiber optic transceiver (B in Fig. 3) is a point to point communications building block that was developed for commercial high-speed serial applications such as ATM and Fibre-Channel [3]. This transceiver is capable of serial data rates up to 200 Mbaud (20 Mbytes/sec effective) and is available in a 100-pin Thin Plastic Quad Flat Pack. Functions performed by this transceiver include the telemetry serializing, deserializing, encoding, decoding, bit synchronization and byte framing for the fiber interface. The transmit section accepts 8-bit parallel data, which is then 8B/10B encoded, serialized and driven out on PECL differential transmission line drivers to the fiber media transceiver. On the receiving end, the receiver synchronizes to the bit stream using an on-board PLL, detects byte boundaries using periodic sync bytes from the transmitter, decodes the data into 8 bit bytes and presents the parallel bytes at the output. All of these functions are performed by a single chip that appears to the controlling electronics as a transmitting and receiving pair of 8-bit parallel buffers. The only external components required are the fiber media transceivers, a bit-frequency oscillator for the receiver PLL, and some passive components for the PECL terminations. Communication can be synchronous with the controlling electronics or asynchronous using on-board FIFO buffers. The asynchronous mode allows the telemetry channel to operate at a fixed rate that is independent of the operation of the controlling electronics, allowing communication at a variable rate or in a burst mode, or for the same telemetry system to interface with multiple systems at different data rates. When operating in asynchronous mode, the transmitter automatically inserts special control or "sync" bytes in the telemetry data that are filtered by the receiver and do not appear as data at the output. These sync bytes are required by the receiver for maintaining bit and byte synchronization.

The Agilent HFCT-53D3 fiber optic media transceiver (C in Fig. 4) is used for the physical interface from the CY7C924ADX to the fiber optic cable. This transceiver consists of a transmitter and receiver pair in a single package that is capable of interfacing to multi-mode or single-mode fiber. The HFCT-53D3 has PECL interfaces for transmit and receive that are compatible with the CY7C924ADX, SC style fiber optic connector receptacles,

and has an industry standard 1 by 9 footprint that can be easily socketed on the circuit board. Communication through lengths of fiber optic cable up to 500 meters for 62.5/125 μm multi-mode fiber and 10 kilometers for 9/125 μm single-mode fiber is possible using this transceiver. Special attention to the terminations for the PECL transmission lines is required and some in-situ adjustments of the termination resistor values were done to achieve optimal performance.

The custom telemetry interface was designed with maximum flexibility in mind to accommodate all of our current and future telemetry needs. The circuit board has 6 sites for crystal oscillators that will accept a variety of standard surface mount or though-hole packages. By including locations for reference resistors, the surface mount oscillator sites can use a VCXO either as a component of a phase locked loop (for synchronization using coax) or as a fixed frequency oscillator by installing appropriate reference resistors. Crystal oscillators required for different applications can be left on the board and selected using jumpers to configure the board for a particular telemetry system. The oscillators are disconnected and deactivated when not required. Prototype spaces along the top and the bottom of the circuit board allow for 50 mil surface mount or 100 mil through-hole components to be added and connected to the circuit by wire-wrap or solder. Figs. 3 and 4 show the space along the bottom of the board used to add Manchester encoder and decoder chips that were used for testing. The top and bottom rows of pads in each space have alternating VCC and GND connections, allowing for convenient connection to power and for bypass capacitors. All 208 pins of the EPM7512AEQC208 PLD are connected to four 5 by 11 pin, 100 mil headers around the perimeter of the chip that extend to the front and the back of the circuit board. This allows for convenient connection of oscilloscope and logic analyzer probes, connection to added components by wire-wrapping, and the addition of daughter boards.

SYSTEM TIMING AND DATA FORMATS

Fig. 6 shows the telemetry and data file formats for the MPL Mid-Frequency Array. Data from the wet-end array sampling system is time-division multiplexed into 272-byte data frames by the wet-end telemetry interface before being serialized, encoded and driven onto the fiber-optic cable. Each data frame contains a 32-bit, pseudo-random code that is detected at the dry-end and used for data frame alignment by the acquisition system. The remaining 268 bytes (134 16-bit slots) contain a single 16-bit sample from each of the 128 hydrophone channels as well as 6 extra slots for additional hydrophones or auxiliary sensors. At the receiving end, the data is detected from the fiber optic cable, decoded, and deserialized into 8-bit parallel bytes that are presented to the PLD on the dry-end telemetry interface. The parallel data stream is then clocked into the input port on the PXI-6534 and into the on-board SRAM. The PLD generates a 1-pulse per second strobe that is synchronized with the uplink telemetry data and is used to trigger the capture of the time stamp with the BC637CPCI time and frequency processor.

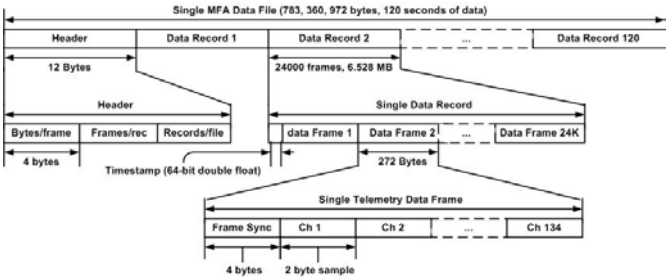

Fig. 6. MFA Telemetry and Data File Formats

The PXI-6534 high-speed parallel interface buffers incoming data in on-board SRAM and moves the data in 1-second records (24000 frames) to CPU system memory via DMA transfers across the PCI bus. A LabVIEW program running on the CPU opens a new data file every 120 seconds, writes the format information into the header, and monitors the data buffers in system memory. As each complete record is written into system memory by the PXI-6534, the CPU retrieves the timestamp from the BC637CPCI, appends it to the front of the record, and writes the record to the data file on the SCSI disk array. The timestamp represents the time of arrival of the first byte of the first frame for each record at the dry-end telemetry interface. The program also checks the frame sync code in the first frame of each record to confirm synchronization. If a frame sync error is detected, an error line is recorded in an ASCII log file, all data buffers are flushed, and the system attempts to resynchronize and restart the acquisition process. If resynchronization fails three times in immediate succession, the acquisition process is aborted and an error LED is lit on the telemetry interface to indicate that human intervention is required.

Fig. 7 shows the CPU and SCSI disk timing for the acquisition of a single MFA data record. The required time for the PXI-6534 to move a one second record of data (6.528 MB) to system memory and for the CPU to read the timestamp and check the validity of the timestamp and frame sync was measured to be just under 80 milliseconds. The remaining 250 milliseconds is required to write the record to the SCSI disk array. Thus, the total time required to record a 1-second record of data from the 6.5 MB/s MFA telemetry stream is 330 milliseconds. It was determined by testing that approximately a 30% safety margin is acceptable for a non-realtime operating system (Windows NT), suggesting that the system in this configuration could probably record data at twice the MFA rate or 13 Mbytes/second, which would require 660 milliseconds per one second record of telemetry data. As can be seen on the timing diagram, the SCSI disks are the clear throughput bottleneck. In an attempt to maximize the disk throughput, an Ultra2 SCSI interface was used with 5 73GB, 10KRPM Fujitsu MAN3735 Ultra-160 disk drives. These 5 disks were configured into a single, 365GB NTFS partition set to allow for up to 15 hours of recording from the MFA. Continuous throughput from the acquisition system to this NTFS partition was measured to be approximately 28 Mbytes/second. Manufacturers of high-

performance SCSI to IDE RAID arrays advertise continuous throughputs in excess of 80 MB/s. If such rates are achievable with this system, total system recording rates up to the 20 MB/s limit of the telemetry interface and PXI-6534 could be achievable.

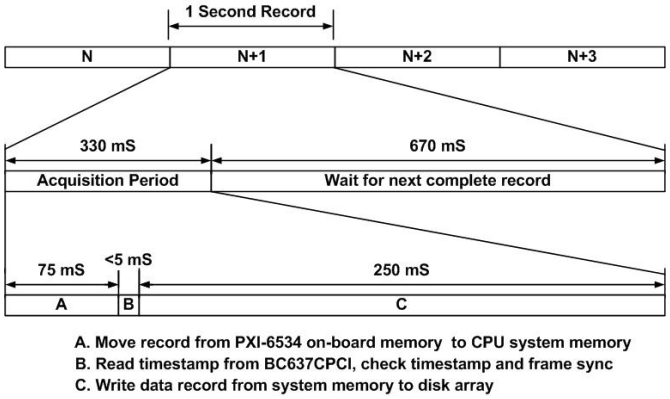

Fig. 7. MFA Data Acquisition System Timing

CONCLUSION

The High-Speed Data Acquisition System described in this paper was used during an experiment aboard the Research Platform FLIP in 2002 to record data from the 128-hydrophone MPL Mid-Frequency Array. Data from the MFA was recorded continuously for several days while data files were simultaneously moved from the SCSI disk array to a UNIX workstation via FTP over gigabit Ethernet and archived to DLT tapes. The continuous recording and FTP processes are taxing to the Compact-PCI CPU which, on a few occasions, resulted in the acquisition system falling behind and losing synchronization with the telemetry data. However, the system was able to reliably detect the error and resynchronize with the telemetry stream and restart the recording process with minimal loss of data. For higher data rate applications, the simultaneous FTP process will not be possible and data will need to be recorded until the SCSI disk array is full. Then recording will need to be stopped while the data is moved to the UNIX workstation for archival. However, this may not be an issue considering the large volume disk arrays that are currently available. As an example, using a 12 disk, 1.6 Terabyte RAID array that was available a year ago (larger ones are certainly available today) and assuming the maximum theoretical acquisition rate of 20 Mbytes/sec, more than 22 hours of continuous data recording would be possible. It is possible that an entire experiment of data could be recorded on one or more disk arrays and archived to tape using a UNIX Workstation back on shore after the experiment has been completed.

As a potential future enhancement, the acquisition system described in this paper could be interfaced to a SCSI to IDE RAID array for recording higher telemetry rates, potentially up to the maximum of 20 Mbytes/sec. This would allow greater flexibility to increase the sampling rates of existing arrays or to increase the number of hydrophone elements. The higher acquisition rate would be required for a 128 element hydrophone array with ½-lambda spacing at 15 kHz and a telemetry rate of 13 Mbytes/sec that is currently under consideration. In addition, it is planned to test the Cypress CY7C924ADX fiber optic transceiver in the asynchronous mode, which would decouple the telemetry clock from the sampling system and acquisition system timing and could potentially allow a single telemetry system running at a fixed rate to function with a variety of arrays and sampling systems.

ACKNOWLEDGEMENTS

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APPENDIX

The flexibility of the telemetry interface developed for this acquisition system has allowed us to upgrade and standardize all of the digital telemetry systems that are used by our research group. In addition to the Mid-Frequency Array (and several other similar arrays), the new telemetry interface has been used with the MPL SRP (Special Research Project) Arrays and the MPL HFPCA (High-Frequency Phase Conjugation Array) and MFPCA (Mid-Frequency Phase Conjugation Array).

The SRP arrays are composed of 64 hydrophones that are sampled at 1500 Hz per element [1]. The uplink data is Manchester encoded and time-division multiplexed over coax at 4.22 Mbits/sec. At the dry-end, the telemetry interface detects the data from the coax, the on-board PLD Manchester decodes the data using a PLL with an external VCXO, and clocks the data into the PXI-6534 as parallel bytes. The data is recorded using the acquisition system described in this paper, with the software and telemetry interface reconfigured for SRP acquisition. A single, software selectable SRP channel is available as an output from the telemetry interface for observation on an oscilloscope.

The HFPCA and MFPCA systems are 29 element, transmitting and receiving transducer arrays that are used for Focused Acoustic Field experiments at 3500 Hz and 850 Hz, respectively [2]. Each system now uses a pair of the new telemetry interfaces, one at the wet-end receiver and transmitter electronics and one at the buoy end where the wireless LAN and controlling electronics reside. The HFPCA/MFPCA systems require bi-directional telemetry at 6.5 Mbytes/sec over coax or fiber (currently only coax is used), with the downlink used for commands and the uplink for continuous data and status information. The wet-end telemetry interface also controls the data bus in the wet-end electronics pressure case and provides all of the general system timing for the 29 individual transmitter and receiver channels.

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