Near-Field Audio and Data Transceiver ASIC

The LibertyLink™ integrated circuit is a highly integrated system-on-a-chip solution for low-power, near-field wireless voice and data communications. Point-to-point applications are served by the transceiver IC. Two way communication is achieved through time division duplex (TDD) of GMSK modulated magnetic fields. The fully integrated diversity transmitter contains a GMSK lookup table, 8-bit IQ DACs, mixer, filters, and coil drivers with output power control. The fully integrated diversity receiver contains an LNA, IF mixer and filter, baseband mixer and filter, and data demodulator. The raw channel data rate is 204.8 kbps. Audio is digitized and encoded using an on-chip ADC and 64 kbps CVSD encoder and, similarly, decoded using a CVSD decoder and DAC. Additionally, integral low and high pass filters on the audio input and output channels provide further signal conditioning. An embedded microprocessor with 5K of on-chip RAM controls the ASIC operation. Analog output audio signals differentially drive a 32-ohm speaker while the audio input is readily compatible with conventional or noise canceling microphones. User defined analog and digital I/O pins also provide the opportunity for product differentiation. An integral NiMH battery charging control circuit further minimizes off chip components.

- Single chip solution
- Advanced near field magnetic communication technology
- 2V operation
- 13.56 MHz system operating frequency
- BER = 10^{-4} @ 18.0 dB SNR
- Small footprint 48 Lead LQFP package
- Firmware Included

Operational Specifications

All values are as obtained from the test schematic and test conditions as specified in Appendix A.

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Power Supply Voltage	$V_{CC\ (max)}$	+3.3	Vdc
DC Vcc or GND Current	Icc	+/- 10	mA
Junction Temperature	T_J	+125	°C
Operating Ambient Temperature Range	T_A	-20 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Lead Temperature (soldering 5 sec.)	T_L	+ 245	°C

Electrical Characteristics (T_A= +25°C)

Characteristics	Symbol	Min	Typ	Max	Unit
Operating Supply Voltage Range	V_{CC}	1.95	2.0	2.5	Vdc
IC supply current, RX Mode (V_{CC} = 2.0V)	$I_{DD,\ RX}$	-	8.5	9.5	mA
IC supply current, TX Mode (V_{CC} = 2.0V)	$I_{DD,\ TX}$[1]	-	6.7	8.0	mA

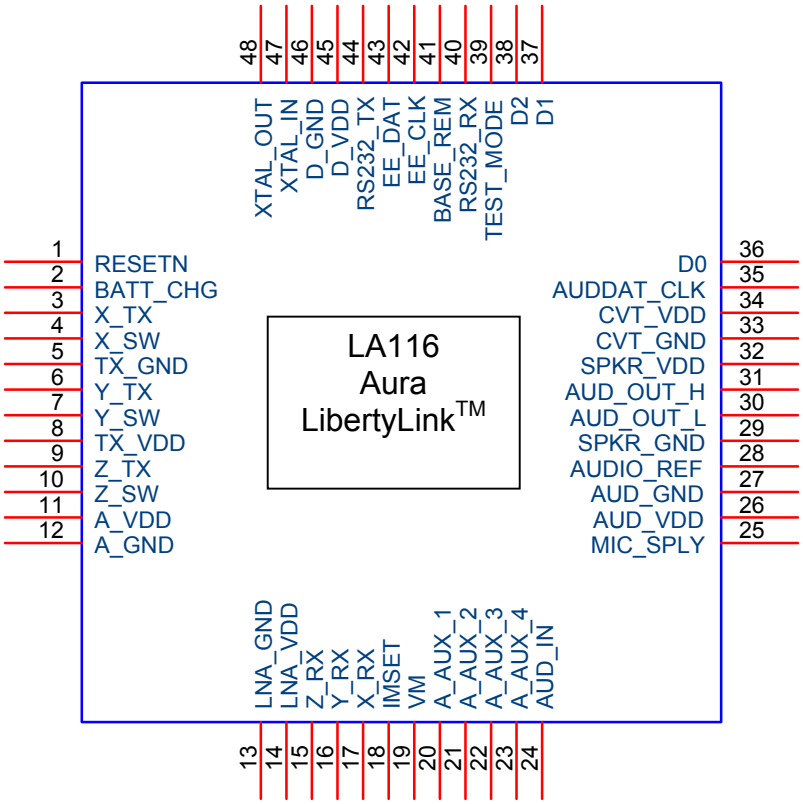
[1] $I_{DD,\ TX}$ measurement made with no antenna load

ASIC Characteristics

Characteristics	Specification
Transmitter/Receiver Carrier Frequency	13.56 MHz
Audio Frequency Response (10 dB)	130 Hz to 3.8 KHz
Duplex Scheme	TDD
Raw Channel Bit Rate	204.8Kbps
Modulation	GMSK (BT= 0.5)
Package	48 pin LQFP
Audio Input Signal Range (Min. mic pre-amp gain)	< 400mV pp
Audio Output Drive (single ended)	1.8 Volt peak to peak into 32 Ω
ESD per JESD 22-A114-B	Class 1A
Latch-up per JEDEC STD 78 Level 1	Pass

Target Electrical Characteristics

Below is the pin out with parameter values under operating conditions defined in Appendix A.



I/O Operating Characteristics (V_{DD} = 2.0V)					
Pin Label	**Pin Number**	**Description**	**Type**	**Value Range**	**Units**
RESETN	1	Chip Reset (- Logic)	Input	0 to V_{DD}	V
BATT_CHG	2	Battery Charge	Analog I/O	0 to 1	V
X_TX	3	X-Axis TX Output	Output	0 to V_{DD}	V
X_SW	4	X-Axis T/R Switch	Analog Out	0 to 7	mV_{p-p}
TX_GND	5	Transmit Ground	Ground	0	V
Y_TX	6	Y-Axis TX Output	Output	0 to V_{DD}	V
Y_SW	7	Y-Axis T/R Switch	Analog Out	0 to 7	mV_{p-p}
TX_VDD	8	Transmit VDD	Power	V_{DD}	V
Z_TX	9	Z-Axis TX Output	Output	0 to V_{DD}	V
Z_SW	10	Z-Axis T/R Switch	Analog Out	0 to 7	mV_{p-p}
A_VDD	11	Analog VDD	Power	V_{DD}	V
A_GND	12	Analog Ground	Ground	0	V
LNA_GND	13	Low Noise Amp Gnd	Ground	0	V
LNA_VDD	14	Low Noise Amp VDD	Power	V_{DD}	V
Z_RX	15	Z-Axis RX Input	AC Input	7	mV_{p-p}
Y_RX	16	Y-Axis RX Input	AC Input	7	mV_{p-p}
X_RX	17	X-Axis RX Input	AC Input	7	mV_{p-p}
IMSET	18	Reference Current Voltage	Analog Out	1.63	V
VM	19	Reference Voltage	Analog Out	V_{DD}-1	V
A_AUX_1	20	User Auxiliary Analog I/O	Input	0 to 1.2	V
A_AUX_2	21	User Auxiliary Analog I/O (De-ice)	Input	0 to 1.2	V
A_AUX_3	22	User Auxiliary Analog I/O (De-ice)	Input	0 to 1.2	V
A_AUX_4	23	User Auxiliary Analog I/O (De-ice)	Input	0 to 1.2	V
AUD_IN	24	Audio In	Input	<400	mV_{p-p}
MIC_SPLY	25	Microphone Bias/Supply	Output	V_{DD}	V
AUD_VDD	26	Audio VDD	Power	V_{DD}	V
AUD_GND	27	Audio Ground	Ground	0	V
AUDIO_REF	28	Audio Ref Level	Analog Out	0.65	V
SPKR_GND	29	Speaker Ground	Ground	0	V
AUD_OUT_L	30	Diff Audio Out- (Line or 32 Ohm)	Output	$V_{DD}/2$	V_{DC}
AUD_OUT_H	31	Diff Audio Out+ (Line or 32 Ohm)	Output	$V_{DD}/2$	V_{DC}
SPKR_VDD	32	Speaker Drive VDD	Power	V_{DD}	V
CVT_GND	33	ADC/DAC Ground	Ground	0	V
CVT_VDD	34	ADC/DAC VDD	Power	V_{DD}	V
AUDDAT_CLK	35	Audio Data Clock for external use(De-ice)	Digital Out	0 to V_{DD}	V
D0	36	User Digital I/O (Vdd -.25/+.5V)	Digital I/O	0 to V_{DD}	V
D1	37	User Digital I/O (Vdd -.25/+.5V)	Digital I/O	0 to V_{DD}	V
D2	38	User Digital I/O (Vdd -.25/+.5V)	Digital I/O	0 to V_{DD}	V
TEST_MODE	39	When High, device in Test Mode (De-Ice)	Digital Input	0 to V_{DD}	V
RS232_RX	40	RS232 Receive	Digital Input	0 to V_{DD}	V
BASE_REM	41	Base or Remote Mode	Digital Input	0 to V_{DD}	V
EE_CLK	42	External EEPROM Clock	Digital Output	0 to V_{DD}	V
EE_DAT	43	External EEPROM Data Bidirectional	Digital Input	0 to V_{DD}	V
RS232_TX	44	RS232 Transmit	Digital Output	0 to V_{DD}	V
D_VDD	45	Digital VDD	Power	V_{DD}	V
D_GND	46	Digital Ground	Ground	0	V
XTAL_IN	47	Crystal In	Input	0 to 1	V
XTAL_OUT	48	Crystal Out	Output	0 to 1	V

Audio Specifications*

Specification	Equipment Settings / Input Levels	Values	Limit
Base Transmit to Remote Receive:	Mic Preamp Gain = 6dB		
THD vs. Input Signal	1 KHz tone	See Figure 1	6 % Max to 50 mV_{rms}
Signal to Noise Ratio (SNR) vs. Input Signal	Audio Analyzer using C-Message Weighting filter and 1 KHz tone	See Figure 2	3 dB below curve
High Pass Filter Cut-on	10dB down from 1kHz signal level	131 Hz (See Figure 3)	± 3%
Low Pass Filter Cut-off	10dB down from 1kHz signal level	3800 Hz (See Figure 3)	± 3%
Remote Transmit to Base Receive:	Mic Preamp Gain = 28dB		
THD vs. Input Signal	1 KHz tone	See Figure 4	6 % Max to 2 mV_{rms}
Signal to Noise Ratio (SNR) vs. Input Signal	Audio Analyzer using C-Message Weighting filter and 1 KHz tone	See Figure 5	3 dB below curve
High Pass Filter Cut-on	10dB down from 1kHz signal level	131 Hz (See Figure 3)	± 3%
Low Pass Filter Cut-off	10dB down from 1kHz signal level	3800 Hz (See Figure 3)	± 3%

* See Appendix A for test conditions

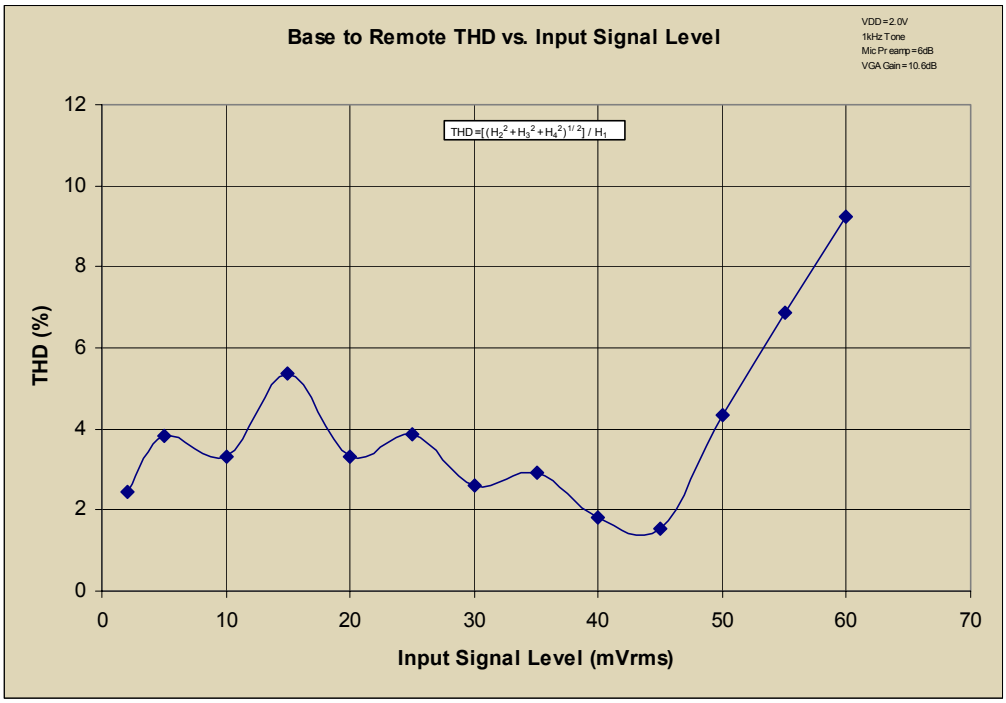


Figure 1– Base transmit to Remote THD

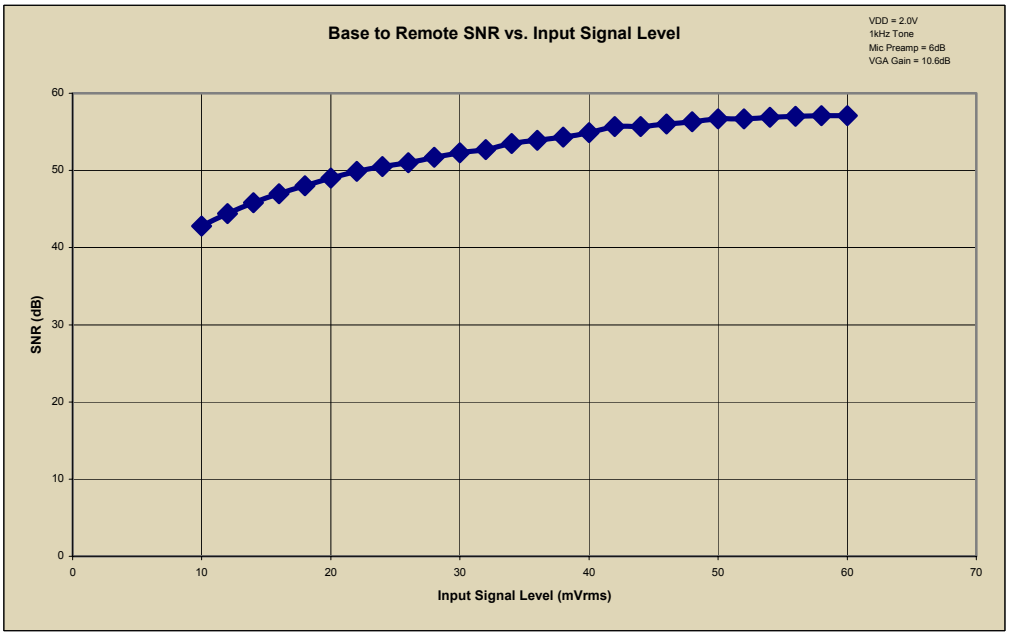


Figure 2 – Base transmit to Remote SNR

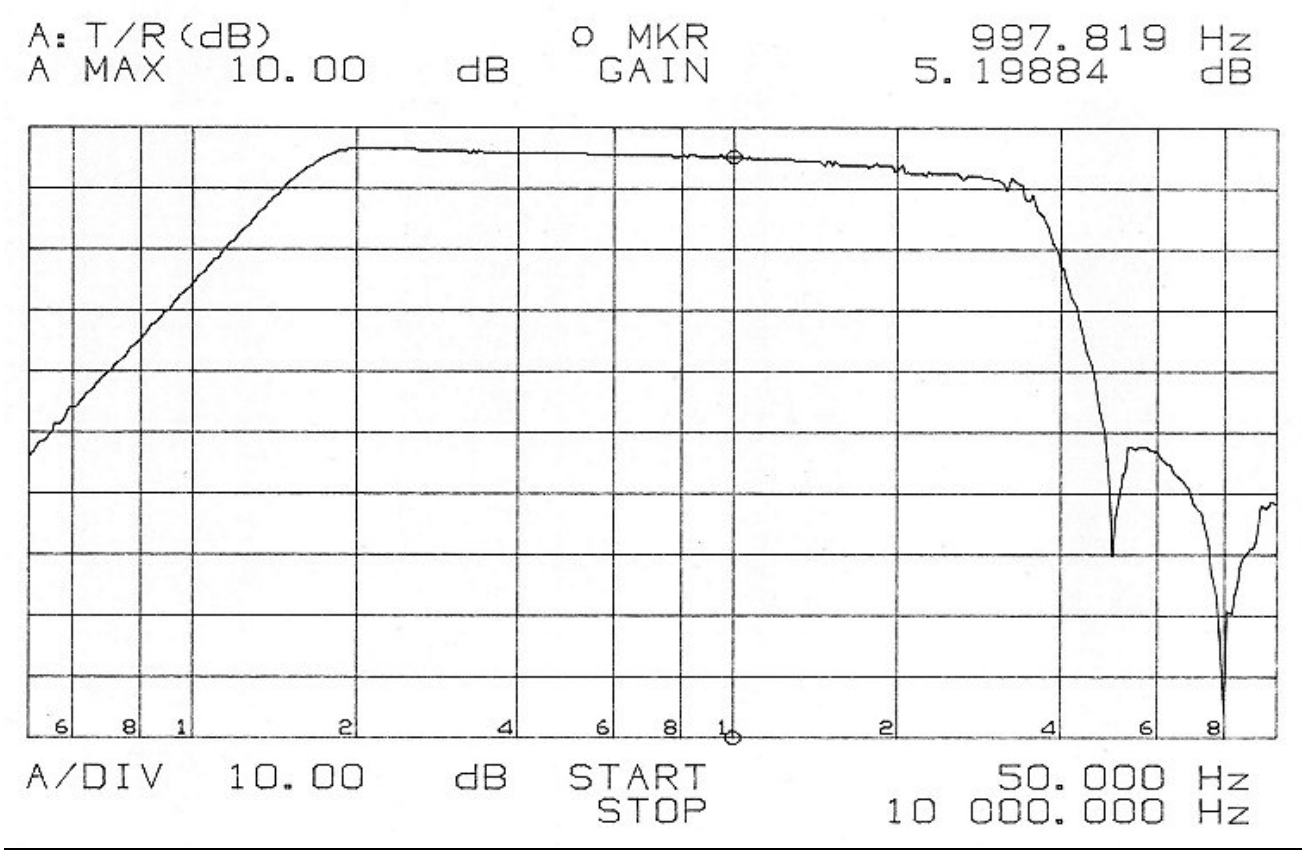


Figure 3 – LibertyLink input stage audio bandwidth defined by the test conditions found in Appendix A. Output stage bandwidth is identical.

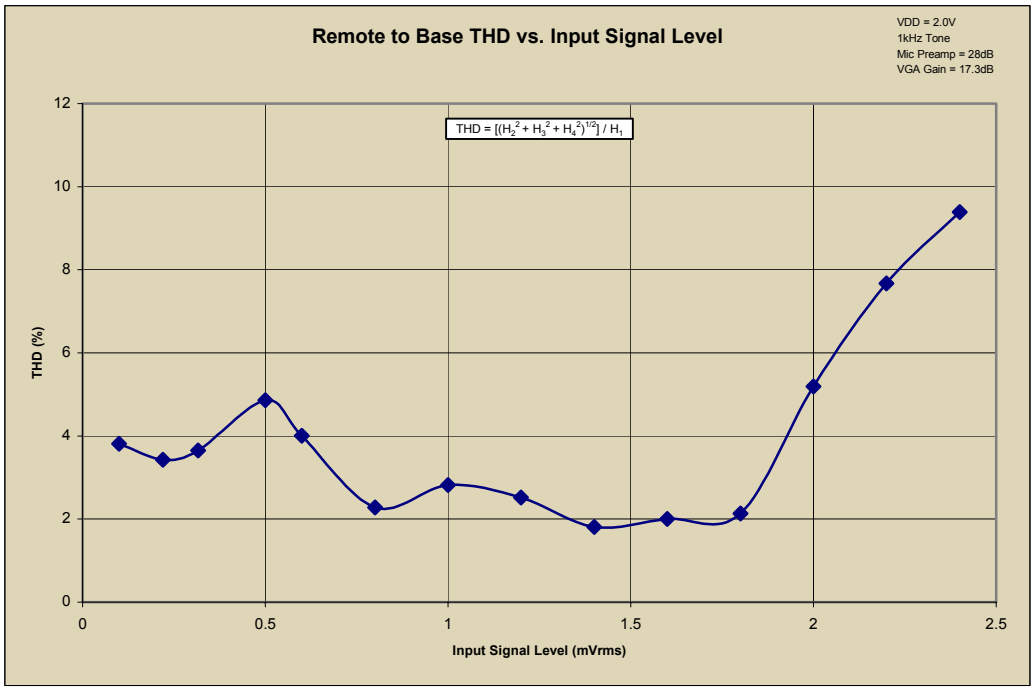


Figure 4 – Remote transmit to Base THD

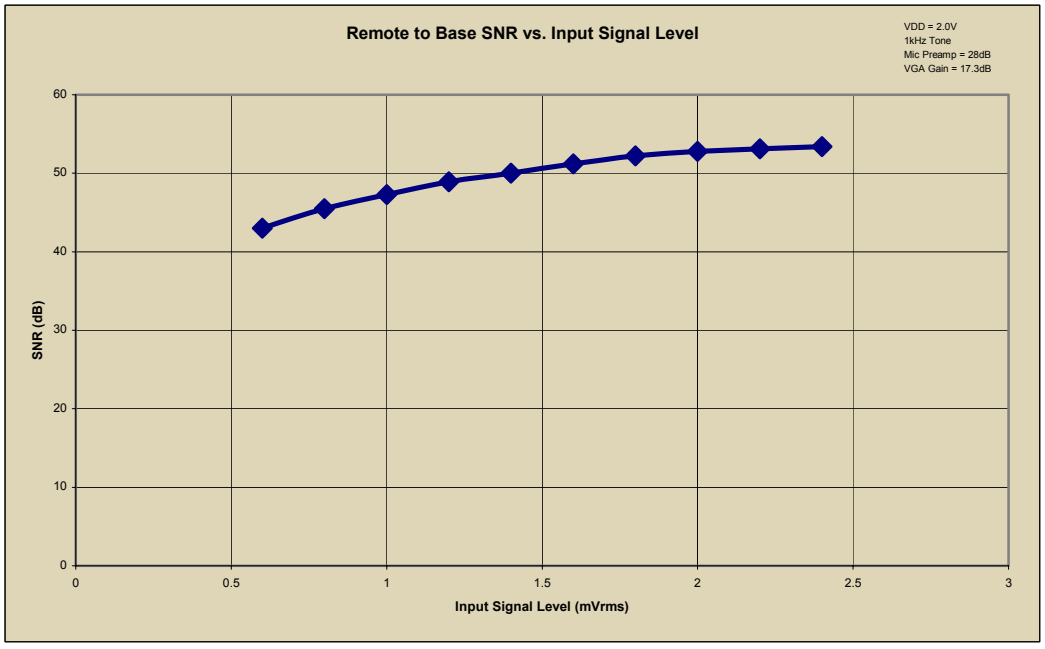
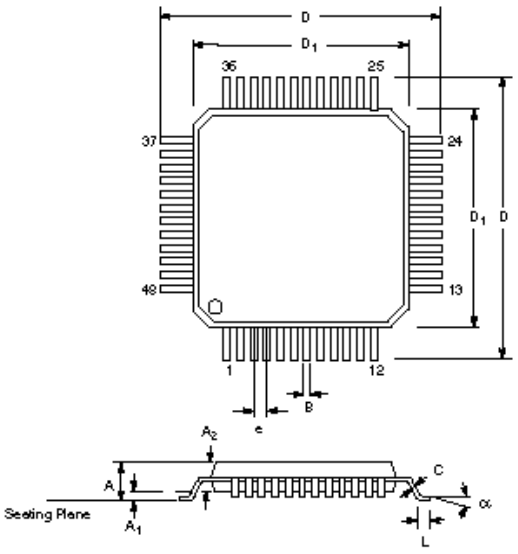


Figure 5 - Remote transmit to Base SNR

Packaging Detail

48 Pin LQFP

Package Reliability	
Specification	**Description**
Moisture Sensitivity Level	JEDEC Level 3
Temperature Cycling	-65°C / 150°C - 1000 Cycles
High Temperature Storage	150°C - 500 Hours
Pressure Cooker Test	121°C, 100% RH, 2 ATM, 168Hours
Liquid Thermal Shock	-55°C / 125°C - 1000 Cycles
Marking	Laser
Packing Option	JEDEC Tray, Tape and Reel



Symbol	Millimeters	
	Min	Max
A	1.400	1.600
A_1	0.050	0.150
A_2	1.35	1.45
B	0.170	0.270
C	0.090	0.200
D	8.850	9.150
D_1	6.850	7.050
e	0.500	
L	0.450	0.750
α	0^o	7^o

Appendix A: Typical Set-up

Test Conditions and Platform Definition

The table below and the schematic define the system test conditions with the Unit Under Test (UUT) in loop-back mode at temperature of +25C with special firmware. (In loopback mode, an audio signal input at AUDIO_IN goes through the audio input circuitry, through the modulator and transmitted on the X-Coil. The signal is received on the Z-Coil, demodulated and the audio is output on AUD_OUT_H.) The performance obtained in this configuration is typical of all other antenna transmit and receive configurations.

Two system configurations are tested. The first emulates transmitting from base to remote. The second emulates transmitting from remote to base. Although the same circuit design is used on both sides of the system, different gain settings are used. The proper settings are shown below for both.

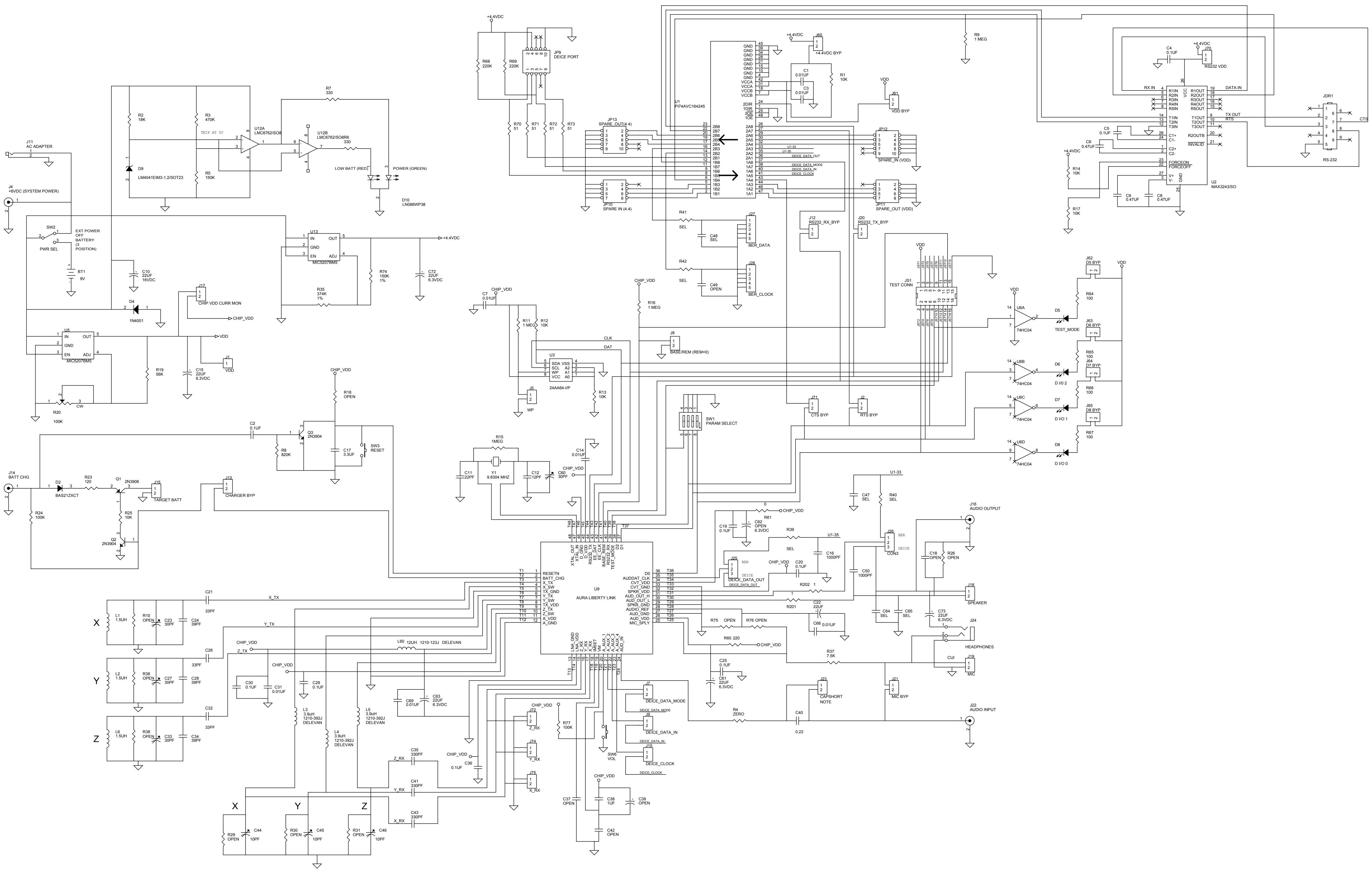
Three key parameters are measured for each configuration: power consumption, distortion and Signal-to-Noise Ratio (SNR).

Test Conditions	
Parameter	**Value**
General	
V_{DD}	+2.0V
Temperature	20°C
Receiver Circuit Parameter	
Input Tuning Select	N/A
Input Attenuation	0dB
Front End Attenuation	0dB
RF VGA Gain	11dB
IF LP Filter Cutoff	756 KHz
IF VGA Gain	2 dB
BB LP Filter Cutoff	300 KHz
Audio Input Settings	
Reference Voltage Bias Current	100 μA
Audio VGA Gain (Remote / Base)	17.3 / 10.6 dB
Microphone Pre-amp Gain (Remote / Base)	28 / 6 dB
Switched Capacitor High Pass Filter 10 dB Cut-on	131 Hz
Switched Capacitor Low Pass Filter 10 dB Cutoff	3.8 kHz
Audio Output Settings	
Side tone Enable	OFF
Switched Capacitor High Pass Filter 10 dB Cut-on	131 Hz
Switched Capacitor Low Pass Filter 10 dB Cutoff	3.8 kHz
Volume VGA Gain (Remote / Base)	-14 / -10 dB
Speaker Driver Bias	Low
Speaker Driver Gain	0dB
'Loopback' Condition	

Test Conditions	
Parameter	**Value**
Transmitting Coil in Loopback	X-Coil Typical
Receiving Coil in Loopback	Z-Coil Typical
Audio DAC Section	
DAC Sampling Rate	16KHz
Audio ADC Section	
ADC Sampling Rate	16KHz
Synthesizers Section	
Audio VCO Frequency	54.0672 MHz M=55/N=10
RX Local Oscillator 2	42,372,413 Hz M=125/N=29
RX Local Oscillator 1	52,202,813 Hz M=154/N=29
TX Local Oscillator	54,236,689 Hz M=160/N=29
Crystal Frequency	9.8304MHz
Crystal Divider	1
Data Format Section	
Randomizer/Derandomizer	OFF
Differential Encoding	ON
Interleaving/De-Interleaving	OFF
CVSD Clock Rate Adjust	ON
Transmitter Section	
Transmitter DAC Gain	Nominal
Transmitter Power	90mA –bit state 8

Test Schematic (Print on 11X17 page for legibility)

All tests are referenced to the circuit below. Individual tests may call out particular test conditions and levels. Each antenna on the load board front-end must be tuned properly. (Resonance at the frequency of interest and Q>40)



Operation controlled by firmware as defined in Aura Document 1225

Contact Information:

Corporate Headquarters
Aura Communications
187 Ballardvale St.
Wilmington, MA. 01887
Tel: +1.978.988.0088
Fax: +1.978.988.3977
Email: info@auracomm.com
www.auracomm.com

This document contains the specifications for the LibertyLink Integrated Circuit (LA116). The specifications in this document supercede all other published specifications for LibertyLink, including datasheets, application notes and website. All operating parameters must be validated for each application by each customer's technical experts.