Features

- 1.25 meter operating range
- 2.0V operation
- 10mA typical,17mA max current
- 100µA typical, 220µA max standby
- Advanced magnetic induction technology
- Time Division Duplex (TDD)
- GMSK Modulation
- 64 kbps CVSD encoding
- 48 Lead LQFP
- Single Chip Solution

Application

The primary application for LibertyLink is wireless voice communication with the Personal Area Network (PAN). A typical product developed with LibertyLink would be a wireless headset for the mobile phone.

Introduction

Aura Communications offers an advanced ASIC designed to provide wireless full duplex audio communication at low power. The Aura LibertyLink transceiver IC is a highly integrated solution for OEMs wishing to add short-range wireless voice capability for cellular or cordless headsets, PDAs, mobile Internet devices or similar applications. Using the same IC on both sides of the wireless link, the LibertyLink delivers complete signal processing and control for high quality audio transmission.

This data sheet describes the Aura LibertyLink IC and the magnetic induction technology. In order to facilitate the discussion, this note has adopted the following nomenclature. Since both ends of the wireless link have a transmitter and receiver, this terminology will be avoided. To that end, one side of the system will be designated the 'Base Unit' and the other side the 'Headset' or 'Remote'. The base unit attaches to the mobile device, while the remote is typically a stand-alone I/O device.

Included herein is a description of each block of the ASIC, including the receiver, the transmitter, timing circuitry, and microprocessor. In addition, all off-chip circuits and the firmware are discussed.

Additional support material available regarding LibertyLink:

Document Description	Aura Document Number
LibertyLink Specification	1212
LibertyLink Wireless Headset Application Note	1220
Wireless Headset/Universal Base Operations Guide	1221
LibertyLink Testing and Tuning Description	1223
Aura Wireless Headset Reference Design	1224
LibertyLink Operational Characteristics	1237

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Description

The LibertyLink is a fully integrated Time Division Duplexed (TDD) digital communication system intended for use in short range inductive wireless communication applications. The system transmits a Gaussian Minimum Shift Keyed (GMSK) magnetic field between the base and remote. The remote uses a single magnetic coil for both transmit and receive. Spatial diversity is achieved through three orthogonal magnetic coils in the base, allowing the system to select the antenna axis that results in the optimum signal to noise ratio (lowest BER) for the link. Near-field magnetic transmission allows a lower cost system that makes more efficient use of power and space compared to conventional RF approaches. It also eliminates many of the problems associated with spectrum re-use in high frequency RF solutions.

LibertyLink is a single chip full duplex wireless transceiver consisting of a receiver, transmitter, codec, frequency synthesizer, microprocessor and memory. This same chip is used for the base and headset implementations, with only minor circuit changes. The LibertyLink is fully integrated and only a handful of low-cost and readily available external components are needed to make a complete system. The versatile microprocessor firmware can be programmed to suit many specialized applications.

Simplified Block Diagram

Below is the simplified block diagram of the LibertyLink chip. Minimal off-chip components are required for the system design and each application will have slightly different components. Each section of the chip is described below and a typical application is discussed.

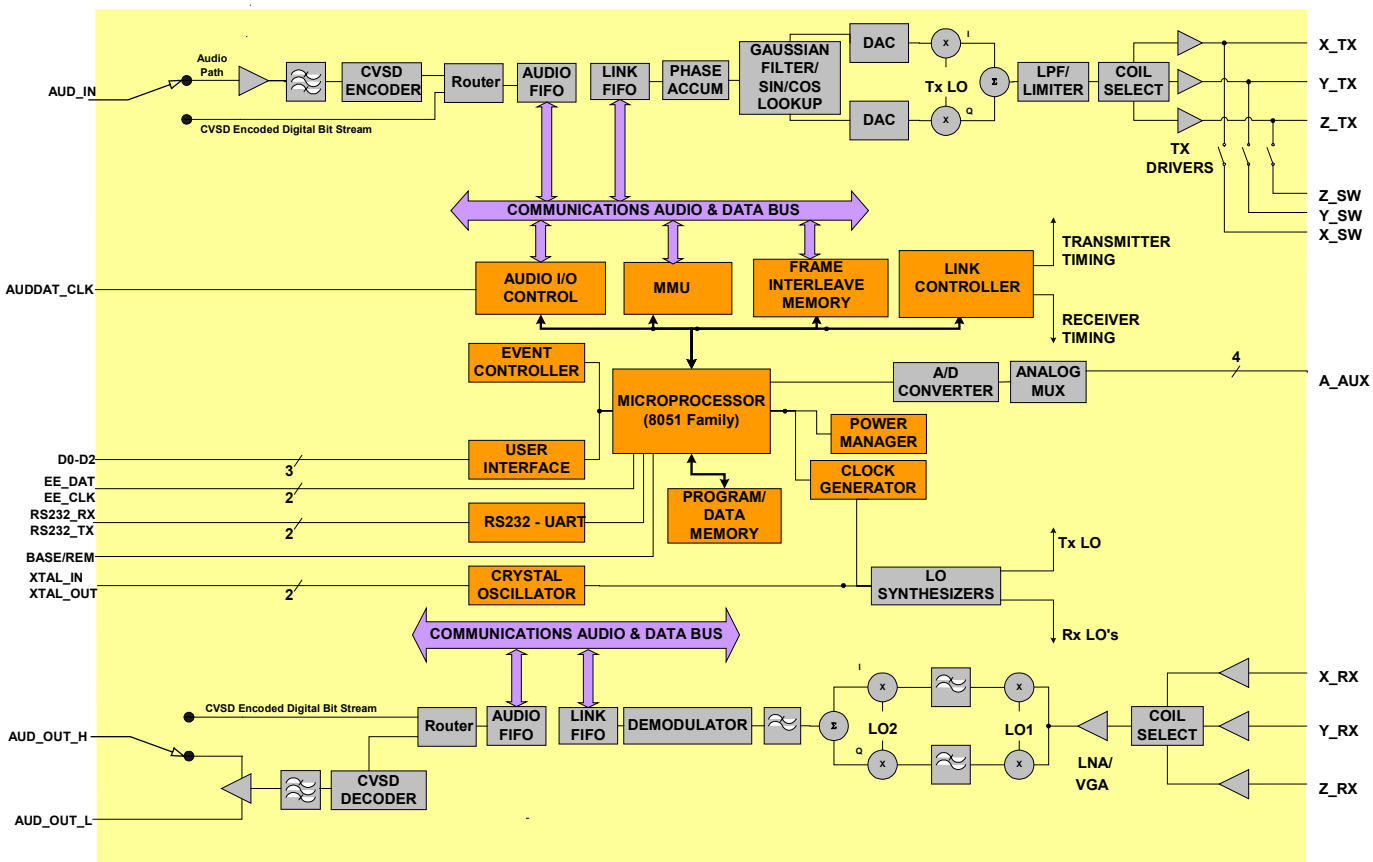


Figure 1: LibertyLink Block Diagram

ASIC Description

For discussion purposes, the LibertyLink system is broken down into five sections; receiver, transmitter, synthesizer block, microcontroller and the front-end.

Because this is a magnetic induction system, optimal magnetic link conditions cannot be maintained by a single coil in both the base and the remote for all relative orientations between the two. Therefore, it is necessary that the Base side of the link have three mutually orthogonal coils. As the base and the remote change orientation with respect to each other, the microcontroller monitors the Base receiver coils to determine the axis with the strongest signal from the remote. Once the best orientation is determined, the base will transmit back on the chosen coil. Hence, the base chip transmitter and receiver are wired to the X, Y and Z axis, while the remote is connected only to the X-axis.

The receiver chain is made up of an antenna block, a low noise amplifier, the IF strip, down converters, the demodulator, the CVSD decoder and audio output stage. Each of these are discussed in detail in the next section.

The transmitter chain consists of the following blocks; audio input stage, CVSD encoder, GMSK modulator, coil driver, and antenna block. Each functional block is described in more detail below. The transmitter chain can convert either microphone or line level audio into a GMSK modulated signal that is applied to a transmit/receive coil. The digitally encoded audio signal is not transmitted continuously over time, rather, each end of the system alternates between transmit and receive in 1.4 millisecond bursts or slots. This allows a single antenna for both transmit and receive modes and eliminates the possibility of the transmitter cross-talk into the receiver.

The synthesizer/timing block, based on a low cost crystal, provides local oscillator and reference clocks for the IF and baseband sections.

The microprocessor/control section and specialized functional blocks control almost every aspect of the system's operation. It is composed of a microprocessor core, MMU controller, DMA unit, link controller, a UART, an audio randomizer and de-randomizer, watchdog timer, a timer/counter, a power manager, a user interface controller, and a system control block.

Detailed Block Descriptions

Receiver

The three (base) antenna coils are selected during the appropriate time slots and the signal is fed through a tuning network and into the X_RX, Y_RX or Z_RX pins on the chip. The Q of the receiving coil, in conjunction with the chain of image-rejection mixers and active filters, reduces adjacent channel interference. On-chip, the microcontroller samples the signal from each coil and makes a determination on the optimal orientation. In addition to selecting the optimal receiver coil, this information is sent to the transmitter to ensure that the proper transmit antenna coil is selected. The receiver amplifies the raw signal delivered by the antenna front-end, and provides filtering while downconverting to IF and baseband in a two stage conversion chain. The resulting baseband FM signal is demodulated to provide the digital data stream to the decoder.

The receiver consists of a Low Noise Amplifier (LNA), an Variable Gain Amplifier (VGA), two mixing stages, two filter stages, and a demodulator/detector stage. A block diagram of the receiver is shown below in Figure 2, followed by the receiver specification table and the frequency plan.

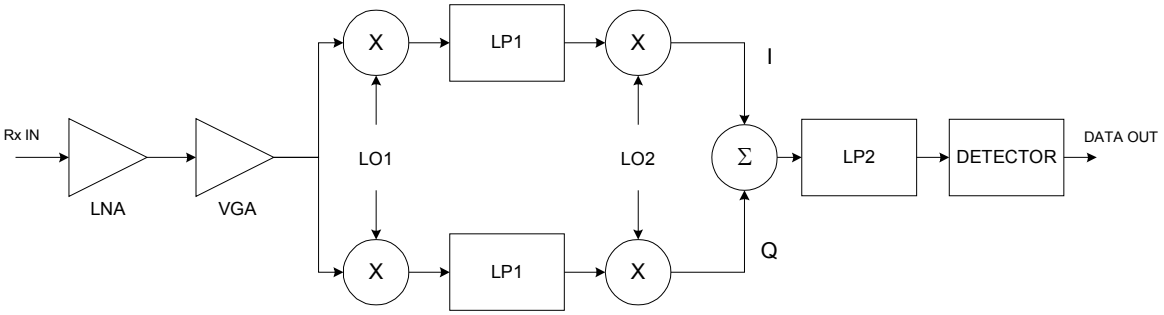


Figure 2: LibertyLink Receiver Block Diagram

Typical Receiver Parameters

Receiver		Min.	Typ.	Max.	Units
Carrier Frequency			13.559		MHz
Modulation	GMSK				
Channel Bandwidth			307.2		KHz
Dynamic Range			80		dB
Baseband Raw Data Rate			204.8		Kbps
Antenna Interface					
Tx/Rx Q			40		
Capacitor Range		1.5		24	pF
Weighting	Binary				
Input Resistance (High Gain)		25	50		KOhms
IF					
IF Frequency			500		KHz
IF Filter Type	Active Butterworth LPF				
Order			8		
Frequency Cutoff (3dB)			500		KHz
IF Coupling Filter Type	Passive HPF				
Order			2		
Frequency Cutoff (3dB)			50		KHz
Baseband					
Baseband Bandwidth			300		KHz
Baseband Channel Filter	Active Butterworth LPF				
Order			8		
Frequency Cutoff (3dB)			300		KHz
Baseband Coupling Filter Type	Passive HPF				
Order			1		
Frequency Cutoff (3dB)			25		KHz

The receiver operates according to the following frequency plan when the input signal appears at 13.5 MHz.

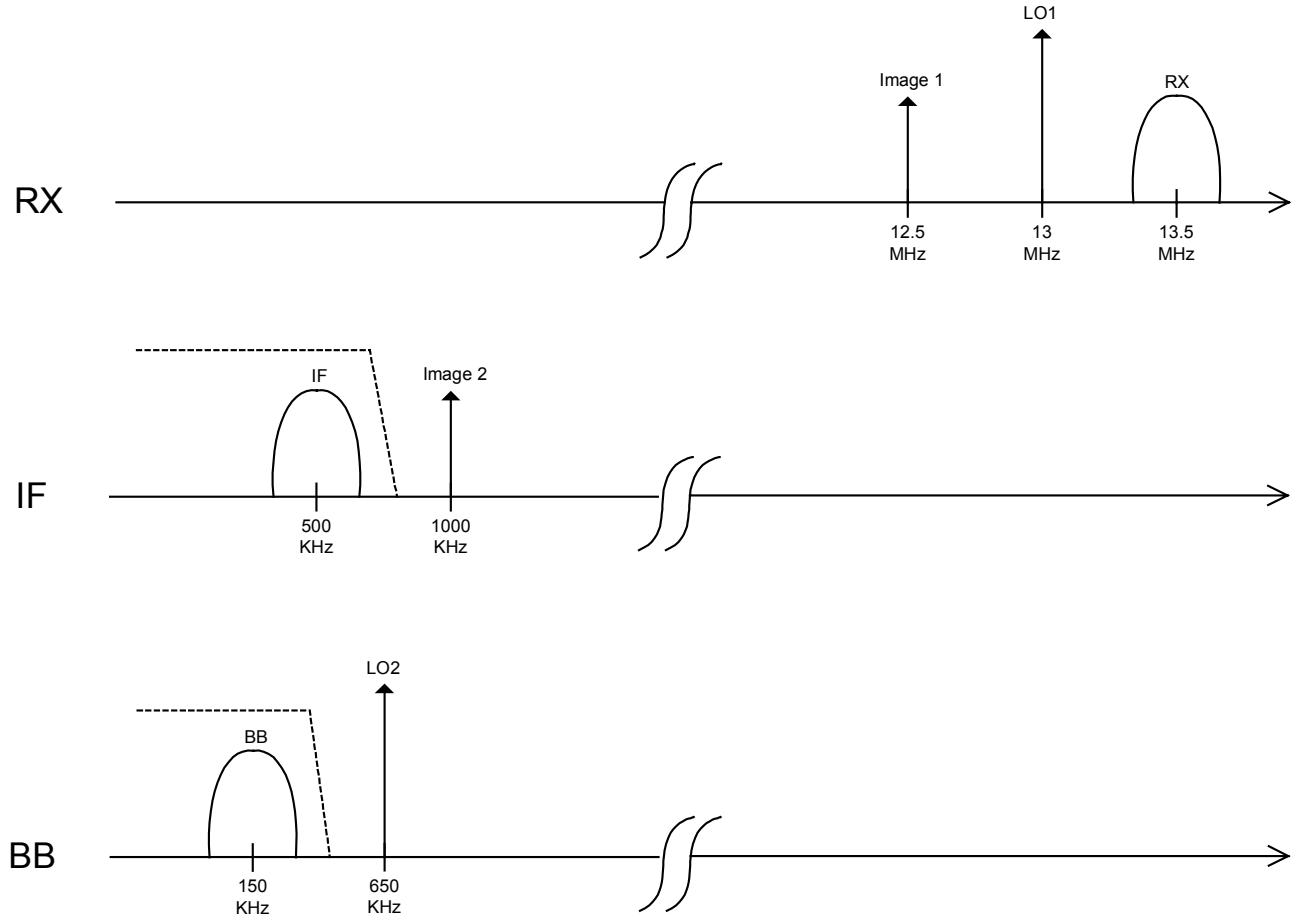


Figure 3: LibertyLink Receiver Frequency Plan

LNA VGA

Two gain stages, the Low Noise Amplifier (LNA) and the Variable Gain Amplifier (VGA), precede the image reject mixer. Both feature variable gain capabilities in order to address the 80dB dynamic range requirement. For small signals, the LNA provides 14dB of gain at 13.5 MHz. Due to the high signal levels experienced when system separation is small, the LNA incorporates signal attenuation circuitry. Since the maximum signal levels exceed the 1dB compression point of the LNA, attenuation is achieved by changing the input resistance of the receiver, resulting in a reduction in antenna Q. Two attenuation steps are possible, for a total of three effective LNA gain states of 14dB, 8dB, and -7dB. The VGA addresses further internal dynamic range issues. A maximum gain of 15dB can be reduced to -9dB in 10 steps.

IF strip

The IF strip consists of in-phase and quadrature (I&Q) conversion and filter chains that are summed and filtered.

As can be seen in the frequency plan of Figure 3, significant selectivity can be achieved through the use of a relatively low intermediate frequency and high-order low pass filters. Removal of all signal components at or below the LO1 frequency occurs after the subtraction of the second mixer quadrature products. At this point, further selectivity is achieved with additional low pass filtering at baseband (LP2).

Demodulator/Detector

The demodulator and detector scheme will be discussed later.

FIFO Buffers

From the demodulator, the serial data bits go through a serial to parallel converter and 8-bit words form a byte. The bytes are collected until a full frame is buffered. The frame is sent over the bus to the frame interleave where the data headers are stripped out. The remaining bytes, now comprised of audio only, are buffered in the audio FIFO and converted back to a serial bit stream. From here the serial bit stream moves to the CVSD decoder.

CVSD Decoder

Although not generally considered part of the receiver, the CVSD decoder is the final stage of the receive chain. The decoder, shown in Figure 4, receives a 1-bit 64Kbps digital signal that indicates the direction and values for two "leaky" digital integrators. The direction and values for the integrators are determined by the incoming bit value. The detection of four (4) consecutive 1's or 0's represents a condition called "slope-over/under load". It signals to the decoder that the estimate no longer has the same slope as the incoming signal and therefore, the integrators value (step-size) needs to be changed. The Syllabic integrator changes its step size up to a maximum value based on the sampling rate and the time constant. This bit also represents as direction (+ or -), based on the bit value of 1 or 0 respectively, of the Syllabic value as it is applied to the principal integrator. The output of the principal integrator feeds a 13-bit Digital-to-Analog Converter and a low-pass filter with an f_C of 3.7 kHz. The DAC output is a reconstructed version of the original baseband audio signal.

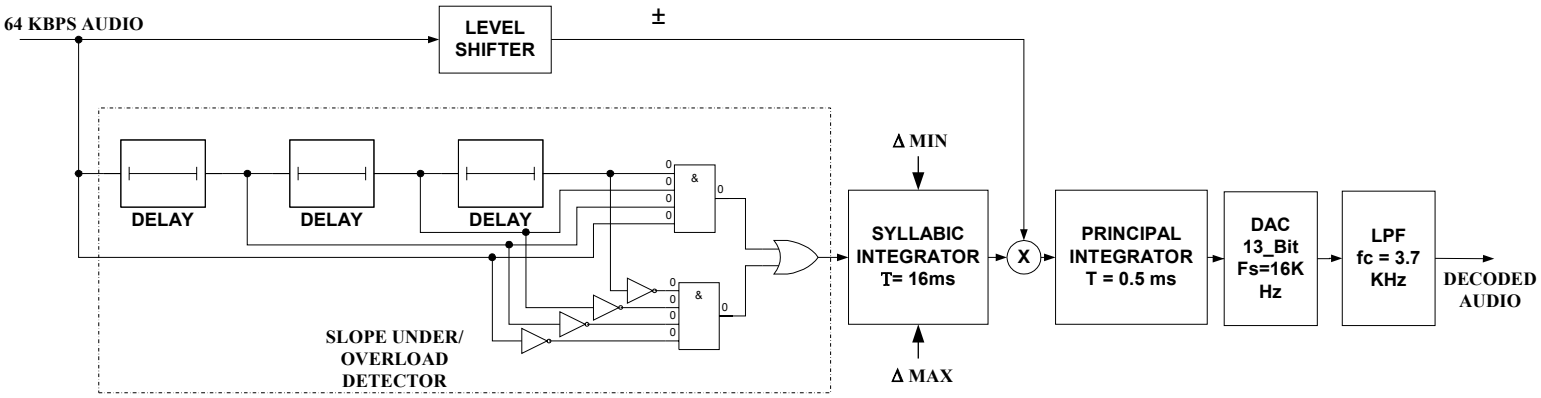


Figure 4: CVSD Decoder

Typical CVSD Decoder Parameters

CVSD Decoder		Min.	Typical	Max.	Units
Clock Frequency			64.251		KHz
Slope Over Load Length			4		samples
Syllabic Integrator Time Constant			16		msec
Input Data Path Width			13		bits
Principal Integrator Time Constant			.5		msec
High Side Frequency Cutoff (3dB)			3.7		KHz

Audio Output Stage

The final stage of the receiver chain is the Audio Output stage. The audio output stage shown in Figure 5 conditions the CVSD decoder's analog output so that it may be applied to a thirty-two ohm speaker or a line level audio input. Reconstructed baseband audio from the CVSD decoder is fed into a programmable frequency response shaping block. This signal is then summed with a tone generator. These tones can be used to signal the user that a low battery condition exists or other useful information. A user or microprocessor controlled variable gain amplifier follows for volume control. A speaker driver follows the variable gain amp to drive low impedance loads such as a speaker.

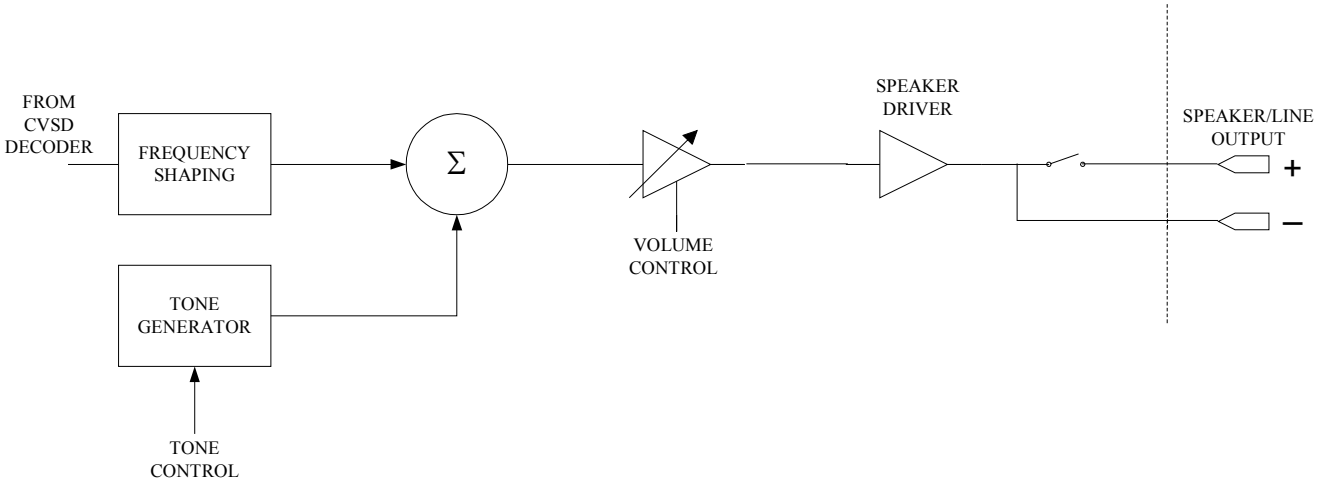


Figure 5: Audio Output Stage Block Diagram

Transmitter

The transmitter system consists of the audio input stage, CVSD encoder, a data register, Gaussian Sine/Cosine lookup ROM's , I-Q 8-bit DAC's, low pass filter stages, Gilbert cell upconversion mixers, anti-alias/squaring circuitry, and the Tx driver.

Transmitter activity begins when a signal is presented at the AUD_IN pin. The signal is gained up, filtered, presented to a 13-bit ADC and input to the CVSD encoder. The driver of the system is the GMSK transmitter shown in block diagram form in Figure 6. It takes the CVSD Encoder's 64 Kbps data stream as well as other data and combines them into a 204.8 Kbps GMSK square wave at the carrier frequency. The input data to the GMSK transmitter is buffered and 8X oversampled. This bit stream is applied to SIN and COS Gaussian lookup tables stored in ROM. It is here that the Gaussian prefiltering with a B_t of 0.5 is performed. The lookup table values for Sine and Cos are then converted to an analog signal by the switched capacitor 8-bit DAC's. Once filtered, the Sine and Cosine signals are filtered and upconverted to become 13.5 MHz I and Q signals. The I and Q signals are then summed, filtered, and squared through a comparator. This signal is then applied to the Tx Driver and fed to the transmitter front end. Below is the block diagram, specification table and a more detailed discussion of the individual blocks.

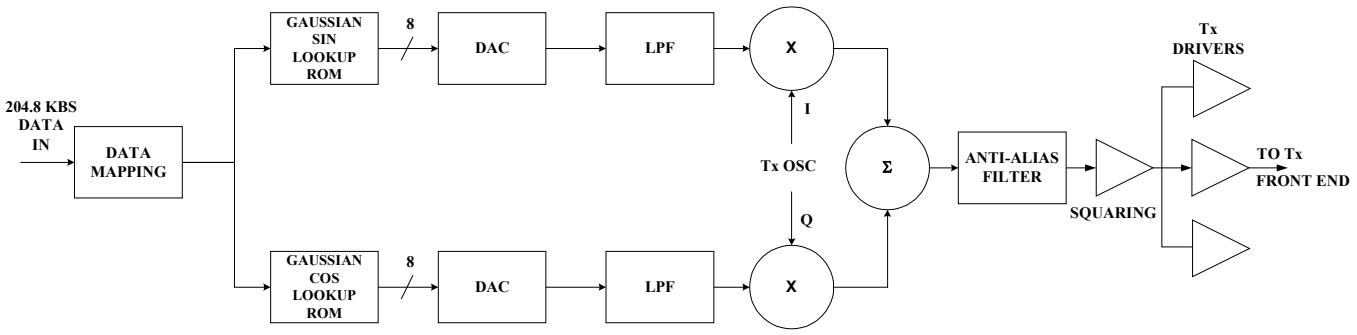


Figure 6: GMSK Transmitter Block Diagram

Typical Transmitter (GMSK Modulator) Parameters

Transmitter		Min.	Typical	Max.	Units
Carrier Frequency			13.559		MHz
Modulation Type	GMSK				
Gaussian Filter Constant (BT)			0.5		
Channel Null-to-Null Bandwidth			307.2		Kbps
Input Data Rate			204.8		Kbps
Encoding	Differential				
Data Oversampling Factor			8		samples / bit
Clock Frequency			1.6384		MHz
Baseband I-Q Filter Type	Butterworth LPF				
Order			4		
Frequency Cutoff (3dB)		165	175	185	KHz
Upconverter Carrier Frequency			13.5		MHz

Audio Input Stage

The audio input stage shown in Figure 7 allows either an electret/condenser microphone or audio line level signal to be used as a source for the wireless system. A preamplifier for use with low-level microphones can be switched in and out of the signal path. The level and frequency response of the audio input is programmed by the microprocessor to suit specific applications and operating conditions.

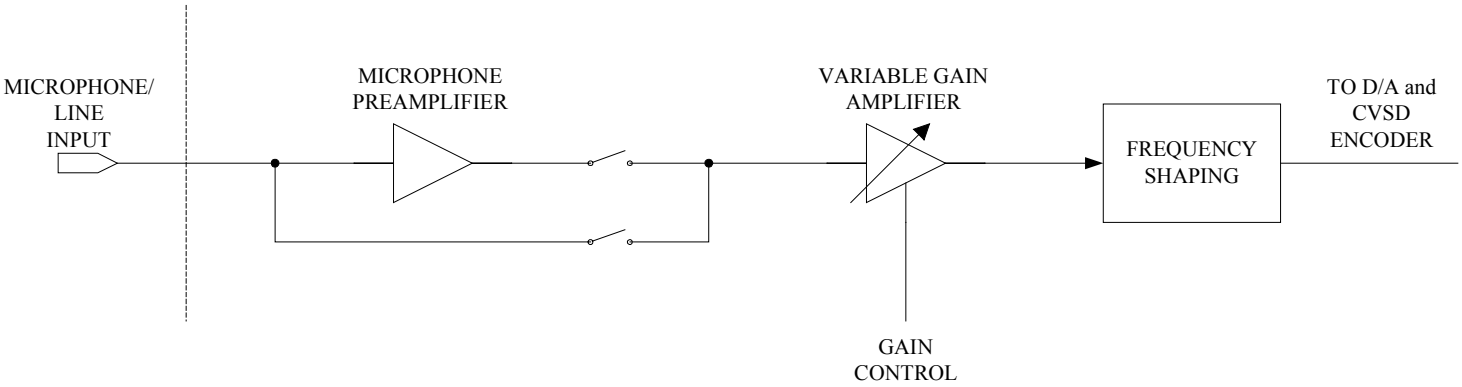


Figure 7: Audio Input Stage Block Diagram.

Typical Audio Line Input Parameters

Microphone/Line Input		Min.	Typical	Max.	Units
Microphone Preamplifier Gain – Headset Mode			28		dB
Microphone Preamplifier Gain – Base Mode			6		dB
Variable Gain Amplifier Gain Range		-10		+20	dB
High Frequency Cutoff (3dB)			3.7		KHz
Low Frequency Cutoff (3dB)			150		Hz

CVSD Encoder

To encode the baseband audio signal, the signal from the audio input is fed to a continuously variable slope delta modulator (CVSD), as shown in Figure 8. This type of digital encoder is used so that an optimal quantization resolution is achieved for any given amplitude of the signal to be encoded. By doing this, quantization noise at low signal levels can be reduced while keeping the data rate low even when large amplitude signals are encoded.

In the encoder, the audio signal is bandwidth limited by a low pass filter with an f_C of 3.7KHz. This signal is then compared to an estimated signal generated by the same type of CVSD decoder that is used at the receiving end of the wireless link. Thus the audio information is represented by a serial bitstream that represents the error between the actual audio signal and its estimated digital representation.

The digital data is collected in the audio buffer, converted to a parallel byte and shipped to the frame interleave where the headers are incorporated. The full frame, payload plus overhead, is sent back to the Link FIFO and is ready for modulation.

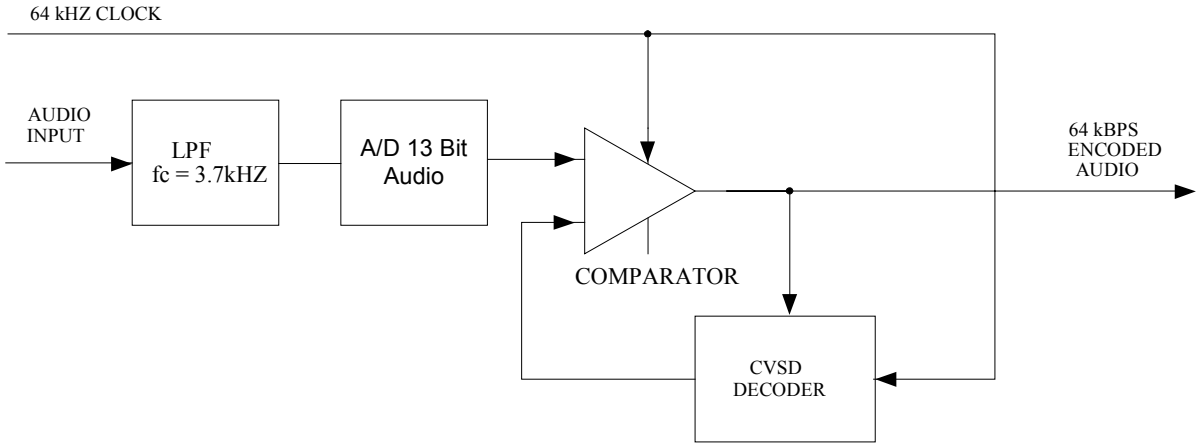


Figure 8: CVSD Encoder

Typical CVSD Encoder Parameters

CVSD Decoder		Min.	Typical	Max.	Units
Clock Frequency			64.251		KHz
Slope Over Load Length			4		samples
Syllabic Integrator Time Constant			16		msec
Input Data Path Width			13		bits
Frequency Cutoff (3dB)		3.0		6.0	KHz

Data Mapping

This block maps the 64Kbps encoded audio data along with other digital data into the I-Q plane based on three samples worth of input data. Mapping into the I-Q plane creates an address for the ROM lookup table. The two most significant bits (MSB) indicate which quadrant of the I-Q plane the data is coded in. The three middle bits indicate last, current, and next data samples. The three LSB's describe the phase angle within each quadrant. Thus each LSB represents 11.25 degrees. This information is used in the ROM table to define the trajectory between constellation points.

Gaussian SIN/COS Lookup ROM

The function of this block is to filter using a Gaussian (B_T=0.5) response and sin/cos lookup the angle output from the data mapper. Gaussian filtering allows spectrally efficient transitions between I-Q constellation points as the data is transmitted.

The output of each table is an 8-bit word. The MSB represents the sign of the signal and the lower seven bits represent the magnitude.

DAC/LPF

Once the data has been Gaussian filtered and Sine/Cosine looked-up, the two 8-bit outputs are converted back into an analog signal. The DAC performs this function using the 3 MSB for a resistor ladder and the lower 5 bits in a switched capacitor array configuration. A low pass filter smoothes and bandwidth limits the DAC output before transmission. This filter is a 4-pole passive network with a 3dB bandwidth of 175kHz.

Upconversion

Once the baseband data has been modulated, it is mixed with the I-Q carrier clocks. In LibertyLink, the default carrier is 13.559MHz.

The in-phase (I) signal chain is mixed with the Tx-I oscillator. The Tx-I oscillator is a square wave at the carrier frequency. Similarly, the quadrature (Q) signal path is mixed with the 90 degree shifted Tx-Q oscillator. The outputs of the I and Q mixers are then summed. The result is a GMSK signal centered at the Tx oscillator carrier frequency.

The mixers themselves are of the linearized Gilbert cell configuration and the output current of the I and Q mixers are summed on a resistor.

Smoothing Filter

The smoothing filter is a pseudo 2-pole, low pass, passive filter with a 14.5 MHz cutoff. It serves to remove unwanted frequency components from the upconverted signal.

Squaring

The squaring circuit is a high-bandwidth comparator which converts the GMSK modulated sine wave output of the smoothing filter into a 50% duty cycle, GMSK modulated square wave.

TX Drivers

The TX driver is comprised of three parallel low output impedance buffers used to amplify the transmitted signal before it is applied to the antenna front end. The driver is also part of the resonant transmitter coil circuit. During receiver operation the output of the driver is switched into a high output impedance state. Power control to the front end is achieved by switching parallel drivers of different channel resistances in and out of the circuit.

Synthesizer/Timing

The Synthesizer/Timing subsystem generates frequencies that represent 4X the in-phase and quadrature TX-LO, RX-LO1, and RX-LO2. These signals are divided down locally in the transmit and receive sections for the I & Q clocks. Figure 9 shows a block diagram of the basic synthesizer. Individual on-chip synthesizers are required for each local oscillator.

The synthesizer uses the classical phase locked loop (PLL) topology. A 9.8 MHz crystal oscillator is the stable frequency reference for each loop. A frequency divider of value N divides the clock and is fed into one input of a digital phase detector. The output of the phase detector is a charge pump and represents the frequency error of the loop. So that the loop is stable under all operating conditions, a simple on-chip capacitor filter network with a stability compensation resistor is used to condition the error charge before it is applied to the VCO. Note that the Tx and LO1 loops have a different VCO scale factor than the lower frequency LO2 loop. The digital output of the VCO is then divided down in frequency by a factor M and fed into the other input of the phase detector. Since a PLL is a closed loop system, the output frequency of the VCO is the frequency of the crystal reference multiplied by M/N.

A wide range of Tx and LO frequencies are programmable using the 12 and 8-bit resolution of the frequency scaling factors M and N. The output of the VCO is actually a factor of four higher than the desired frequency. This allows the I/Q logic section to create 50% duty I and Q signals at the appropriate frequency.

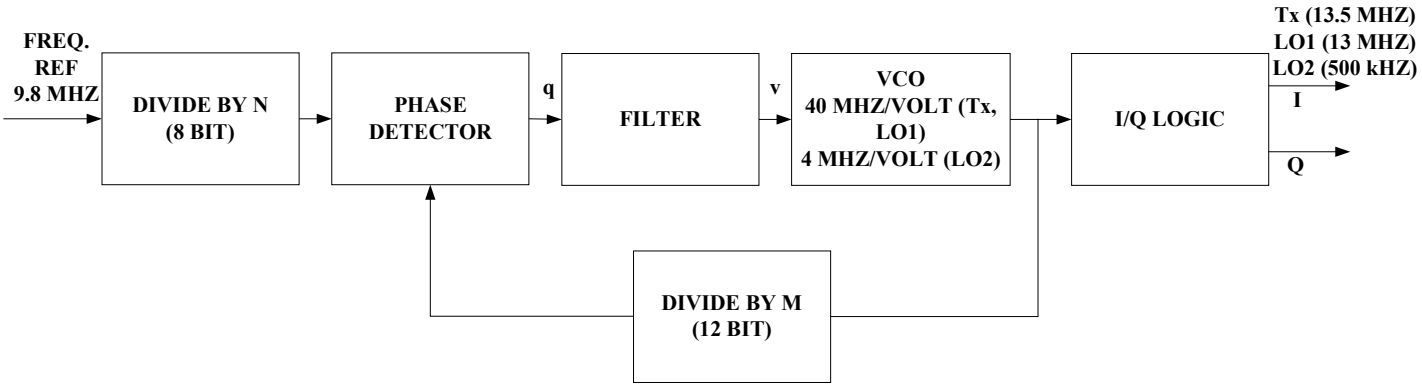


Figure 9: Synthesizer Block Diagram

Microprocessor/Control

The Microprocessor/Control subsystem, shown in Figure 10, performs all control logic, data management, and timing functions in the system. A control program resides in an external EEPROM. This program determines virtually every aspect of system operation and is executed by the microprocessor core.

Microprocessor Core

The microprocessor core is an 8-bit, 8051 processor. The processor is capable of addressing external data/program memory to fill the 5K pagable RAM. Internal memory consists of 8 general purpose registers and an arithmetic logic unit. A second set of general purpose registers are utilized during interrupts to minimize the context switch time. These design improvements yield a performance gain of 6X over the original 8051 architecture.

Audio I/O Controller

The Audio I/O Controller manages the audio buffer memories. In addition to these functions, the controller also sets the gains of the audio inputs and outputs, performs muting functions, controls the frequency response of the various programmable audio filters and generates the I/O sample rate.

Memory Management Unit

The MMU controls the data transfer between the TX/RX buffers, the audio I/O buffers, and the frame interleave memory. Its transfer rate is in excess of 1Mbyte per second. Byte interleave for encoding data and audio frames is programmable.

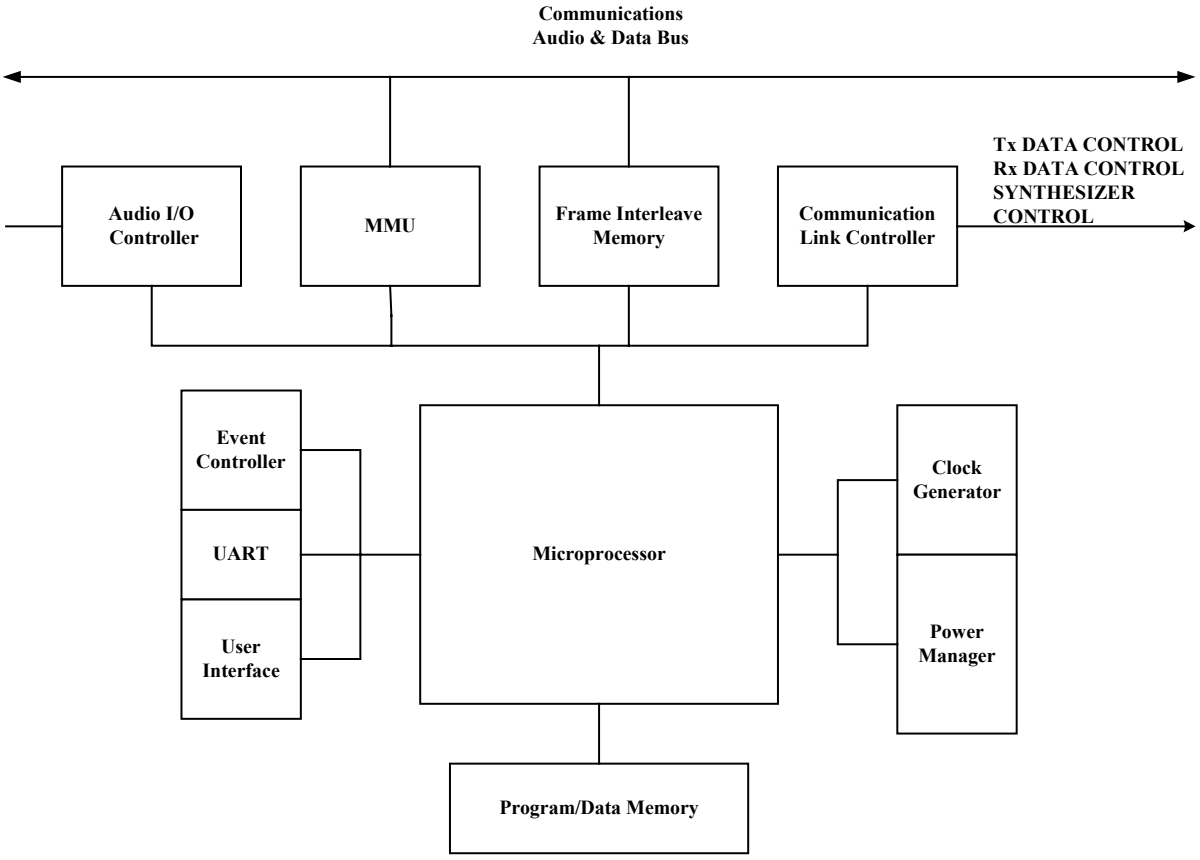


Figure 10: Microprocessor/Control Block Diagram

Frame Interleave Memory

The frame interleave memory is a 1K x 8 dual port type. Both inbound and outbound audio data are buffered prior to encoding during transmission and decoding prior to conversion. In doing this, the interleave memory forms a bridge between the CPU bus and the Audio/Data bus.

Link Controller

The Link Controller is a programmable state machine that controls the transmitter and receiver logic. It selects the proper transmitter and receiver coils (Only one coil either transmits or receives at a time) based on both base and remote unit received signal strength indicator (RSSI). Receiver gain and transmitter power levels are also controlled by this block. Base/Remote synchronization status and RSSI are also monitored.

The Link Controller also performs data formatting functions such as selecting the bit rate and packet length.

Event Controller

The Event Controller synchronizes external events to the CPU clock. It also serves as a real-time clock and provides programmable system timers. Events, such as a change in the RX and Audio buffer levels or the receipt of a frame, can trigger an interrupt.

User Interface

The user interface consists of three digital and one test I/O lines that can be programmed to perform a variety of functions. These lines can be connected to pushbutton switches for volume and mute functions, or to external signals such as “switch hook”. LED’s can also be driven.

Program/Data Memory

During system operation the main program is transferred from the external EEPROM to the Program/Data memory. All of the temporary data that the system creates during operation is stored in this block. This includes transmitter power levels, channel information, etc.

Clock Generator

This section generates all of the clock references used throughout the system that are not generated by the frequency synthesizer (e.g. LO1, LO2, Tx).

Power Manager

The power manager shuts down various parts of the chip depending on the operating mode.

Band gap Reference

The system needs a voltage and current reference to perform its myriad of functions. A band gap reference is used as the voltage reference in the system, from this voltage all of the reference currents are derived.

Off-Chip Functions

Front-end

The Front End block diagram is shown in Figure 11. The transmit portion of the front-end converts the GMSK square wave output into a sine wave current in the antenna coil. This current through the antenna creates a modulated signal at the air interface. For receiver operation, the front-end must also convert the incident magnetic field from the transmitting unit into a voltage signal that can be measured and demodulated.

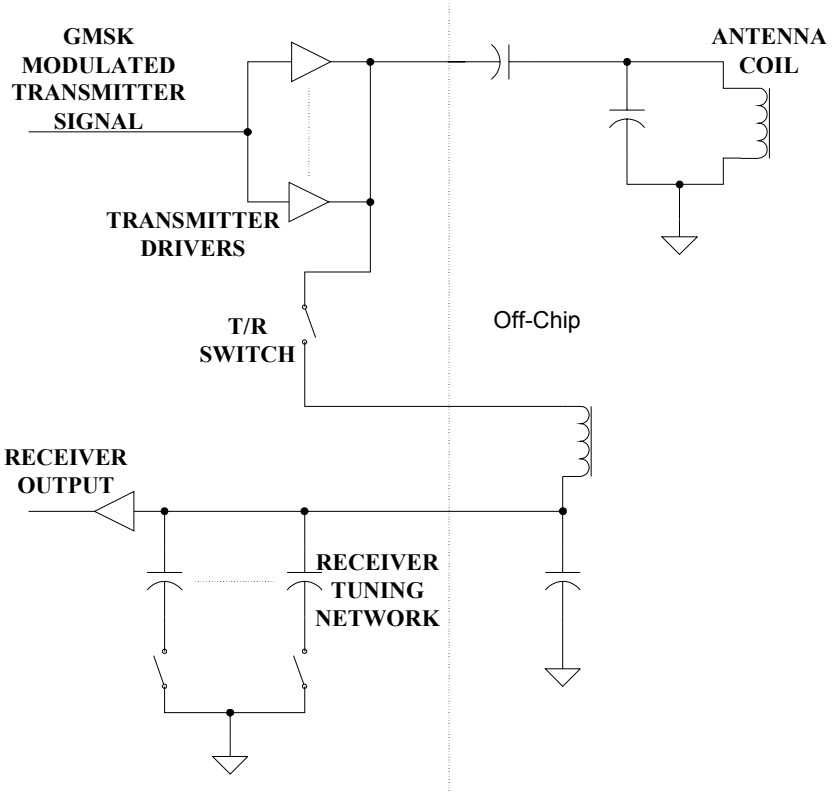


Figure 11: Front End Block Diagram

Since LibertyLink is a TDD system, the front end must be configured to alternately transmit and receive in synchronism with the remote unit. During a transmit frame, the T/R switch is open and the transmitter driver applies a 50% duty GMSK modulated square wave to the transmitter tuning network. This front-end network, the antenna coil, and some impedance scaling capacitors form a band pass filter that is centered at the carrier frequency. The result is a GMSK modulated sine wave coil current.

During receive mode, the low impedance of the transmitter driver must be removed from the circuit. This is accomplished by setting the drivers to a high output impedance state. The T/R switch is closed and the receiver tuning network, using the calibration information for the channel in use, switches the capacitors into the circuit that gives the highest signal amplitude. In this mode, the series tuned band pass response of the transmitter path has been converted into a purely parallel band pass response.

Crystal Reference

The 9.8304 MHz crystal oscillator shown in Figure 12 is the stable frequency reference for the system. An on-chip, low gain inverter is used as the oscillator amplifier. Specific values for all external passive components depend on the type and manufacturer of the crystal. A higher gain buffer squares the oscillator output and distributes it throughout the chip.

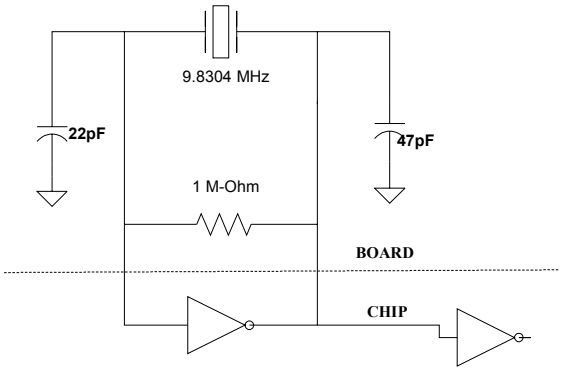


Figure 12: Crystal Reference

Overall System Operation

Both the base and remote unit can be in one of two basic operating modes; Active (On) or Standby (Off). Both of these modes have several sub-modes of operation. For the purposes of this explanation it is assumed that the base and the remote unit follow the same algorithms for link control even though they may execute some of the details differently.

These modes are primarily concerned with establishing a link between the base and the remote unit. A link is established when the base and the remote unit have detected each other's magnetic signal and have synchronized their transmit and receive frame timing.

Standby
As soon as battery power is applied to either a base or remote unit, it immediately goes into standby mode, that is, it begins to search for either a base or remote unit to link with. In standby, the unit continually searches for a mating unit. It draws about 150uA in standby.

Active
A system is referred to as "active" if a base and remote unit have synchronized their data transmission. The modes of operation when the system is linked are described below.

Active
The mode of the headset/base while in typical use. In this mode bi-directional audio communication occurs. The headset leaves this mode if it goes Out of Range or if the Flash switch is pressed (Flash is equal to pulling up the D0 line). The base leaves this mode if the headset goes Out of Range.

Out of Range
If the headset and base are in communications and they are separated beyond 1.25 meters, they go into Out of Range mode. The headset will beep to signal Out of Range and the user has eight seconds to move back into range. If communications is not reestablished within eight seconds, the headset and base go into standby.

Frame Timing and Partitioning

In a TDD system, such as this, the base and remote units alternately transmit to one another in synchronism. Each burst of transmitted data is referred to as a slot. A slot contains primarily the digital representation of the audio signal that is being transmitted, but it also contains information that must be shared between the base and remote unit.

Each level of data organization is described in more detail below. See Figure 13 for framing diagram.

Frame (4,896 bits)
A frame consists of a sequence of four receive/transmit slot pairs with a smaller 'diversity' slot, followed by four more RX/TX slot pairs and a final diversity slot. A total of 18 slots are in a frame, of which eight are RX, eight are TX and two that are used to transmit the antenna diversity information.

Using a 4.88μs bit, a frame is $(4.88*10^{-6})*4896$ bits = 23.89ms, or 41.8 frames per second. Therefore, each frame has a (41.8 frame/second) * (4,896 bits/ frame) = 204.8 Kbps raw data rate. This data rate can be partitioned via the firmware into several configurations. Most commonly, for full duplex voice, the frame can handle 64kbps of transmitted and received audio.

Slot
Each slot contains 296 bits. This slot width along with the frame timing is controlled by the firmware. The majority of the bits (62%) in each slot represent the encoded audio and data. All other bits are used for command, control, and error correction/detection. Each of these is discussed below.

Guard (G, 16 bits)
This collection of bits serves as a buffer between slots. Lasting 78μs, it allows synthesizer and front end transients to decay before data processing begins.

Preamble (PR, 24 bits)
The preamble is an "up-down" bit sequence of alternating ones and zeros. It serves to identify the transmitted slot as valid and allow for receiver synchronization.

Synchronization (SYN, 16 bits)
These bits are randomly coded and serve to synchronize the receiver to the incoming data.

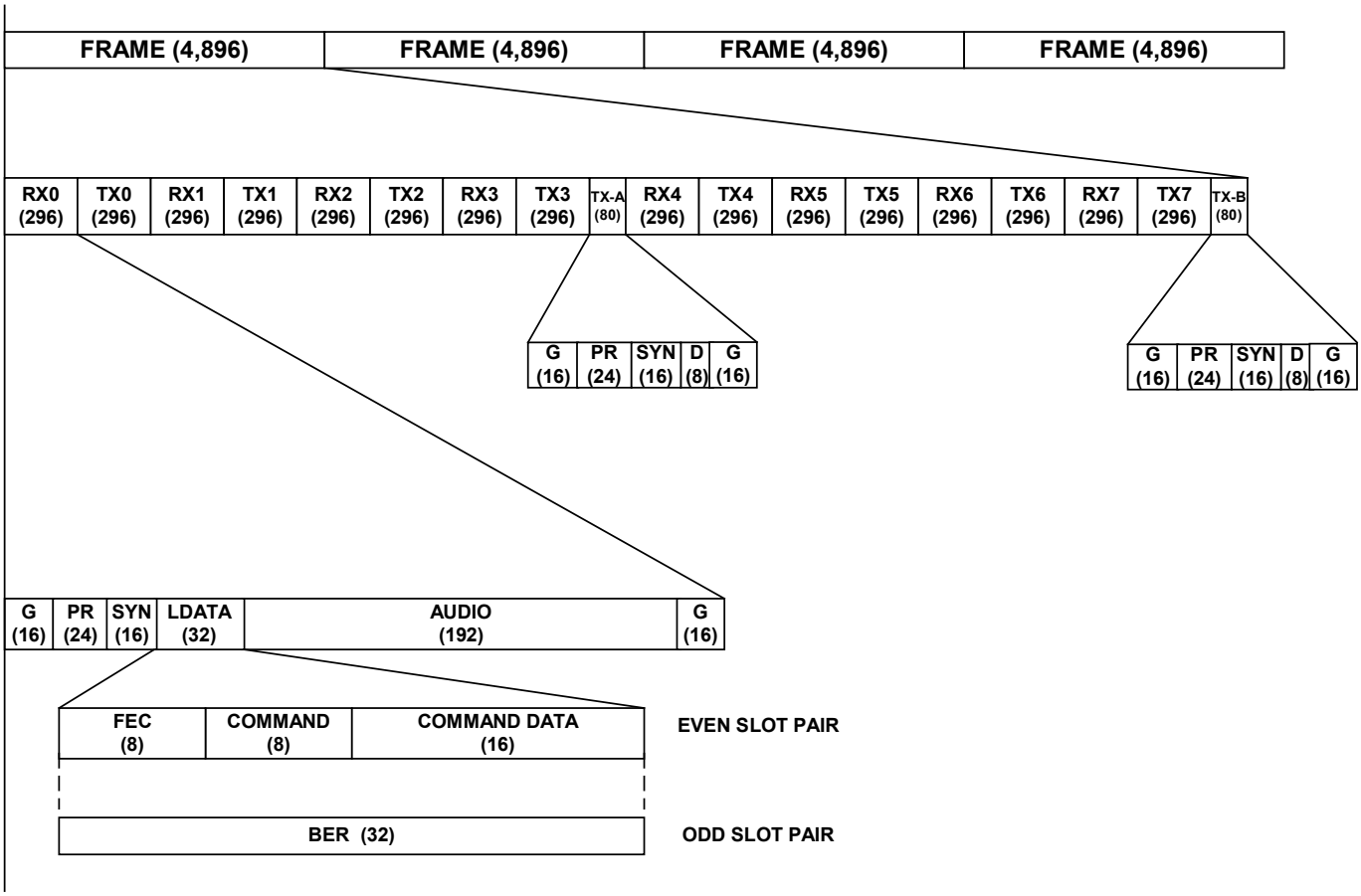
Forward Error Correction (FEC, 8 bits)
Bits reserved for forward error correction of the Slot ID, Command, and Command Data.

Command (8 bits)
The command bits identify a specific command that is to be executed by the remote unit. For example, a change in the remote unit transmitter power level might be commanded.

Command Data (16 bits)
If a quantity is associated with one of the above commands, it will be transmitted by these 16 bits. In the case of a change in the remote unit's transmitter power, these bits would specify the level.

Bit Error Rate (BER, 32 bits)
In this system, it is important to constantly monitor the performance of the wireless link. Bit error rate can be used for this purpose. Here, a 32-bit sequence is known by both the base and the remote unit. By comparing the received BER data with the known sequence, bit error rate can be calculated. Note that the BER takes place during the odd slot pair while the above FEC, Command and Command Data use those 32 bits during the even slot pair.

Audio (192 bits)
These bits represent the CVSD encoded and randomized audio data. Recall that the audio is encoded at approximately 64 Kbps. Since one side of the system transmits only half the time, enough data must be in this 192 bit interval so that the user will not perceive an interruption in the audio. This 192 bit payload is divided into 24 eight bit words.



FRAME TIMING
(LOW DELAY AUDIO)

Figure 13: Typical Framing Diagram for Point-to-Point Voice Applications

Firmware

The LibertyLink chip contains only a boot ROM and relies on an off-chip EEPROM for operating instructions. At power up, program code and data is automatically uploaded into LibertyLink's 5K pagable RAM. This firmware is furnished to customers by Aura. This firmware can be burned into the EEPROM (Microchip 24AA64-I/ST) using a Data I/O Optima EEPROM writer.

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All specifications in this document are based on a reference headset design using a 4 x 45mm ferrite antenna and a base unit that uses 4 x 10mm ferrite antennas. Varying the dimensions of these antennas will affect performance.

This document is intended to facilitate the use of the LA116 Integrated circuit that is defined in the Product Specification. All operating parameters and product descriptions are provided as design aids and must be validated at each customer's technical team