Micromodem Analog Input Board v1.1 Hardware Documentation

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This document describes the hardware for the micromodem's external analog input board, providing additional explanation and description of its circuit schematics. The external analog input board supports up to eight hydrophone receive channels in two banks of four. Sampling rates of up to 250 ksample/sec/channel are supported for four channels, and up to 125 ksample/sec/channel for eight channels. The board supports voltage-mode hydrophones at 3.3V and 4.5V. An additional power, conditioning, and termination circuit is required for current-mode hydrophones.

TABLE OF CONTENTS

MUX/ADC:

Rather than using a multi-channel analog-to-digital converter (ADC), or multiple ADCs, the analog input board uses a single high-speed ADC. The eight input channels are stepped through in order with a multiplexor (mux), and each one in turn is connected to the ADC to be sampled.

The ADC, U7, is an Analog Devices AD7475BR, a 12-bit, 1Msample/sec converter. When switched over four channels, the ADC can sample at up to 250ksamples/sec per channel; over eight channels, 125ksamples/sec per channel.

The mux, U6, is an Analog Devices ADG708 8-to-1 analog mux. The mux is break-before-make, so temporarily its output is high-impedance before switching to the next channel. Because of this, the mux output is tied to 1.25V via pullup R2. This is because 1.25V is the midpoint of the ADC (range: 0-2.5V), effectively the zero value.

Op amp U8, a Burr-Brown OPA350, is a very high-speed, high-slewrate op amp, to accommodate potentially large changes from one mux channel to the next, while driving the input to the ADC. The signal path from op amp U8 to ADC U7 has a low-pass filter (R141, C136) with a very high-frequency rolloff (order 10 MHz) to dampen any ringing which might occur after the op amp buffer.

The mux can step through the low four channels (1-4), the high four channels (5-8), or all eight channels. The mux select lines, A0-A2, are generated primarily by counter U1, which is incremented when EXPFS goes high, for each ADC sample. The control register bits 4HI and ALL8 determine whether the mux steps through channels 1-4, 5-8, or 1-8, and so NAND gate U2 modifies the output of counter U1 appropriately based on the control register state. The mux select lines are incremented when EXPFS goes high, i.e. when the ADC is deselected after a sample, allowing the signal from the new channel to settle before it is sampled.

DSP and Software Interface:

The ADC is a SPI serial peripheral, and is connected to McBSP#0 on the micromodem's DSP. McBSP#0 is set up in software to generate clock EXPCLK and frame sync EXPFS, dividing down the DSP's internal clock.

The sample word format of the 12-bit ADC is four leading zeros, followed by the 12 bits of the data word. To verify that samples are not dropped, we wanted a tagbit to be inserted into the datastream, marking the first of the four (or eight) channels. The value for this tagbit is generated from the mux select lines by gates U38 and U2D, along with U4A and flip-flop U5. The tagbit is inserted into the datastream immediately after EXPFS goes high (and the ADC tristates its SDAT data pin), using NAND gates U4B,C,D. R1 provides a pulldown when SDAT is tristated. In software, McBSP#0 inserts an extra bit delay. This extra delay drops the first leading zero from the ADC's data word, so the sample word becomes three leading zeros, followed by 12 bits of data, followed by the tagbit. The tagbit is one for the lowest channel, zero otherwise.

The DSP's steps for initializing a new stream of data include:

1.) Loading the correct values into the McBSP#0 registers

2.) Setting EXPDO to 1. This enables counter U1 and flip-flop U5, allowing them to come out of reset. (EXPDO is McBSP#0's data out pin, in general-purpose I/O mode. On the analog input board, it is labeled CTREN.

3.) Enable frame sync EXPFS. At this point, repeated strobes of EXPFS will start the ADC sampling and the mux stepping. On the micromodem mainboard, DMA transfers will start from the McBSP#0 port into data memory, with the first sample synced to the tagged lowest channel.

ANALOG INPUT, CHANNELS 1-8:

Each of the eight input channels has an identical filtering and amplification path. The programmable-gain amplifier, however, can set the gain for each channel independently.

The analog input filtering consists of an AC-coupling high-pass filter (C25, R44 for channel 1; all subsequent components labeled in this section will be for channel 1), followed by a fixed gain stage, U22A. At high gains, amplifier U22A includes a high-pass filter. A programmable-gain amplifier is next, built around U22B. C28 provides stability in case the traces to the digital potentiometer are a little long. C30 provides some high-pass filtering for higher gains, as C29 does for the fixed-gain stage. The final filtering done is to pass the signal through a 4-pole Sallen-Key low-pass anti-aliasing filter, configured as a Butterworth filter. The outputs of the anti-aliasing filters, AIN1, etc, go directly into the mux as analog inputs.

CONNECTORS:

There are connectors for the micromodem mainboard signals, the hydrophones, and for a flash memory board.

JP1 Micromodem connector:

The signals from the micromodem are for two SPI serial ports, high- and low-speed. High speed: EXPFS, EXPCLK, EXPDI; EXPDO used as general-purpose I/O as CTREN, a reset line for the mux/tagbit state. Low speed: SCLK, SDO, SCLK; SDI unused. The high-speed port is used for the ADC; the low-speed port is used for both the control register (selected by EXTSEL1), and for the programmable-gain amplifier potentiometers (selected by a line in the control register).

JP2 hydrophone connector:

The hydrophone connector includes eight channels of inputs from voltage-mode hydrophones, as well as four shared grounds and several voltage supplies. The voltage supplies are the independently-switched 3.3V supplies +VPRE1 and +VPRE2, and supply +VLR, which comes from the linear regulator on the power supply page (usually 4.5V, to support the REMUS USBL head).

In addition, this connector has pins for a battery connection, to supply the +VLR linear regulator. The regulator is internally protected against reverse-voltage connections.

Although JP2 is one 18-pin connector, it can be thought of in several sections:

First is the power input, pins 1 and 2, which are +VB and GND. These are intended to connect to a battery, to supply legacy voltage-mode hydrophones via linear regulator U41 (U41 is adjustable; it will typically be used with a 4.5V or 5V output on +VLR). A battery only needs to be connected to these pins if the phones are not 3.3V voltage-mode phones.

The second set of signals on JP2 are for hydrophones 1-4, pins 3-10. These signals are analog signal (voltage) inputs from the phones (pins 3, 4, 7, 8). Pins 5 and 6 are grounds. Pin 9 is +VPRE1, a switchable 3.3V rail for supplying 3.3V voltage-mode phones. Pin 10 is +VLR, a switchable rail for supplying legacy voltage-mode phones (such as the REMUS USBL head, which uses voltage-mode phones operating from a rail above 4.5V).

Finally, hydrophones 5-8 use pins 11-18 as described above for phones 1-4. (Pins 11, 12, 15, 16 are analog signal (voltage) inputs. Pins 13 and 14 are grounds. Pins 17 and 18 are +VPRE2 and +VLR switchable power supply rails.)

Although +VPRE1 and +VPRE2 are independently-switchable rails for each bank of four phones, +VLR is shared between both banks.

Cables connecting to JP2 might break out into three bundles, corresponding to the signal sets described above in this section, or might remain as a single bundle, depending upon the application.

JP6, JP8 flash memory connectors:

These connectors provide a pass-through for signals from the micromodem mainboard to an external flash memory board. None of these signals is used on this board.

CONTROL REGISTER:

Included in the control register are enable lines for the switchable power supplies (+VA, +VPRE1, +VPRE2, and +VLR); the programmable-gain potentiometer chip select line /PGASEL; and mux switching settings 4HI and ALL8.

The control register itself is an SPI peripheral composed of discrete parts. It is selected by EXTSEL1 going high, data is shifted into shift register U13 from data pin SDO, and the shift register contents are latched into parallel register U12 when EXTSEL1 returns low.

Control register bits controlling mux switching (all reset to zero):

4HI	ALL8	Mux switches through channels:
0	0	1-4
1	0	5-8
X	1	1-8

PGA POTENTIOMETERS:

There is an independently-controllable programmable-gain amplifier for each of the eight input channels. This is implemented with two 4-channel digital potentiometers, U20 and U21, Analog Devices AD8403s.

The pots have 256 steps to go from zero to full scale (50k), on each of 4 channels. They are SPI serial devices, with the data word being the 2-bit address of the channel, followed by an 8-bit potentiometer value for that channel. The SDO data out line for U21 is actually the input (with a pullup R140, as SDO is open-drain) for U20. Potentiometers values written to U21 will get passed through to U20 in such a way that all eight potentiometers can be set independently. See the AD8403 datasheet for more details.

POWER SUPPLY :

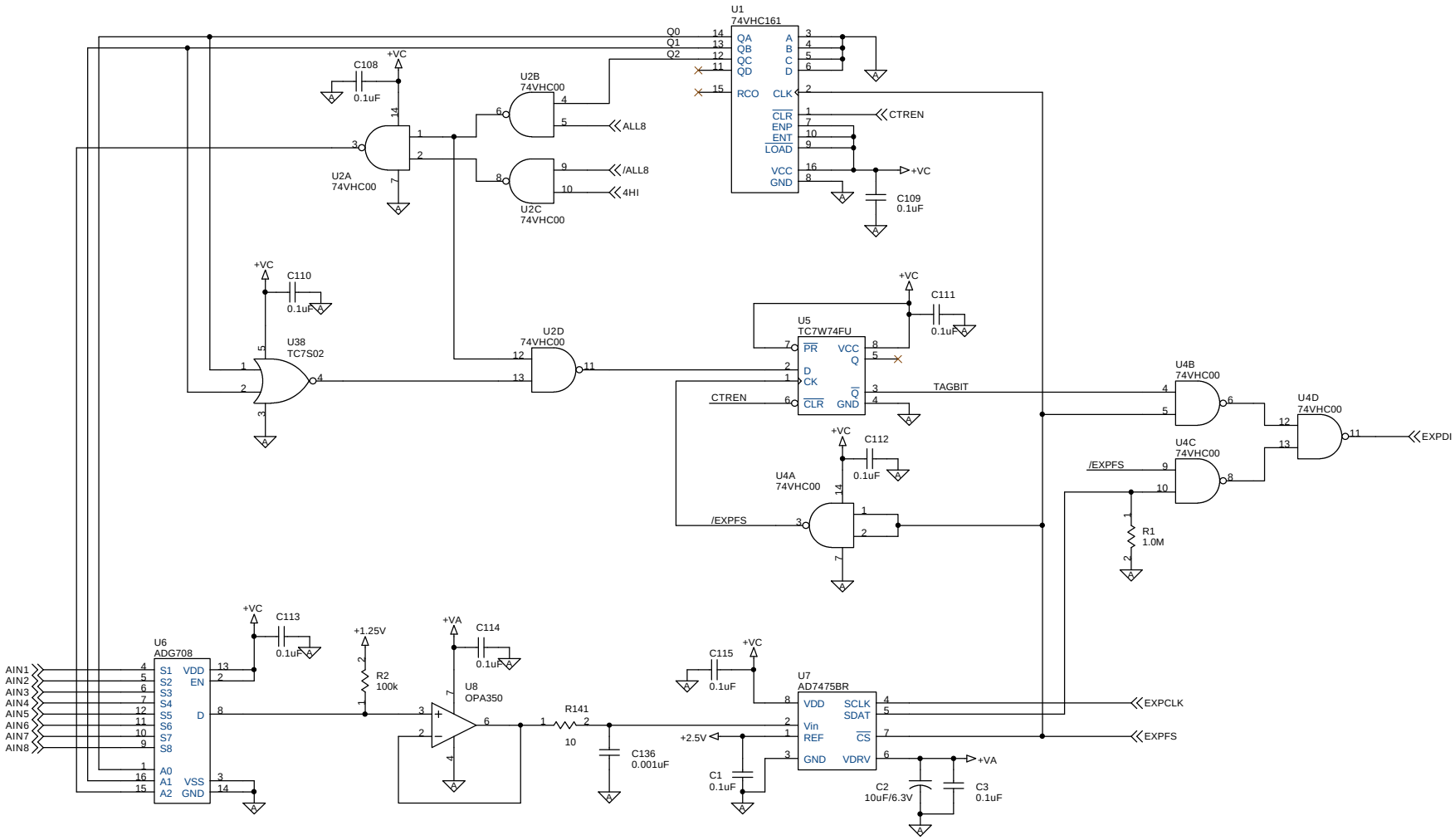
Conceptually, the main part of the power supply is the set of three switches for power supply rails +VA, +VPRE1, +VPRE2. +VC powers all of the digital logic, but various higher-power analog parts can be switched off: the high-speed op amp U8 and the voltage reference rails are switched by VA_ON; VPRE1_ON and VPRE2_ON switch +VPRE1, +VPRE2, which are the preamp/filter power supplies for the two banks of channels, 1-4 and 5-8. In addition, +VPRE1, +VPRE2 are the 3.3V voltage-mode supplies for the hydrophones.

The ADC has its reference set by the 2.5V zener diode U45, which is then divided in half and buffered to become the 1.25V reference used as a midpoint value via pullups in each of the channel's preamp stage, as well as immediately following the mux.

The 1.25V reference has an op amp buffer, as opposed to the 2.5V reference, due to its higher current load.

A linear regulator, with voltage input from a battery, provides the 4.5V rail needed for the REMUS USBL head, +VLR.

Finally, a reset part clears the control register on power-up. The only other state stored on this board is in the mux/tagbit generation logic, and is cleared by the CTREN line (EXPDO).



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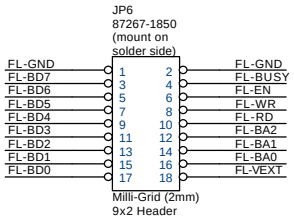
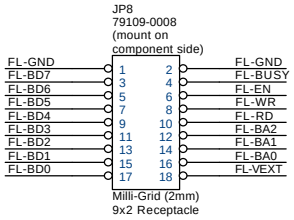
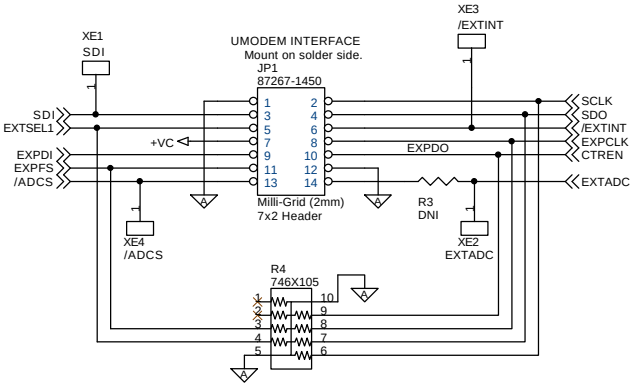
Size B	Document Number 241002-1	Rev V1.1
Date: Thursday, March 20, 2003	Sheet 1 of 9	

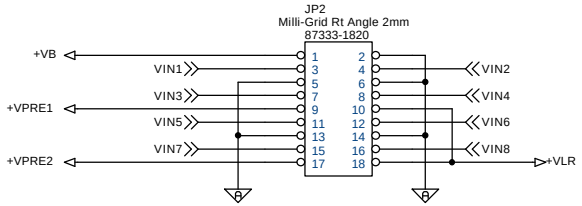
FLASH PASS-THROUGH







The following nets are not connected:
/ADCS, /EXTINT, EXTADC, SDI



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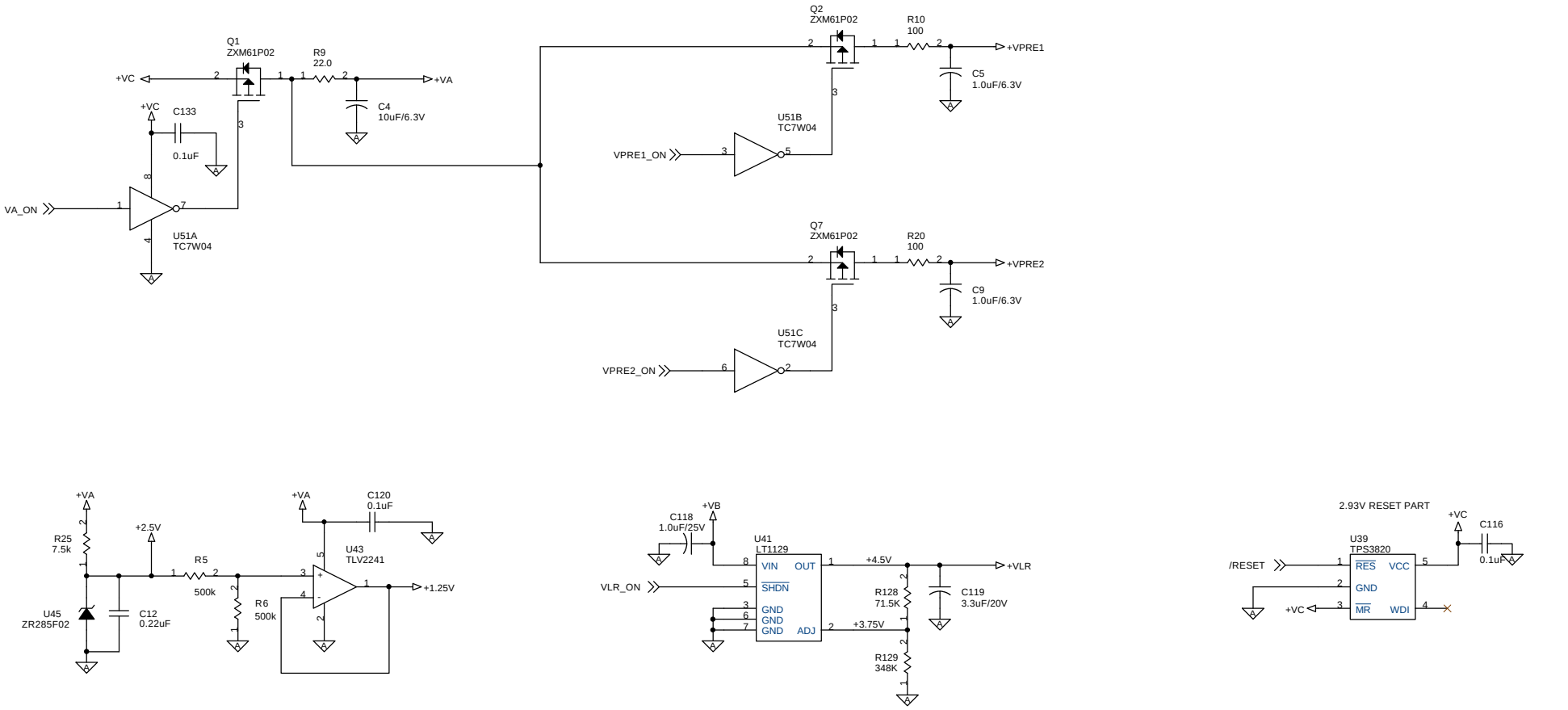
Date: Thursday, March 20, 2003	Sheet 2 of 9	



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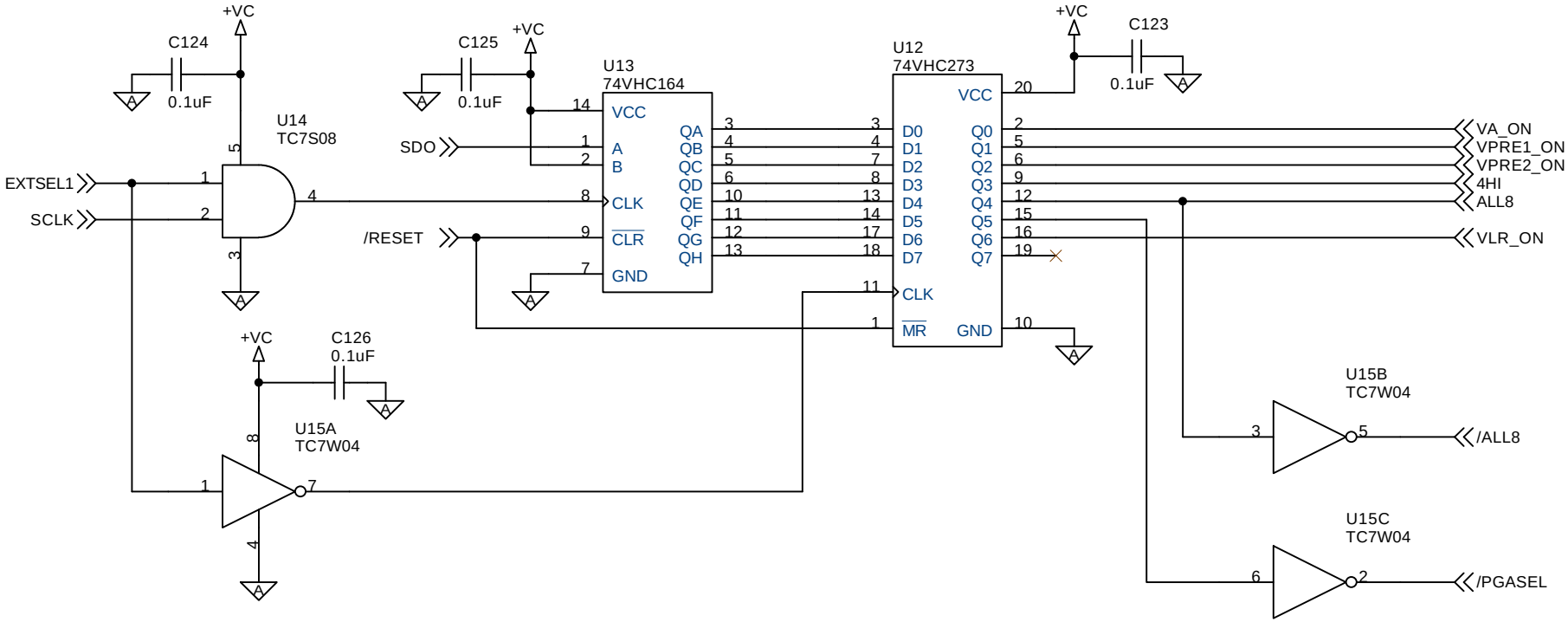
Date: Thursday, March 20, 2003	Sheet 3 of 9	



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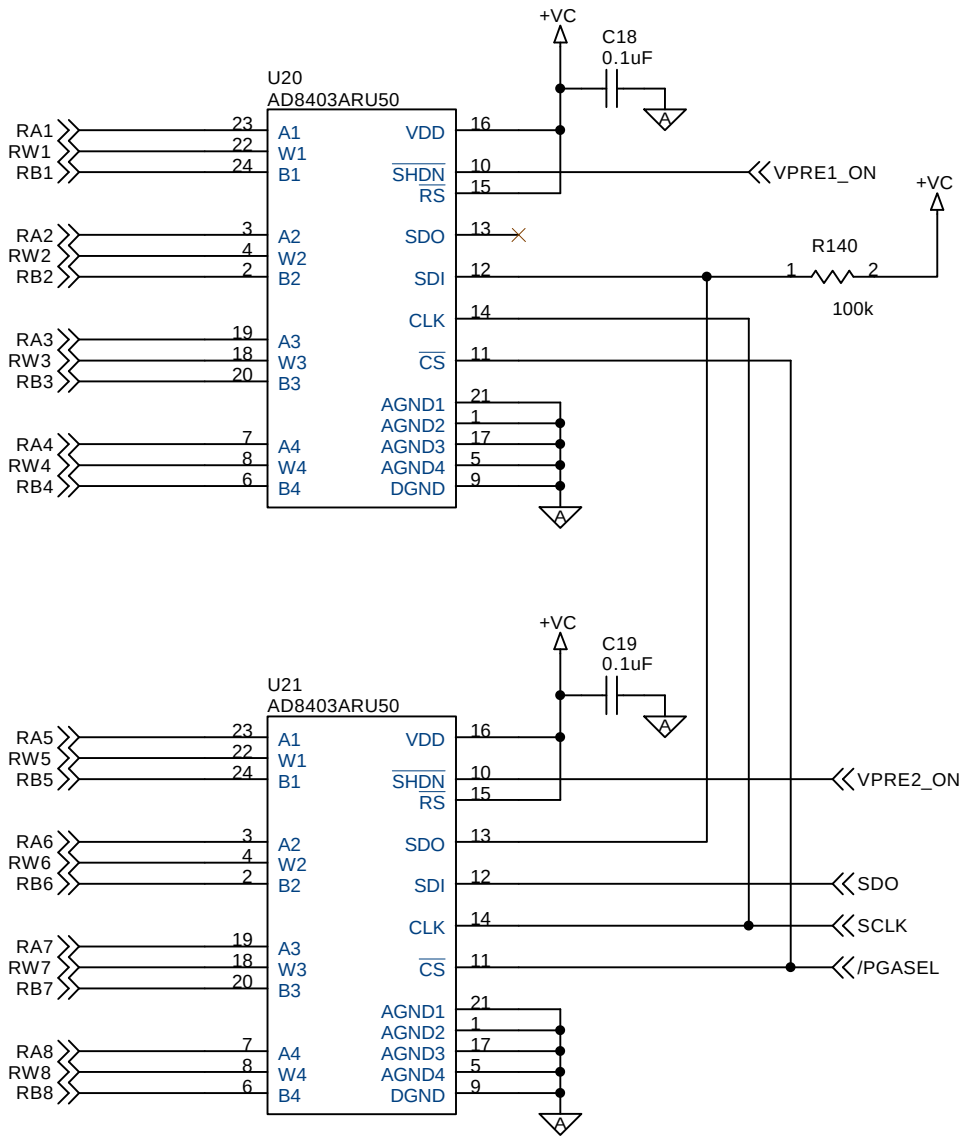
Date: Thursday, March 20, 2003	Sheet 4 of 9	



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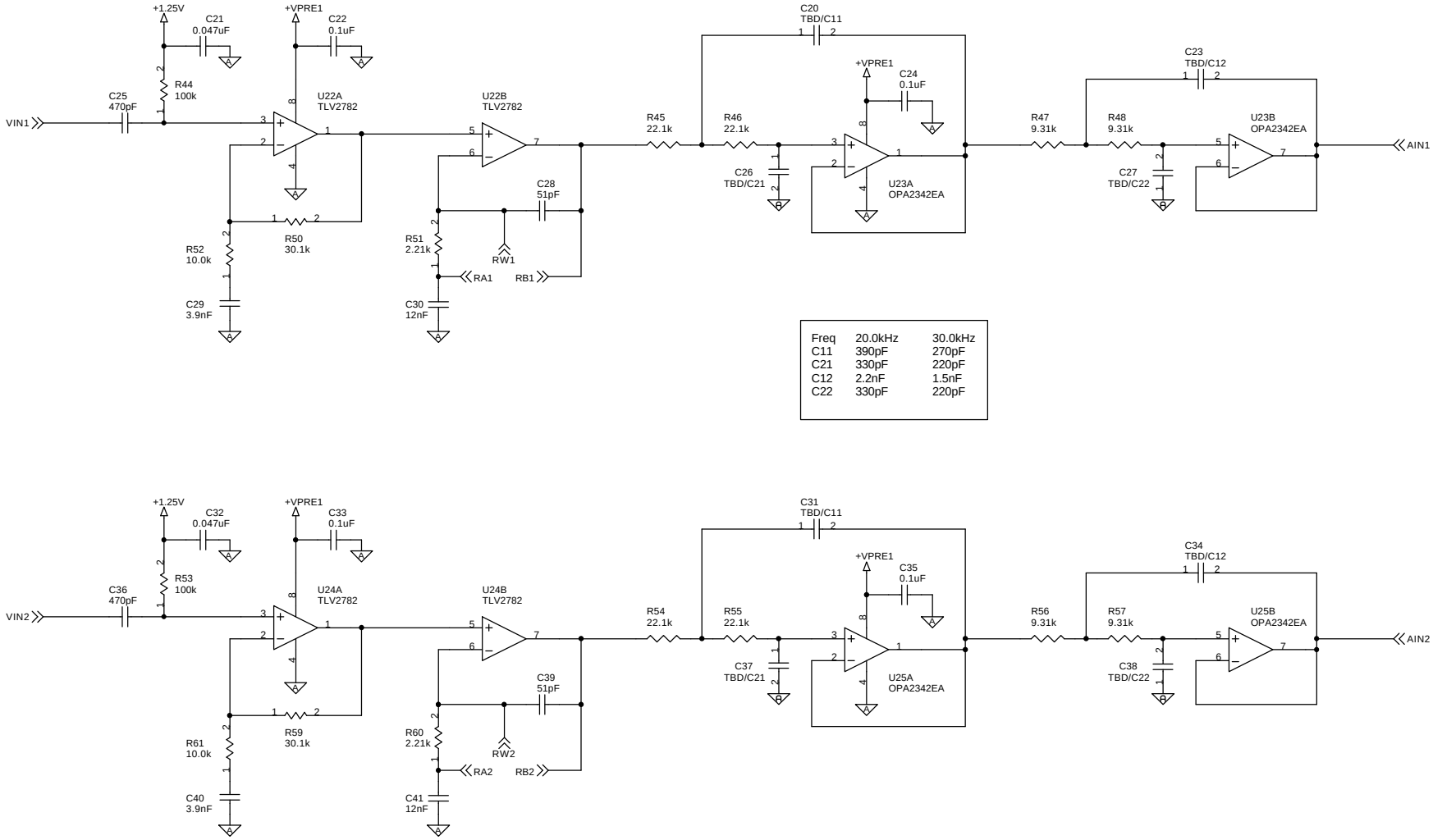
Date: Thursday, March 20, 2003	Sheet 5 of 9	



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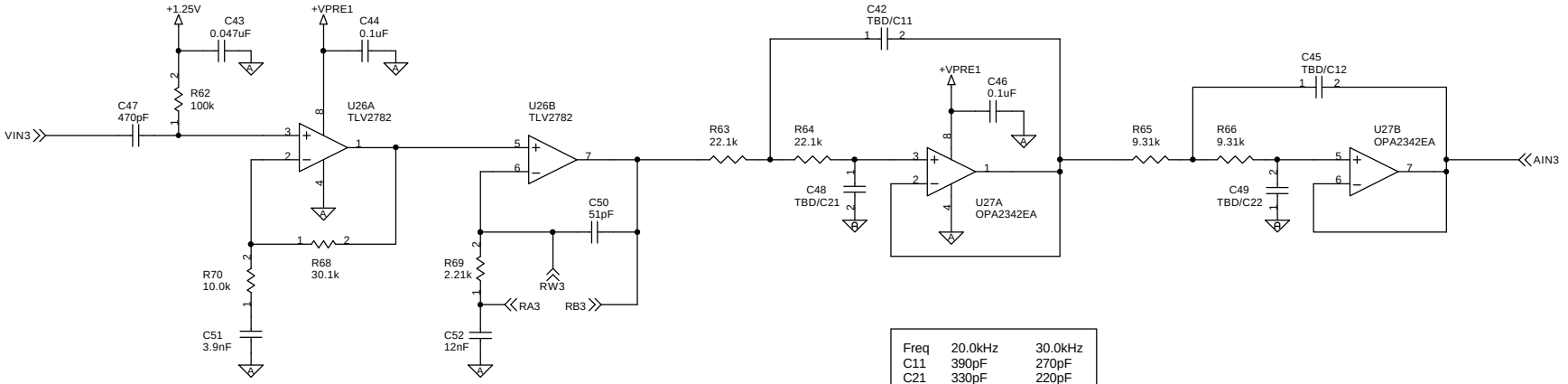
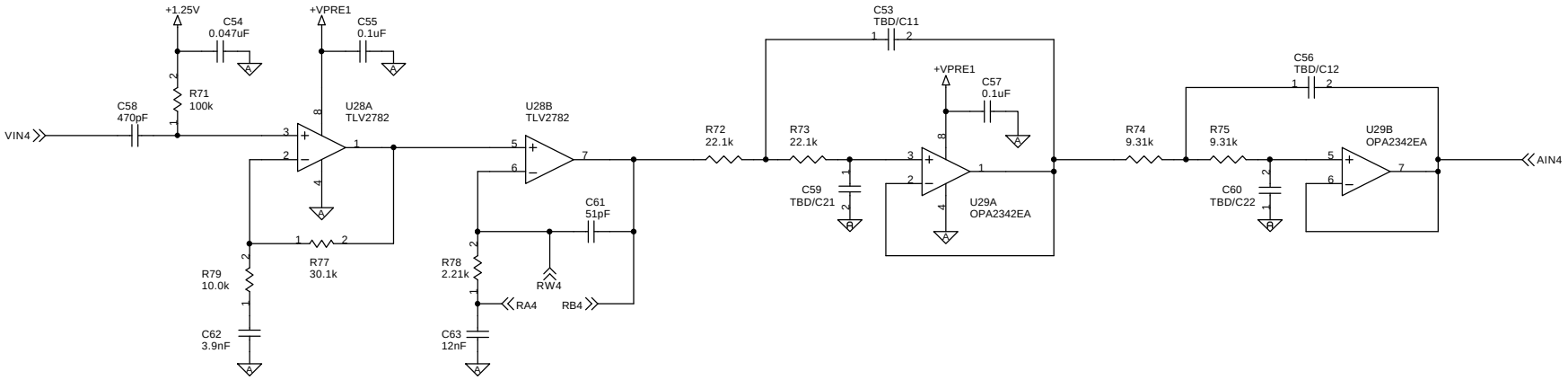
Document Number	241002-6
Rev	V1.1
Date:	Thursday, March 20, 2003
Sheet	6 of 9



Freq	20.0kHz	30.0kHz
C11	390pF	270pF
C21	330pF	220pF
C12	2.2nF	1.5nF
C22	330pF	220pF



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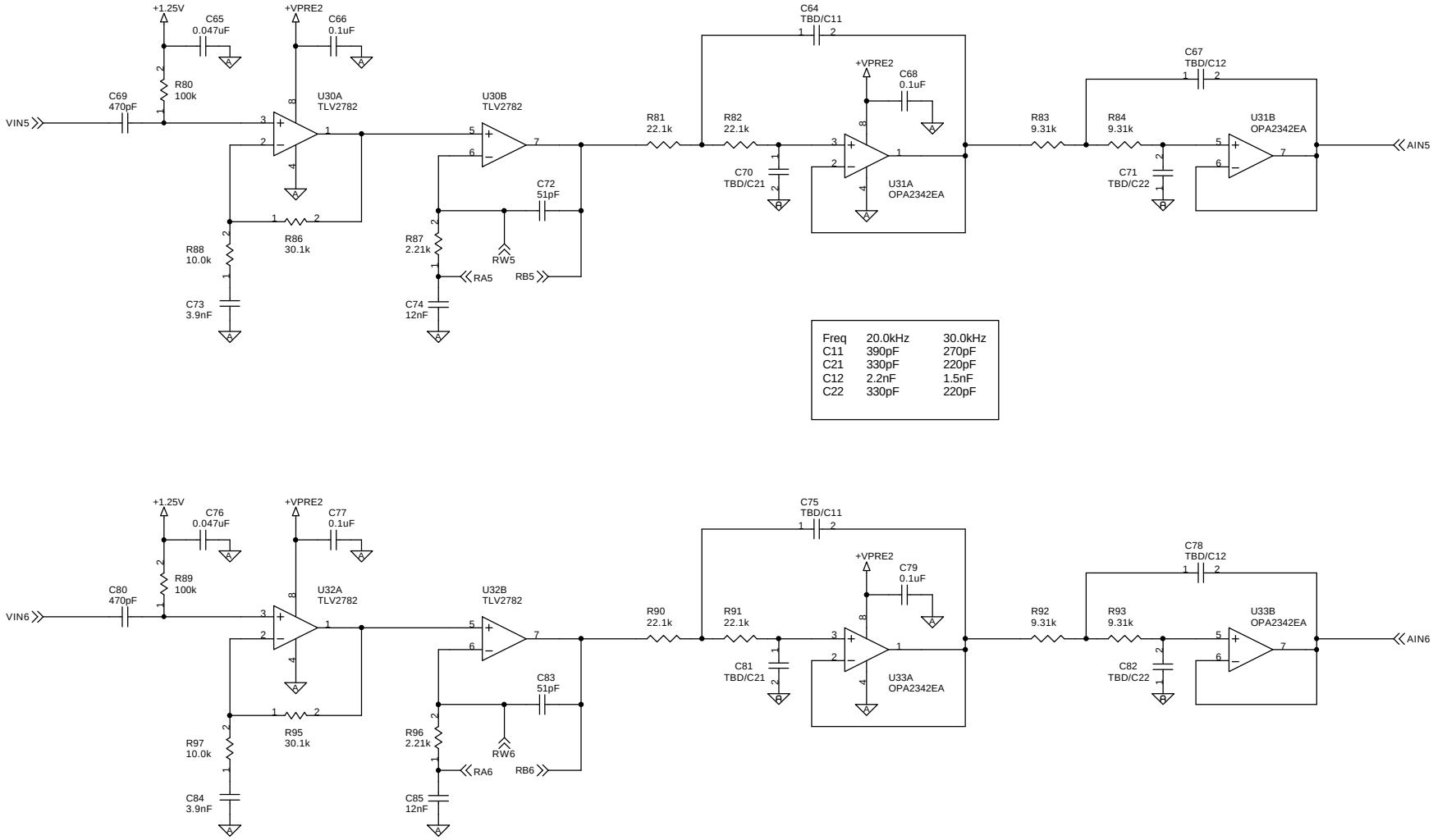
Size B	Document Number 241002-7		Rev V1.1
Date:	Thursday, March 20, 2003	Sheet 7 of 9	

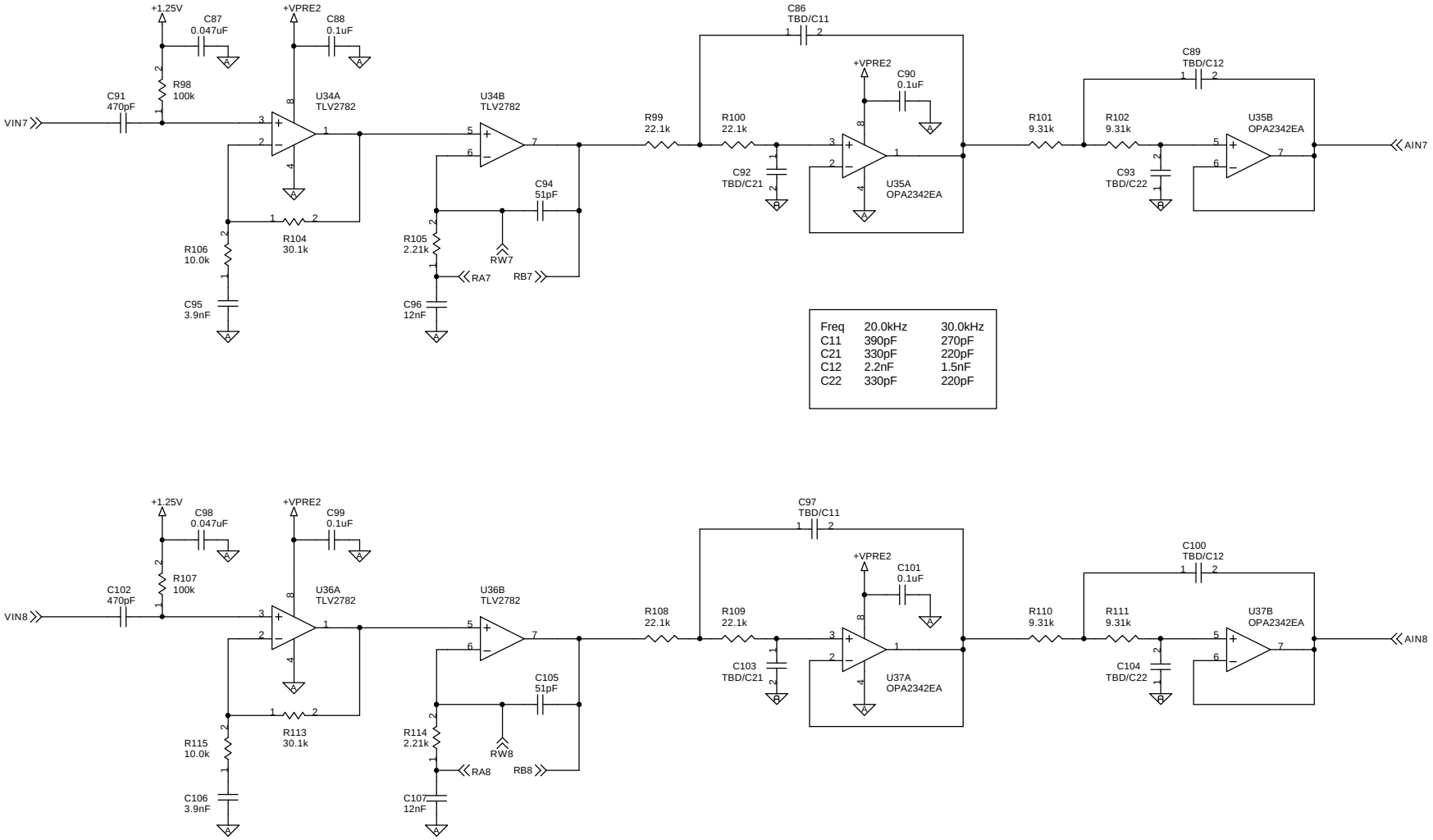


Freq	20.0kHz	30.0kHz
C11	390pF	270pF
C21	330pF	220pF
C12	2.2nF	1.5nF
C22	330pF	220pF

Title: ANALOG INPUT CH5-6

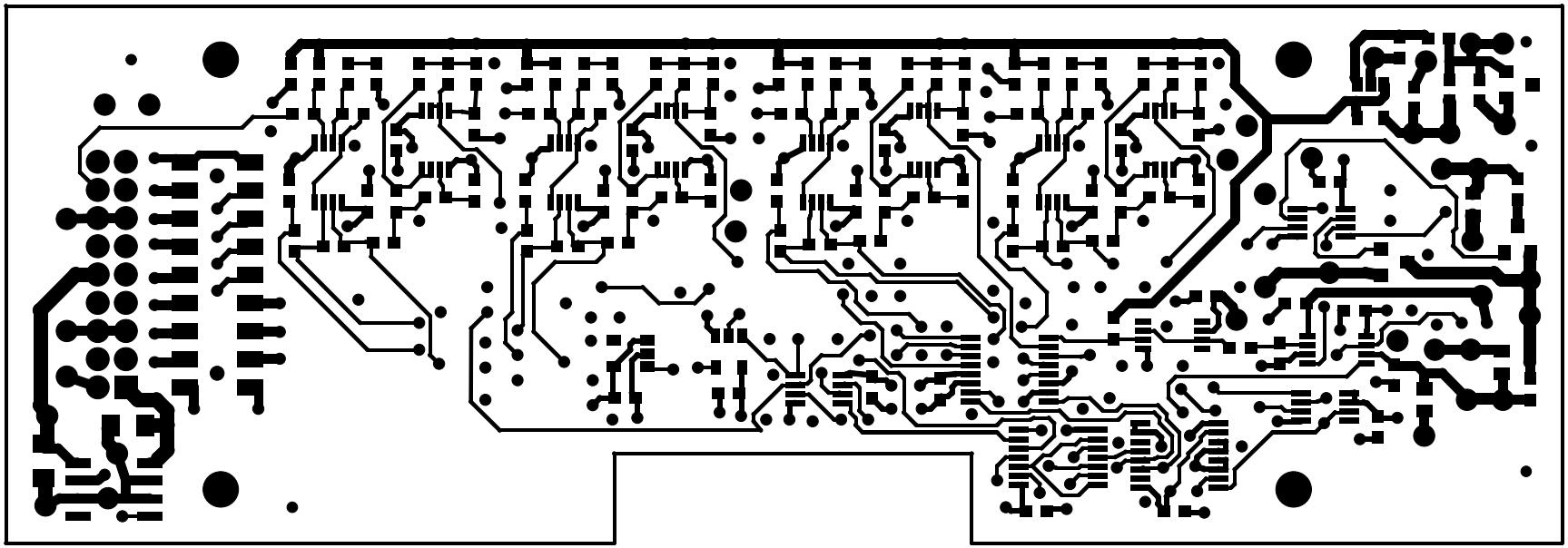
Size: B | Document Number: 241002-8 | Rev: V1.1

Date: Thursday, March 20, 2003 | Sheet 8 of 9



Freq	20.0kHz	30.0kHz
C11	390pF	270pF
C21	330pF	220pF
C12	2.2nF	1.5nF
C22	330pF	220pF

Title	ANALOG INPUT CH7-8	
Size B	Document Number 241002-9	Rev V1.1
Date: Thursday, March 20, 2003	Sheet 9 of 9	



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WOODS HOLE OCEANOGRAPHIC INST.
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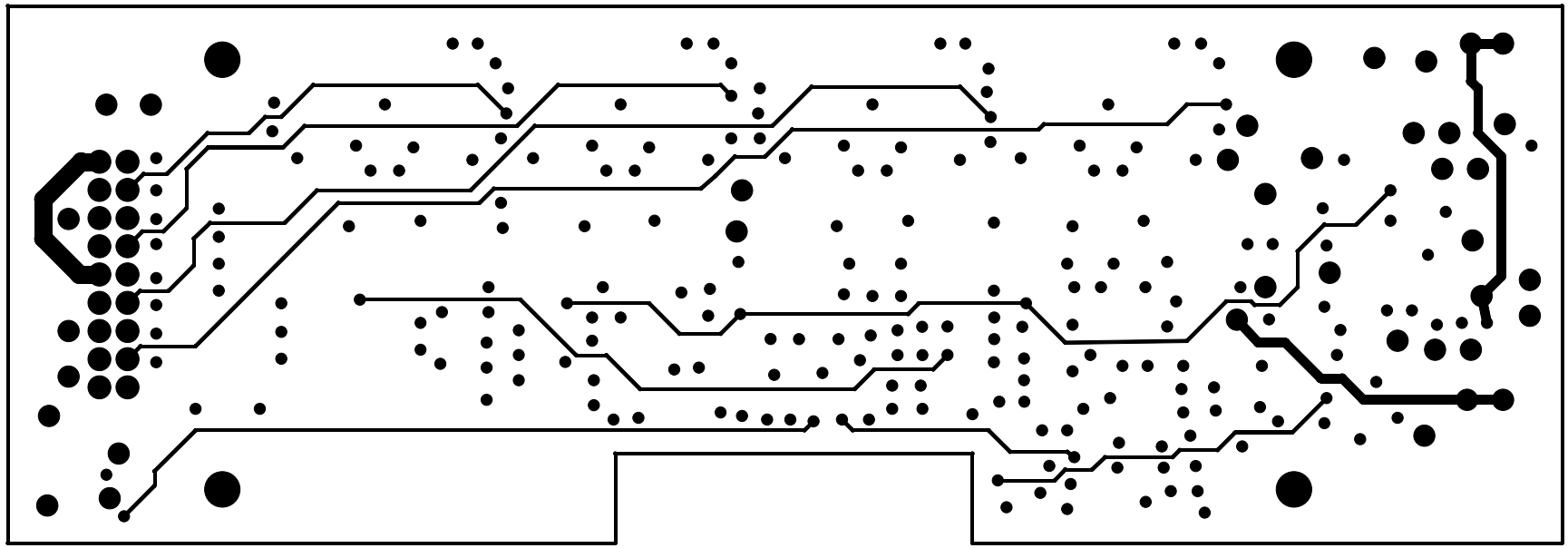

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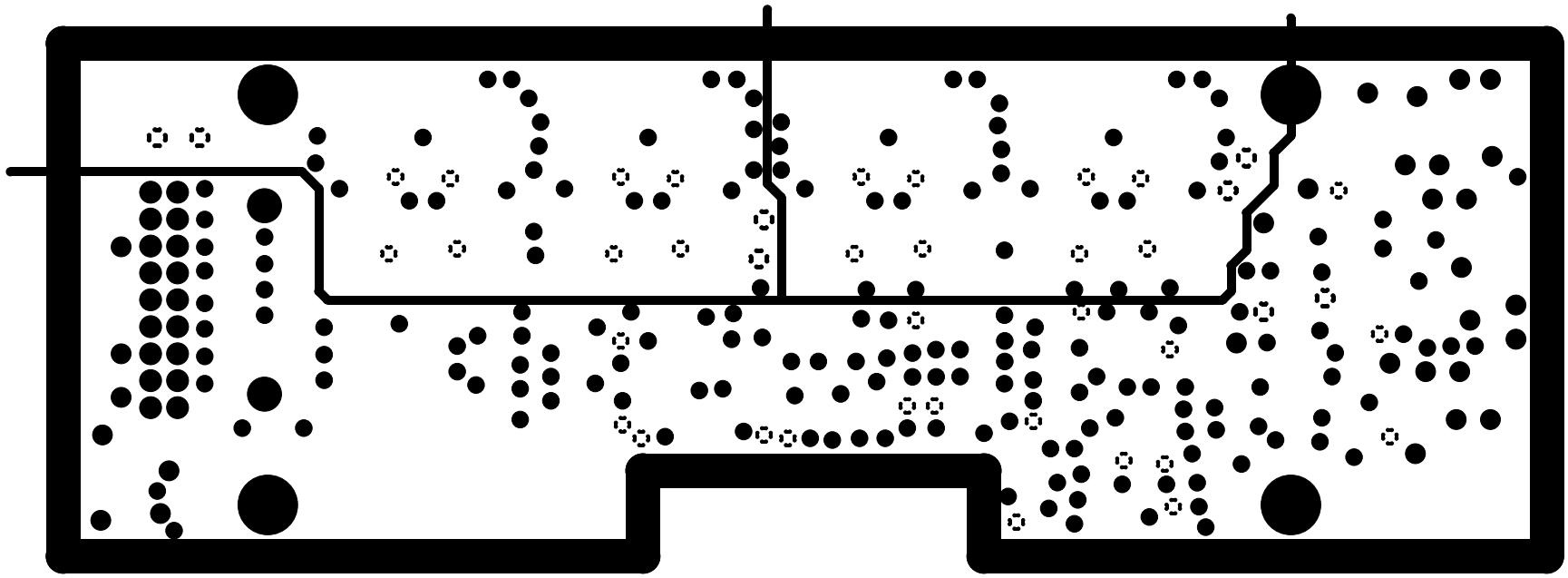

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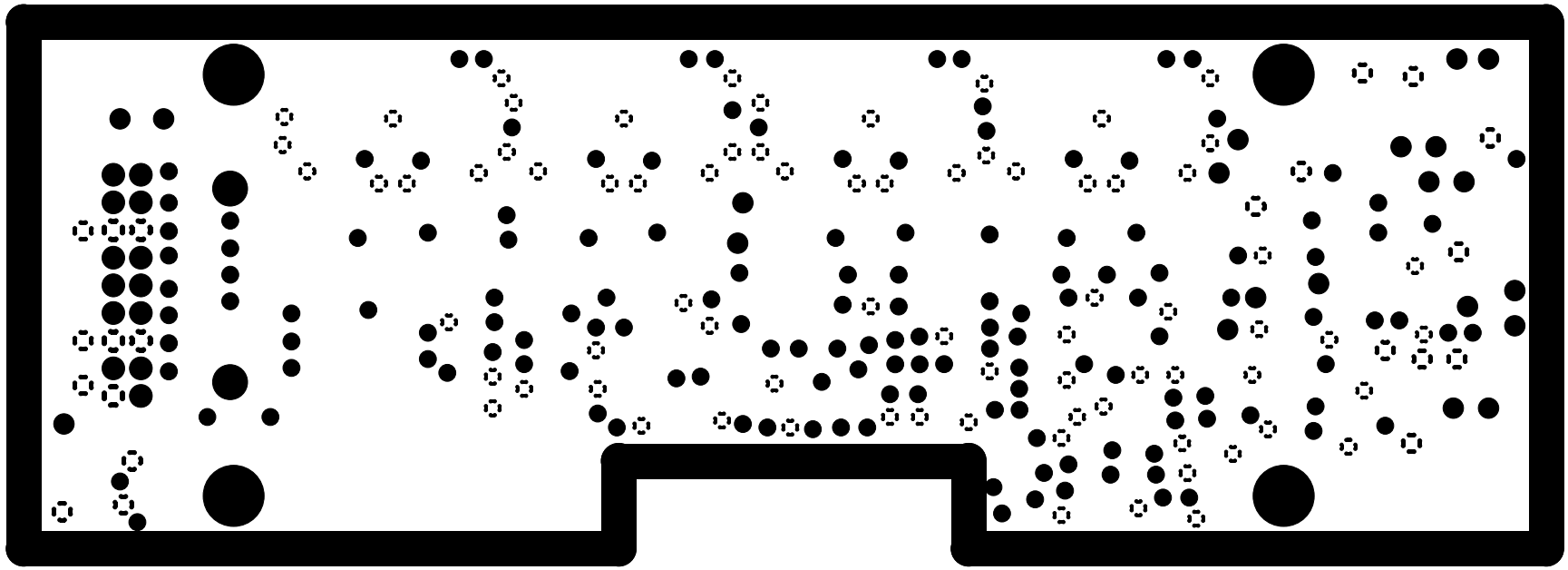

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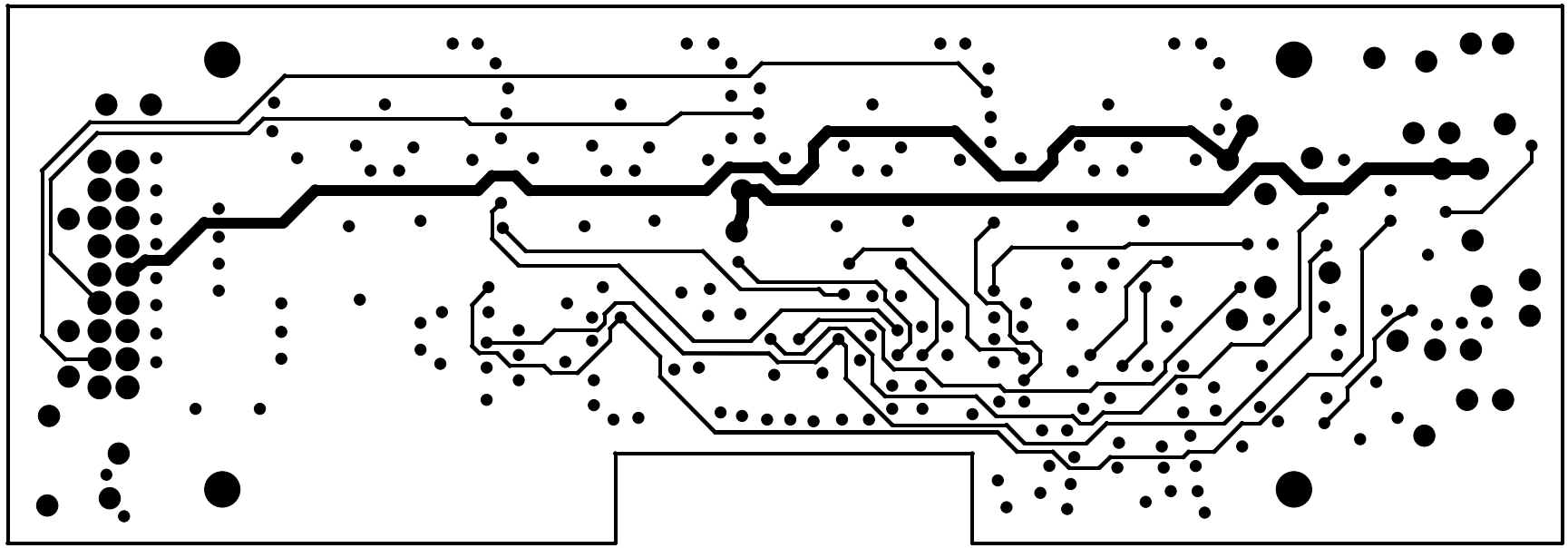

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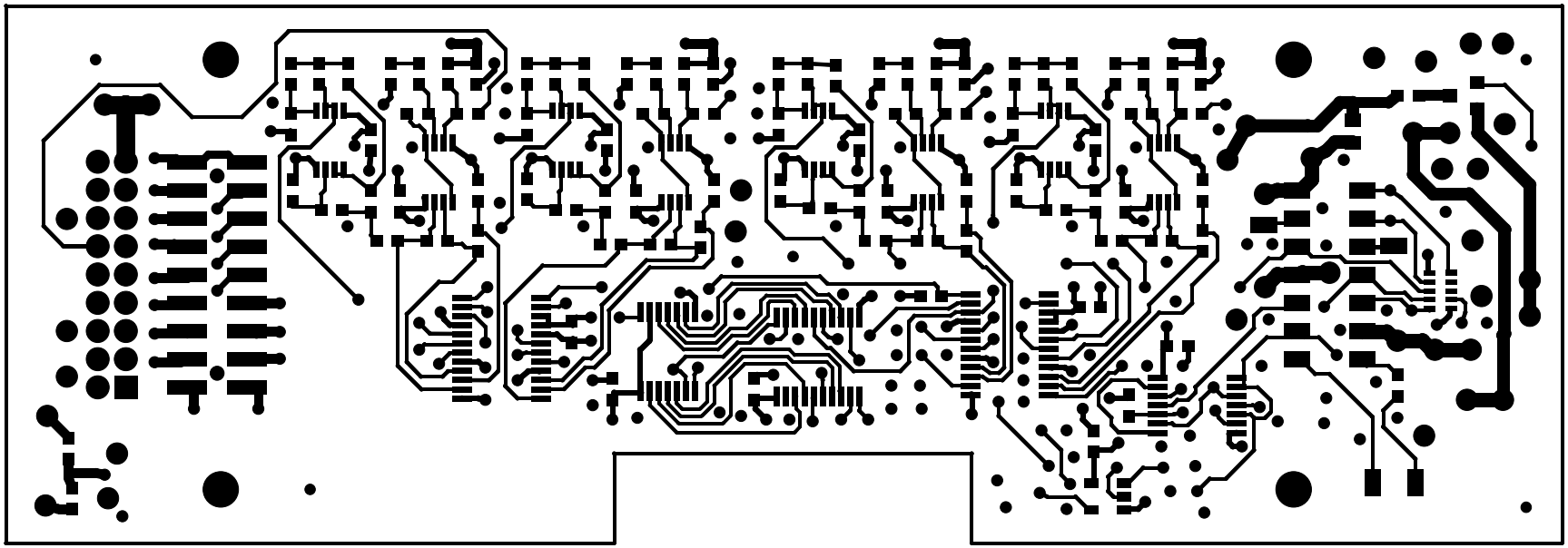

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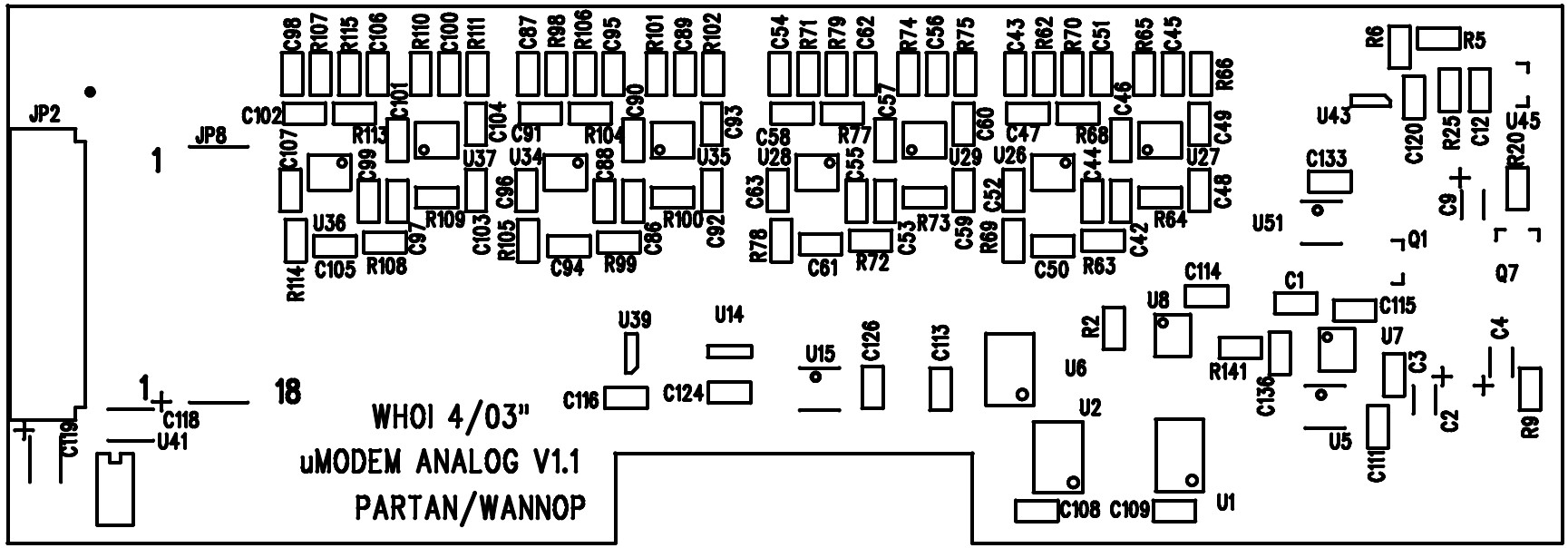

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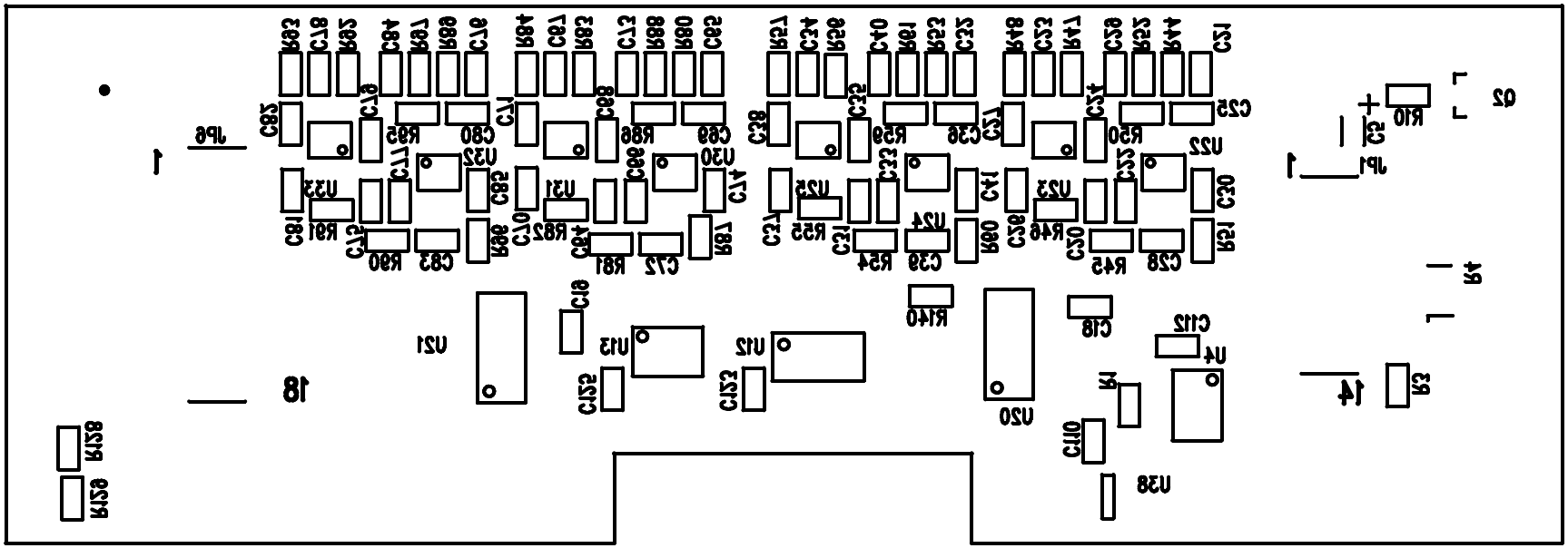

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