Woods Hole Oceanographic Institution

WHOI Micromodem-1.1B

9 January 2004
Document Revision: E

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Table of Contents:

Revision History:

Revision E, 9 Jan 2004, Jim Partan: updated Production Notes and Assembly Rules to note that U36 is a programmable part, and a sticker should be used to identify a programmed EPROM versus a blank EPROM.

Revision D, 16 Nov 2003, Jim Partan: re-saved PDF document with all bookmark hierarchies defaulted to closed.

Revision C, 16 Nov 2003, Jim Partan: added Revision history section, renumbered Table of Contents.

Revision B, 15 Nov 2003, Jim Partan: increased margins on schematics for binding, increased margins on Gerber Layout Overview for binding, clarified Soldermask/Solderpaste in Table of Contents.

Revision A, 14 Nov 2003, Jim Partan: initial release.

Revision History, cont.

Producing a batch of Micromodem-1.1B's

Jim Partan, WHOI, 9 Jan 2004. Document Revision: B

1.) Get quote from vendor(s) for turnkey production (parts procurement, board fabrication, board assembly) by supplying the following files:

a.) Micromodem_V11B_rules.pdf	(Fabrication and Assembly rules)
b.) Micromodem_V11B_gerbers.zip	(Gerber files for board and stencils)
c.) Micromodem_V11B_assembly.zip	(Assembly files in DXF format)
d.) Micromodem_V11B_BOM.xls	(Bill of Materials, Excel format)
e.) Micromodem_V11B_eprom.hex	(Tektronix-format hex file for EPROM)
f.) Micromodem_V11B_netlist.p2k	(Netlist for testing fabricated boards)

Note that the netlist above is in PADS-2K format. Vendors generally want netlists in IPC-356 format for electrical testing of the fabricated boards. Our schematic capture program, Orcad Capture, cannot produce IPC-356 netlists, but the vendor may accept a PADS-2K netlist, or the vendor may be able to extract an IPC-356 netlist from the Gerber files.

Also note that at WHOI we typically do not do complete turnkey operation, and we use the files Micromodem_V11B_rules_whoi.pdf and whoi_supplied_parts.pdf in place of Micromodem_V11B_rules.pdf. The reasons are the following:

Item 88 (U33): These flash parts can be hard to procure, and normally have minimum quantity orders (96+). We have been buying these parts directly, and supplying them to the vendor, since our production runs are usually smaller than the minimum quantity order.

Item 91 (U36): These EPROMs need to be programmed with Micromodem_V11B_eprom.hex prior to assembly. We normally program the parts at WHOI and send them out to the vendor for assembly. **Important:** Identify programmed parts with a sticker after programming to avoid potential confusion with blank EPROMs.

Item 106 (Y3): These crystals can have very long lead times (8-10 weeks). We typically have several hundred on hand at WHOI and supply them ourselves to the vendor to reduce production time.

GE Silicones RTV162: We just want to make sure they actually use our specified adhesive.

2.) For complete turnkey operation, the vendor should be ready to go with the files above. If you are supplying any parts, procure them, prepare as appropriate (programming, etc), and ship them to the vendor. If you program the EPROMs in-house, make sure to identify programmed parts with a sticker.

3.) Vendors we (WHOI) have used include:

Phoenix Resources, Rick Costello, rc@phoenixpwb.com, 603-863-9096
193 Lempster Coach Road, Goshen, NH 03752, Fax: 603-863-9099
www.phoenixpwb.com

Nexlogic Technologies, Justin Proulx, justin@nexlogic.com, 408-436-8150 x112
345 East Brokaw Road, San Jose, CA 95112, Fax: 408-436-8156
www.nexlogic.com

4.) For modified designs, redesign schematics in Orcad Capture, produce new netlist and bill of materials, contract for new layout design (contact Rick Costello, listed above, for contracting Mike Chaney as layout designer). See Micromodem_Layout.pdf for layout rules.

Micromodem-1.1B Fabrication and Assembly Rules (Complete Turnkey Version)
Document Revision: C
9 Jan 2004

Customer Contact Information:
Name:
Phone:
Fax:
Email:
Mail:

Fabrication Rules:
1.) Board material is to be FR4, overall thickness
not to exceed 0.062" (62 mils).
2.) Board dimensions shall be 4.50" x 1.75".
3.) Board edges shall be finished, not V-scored.
4.) Outer and inner layer copper weight shall be 1 ounce.
5.) Soldermask (solder resist) shall be on top and bottom layers.
6.) Silkscreen shall be on top and bottom layers.
7.) Surface-mount components are on top and bottom layers.
8.) Through-hole components are on the top layer only.
9.) "Bed of Nails"-style testing, or similar, shall be performed.

Assembly Rules:
1.) Vendor shall supply all parts.
2.) Do not install:
a.) Item 28 (reference D7)
b.) Item 47 (references R9, R65, R82)
c.) Item 67 (references TP1, TP2)
3.) Vendor shall program Item 91 (reference U36, Atmel AT27LV256A-55RC one-time programmable EPROM) with Tektronix-format file "Micromodem_V11B_eprom.hex" prior to installation. A sticker to distinguish programmed EPROMs from blank EPROMs may be used, but is not required.
4.) Item 106 (reference Y3) and Item 1 (reference BT1) are to be installed by hand as follows:
a.) Item 106 (reference Y3)
i.) Lay flat on board, as indicated by silkscreen outline.
ii.) Place a small dot of RTV beneath Y3 to secure it to the board.
(Do not use the tie-down holes associated with Y3.)
iii.) RTV to be G.E. Silicones RTV162, SUPPLIED BY VENDOR.
b.) Item 1 (reference BT1)
i.) Bottom of BT1 must not come in contact with metal can of Y3.
5.) Finished boards are to be given a unique serial number.
6.) Finished boards are to be given a visual Quality Assurance inspection.
7.) Unused parts charged to customer shall be returned to customer at above address.

DESIGN RULES FOR FABRICATION OF THE μMODEM V1.0 PRINTED CIRCUIT BOARD:

Mark Johnson, WHOI
Majohnson@whoi.edu
Ph. 508-289-2605

Tom Hurst, WHOI
thurst@whoi.edu
Ph. 508-289-2906

14 March 2000

1. 8 Layer board with layer stackup:

Front of board -	Layer 1	SIGNAL 1
	Layer 2	DGND/AGND (split plane)
	Layer 3	SIGNAL 2
	Layer 4	+VD
	Layer 5	+VD/+VL (split plane)
	Layer 6	SIGNAL 3
	Layer 7	DGND
Back of board -	Layer 8	SIGNAL 4

2. Board dimensions: 4.5” x 1.75”. Thickness not to exceed 0.07”.

3. 0.05” component, track and plane keep out on all sides excluding connectors.

4. 4ea 0.094" mounting holes (A) placed per "umodem v1.0 mechanical dwg". Include 0.125" trace keepout; 0.175" component keepout.

5. Maximum component height on back of board is 0.075” excluding JP6.

6. Minimum track width and spacing is 0.005”.

7. Silkscreen with polarity indication for capacitors, diodes, BT1. Pin 1 indicators on all I.C.s and crystals. Corner pin numbers on PQFP packages and connectors.

8. Legend: “μmodem v1.0, WHOI 3/00, mark johnson” to be visible on front of board when board is assembled.

9. Placement:

- place connectors (JP1 - JP8) according to "umodem v1.0 mechanical drawing"; LOCATE PIN 1 ACCORDING TO DIMENSIONS ON DWG; connectors have been placed to align mechanically with external components and thus locations may not deviate
- power supply components (located lower right on the placement dwg) must be placed as shown on placement dwg; ground connections here are to be starred to JP8 as shown; components include: U23, U24, D3, D4, D7, D8, L1, L2, CC21, C23, C25, C26, C28, C30, C33, C74, C99
- C12-20 must be on the same side and close to U20, U21.
- D9 (led) on back of board under JP4, near board edge.
- U41 on back of board.
- U36, BT1, L1, L2, C25, C33, C99 on front of board.
- all analog components on front of board near JP2, JP5 (this means U25, U26, U28, U42, U43, U50, U52, D4, and their related passives).
- Y1, Y2, Y3 on front of board.

10. Layout – special routes:

- Star ground connections of power supply components to JP8 as shown on placement dwg.
- Y1 and associated components to be placed and routed as shown on placement dwg

- very short, no vias, no plane layer immediately beneath:
  XOSCI, XOSCO, XOSCT, X2A, X2B.
- short routes, minimize vias:
  UARTX1, UARTX2, HICLK, AINF, AIN, VREF2, EMU0, EMU1, TDO,TDI, /TRST, TCK, TM, VSW1,VSW2, VSP1, VSP2, VFB2, VLIMIT1, VLIMIT2, VPGA, HYDW1.
- wide routes (0.01" minimum):
  +VC, +VEXT, +VA, VPREAMP.
- wide routes (0.015" minimum), minimize vias, use double vias wherever a via is necessary:
  +VB, V1 (only between JP8.1 and D8), V2 (only between JP8.3 and D7), VLIMIT1, VLIMIT2, VSP1, VSP2, VSW1, VSW2

11. Please Check Netlist Wiring of Following Components versus Mechanical Data Sheet:
(ignore pin numbers on data sheets)

BT1	- netlist/schematic pin 1 is POS - netlist/schematic pin 2 is NEG
All Tantalum Caps	- netlist/schematic pin 1 is POS - netlist/schematic pin 2 is NEG
All 2-Terminal Diodes	- netlist/schematic pin 1 is ANODE - netlist/schematic pin 2 is CATHODE
ZR285F02	- netlist/schematic pin 1 is VR - netlist/schematic pin 2 is GND
NDS332P	- netlist/schematic pin 1 is DRAIN - netlist/schematic pin 2 is SOURCE - netlist/schematic pin 3 is GATE
SML-LX1210	- netlist/schematic pin 1 is ANODE LED A - netlist/schematic pin 2 is ANODE LED B - netlist/schematic pin 3 is CATHODE LED B - netlist/schematic pin 4 is CATHODE LED A
ZMR250	- netlist/schematic pin 1 is GND - netlist/schematic pin 2 is VIN - netlist/schematic pin 3 is VOUT

12. Additional Notes

- Placement drawing has been included as an aide; components may be moved around and rotated to facilitate more efficient routing so long as the general location is not altered and design rules for placement and routing are not violated.
- Pin numbers for all connectors have been included on the mechanical drawing.

Micromodem v1.1B Hardware Documentation

16 Nov 2003
Jim Partan, WHOI
Document Revision: A

This document is a companion to the Micromodem v1.1B schematics, providing an overview of its design and subsystems.

TABLE OF CONTENTS

ADC/DAC:

The analog-to-digital converter (ADC) and digital-to-analog converter (DAC) are both serial devices, sharing one of the '54x DSP's McBSP SPI serial ports. Because they share serial port control lines (in particular /ADCS), they operate at the same sampling frequency. As described in the section on the timing generator (see below), the possible sampling rates are:

fs = (Crystal Oscillator Frequency) ./ [64:255]

With a 6.00MHz crystal, as on the micromodem 1.1A, the possible sampling frequencies range from 23.5kHz to 93.75kHz.

The ADC, U50, is a 12-bit ADS7822 from Burr-Brown. When run from a 3.3V rail, it has a maximum sampling rate of 200 ksamples/sec. (The 75 ksample/sec maximum which is prominently mentioned in the data sheet would be the limit if the part were operated from a 2.7V rail. See page 4 of the data sheet for sampling rate versus Vcc.)

The DAC, U42, is a 12-bit TLV5616 from Texas Instruments. Its typical settling time for a full-scale change is 3 microseconds in fast mode (which is what we use). With the sampling frequencies as above (the DAC and ADC necessarily have the same sampling rate, due to the shared /ADCS strobe line), this short settling time is more than adequate. Immediately following the DAC, on the micromodem mainboard, there is a 2-pole Sallen-Key low-pass reconstruction filter, normally set with a 30kHz rolloff. The output will have further filtering applied to it by external components, such as a power amplifier and transducer, etc.

Test point TP3 can be used to display the analog input on a scope, just prior to its being sampled.

ADDRESS / CONTROL:

There are two functions on this page: address decoding for memory-mapped chips, and a control register. The control register selects SPI serial devices, sets power states, turns LEDs on and off, among other things.

Control register bits (all reset to zero):

0x0001 LED1	1 turns on green LED
0x0002 LED2	1 turns on red LED
0x0004 ADCEN	1 enables ADC
0x0008 /DACEN	0 enables DAC
0x0010 /VAON	Set to 0 to power up on-board preamp/filter op-amps
0x0020 PREAMPON	Set to 1 to enable external preamp
0x0040 SLEEP	Set to 1 to turn off crystal oscillator clock
0x0080 HIBERNATE	1 powers down entire board except Hibernate circuit
0x0100 EXTON	Set to 1 to enable power, addressing on ext. flash board
0x0200 RTCSEL	1 chip-selects the real-time clock
0x0400 /PGASEL	0 chip-selects the programmable-gain amplifier
0x0800 FSSEL	1 chip-selects the timing generator shift register
0x1000 EXTSEL1	External select on JP2
0x2000 EXTSEL2	External select on JP5
0x4000 EXTSEL3	External select on JP6, BUT ALSO enables VPWRAMP!!
0x8000 /SADCSEL	0 chip-selects the sensor ADC

I/O space memory-mapped addresses:

0x0000	Flash chip on mainboard (also note use of A0, A1 as CLE, ALE)
0x2000	External flash memory board (requires EXTON on DSP HPI to be set)
0x4000	UART A (also note use of A0-A2)
0x6000	UART B (also note use of A0-A2)
0x8000	control register (only when writing)
0xa000	Unused
0xc000	Unused
0xe000	unused

Note: except as noted above, A0-A12 are ignored in I/O space, so, for example, the control register will respond when writing to any address 0x8000-0x8fff.

CONNECTORS:

There are connectors for power, UART serial ports, an external flash memory board, add-on daughter cards, and a JTAG debugging interface.

Battery connector:

JP8 is the battery connector. The input voltage must be in the range 4V-16V. Diodes are included for reverse-polarity protection, but not over-voltage protection. (Diode D7 is generally not installed for boards which might be used with 24V power amp cards; the wiring harness for the 24V power amp card and micromodem 1.1A mainboard is wired in such a way that removing D7 will prevent the micromodem mainboard from being damaged in case the connectors are plugged into the wrong boards.)

DTE and HOST port:

JP1 and JP4 are the the UART serial port connectors. In addition to the pins for the UART, they have EXTWAKE active-high external wake-up lines to wake the micromodem from its hibernation state (0-14V max). EXTWAKE is also a manual hardware reset input. CTS1 and CTS2 are general-purpose inputs (+/- 25V max). On reboot, CTS1 and CTS2 are checked to see if a programming dongle is connected. If a dongle is connected, the micromodem enters its bootmanager mode, where new executables can be downloaded.

(Details: A programming dongle connects the standard UART pins 2,3,5 straight-through, to support normal serial port operations. It also connects in 4 on the PC's 9-pin connector (DTR) to pin 1 on the micromodem's UART connector (CTS). A PC will put its DTR (Data Terminal Ready) line to +12V, which, when a dongle is present, is then connected to the micromodem's CTS input. CTS is just being used as a general-purpose input here, not in a Clear-to-Send handshaking mode. At hardware reset, when booting, the micromodem will test the CTS line. If a PC and dongle are present, then it will enter the bootmanager mode, and new executable code can be downloaded.)

External Interface:

JP3 provides the signals for an external flash memory expansion board. Note that the busy signal for the external flash is actually sampled at the UART.

External ADC board:

JP2 provides the signals for an external interface board, in particular those for an external multi-channel ADC board.

External power amplifier board:

JP5 and JP6 provide the almost exactly the same set of signals, designed primarily for external power amplifier boards, with both transmit and receive capability.

JTAG interface:

JP7 provides the JTAG debugging interface signals.

DSP:

The DSP schematic has several subsystems of note, namely SPI serial port support, interrupts, serial EEPROM booting interface, HPI port and general-purpose I/O lines, and clock input.

SPI Serial ports:

The '5416 DSP has three McBSP enhanced SPI serial ports. (For reference, see TI '54x reference set volume 5, "Enhanced Peripherals". The chapter on serial ports in volume 1, "CPU and Peripherals" doesn't cover the enhanced SPI serial ports.)

On the micromodem 1.1A, the relatively low-speed SPI peripherals (real-time clock, programmable-gain amplifier, sensor ADC, timing generator shift register, external peripherals using SDO, SDI, SCLK signals) are connected to McBSP#1, and McBSP#2 is reserved for the higher-speed ADC/DAC. McBSP#0 is reserved for a high-speed external ADC daughterboard.

As an aside, note that the low-speed SPI peripherals (on McBSP#1) do not use hardware SPI, but rather use the SPI port pins in general-purpose I/O mode, via software control ("bit-banging").

Interrupts:

There are four external interrupt sources: UART A, UART B, PPS, and external.

Booting:

The micromodem 1.1A boots from a one-time-programmable EPROM with an 8-bit-wide parallel interface. R42 pulls up data line D15, while all other data lines are pulled down, to indicate the location of the parallel EPROM. The setup is described in the '5416 bootloader documentation.

The one-time-programmable EPROM has a bootmanager program burned onto it. The actual micromodem executable is stored in flash, allowing the software to be upgraded repeatedly. The EPROM bootmanager manages the excutable stored in flash, either booting from it, or replacing it with a new executable.

General-Purpose I/O:

Several DSP pins are used as general-purpose I/O.

XF is a general-purpose output and toggles the watchdog timer if resistor R11 is installed. Remove R11 if running via JTAG, otherwise the board will reset if the CPU is halted and XF is not toggled.

BIO is used as a general-purpose input, to sense the busy signal from the flash memory chip.

Clock input:

Clock input is 6.00MHz, from crystal Y1 on the Wake-up/Interrupts schematic. When SLEEP is 1, the clock is off, both for the DSP and for the timing generator which drives the ADC, DAC. Any of the four external interrupts will turn the clock back on. When HIBERNATE goes to 1, the entire board powers down except for Hibernate circuit (see below). To wake out of hibernate, either EXTWAKE must go high (above about 3.4V), or the real-time clock alarm must go off.

The DSP contains internal clock-dividers and clock-multiplying phase-locked loops, so the DSP's internal clock can be [0.25 0.5 1:15] times the clock oscillator frequency. For the micromodem 1.1A, this means that the DSP can run at up to 90 MIPS.

EPROM:

The EPROM – U36, an Atmel one-time-programmable AT27LV256A-55RC – holds the boot loader code, up to 64 kbytes. It cannot be programmed in-circuit, and must be programmed before being installed onto the micromodem-1.1B mainboard.

EXTERNAL INTERFACE:

This is simply a bus transceiver; to drive bi-directional multiplexed data/address lines (BD0-BD7) to the external flash memory board, along with some control signals (BA0-BA2, /BRD, /BWR, /BEN).

FLASH:

The flash memory chip provides local non-volatile memory storage. It is used for both the micromodem program code storage, and for storage of user data.

The chip on the micromodem 1.1B is a 16Mbyte part from Samsung. Previous 1.1 mainboards used an equivalent Toshiba part. The range of NAND flash memory chips from Toshiba and Samsung are pin-compatible, and largely software-compatible; with software changes only, therefore, the flash memory on the mainboard can be expanded up to 256 Mbytes (as of Jan 2003). The software issue is that the larger chips require more words of addressing, a minor change to the existing code. Note, however, that the EPROM image is fixed code, and larger chips may or may not work with the existing EPROM image.

As the flash memory chip sees it, the bus is multiplexed data and address. From the DSP's point of view, it's a data bus, sometimes with addressing information, sometimes with data information. Note the use of A0, A1 as CLE, ALE. Note /FLASHBUSY is monitored by BIO on the DSP.

HIBERNATE:

In hibernation, the entire micromodem is powered off, aside from just a few chips. To enter hibernation, the software must bring the HIBERNATE line high in the control register. To wake out of hibernation, either EXTWAKE needs to go high, or the real-time clock alarm needs to go off.

The hibernate circuit provides a low-power monitoring of the EXTWAKE line and the real-time clock alarm. A low-power 2.5V low-dropout linear regulator supplies two chips, U31 and U32, to monitor those signals and to restart the power supplies if necessary.

In hibernate mode, the power dissipated is (2uA+1uA+625uA)*2.5V + (2*6uA + 30uA)*Vbattery. For a 12V battery supply, this would be 2mW. Almost all the power is dissipated across R24. For low-power applications, R24 can be replaced with a diode, for instance an MA112, with the cathode connected to U32.1, and the anode connected to U22.7. This would reduce the hibernate power consumption to approximately 0.5mW.

If the real-time clock alarm goes off, or if EXTWAKE goes above about 3.4V (dependent upon voltage divider R32, R83), then the hibernate circuit will re-start the power supplies, and bring the micromodem out of hibernation.

The power dissipation calculations above are from:

U32,	74VHC02: 2uA at 2.5V
U31,	TC7S04: 1uA at 2.5V
U23,	U24 2 x LTC1474: 6uA each at Vbattery
U27,	ZMR25H: 30uA at Vbattery
R24	2.5V across 4.02k: 621uA at 2.5V

POWER SUPPLY:

The power supply circuitry includes switch-mode supplies for converting from the battery voltage to the primary mainboard supply rails, as well as switches for auxiliary rails (on-board preamp, external preamp, external power amp, and external flash memory interface). It also provides a reset/watchdog part and voltage references for the analog circuitry.

There is a 3.3V supply for general logic and analog parts, and a 1.5V supply for the DSP core, each based on the LTC1474 (U23 and U24).

The battery voltage input for the LTC1474 could be in the range 4V-18V, but cannot go above 16V when used with the power amp card, version 1.0. This is because v1.0 of the power amp card also takes power directly from the battery, and it has capacitors rated at

only 16V. (So at a 16V battery voltage, v1.0 of the power amp card nominally has no safety margin. It has, however, worked at this voltage in the past in deployed systems.)

If a different DSP is used in the future, with a different core voltage, the ratio of R19 to R21 can be changed to set +VL. See the LTC1474 datasheet for details.

R14 is non-zero (as opposed to R13, R20, which are zero-Ohm resistors) to provide a bit of filtering on the +VC clean analog supply. R14 is not very big, however, to avoid dropping too much voltage between +VD and +VC. This is important, for example, because the ADC runs off +VC, and its maximum sampling rate is highly dependent on the level of +VC.

The grounding for this part of the board is critical, and the various grounds from the power supplies are starred together back to the battery connector, at which point it connects to the ground plane.

Note that the external interrupt, /EXTINT, and the external wake signal, EXTWAKE, use the low battery input of the LTC1474, which allows a wide-range input. The open-drain logic-level outputs require pull-ups. EXTWAKE becomes BWAKE, which then becomes the manual reset signal for the watchdog, part of the TPS-3305 microprocessor supervisor chip, U22.

It turns out that there is no TPS-3305-15, the part which would be required to monitor both the 3.3V rail and the 1.5V core rail. By connecting U22.2 (SENSE2, usually for the core voltage) to U22.1 (SENSE1, for the 3.3V rail), we can partially avoid this problem, and continue to use a TPS-3305-25. The core voltage is not monitored, but no ECO's will be required for the board to prevent it from resetting.

For working on JTAG, remove R11. By removing R11, the watchdog timer will not need to be toggled every 1.1 seconds, and so you will be able to use single-step debugging over the JTAG interface without continual resets.

The analog reference voltages VREF2 and VREF are taken from 2.5V Zener diode D4. VREF2 is a 2.5V reference, and is used by the ADC. VREF is a 1.25V reference, and is used by the DAC and as a DC bias following the AC coupling at the input to the preamp/filtering circuit.

PREAMP / FILTERS:

The filters on this schematic receive signals from the external preamp card (normally called the power amp card, as it also has the transmit circuit), and condition them for digital sampling.

The input is AC-coupled and high-pass filtered across C40, R28 and R26. It then is amplified by a programmable-gain amplifier (U26, U28). C44 and R29 provide additional high-pass filtering at higher PGA gains.

The signal then goes through a 4-pole Sallen-Key filter configured as a Butterworth low-pass anti-aliasing filter (U25A, U25B). This anti-aliasing filter is normally set with a rolloff frequency of 28kHz.

Finally, there is a final single-pole low-pass filter (R58, C62), which is actually on the ADC/DAC schematic, right before the ADC.

RS232:

These MAX3225E's (U20, U21) provide the translation from logic levels to RS232 voltage levels, and vice versa. The inputs are tolerant to +/- 25V, and the RS232-level outputs will swing to at least +/- 5V when driving 3k resistive loads.

RTC:

The real-time clock– U19, a Dallas/Maxim DS1306 – keeps track of time (including when the micromodem has no external power), keeps track of and raises alarms, allows user data storage in its battery-backed non-volatile RAM (NVRAM), and can trigger pulse-per-second interrupts (see the Wakeup/Interrupt page).

Pulse-per-second:

The DS1306 datasheet does not specify the polarity or duty cycle of the open-drain 1Hz (PPS) output. I asked Dallas/Maxim tech support, and Curtis Rutter, an applications engineer from Dallas Semiconductor (voice 972-371-4997, TimeKeeping.Support@ dalsemi.com) reported: "The 1Hz output goes low at the same time that the seconds counter increments, and goes high 500msec later."

Alarm:

The real-time clock can have its alarm set to wake the micromodem out of hibernation. The alarm has can be set to trigger once per second, once per minute at a particular second, once per hour at a particular minute and second, once per day at a particular hour, minute, and second, and finally, once per week, at a particular day, hour, minute, and second. There are two alarms, Alarm 0, triggering /INT0 (not connected on the micromodem), and Alarm 1, triggering INT1. See the DS1306 datasheet for more information.

Backup Battery:

The backup battery, BT1, powers the real-time clock when the micromodem is powered off. BT1 is a 3V, 48mA-hour coin cell (Digi-Key #P061-ND). Its nominal initial voltage is 3.4V, but will quickly drop below that level when used. If VBAT on the DS1306 is greater than VCC1-0.2V=3.1V, then the device is write-protected. The diode D11 is required so that the BT1 battery voltage will not be above the 3.3V +VD voltage. This ensures that the user non-volatile RAM is writable when the micromodem is powered up with a fresh backup battery. The current drawn from BT1 by the DS1306, however, is

only 550nA. At that current, the voltage drop across D11 is quite small, perhaps not quite enough to force VBAT below 3.1V. For this reason, R8 is in the circuit to increase the current through D11, increasing its voltage drop, and decreasing VBAT. The lifetime of the backup battery without R8 installed is approximately 9.9 years; with R8 installed, the lifetime drops to approximately 4.3 years. (Calculation: (3V*48mA*1hour)/(3V*Ibat), where Ibat=550nA without R8 installed, Ibat=(550nA+700nA)=1.3uA with R8 installed.) For long deployments, therefore, you should consider removing R8 after verifying that the realtime clock NVRAM is writable.

Schottky diode clamp:

Diode D2 protects the realtime clock's NVRAM against corruption from negative voltage spikes. A switch-mode power supply, like the Micromodem's, typically has negative voltage spikes upon power-up or power-down. Maxim/Dallas Application Note 504, "Design Considerations for Dallas Real-Time Clocks", specifically recommends using a Schottky diode to clamp the VCC1 rail against negative voltage spikes. A negative voltage spike can cause corruption of the DS1306's NVRAM.

SENSOR ADC:

U52, an LTC1098L, is a general-purpose, relatively slow (16 ksample/sec max), SPI serial 8-bit ADC. It has two channels, one of which monitors the battery voltage, and the other one uses the EXTADC input. The voltage dividers and filter capacitors are user-changeable if the pre-installed values are not appropriate.

SRAM:

U18, a Cypress CY62146V SRAM part, provides 256k x 16 in eight 32-kword segmented pages. Note that A15 and A16 from the DSP's address bus are not connected to the SRAM. The memory map is therefore (program space only):

0x00000-0x07fff	Program memory page 0
0x20000-0x27fff	Program memory page 2
0x40000-0x47fff	Program memory page 4
0x60000-0x67fff	Program memory page 6
0x80000-0x87fff	Program memory page 8
0xa0000-0xa7fff	Program memory page 10
0xc0000-0xc7fff	Program memory page 12
0xe0000-0xe7fff	Program memory page 14

Note that there is internal on-chip memory on the '5416, which maps over part of external memory pages 0 and 2. The SRAM is available in program space only, and not in data space or I/O space. This memory can be reclaimed by remapping it: for instance, external page 0 can also be mapped to 0x100000-0x107fff, and external page 2 can also be mapped to 0x120000-0x127fff.

TIMING GENERATOR:

The timing generator generates the clock and frame sync strobes for the ADC and DAC.

The timing generator is made of discrete parts, instead of using the DSP's McBSP to generate pulses, because of an obscure power-saving feature. The DSP can go into an idle mode (assembly IDLE instruction) and shut down its internal clock. If the McBSP is clocked externally, however, it can continue to work away, streaming samples via DMA into memory. Upon reaching buffer-full or buffer-half-full (in ABU DMA mode —see reference set volume 5, "Enhanced Peripherals", again), an interrupt can fire, waking the DSP out of idle. This only works if the McBSP is clocked externally, however, hence the discrete timing generation circuit.

First, the sample rate value is loaded into the U14 shift register. This value for a given sampling rate, fs, can be calculated as follows:

- Let divisor = (clock/4)/fs
- Round divisor to nearest 1/4. Value must be between 16 and 64.25
- Use following table to determine N, skip1, skip0:
- Let value = (N<<2 | skip1<<1 | skip0)

divisor	N	skip1	skip0
m	m-1	1	1
m + 0.25	m-1	1	0
m + 0.50	m	0	1
m + 0.75	m	0	0

(m is an integer, 16..64)

When ADCEN is brought high, the reset of the timing generator is brought out of reset. N is loaded into the '40103 counter (U15), skip1 and skip0 are loaded into U61A-U61C. HICLK (10.24MHz) clocks the '161 counter (U12), and generates LOCLK. LOCLK is approximately HICLK/4, with some fiddling from skip1,skip0. LOCLK then clocks U15, which periodically strobes/ADCS from the flip-flop, U17A. /ADCS is the chip select for both the ADC and DAC (which is why they both run at the same sampling frequency).

R9 is never installed; U12 is always installed.

Again, available sampling frequencies are fs = (Crystal Oscillator Frequency) ./ [64:255]

UART:

The UART provides two channels of asynchronous serial I/O, at all the standard baud rates. The UART, U9, an Exar XR16C2850CM, is memory-mapped into I/O space. Address lines A0-A2 select internal registers.

In addition to the standard serial port signals, RTSA and RTSB can be used as general purpose outputs, brought out to the UART DTE and HOST connectors. /EXTBUSY, /BEXTINT, and BWAKE are all sampled at the UART as general-purpose inputs.

/RIB is available for another general-purpose input, if R6 is removed and a wire is tacked to its pad. OPA and OPB are not useful as general-purpose outputs, unfortunately.

WAKE UP / INTERRUPTS:

This schematic contains the oscillator, as well as its shutdown and start-up circuit, and various interrupt logic.

The oscillator, Y1, is a standard 6.00MHz crystal, which allows 80kHz audio sampling, as well as a moderately high internal clock rate (90 MIPS) for the DSP.

In sleep (or hibernate), the clock is disabled. An interrupt will bring the micromodem out of sleep and restart the clock. An external wake on EXTWAKE or a real-time clock alarm will wake the micromodem out of hibernation.

On various interrupt logic, /BEXTINT needs a pull-up after the open-drain output of the LTC1474 on the Power Supply page. That pull-up, R5, is here.

/PPS has a rising edge at the start of a second tick. The /PPSCAP interrupt is therefore triggered at the start of a second tick. R3 is a pull-up for the open-drain output of the real-time clock, and C73 and R25 differentiate the square wave into pulses suitable for the flip-flop formed from U11C and U11D.

/IACK clears all interrupts when the DSP jumps to any interrupt service routine.

U65E, U65F convert the UART interrupts into more traditional active-low signals.

LAYOUT AND CIRCUIT REVISION HISTORY:

Micromodem-1.1B, Oct 2003: Added realtime clock Schottky clamp diode D2 and resistor R8 to increase voltage drop across diode D11. Both changes are to reduce chance of DS1306 NVRAM corruption or mis-reading. Changed flash chip to a Samsung part, as Toshiba part is no longer available.

Micromodem-1.1A, Aug 2003: Changed layout of power supply supervisor U22 to ignore +VL. Fixed incorrect “Q7” label to read “D11”. On power supply schematic, changed R24 value to 4k, to allow EXTWAKE hardware reset, and changed R15 value to 5k to stiffen voltage references.

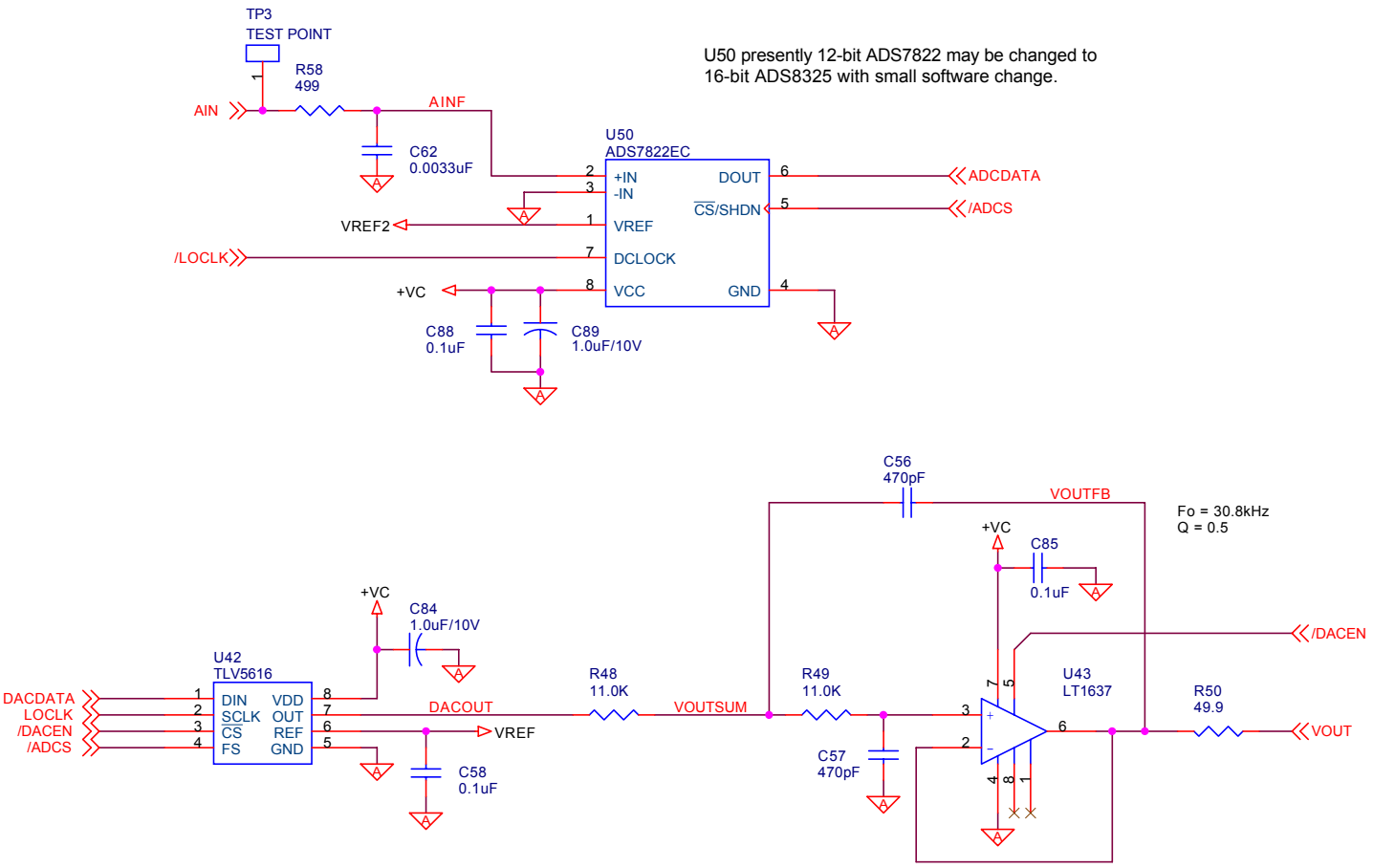
Micromodem-1.1[newer], Aug 2002: Changed preamp PGA op-amp U26 to OP162 for wider GBW product. Added TP3 at ADC input. Changed DSP to ‘5416, changed power supply to operate at lower core voltage. New layout for wider U36 EPROM.

Micromodem-1.1[older], Sept 2001: Various fixes from v1.0. New layout for flash chip. Smaller JP4 HOST UART connector. Use EXTSEL3 as control line for VPWRAMP. Changed realtime clock Q7 to diode D11.

Micromodem-1.0, April 2000: Original board.

DOCUMENT REVISION HISTORY:

Revision A, 16 Nov 2003, Jim Partan: Initial Micromodem-1.1B release. (Earlier versions were for Micromodem-1.1A.)



Title	ADC/DAC	
Size A	Document Number 201110B uModem V1.1B	Rev B
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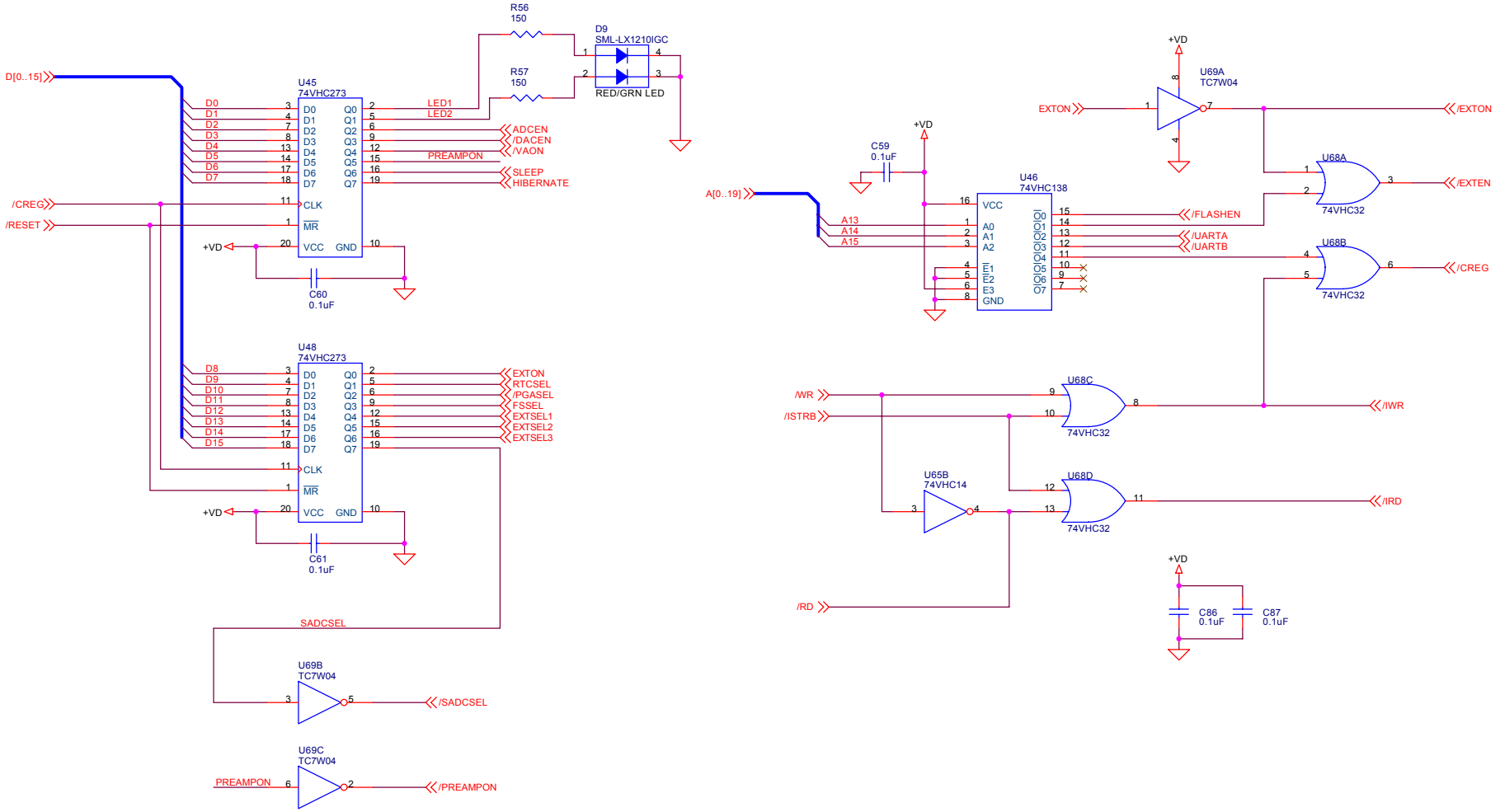
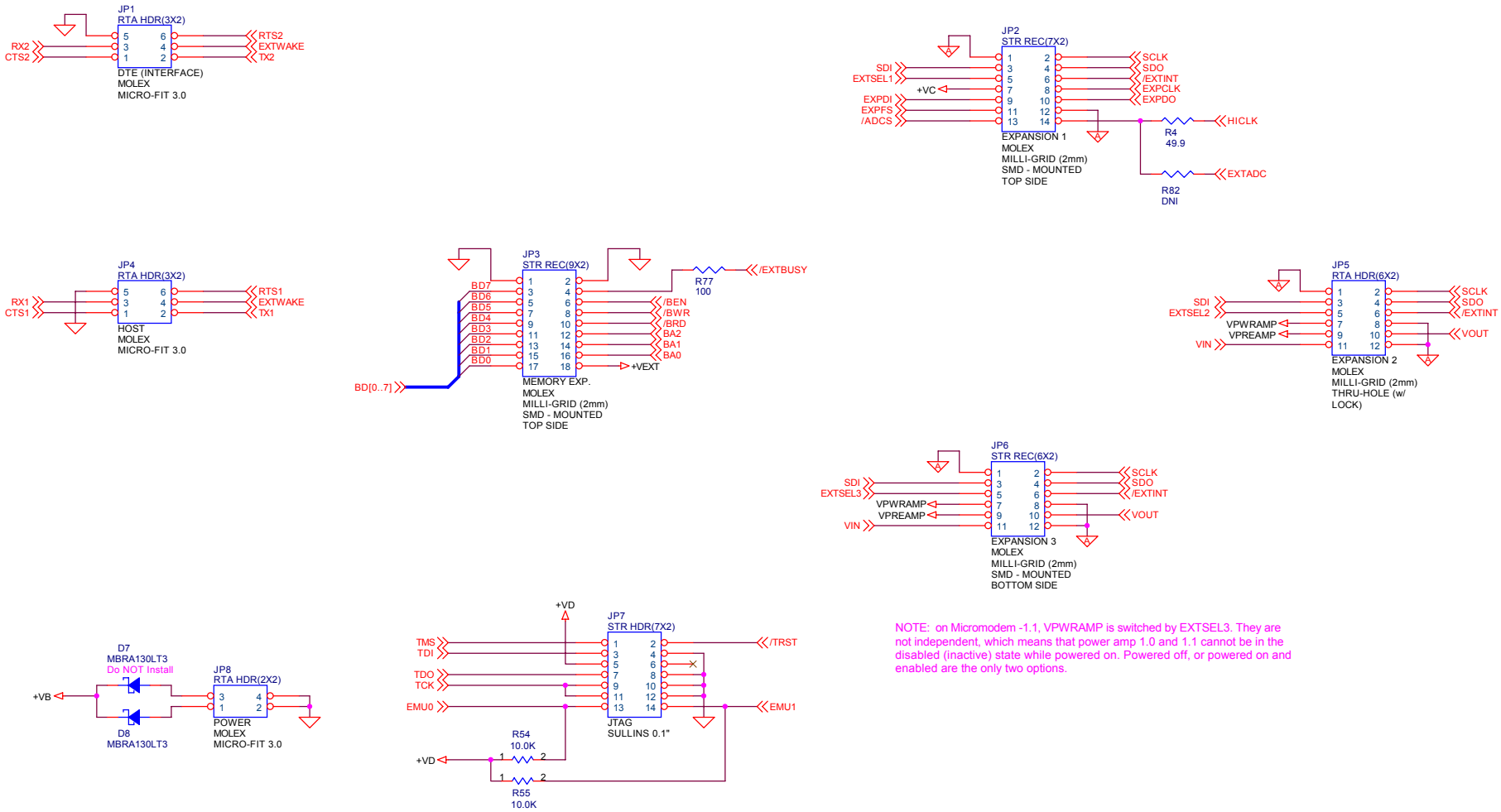
File: 201110B uModem V11B



Title	ADDR DECODING AND CONTROL REGISTER	
Size B	Document Number 201110B uModem V1.1B	Rev B
Date: Friday, October 24, 2003	Sheet 2 of 17	

File: 201110B uModem V11B


JP1
RTA HDR(3X2)
RX2
CTS2
RTS2
EXTWAKE
TX2
DTE (INTERFACE)
MOLEX
MICRO-FIT 3.0
JP2
STR REC(7X2)
SDI
EXTSEL1
+VC
EXPDI
EXPFS
/ADCS
SCLK
SDO
/EXTINT
EXPCLK
EXPDO
HICLK
R4
49.9
EXTADC
R82
DNI
EXPANSION 1
MOLEX
MILLI-GRID (2mm)
SMD - MOUNTED
TOP SIDE
JP4
RTA HDR(3X2)
RX1
CTS1
RTS1
EXTWAKE
TX1
HOST
MOLEX
MICRO-FIT 3.0
JP3
STR REC(9X2)
BD7
BD6
BD5
BD4
BD3
BD2
BD1
BD0
BD[0..7]
R77
100
/EXTBUSY
/BEN
/BWR
/BRD
BA2
BA1
BA0
+VEXT
MEMORY EXP.
MOLEX
MILLI-GRID (2mm)
SMD - MOUNTED
TOP SIDE
JP5
RTA HDR(6X2)
SDI
EXTSEL2
VPWRAMP
VPREAMP
VIN
SCLK
SDO
/EXTINT
VOUT
EXPANSION 2
MOLEX
MILLI-GRID (2mm)
THRU-HOLE (w/
LOCK)
JP6
STR REC(6X2)
SDI
EXTSEL3
VPWRAMP
VPREAMP
VIN
SCLK
SDO
/EXTINT
VOUT
EXPANSION 3
MOLEX
MILLI-GRID (2mm)
SMD - MOUNTED
BOTTOM SIDE
D7
MBRA130LT3
Do NOT Install
D8
MBRA130LT3
+VB
JP8
RTA HDR(2X2)
POWER
MOLEX
MICRO-FIT 3.0
+VD
JP7
STR HDR(7X2)
TMS
TDI
TDO
TCK
EMU0
/TRST
EMU1
JTAG
SULLINS 0.1"
R54
10.0K
R55
10.0K
+VD
NOTE: on Micromodem -1.1, VPWRAMP is switched by EXTSEL3. They are not independent, which means that power amp 1.0 and 1.1 cannot be in the disabled (inactive) state while powered on. Powered off, or powered on and enabled are the only two options.
Title
CONNECTORS
Size
B
Document Number
201110B uModem V1.1B
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B
Date:
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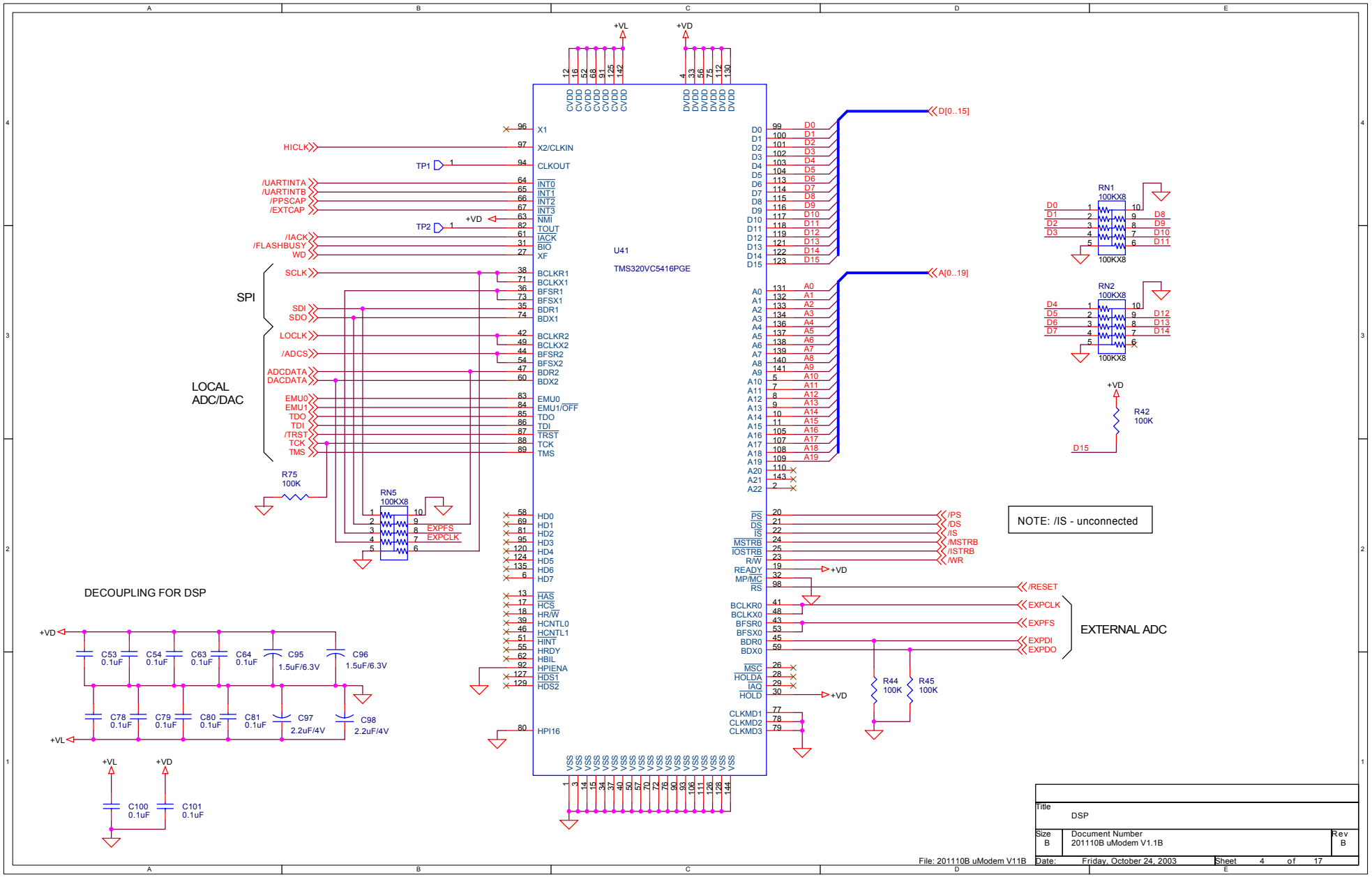
U41
TMS320VC5416PGE
SPI
LOCAL
ADC/DAC
DECOUPLING FOR DSP
EXTERNAL ADC
NOTE: /IS - unconnected
X1
X2/CLKIN
CLKOUT
HICLK
TP1
TP2
/UARTINTA
/UARTINTB
/PPSCAP
/EXTCAP
/IACK
/FLASHBUSY
WD
SCLK
SDI
SDO
LOCLK
/ADCS
ADCDATA
DACDATA
EMU0
EMU1
TDO
TDI
/TRST
TCK
TMS
R75
100K
RN5
100KX8
EXPFS
EXPCLK
D[0..15]
A[0..19]
RN1
RN2
R42
100K
/PS
/DS
/IS
/MSTRB
/ISTRB
/WR
READY
MP/MC
RS
/RESET
BCLKR0
BCLKX0
BFSR0
BFSX0
BDR0
BDX0
EXPCLK
EXPFS
EXPDI
EXPDO
MSC
HOLDA
IAQ
HOLD
R44
100K
R45
100K
CLKMD1
CLKMD2
CLKMD3
HD0
HD1
HD2
HD3
HD4
HD5
HD6
HD7
HAS
HCS
HR/W
HCNTL0
HCNTL1
HINT
HRDY
HBIL
HPIENA
HDS1
HDS2
HPI16
+VL
+VD
C53 0.1uF
C54 0.1uF
C63 0.1uF
C64 0.1uF
C95 1.5uF/6.3V
C96 1.5uF/6.3V
C78 0.1uF
C79 0.1uF
C80 0.1uF
C81 0.1uF
C97 2.2uF/4V
C98 2.2uF/4V
C100 0.1uF
C101 0.1uF
Title
DSP
Size B
Document Number
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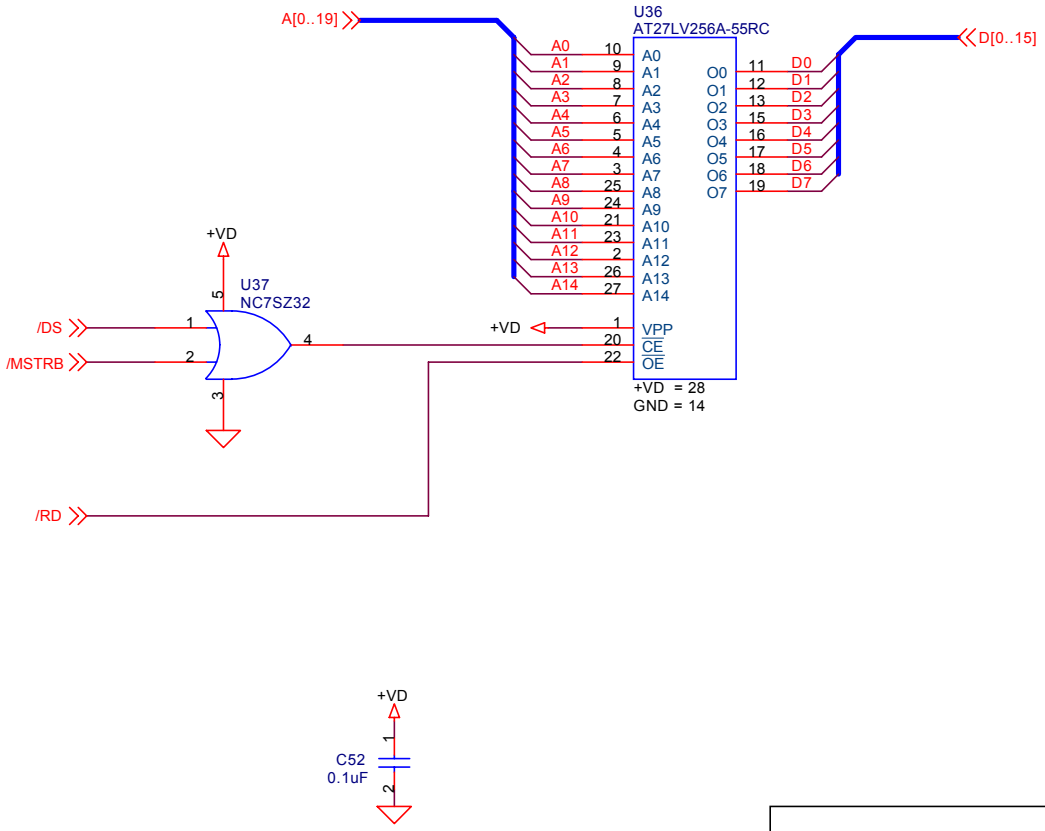
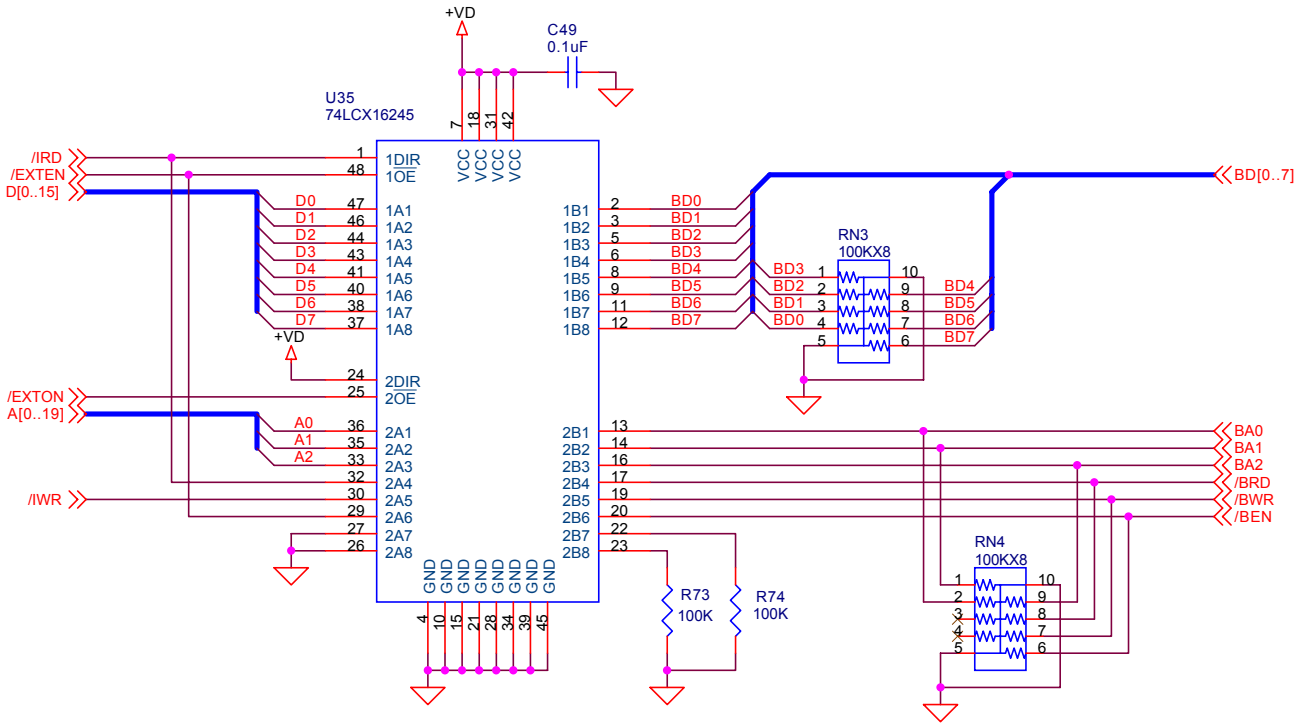
Microchip 27LV256-20 obsolete
Replace with:
Atmel AT27LV256A-55RC

Newer 1.1 layouts are for 330 mil pakcages, namely the Atmel AT27LV256A



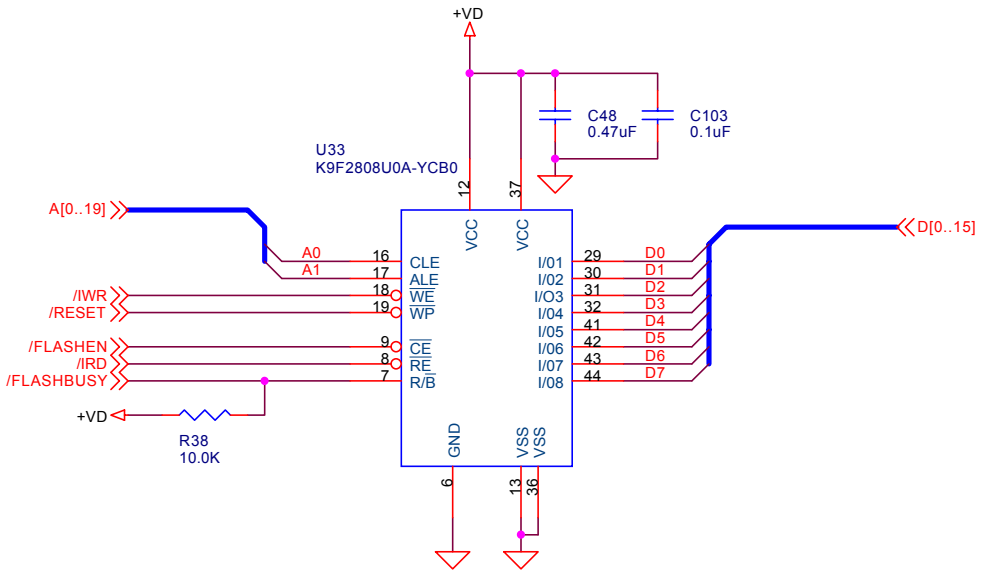
Title	EPROM	
Size A	Document Number 201110B uModem V1.1B	Rev B
Date: Friday, October 24, 2003	Sheet 5 of 17	

File: 201110B uModem V11B



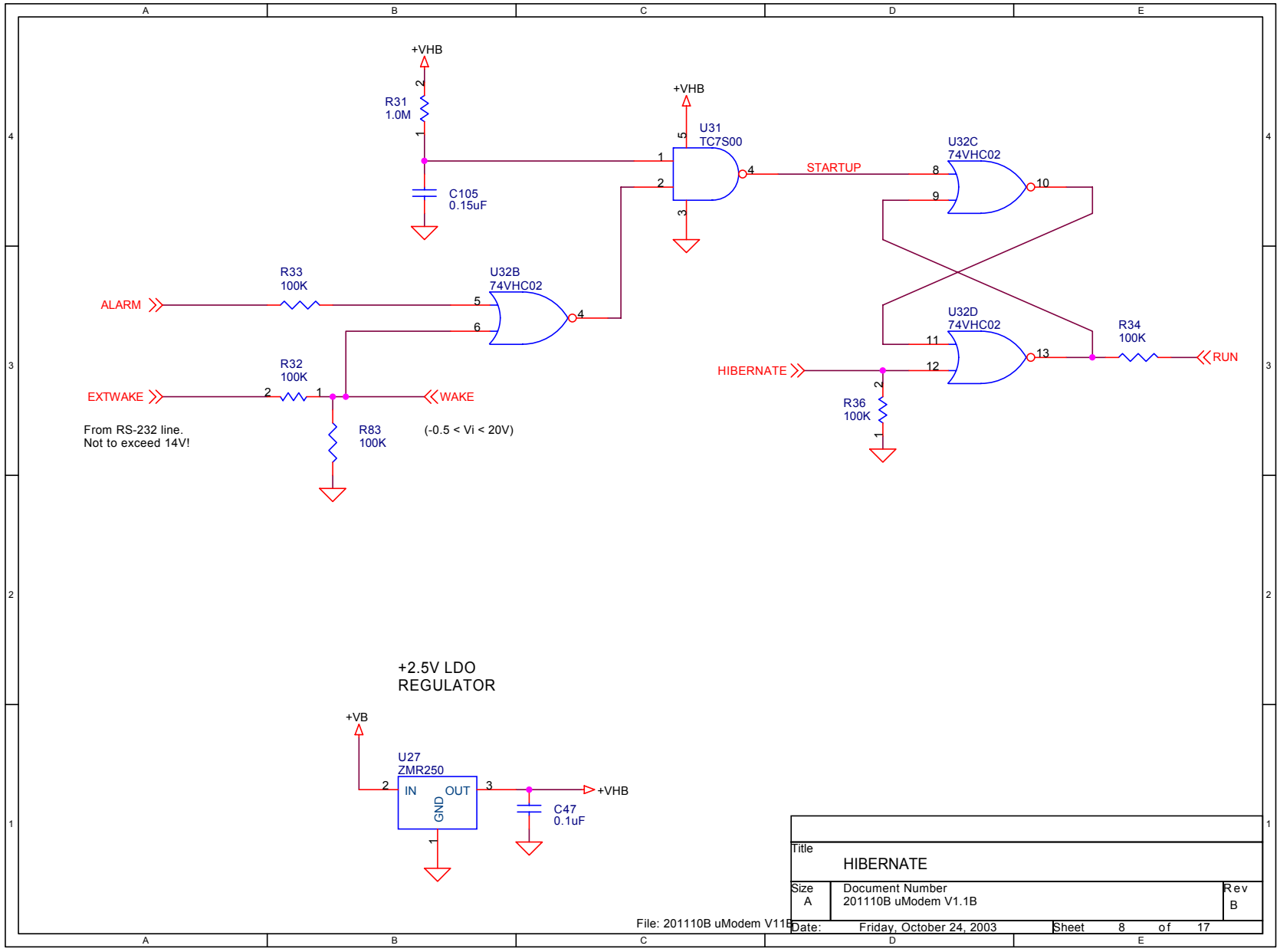
Title	EXTERNAL INTERFACE	
Size A	Document Number 201110B uModem V1.1B	Rev B
Date: Friday, October 24, 2003	Sheet 6 of 17	

File: 201110B uModem V11B



Title	FLASH MEM. (16Mx8)		
Size A	Document Number 201110B uModem V1.1B		Rev B
Date: Friday, October 24, 2003	Sheet 7 of 17		

File: 201110B uModem V11B


+VHB
R31
1.0M
C105
0.15uF
+VHB
U31
TC7S00
STARTUP
U32C
74VHC02
U32D
74VHC02
R34
100K
RUN
HIBERNATE
R36
100K
R33
100K
U32B
74VHC02
ALARM
R32
100K
EXTWAKE
WAKE
R83
100K
From RS-232 line.
Not to exceed 14V!
(-0.5 < Vi < 20V)
+2.5V LDO
REGULATOR
+VB
U27
ZMR250
IN
OUT
GND
+VHB
C47
0.1uF
Title
HIBERNATE
Size
A
Document Number
201110B uModem V1.1B
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B
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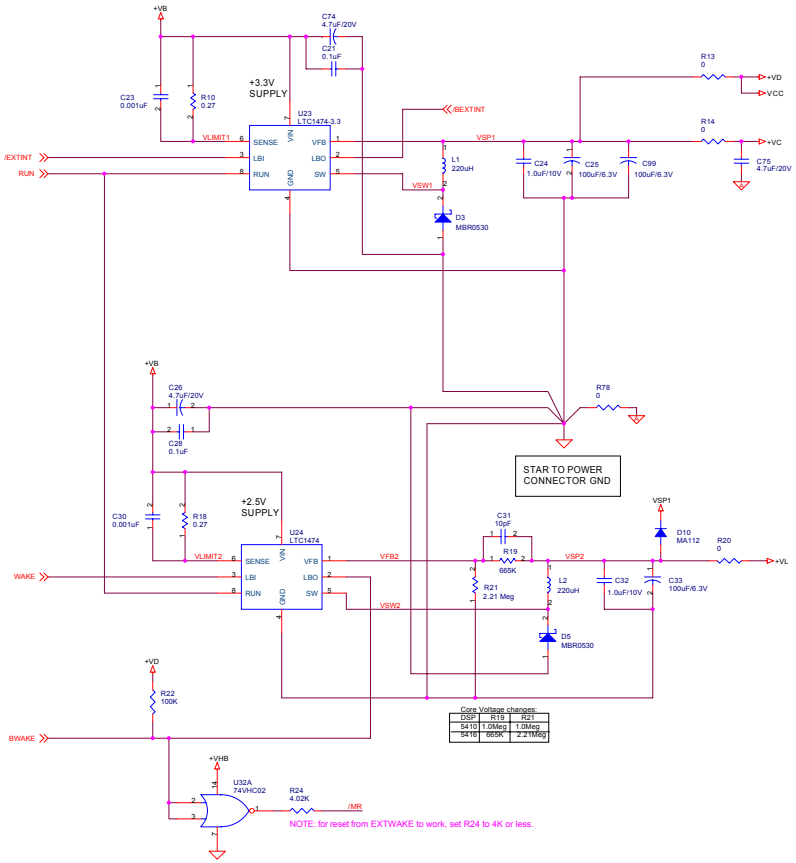
17
File: 201110B uModem V11B

+VB: External Battery Voltage (4-18V)

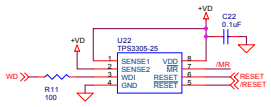


Changes required for 5416 DSP:

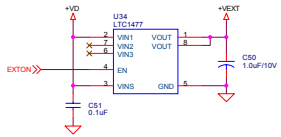
1. R19 = 665k
2. R21 = 2.21M
3. lift U22.2 and tie to U22.1

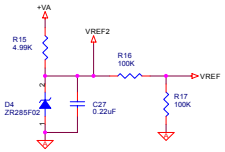
Aug '03 V1.1A Changes
Change value R15 from 10.0K to 4.99k
Change value R24 from 100K to 4K
Change U22.2 from +VL to +VD

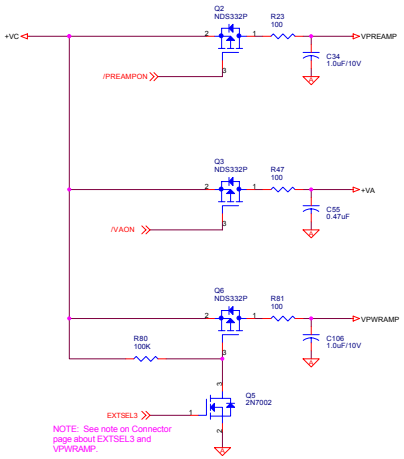
UMODEM SVS



EXTERNAL INTERFACE SUPPLY







SWITCHED ANALOG SUPPLY

NOTE: See note on Connector page about EXTSEL3 and VPWRAMP.

Title: POWER SUPPLIES / RESET

Size	Document Number	Rev
C	201110B uModem V1.1B	B

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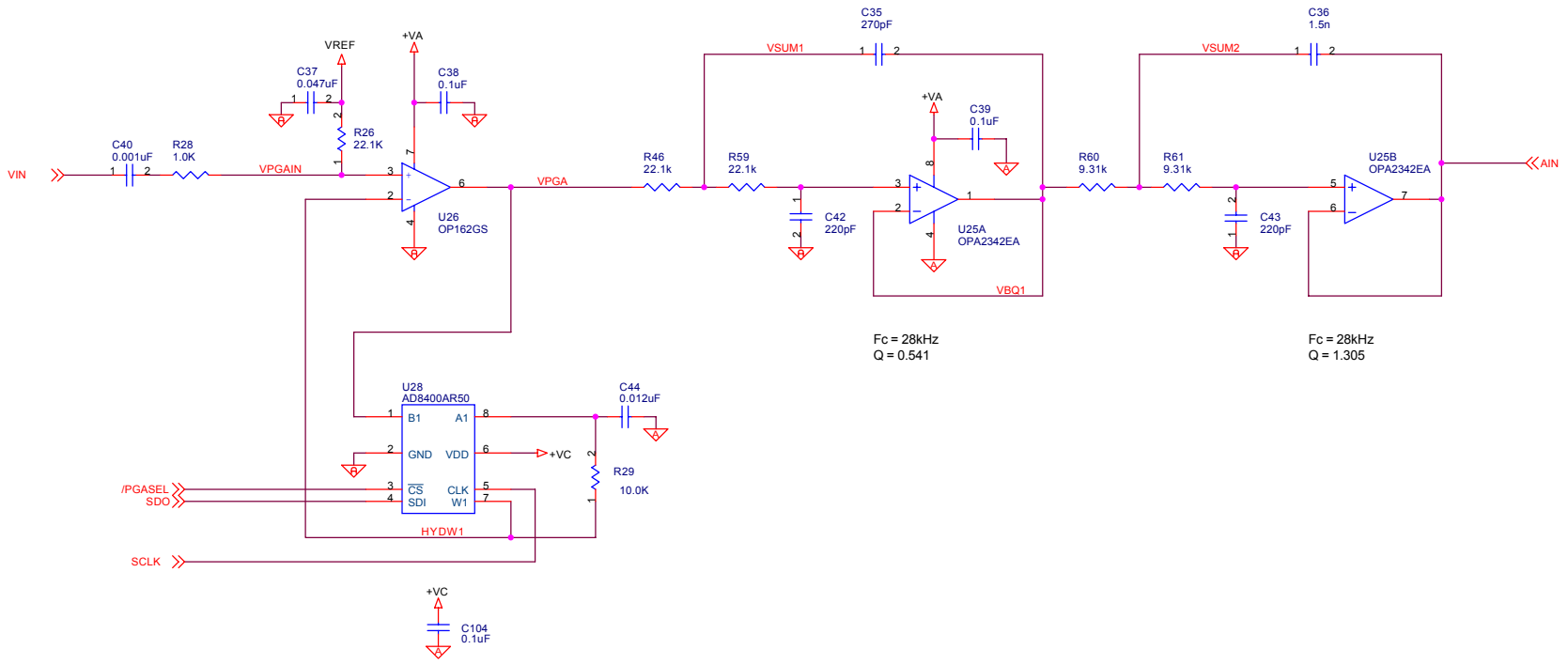
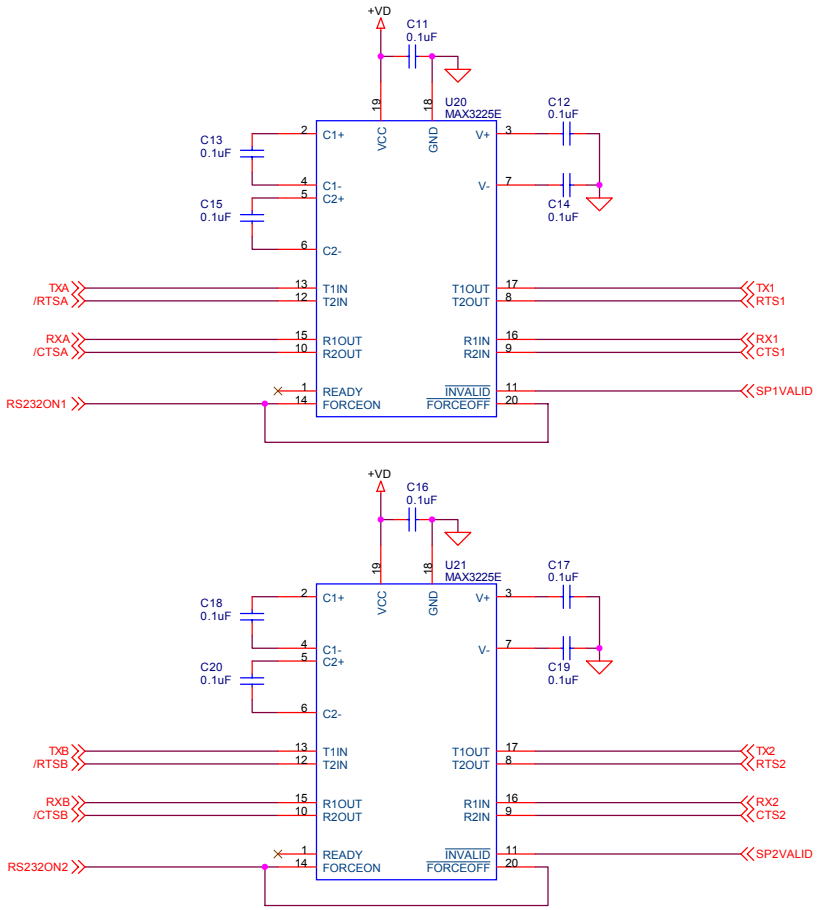
Band	Band A Values 3/2003	Band B Values 3/2003	Band C Values 3/2003
Band A 7-13 KHz Band B 20.0 KHz Band C 30.0 KHz	R46,R59 9.31K R60,R61 9.31K C35 10000 pF C42 680 pF C36 5600 pF C43 390 pF	R46,R59 22.1K R60,R61 9.31K C35 390 pF C42 330 pF C36 2200 pF C43 330 pF	R46,R59 22.1K R60,R61 9.31K C35 270 pF C42 220 pF C36 1500 pF C43 220 pF

Band C used as default values.

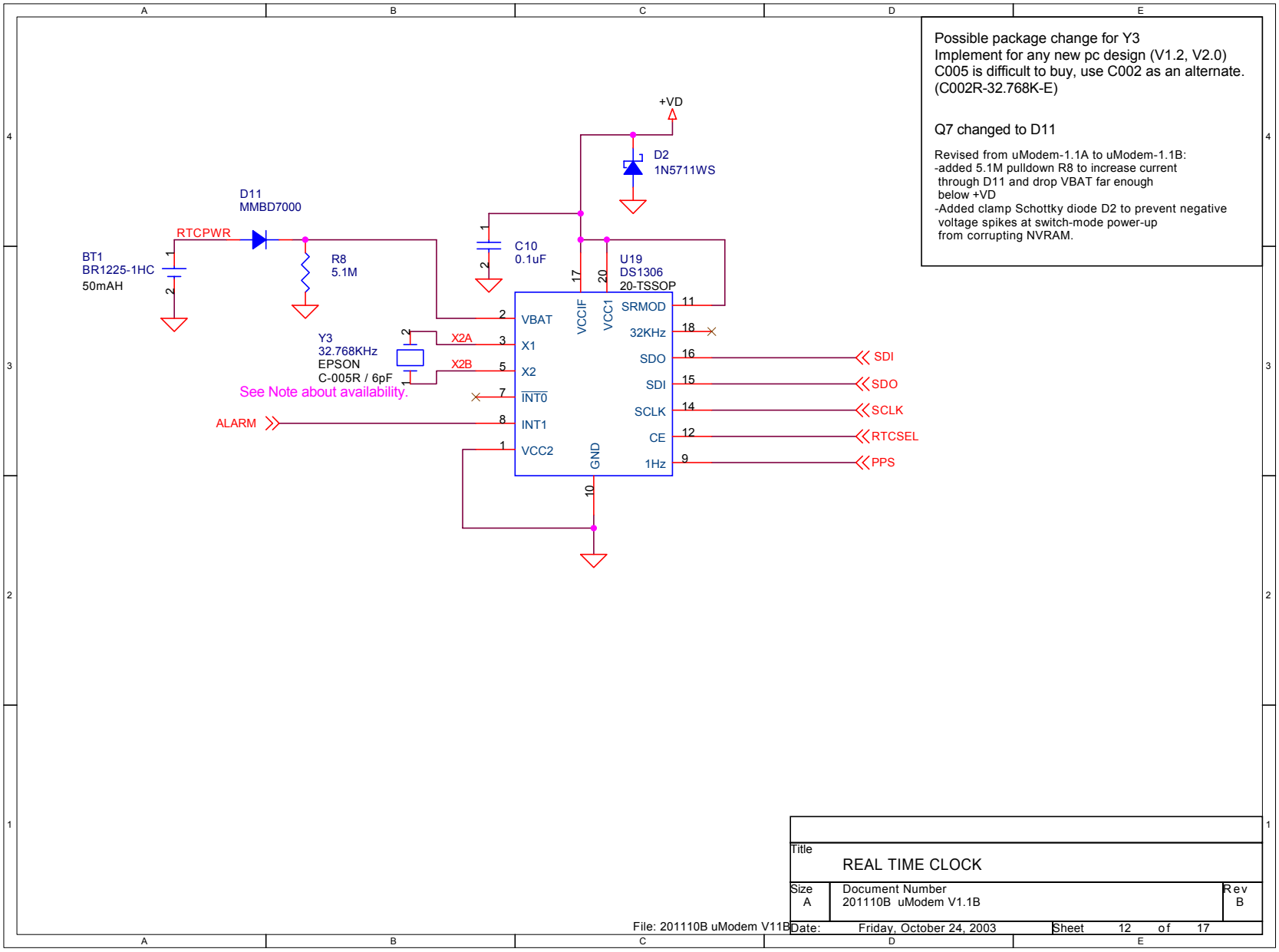


Title	PREAMP & FILTER	
Size B	Document Number 201110B uModem V1.1B	Rev B
File: 201110B uModem V11B	Date: Friday, October 24, 2003	Sheet 10 of 17



Title	RS232 INTERFACE	
Size B	Document Number 201110B uModem V1.1B	Rev B
Date: Friday, October 24, 2003	Sheet 11 of 17	

File: 201110B uModem V11B


Possible package change for Y3
Implement for any new pc design (V1.2, V2.0)
C005 is difficult to buy, use C002 as an alternate.
(C002R-32.768K-E)
Q7 changed to D11
Revised from uModem-1.1A to uModem-1.1B:
-added 5.1M pulldown R8 to increase current through D11 and drop VBAT far enough below +VD
-Added clamp Schottky diode D2 to prevent negative voltage spikes at switch-mode power-up from corrupting NVRAM.
+VD
D2
1N5711WS
D11
MMBD7000
RTCPWR
BT1
BR1225-1HC
50mAH
R8
5.1M
C10
0.1uF
U19
DS1306
20-TSSOP
VBAT
X1
X2
INT0
INT1
VCC2
VCCIF
VCC1
GND
SRMOD
32KHz
SDO
SDI
SCLK
CE
1Hz
Y3
32.768KHz
EPSON
C-005R / 6pF
X2A
X2B
See Note about availability.
ALARM
SDI
SDO
SCLK
RTCSEL
PPS
Title
REAL TIME CLOCK
Size
A
Document Number
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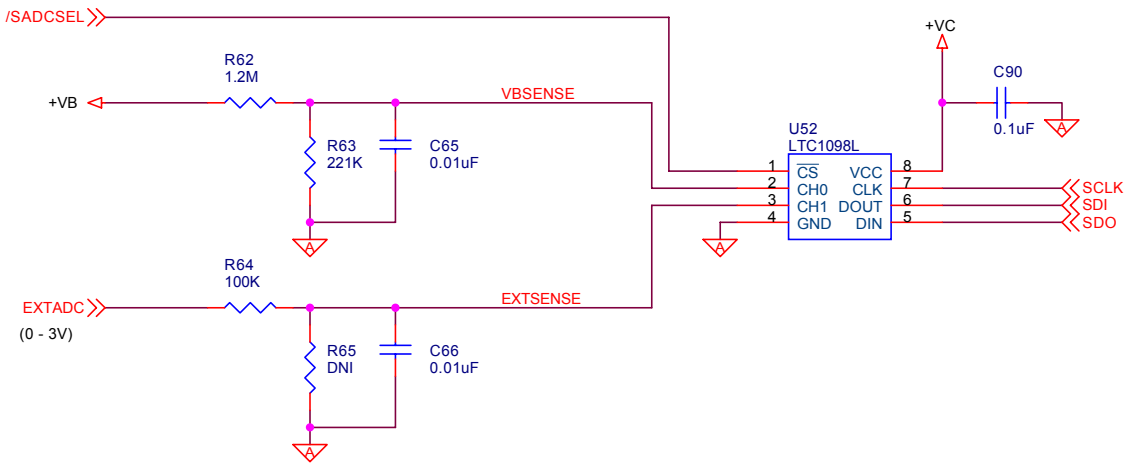
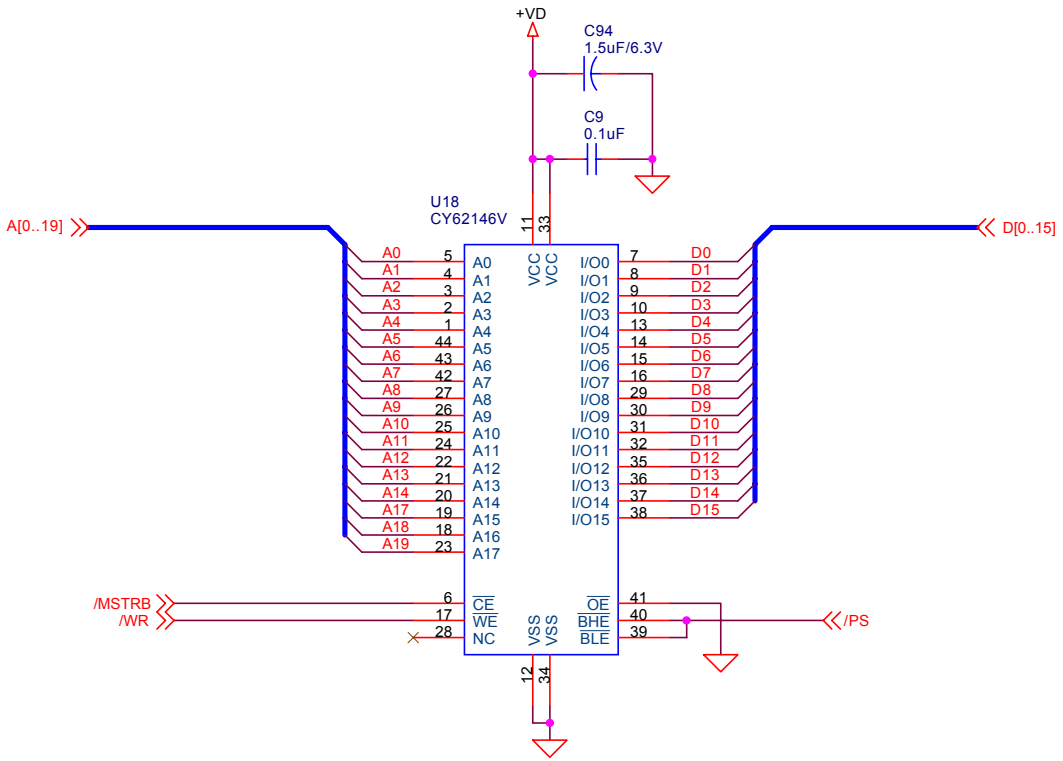


Title	SENSOR ADC (8 BIT)	
Size A	Document Number 201110B uModem V1.1B	Rev B
Date: Friday, October 24, 2003	Sheet 13 of 17	

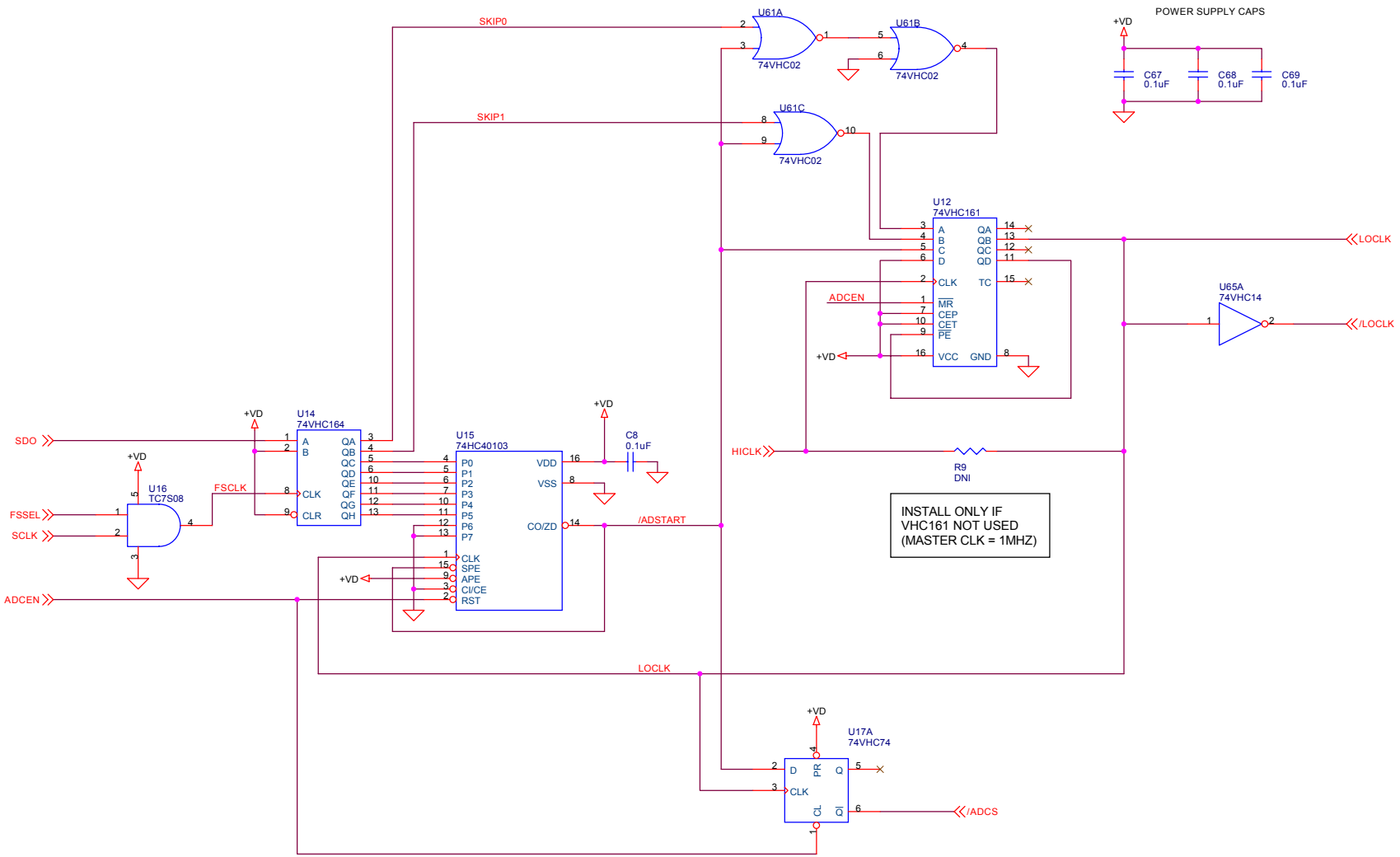
File: 201110B uModem V11B



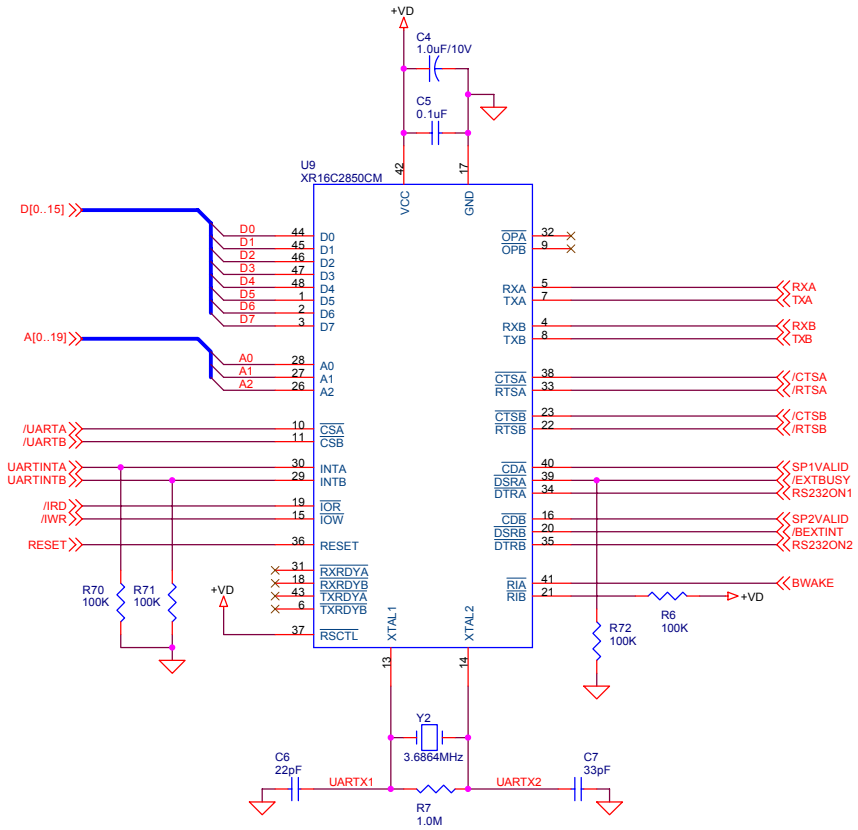
NOTE: A15, A16 from DSP not connected to U18, leading to segmented memory map.

Title: SRAM (256Kx16)		
Size: A	Document Number: 201110B uModem V1.1B	Rev: B
Date: Friday, October 24, 2003	Sheet 14 of 17	

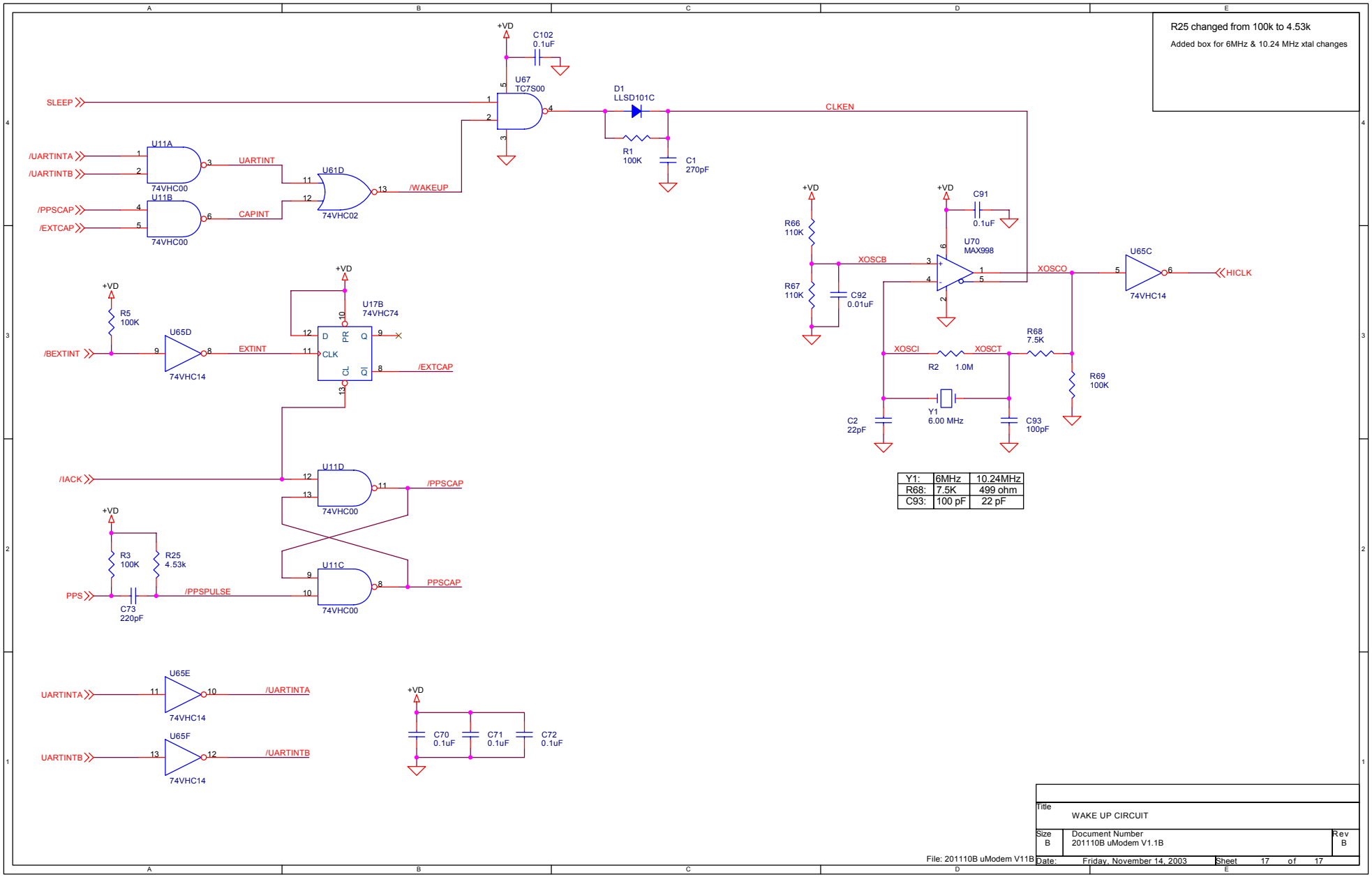
File: 201110B uModem V11B



Title	TIMING GENERATOR	
Size B	Document Number 201110B uModem V1.1B	Rev B
File: 201110B uModem V11B	Date: Friday, October 24, 2003	Sheet 15 of 17



Title	UART	
Size B	Document Number 201110B uModem V1.1B	Rev B
File: 201110B uModem V11B	Date: Friday, October 24, 2003	Sheet 16 of 17


R25 changed from 100k to 4.53k
Added box for 6MHz & 10.24 MHz xtal changes
+VD
C102
0.1uF
U67
TC7S00
SLEEP
D1
LLSD101C
CLKEN
R1
100K
C1
270pF
/UARTINTA
/UARTINTB
U11A
74VHC00
UARTINT
U61D
74VHC02
/WAKEUP
/PPSCAP
/EXTCAP
U11B
74VHC00
CAPINT
R66
110K
R67
110K
XOSCB
C92
0.01uF
U70
MAX998
C91
0.1uF
XOSCO
U65C
74VHC14
HICLK
XOSCI
XOSCT
R68
7.5K
R2
1.0M
R69
100K
Y1
6.00 MHz
C2
22pF
C93
100pF
R5
100K
/BEXTINT
U65D
74VHC14
EXTINT
U17B
74VHC74
D
CLK
PR
CL
Q
QI
/EXTCAP
/IACK
U11D
74VHC00
/PPSCAP
R3
100K
R25
4.53k
PPS
C73
220pF
/PPSPULSE
U11C
74VHC00
PPSCAP
U65E
UARTINTA
74VHC14
/UARTINTA
U65F
UARTINTB
74VHC14
/UARTINTB
C70
0.1uF
C71
0.1uF
C72
0.1uF
Y1: 6MHz 10.24MHz
R68: 7.5K 499 ohm
C93: 100 pF 22 pF
Title
WAKE UP CIRCUIT
Size B
Document Number
201110B uModem V1.1B
Rev B
File: 201110B uModem V11B
Date: Friday, November 14, 2003
Sheet 17 of 17

WHOI Micromodem v1.1B Bill of Materials, 14 Nov 2003, 17:40:00
Document Revision: C

WHOI Micromodem part number: 201110B

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Bill Of Materials 14 Nov 2003, 17:40:00

Item	Quantity	Reference	Part	PCB Footprint	MFG	MFG PN	Notes
1	1	BT1	BR1225-1HC	BR1225-1HC	PANASONIC	BR1225-1HC	
2	2	C1,C35	270pF	603	PANASONIC	ECU-V1H271JCV	Alternate Part: ECJ-1VC1H271J
3	2	C2,C6	22pF	603	PANASONIC	ECU-V1H220JCV	Alternate Parts: ECJ-1VC1H220J,
							C0603C220J5GACTU
4	8	C4,C24,C32,C34,C50,C84,	1.0uF/10V	TES-P	PANASONIC	ECS-T1AP105R	
		C89,C106					
5	52	C5,C8,C9,C10,C11,C12,C13,	0.1uF	603	PANASONIC	ECJ-1VB1C104K	
		C14,C15,C16,C17,C18,C19,					
		C20,C21,C22,C28,C38,C39,					
		C47,C49,C51,C52,C53,C54,					
		C58,C59,C60,C61,C63,C64,					
		C67,C68,C69,C70,C71,C72,					
		C78,C79,C80,C81,C85,C86,					
		C87,C88,C90,C91,C100,					
		C101,C102,C103,C104					
6	1	C7	33pF	603	PANASONIC	ECU-V1H330JCV	Alternate Part: ECJ-1VC1H330J
7	3	C23,C30,C40	0.001uF	603	PANASONIC	ECU-V1H102KBV	Alternate Part: ECJ-1VB1H102K
8	3	C25,C33,C99	100uF/6.3V	C-CASE	KEMET	T494C107M006AS	
9	3	C26,C74,C75	4.7uF/20V	B-CASE	KEMET	T494B475M020AS	
10	1	C27	0.22uF	603	PANASONIC	ECJ-1VB1A224K	
11	1	C31	10pF	603	PANASONIC	ECJ-1VC1H100D	
12	1	C36	1.5n	603	PANASONIC	ECJ-1VB1H152K	
13	1	C37	0.047uF	603	PANASONIC	ECJ-1VB1E473K	

14	3	C42,C43,C73	220pF	603	PANASONIC	ECJ-1VC1H221J	
15	1	C44	0.012uF	603	PANASONIC	ECU-V1H123KBV	Alternate Part: ECJ-1VB1H123K
16	2	C55,C48	0.47uF	603	PANASONIC	ECJ-1VBOJ474K	
17	2	C57,C56	470pF	603	PANASONIC	ECJ-1VC1H471J	
18	1	C62	0.0033uF	603	PANASONIC	ECU-V1H332KBV	Alternate Part: ECJ-1VB1H332K
19	3	C65,C66,C92	0.01uF	603	PANASONIC	ECJ-1VB1H103K	
20	1	C93	100pF	603	PANASONIC	ECU-V1H101JCV	Alternate Part: ECJ-1VC1H101J
21	3	C94,C95,C96	1.5uF/6.3V	TES-Z	PANASONIC	ECS-TOJZ155R	
22	2	C98,C97	2.2uF/4V	TES-Z	PANASONIC	ECS-TOGZ225R	
23	1	C105	0.15uF	805	PANASONIC	ECJ-1VB1C154K	
24	1	D1	LLSD101C	MMELF	VISHAY/LITEON	LLSD101C	
25	1	D2	1N5711WS	SOD323	Diodes, Inc	1N5711WS	
26	2	D3,D5	MBR0530	SOD-123	MOTOROLA	MBR0530	
27	1	D4	ZR285F02	SOT-23	ZETEX	ZR285F02	
28	1	D7	MBRA130LT3	DIODE_SMA	MOTOROLA	MBRA130LT3	Do Not Install
	1	D8	MBRA130LT3	DIODE_SMA	MOTOROLA	MBRA130LT3	
29	1	D9	SML-LX1210IGC	SMLX1210	LUMEX	SML-LX1210IGC	
30	1	D10	MA112	S-MINI	PANASONIC	MA112	
31	1	D11	MMBD7000		Motorola	MMBD7000	
32	2	JP1,JP4	RTA HDR(3X2)	43045-6	MOLEX	43045-0602	
33	1	JP2	STR REC(7X2)	79109-14	MOLEX	79109-0006	
34	1	JP3	STR REC(9X2)	79109-18	MOLEX	79109-0008	
35	1	JP5	RTA HDR(6X2)	87333-12	MOLEX	87333-1220	
36	1	JP6	STR REC(6X2)	79109-12	MOLEX	79109-0005	
37	1	JP7	STR HDR(7X2)	VHDR7X2	SULLINS	PZC07DAAN	
38	1	JP8	RTA HDR(2X2)	43045-4	MOLEX	43045-0402	
39	2	L1,L2	220uH	DS1608	COILCRAFT	DS1608-224	
40	3	Q2,Q3,Q6	NDS332P	SOT-23	FAIRCHILD	NDS332P	
41	1	Q5	2N7002	SOT-23	FAIRCHILD	2N7002	
42	5	RN1,RN2,RN3,RN4,RN5	100KX8	CTS-746	CTS	746X101104J	
43	24	R1,R3,R5,R6,R16,R17,R22,	100K	603	PANASONIC	ERJ-3EKF1003V	
		R32,R33,R34,R36,R42,R44,					
		R45,R64,R69,R70,R71,R72,					
		R73,R74,R75,R80,R83					
44	3	R2,R7,R31	1.0M	603	PANASONIC	ERJ-3EKF1004V	
45	2	R4,R50	49.9	603	PANASONIC	ERJ-3EKF49R9V	
46	1	R8	5.1M	603	Panasonic	ERJ-3GEYJ515V	

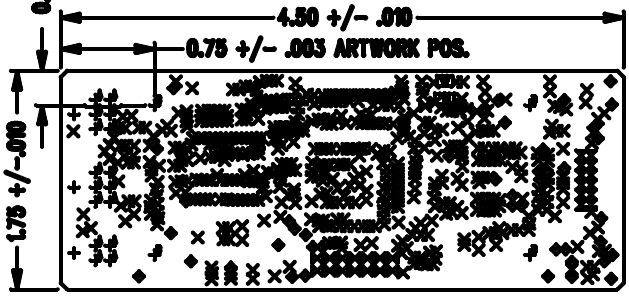
47	3	R9,R65,R82	DNI	603	PANASONIC	ERJ-3EKFxxxx	Do Not Install
48	2	R10,R18	0.27	805	PANASONIC	ERJ-6RQFR27V	
49	5	R11,R23,R47,R77,R81	100	603	PANASONIC	ERJ-3EKF1000V	
50	4	R13,R14,R20,R78	0	603	PANASONIC	ERJ-3GEYJ0R0V	
51	1	R15	4.99K	603	PANASONIC	ERJ-3EKF4991V	
52	1	R19	665K	603	PANASONIC	ERJ-3EKF6653V	
53	1	R21	2.21 Meg	603	PANASONIC	ERJ-3EKF2214V	
54	1	R24	4.02K	603	PANASONIC	ERJ-3EKF4021V	
55	1	R25	4.53k	603	PANASONIC	ERJ-3EKF4531V	
56	3	R26,R46,R59	22.1k	603	PANASONIC	ERJ-3EKF2212V	
57	1	R28	1.0K	603	PANASONIC	ERJ-3EKF1001V	
58	4	R29,R38,R54,R55	10.0K	603	PANASONIC	ERJ-3EKF1002V	
59	2	R48,R49	11.0K	603	PANASONIC	ERJ-3EKF1102V	
60	2	R56,R57	150	603	PANASONIC	ERJ-3EKF1500V	
61	1	R58	499	603	PANASONIC	ERJ-3EKF4990V	
62	2	R60,R61	9.31k	603	PANASONIC	ERJ-3EKF9311	
63	1	R62	1.2M	603	PANASONIC	ERJ-3EKF1204V	
64	1	R63	221K	603	PANASONIC	ERJ-3EKF2213V	
65	2	R66,R67	110K	603	PANASONIC	ERJ-3EKF1103V	
66	1	R68	7.5K	603	PANASONIC	ERJ-3EKF7501V	
67	2	TP1,TP2	T POINT F	TPSMD			Do Not Install
68	1	TP3	TEST POINT		Keystone	5015	
69	1	U9	XR16C2850CM	TQFP-48	EXAR	XR16C2850CM	
70	1	U11	74VHC00	TSSOP-14	FAIRCHILD	74VHC00MTC	
71	1	U12	74VHC161	TSSOP-16	FAIRCHILD	74VHC161MTC	
72	1	U14	74VHC164	TSSOP-14	FAIRCHILD	74VHC164MTC	
73	1	U15	74HC40103	TSSOP-16	PHILIPS	74HC40103PW	
74	1	U16	TC7S08	SSOP5-P-0.95	TOSHIBA	TC7S08F	
75	1	U17	74VHC74	TSSOP-14	FAIRCHILD	74VHC74MTC	
76	1	U18	CY62146V	TSOP-II	CYPRESS	CY62146VLL-70ZI	
77	1	U19	DS1306	TSSOP-20	DALLAS	DS1306E	
78	2	U20,U21	MAX3225E	SSOP-20	MAXIM	MAX3225EAP	
79	1	U22	TPS3305-25	MSOP-8	TEXAS INST	TPS3305-25DGN	
80	1	U23	LTC1474-3.3	MSOP-8	LINEAR TECH.	LTC1474CMS8-3.3	
81	1	U24	LTC1474	MSOP-8	LINEAR TECH.	LTC1474CMS8	
82	1	U25	OPA2342EA	MSOP-8	BURR-BROWN	OPA2342EA	
83	1	U26	OP162GS	SO-8	ANALOG DEVICES	OP162GS	

84	1	U27	ZMR250	SOT-23	ZETEX	ZMR250F	
85	1	U28	AD8400AR50	SO-8	ANALOG DEVICES	AD8400AR50	
86	2	U67,U31	TC7S00	SSOP5-P-0.95	TOSHIBA	TC7S00F	
87	2	U61,U32	74VHC02	TSSOP-14	FAIRCHILD	74VHC02MTC	
88	1	U33	K9F2808U0A-YCB0	TSOP-I	Samsung	K9F2808U0A-YCB0	
89	1	U34	LTC1477	SO-8	LINEAR TECH	LTC1477CS8	
90	1	U35	74LCX16245	TSSOP-48	FAIRCHILD	74LCX16245MTD48	
91	1	U36	AT27LV256A-55RC	SO-28	ATMEL	AT27LV256A-55RC	
92	1	U37	NC7SZ32	SSOP5-P-0.95	FAIRCHILD	NC7SZ32M5	
93	1	U41	TMS320VC5416PGE	PQFP-G144	TEXAS INST	TMS320VC5416PGE	
94	1	U42	TLV5616	MSOP-8	TEXAS INST	TLV5616CDGK	
95	1	U43	LT1637	MSOP-8	LINEAR TECH	LT1637CMS8	
96	2	U45,U48	74VHC273	TSSOP-20	FAIRCHILD	74VHC273MTC	
97	1	U46	74VHC138	TSSOP-16	FAIRCHILD	74VHC138MTC	
98	1	U50	ADS7822EC	MSOP-8	BURR-BROWN	ADS7822EC	
99	1	U52	LTC1098L	SO-8	LINEAR TECH	LTC1098LCS8	
100	1	U65	74VHC14	TSSOP-14	FAIRCHILD	74VHC14MTC	
101	1	U68	74VHC32	TSSOP-14	FAIRCHILD	74VHC32MTC	
102	1	U69	TC7W04	SOP8-P-1.27	TOSHIBA	TC7W04F	
103	1	U70	MAX998	SOT-23-6	MAXIM	MAX998EUT-T	
104	1	Y1	6.00 MHz	HCM49	CITIZEN	HCM49-6.000MABJ	
105	1	Y2	3.6864MHz	HCM49	CITIZEN	HCM49-3.6864MABJ	
106	1	Y3	32.768KHz	C-005R	EPSON	C-005R-32.768K-E	

PWB SKETCH WOODS HOLE OCEANOGRAPHIC INST. uMODEM V1.1B OCT 28 2003

NOTES:

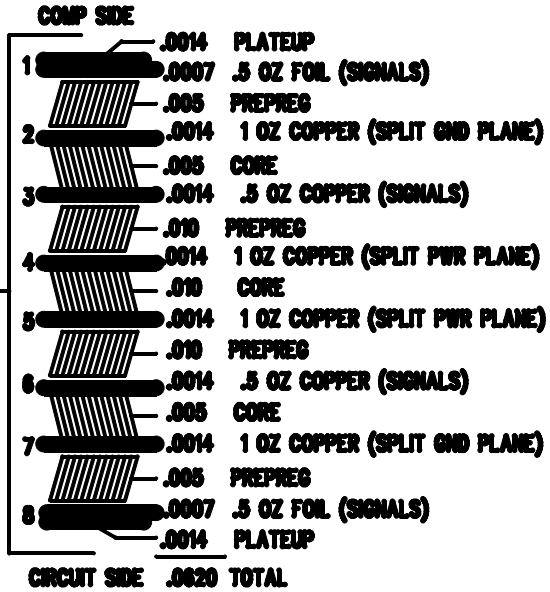
1. FABRICATE USING GERBER MASTERS MARKED uMODEM V1.1B OCT 28 2003.
2. FABRICATE AND TEST PER ANSI/IPC-RB-276 AND ANSI/IPC-A-600, CLASS 2. MATERIAL TO BE TYPE FR-4 PER MIL-P-13949/4. ALL LAYERS TO BE ONE OUNCE COPPER, INNER SIGNAL MAY BE 1 OR 1/2 OUNCE.
3. UNLESS OTHERWISE SPECIFIED, ALL HOLES AND CONDUCTORS SHALL BE COPPER PLATED.
4. MINIMUM CONDUCTOR WIDTH TO BE .005" (SPACING IS .005).
5. BOARD THICKNESS SHALL BE .062 +/- .007 INCLUDING ALL PLATINGS AND COATINGS, AND SHALL BE MEASURED ACROSS THE BOARD THICKNESS EXTREMES.
6. VENDOR CAGE CODE NUMBER, DATE AND/OR LOT IDENTIFICATION NUMBER SHALL BE MARKED ON PRINTED WIRING BOARD, LOCATION OPTIONAL.
7. SILKSCREEN COMPONENT OUTLINES AND REFERENCE DESIGNATORS ON BOTH SIDES USING CONTRASTING COLORED INK.
8. SOLDERMASK SHALL BE LIQUID PHOTOIMAGEABLE (LPI) (MATTE FINISH PREFERRED) APPLIED ON BOTH SIDES OVER BARE COPPER AND SHALL MEET SPEC IPC-SM-840 CLASS 3 (LATEST REV). ALL VIAS ARE TENTED.
9. SOLDERCOAT CONDUCTORS NOT COVERED BY SOLDERMASK; HASL.
10. LAYUP PER DETAIL A.

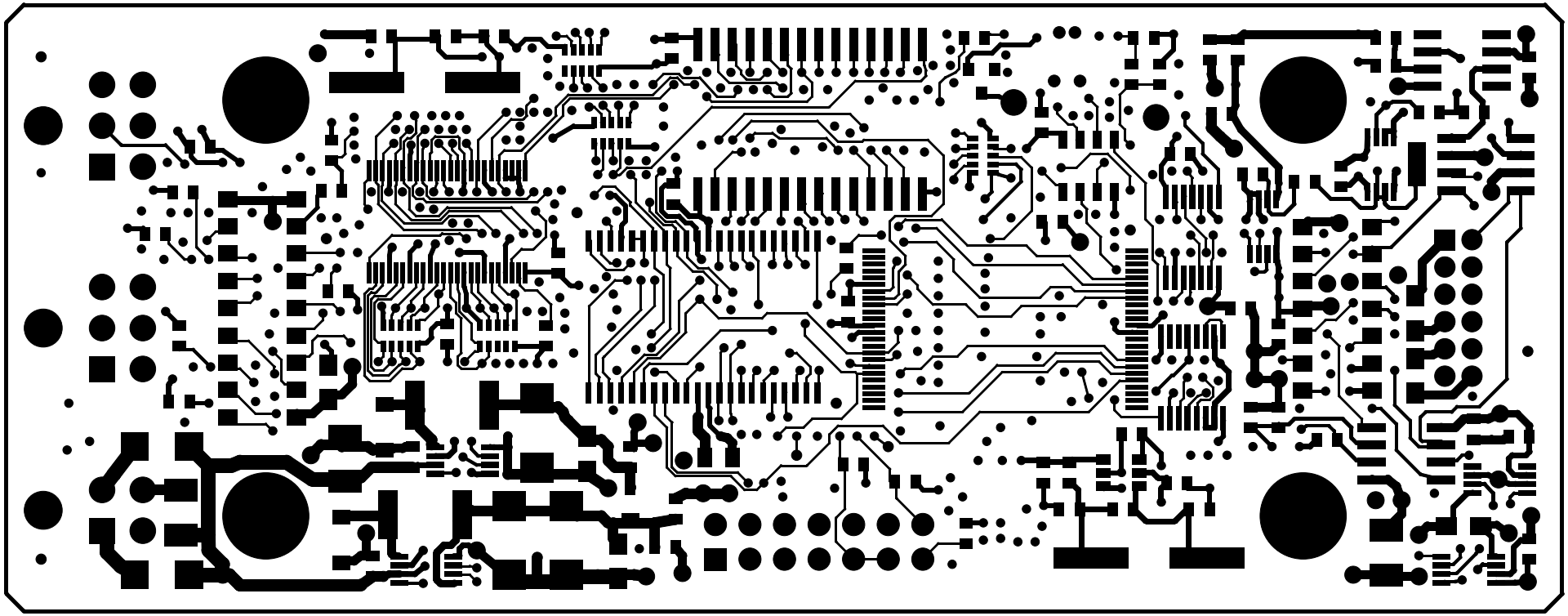


HOLE DATA (AFTER PLATING)			
SYM	DESCRIPTION	QTY	
+	.118 +/- .004	3	UNPLATED
X	.010 +.003/-.010	564	PLATED
□	.013 +/- .003	4	PLATED
◇	.025 +/- .003	41	PLATED
⧗	.032 +/- .003	12	PLATED
⋈	.035 +/- .003	16	PLATED
+A	.040 +/- .003	16	PLATED
+B	.094 +/- .003	4	PLATED

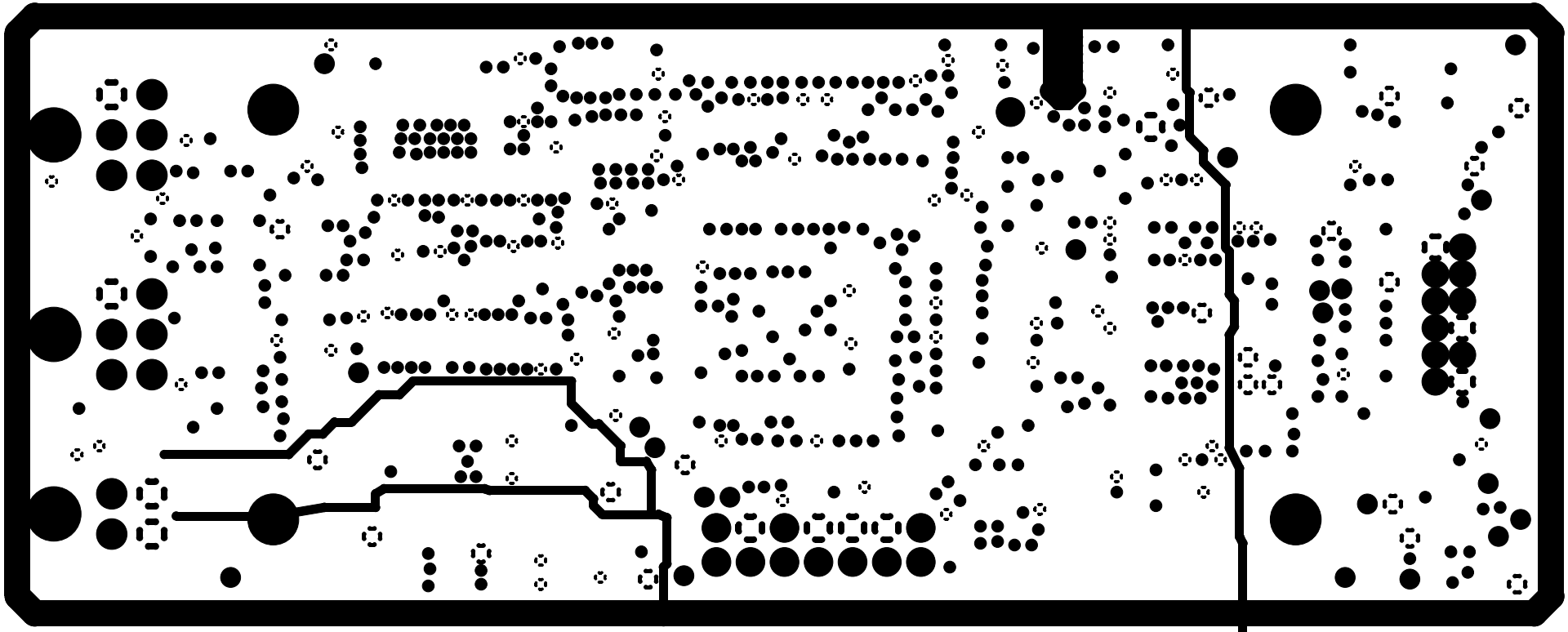
8 LAYERS
.062 +/- .007

DETAIL A

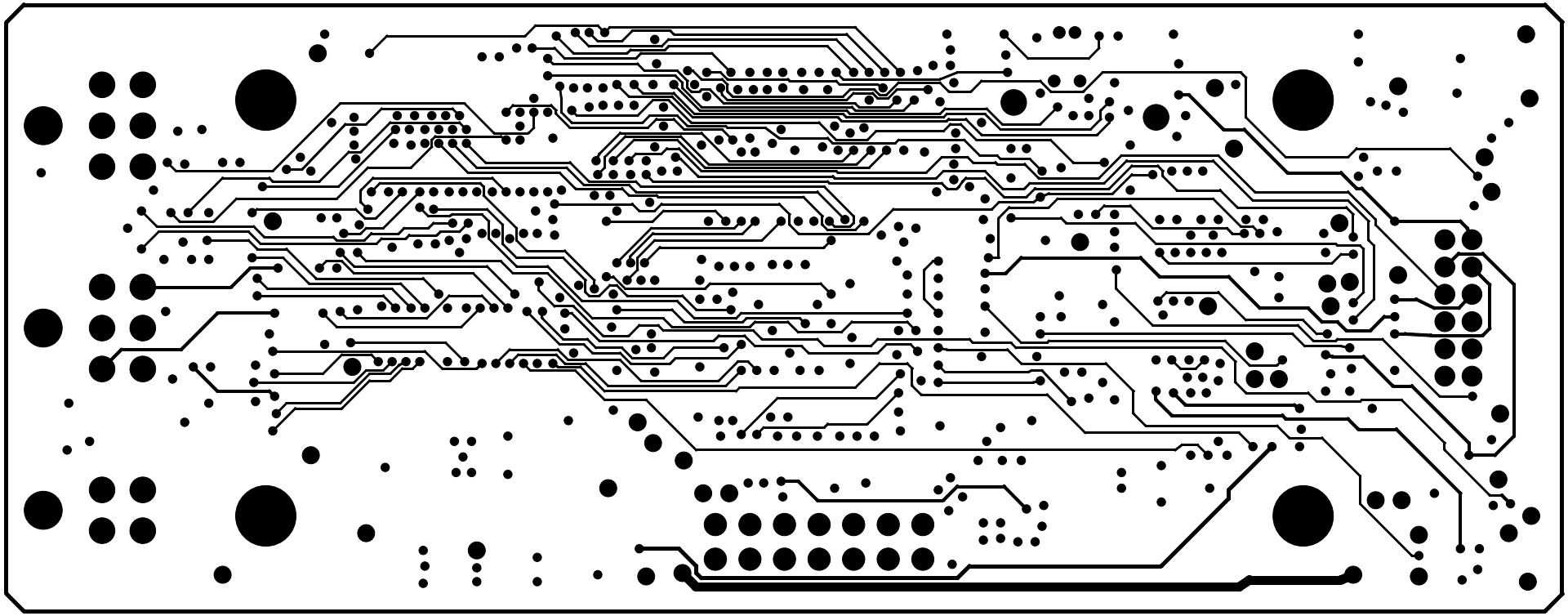




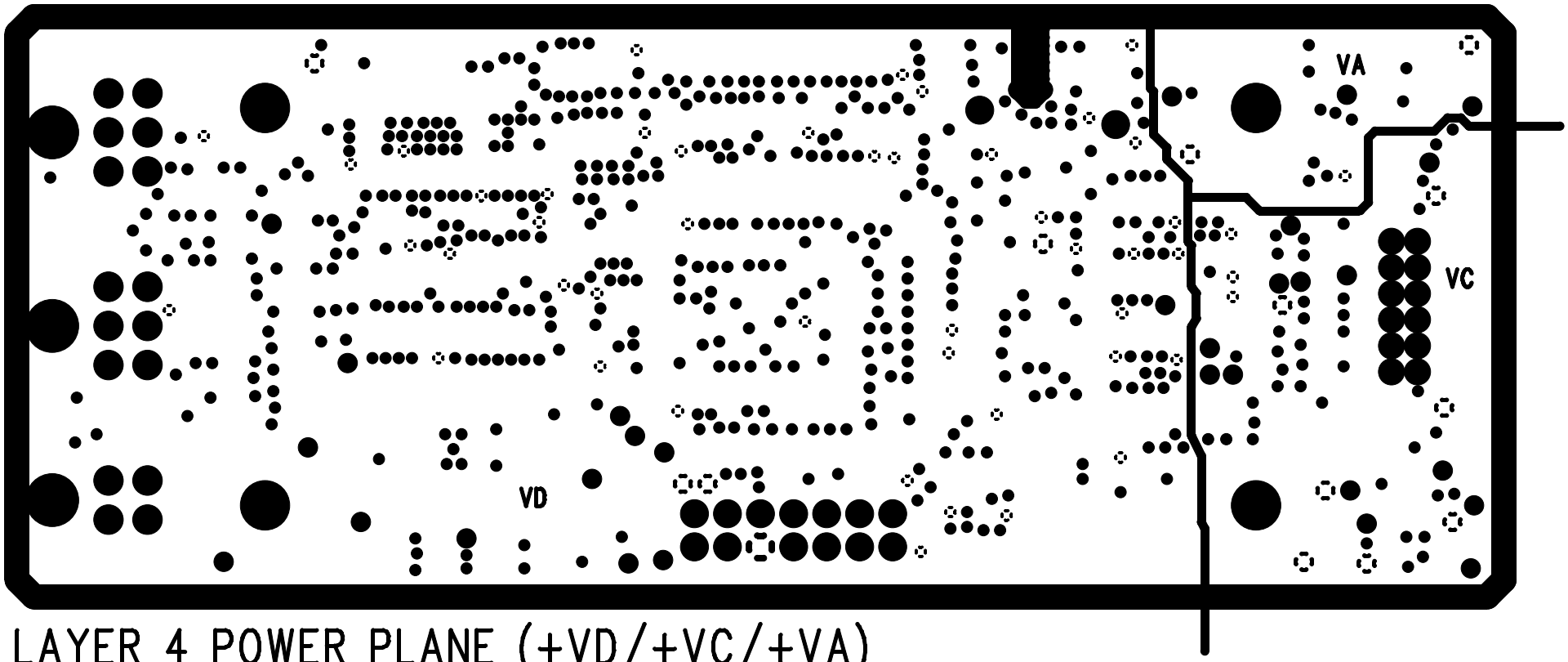
COMPONENT SIDE LAYER 1
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



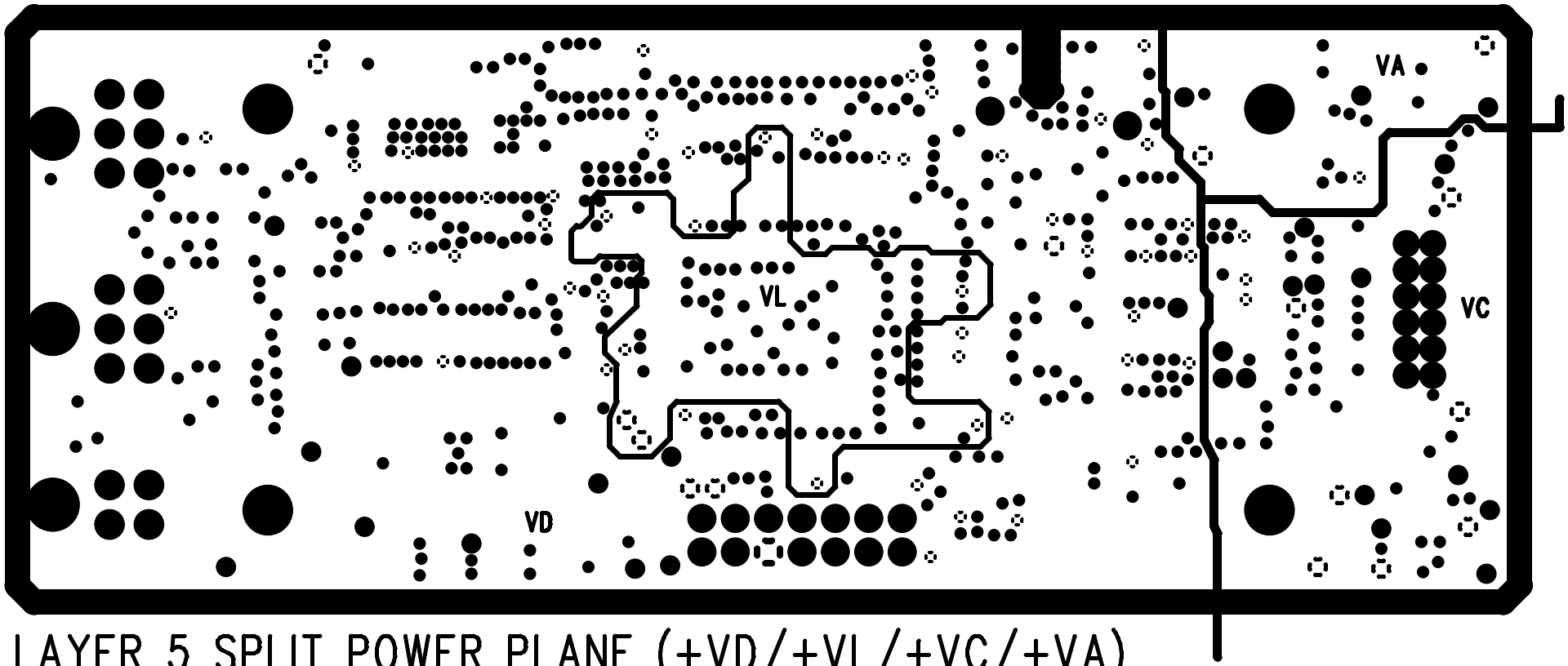
LAYER 2 SPLIT GROUND PLANE (GND/AGND)
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



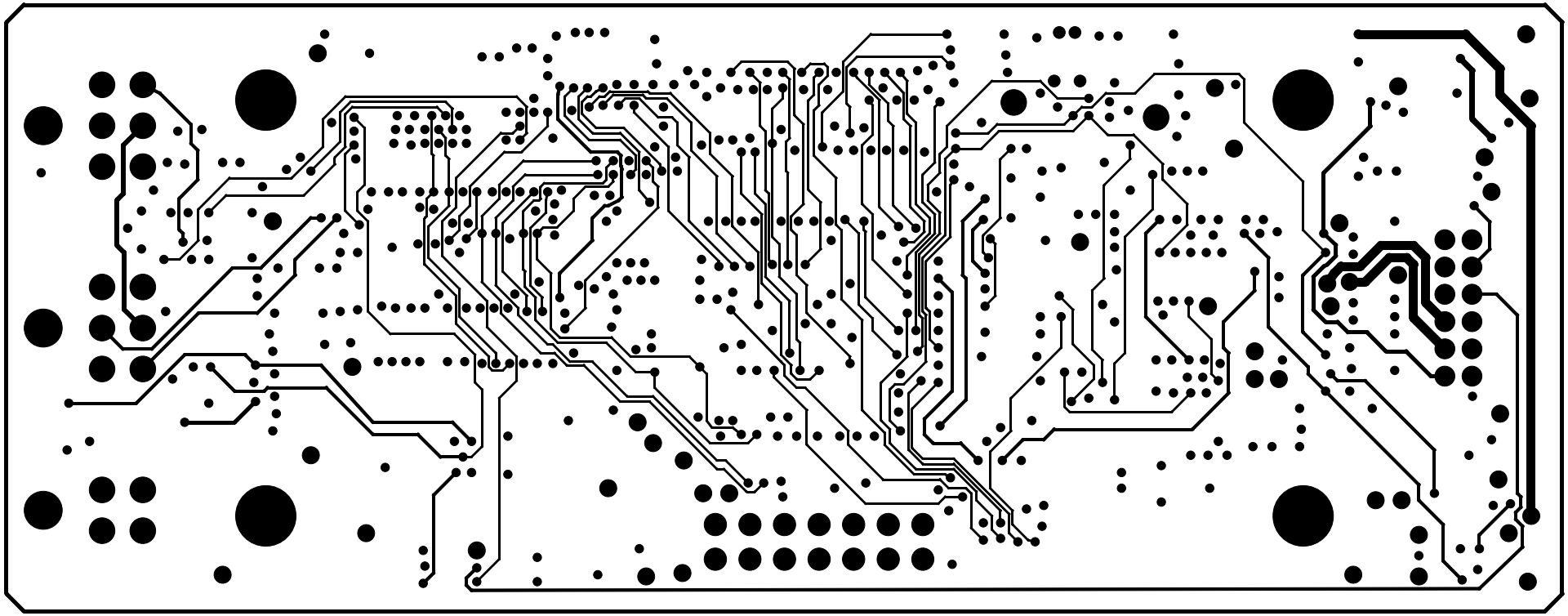
LAYER 3 SIGNALS
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



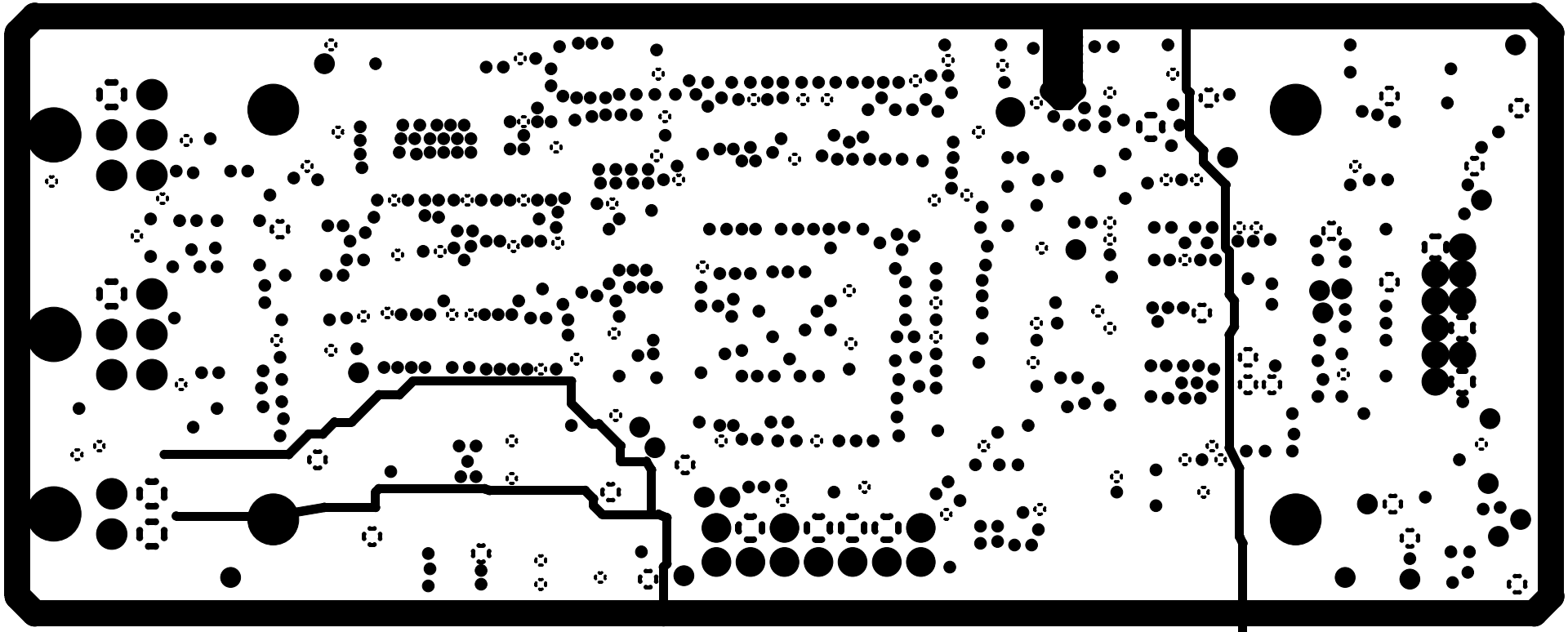
LAYER 4 POWER PLANE (+VD/+VC/+VA)
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



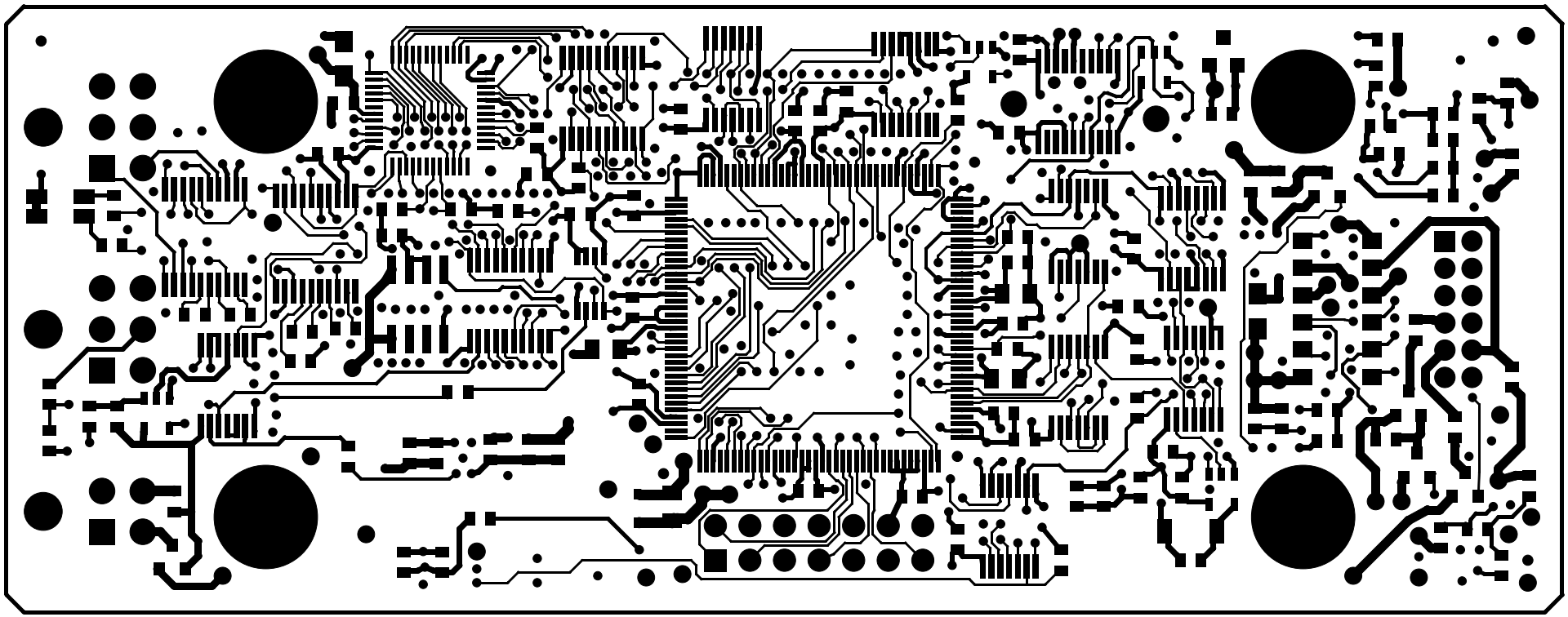
LAYER 5 SPLIT POWER PLANE (+VD/+VL/+VC/+VA)
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



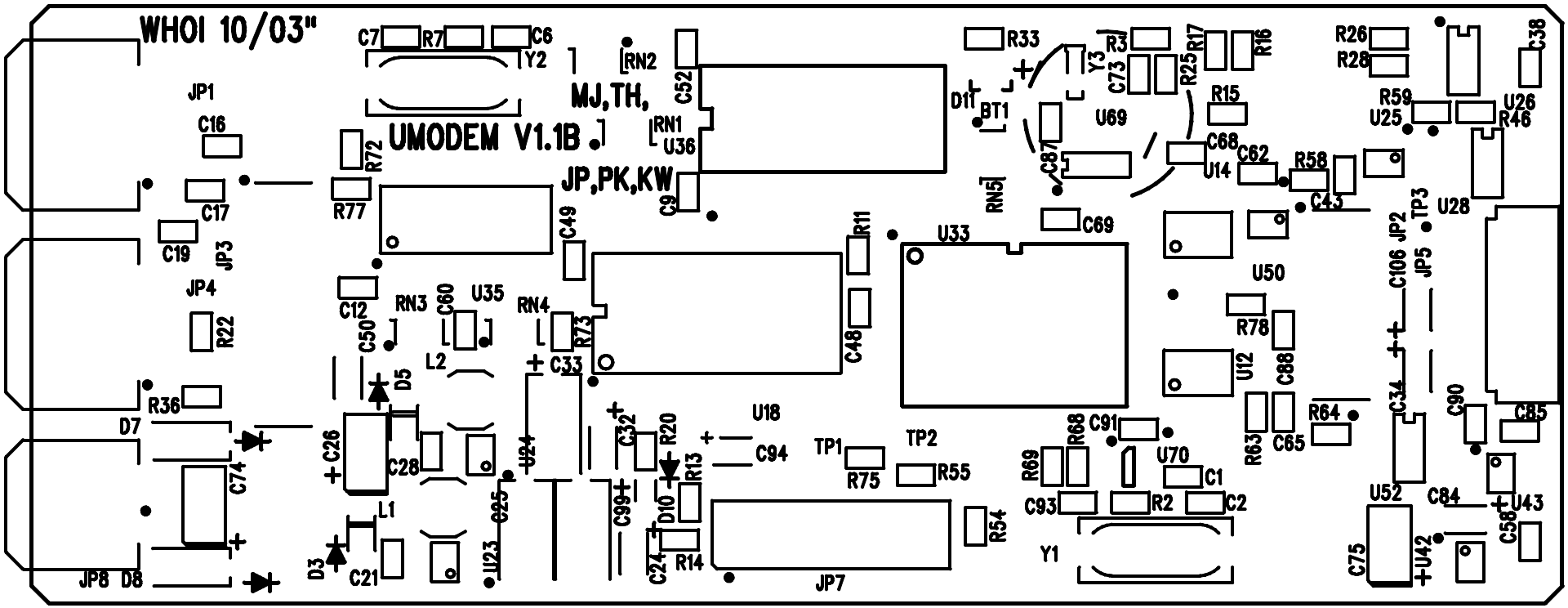
LAYER 6 SIGNALS
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



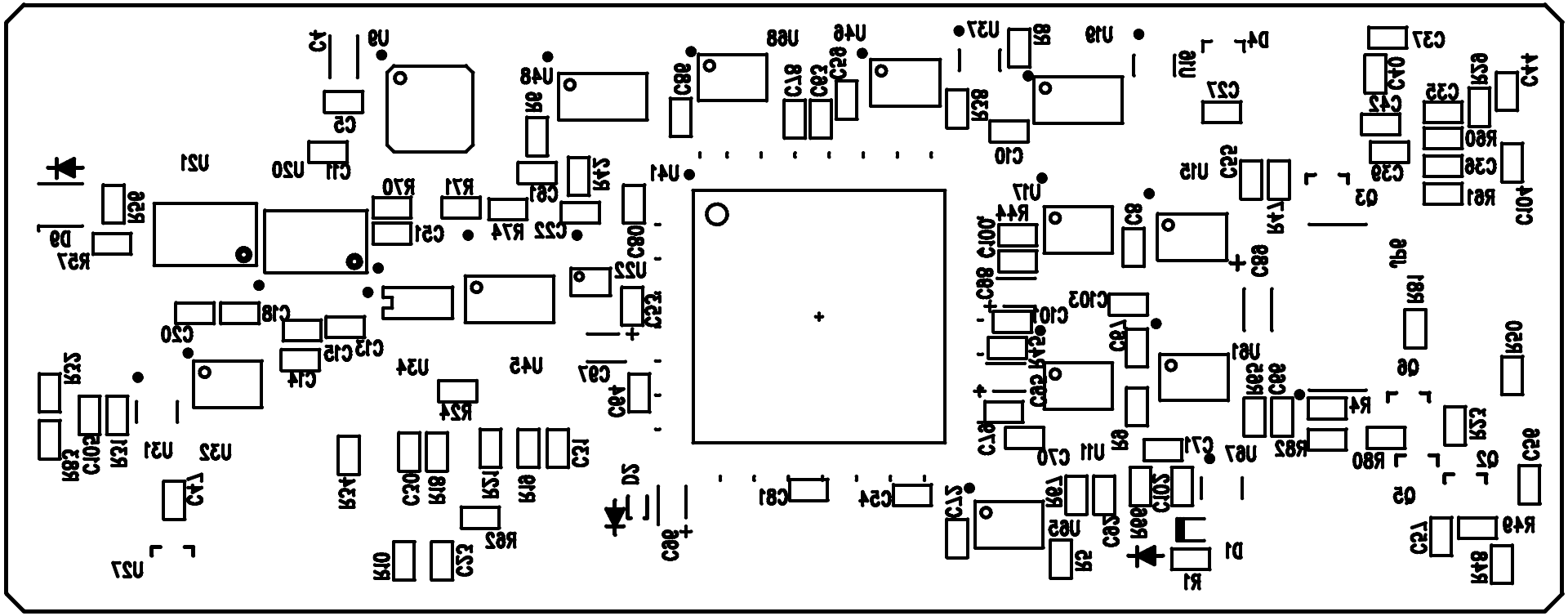
LAYER 7 SPLIT GROUND PLANE (GND/AGND)
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



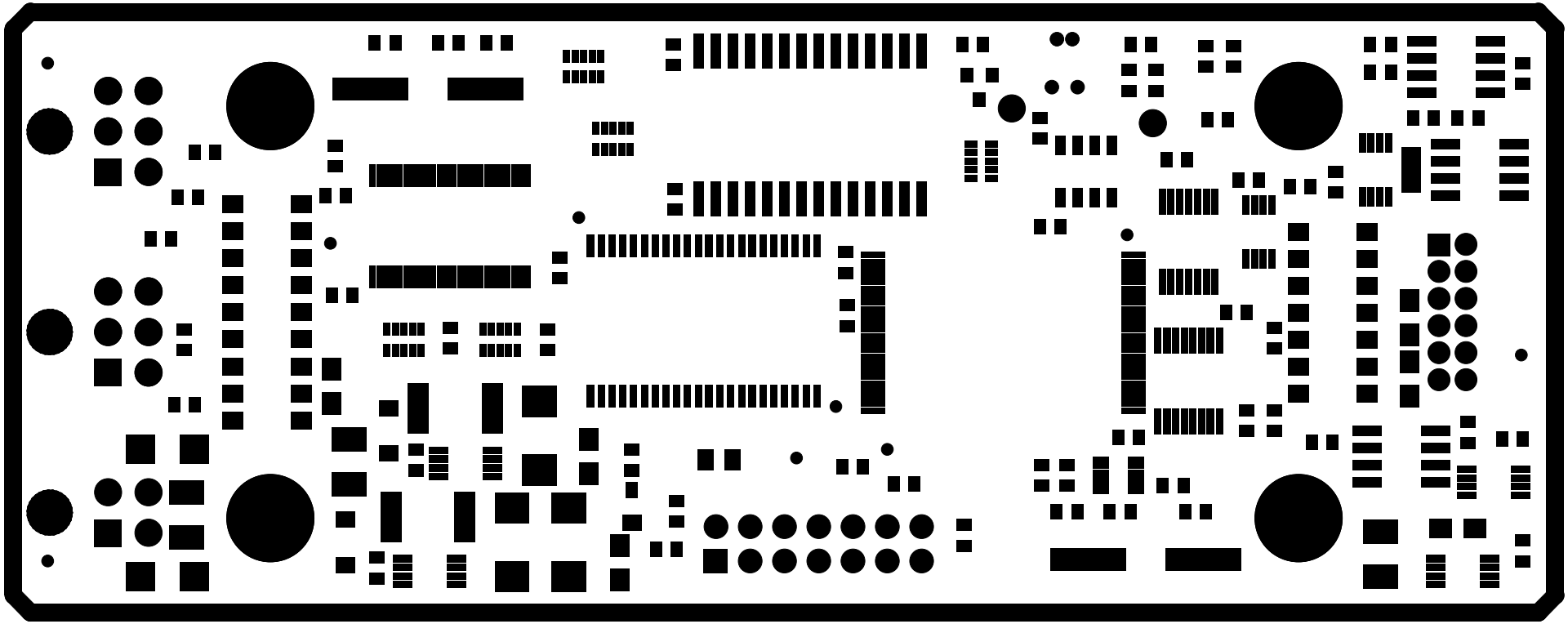
CIRCUIT SIDE LAYER 8
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



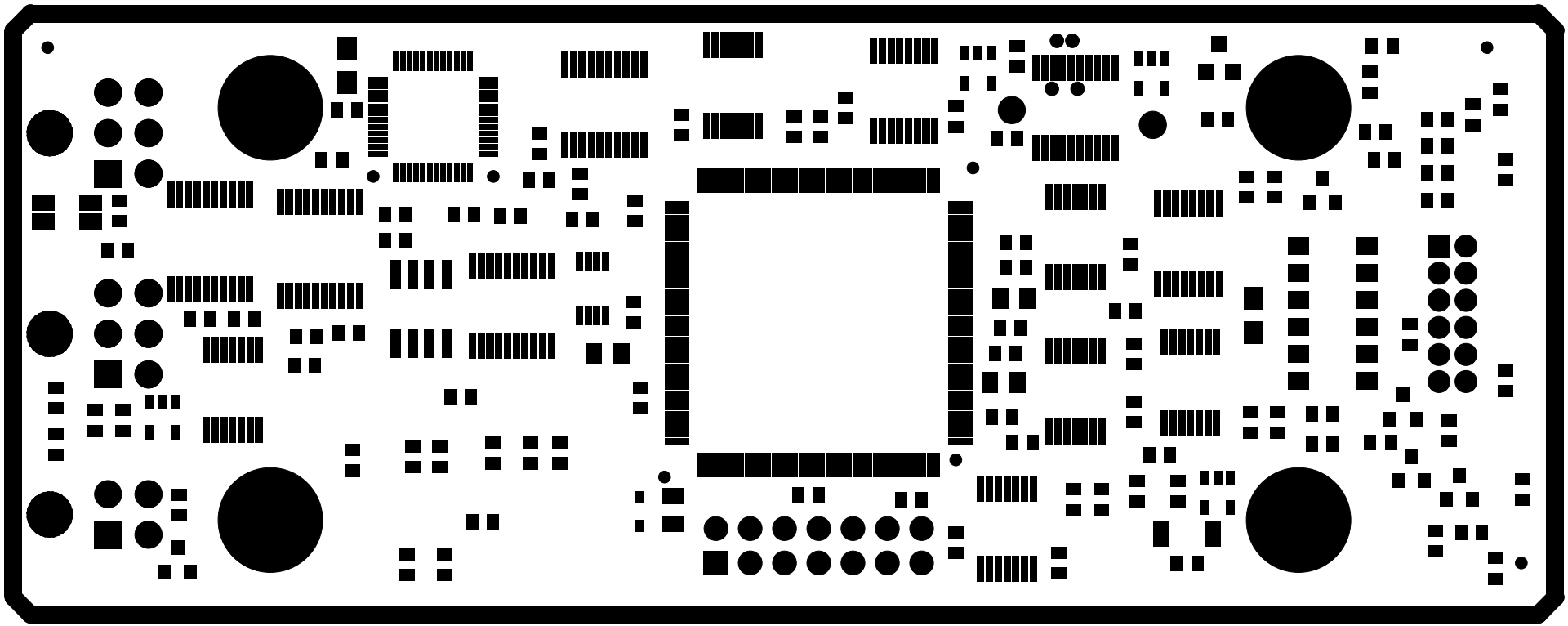
SILKSCREEN LAYER 1
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



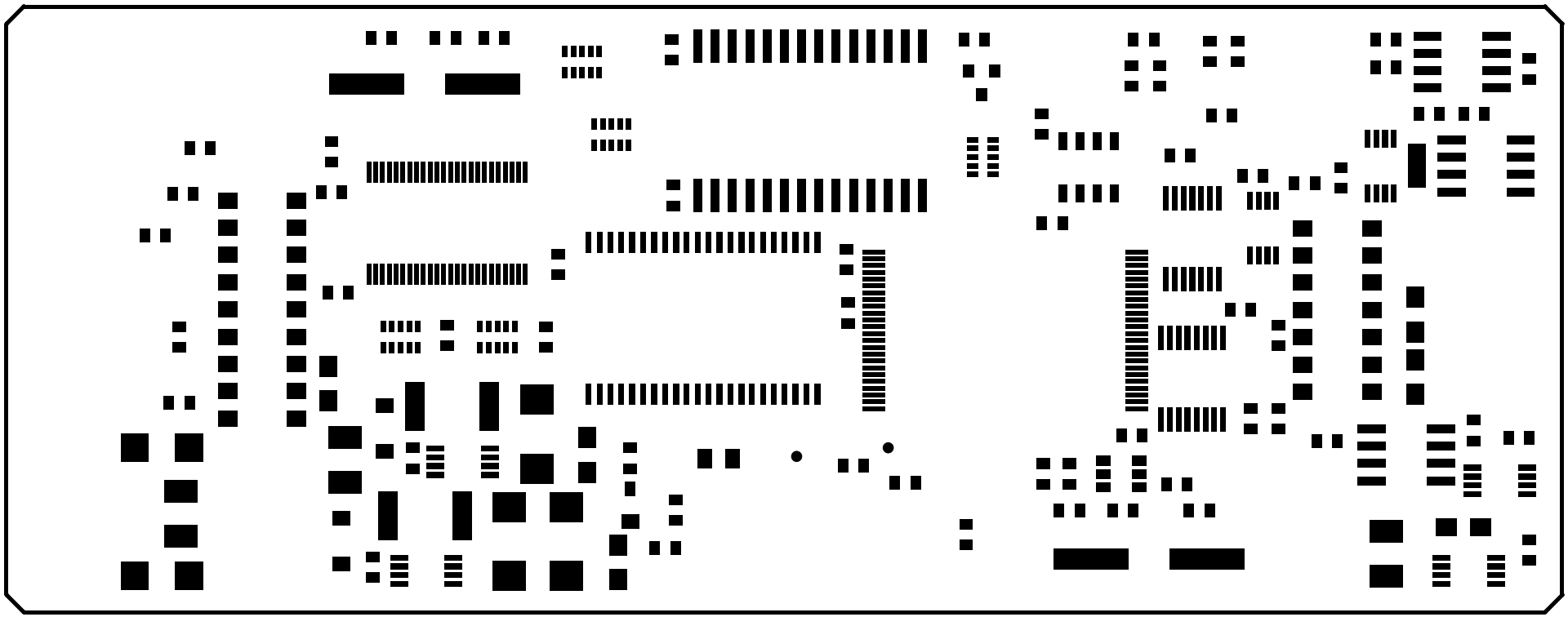
SILKSCREEN LAYER 8
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



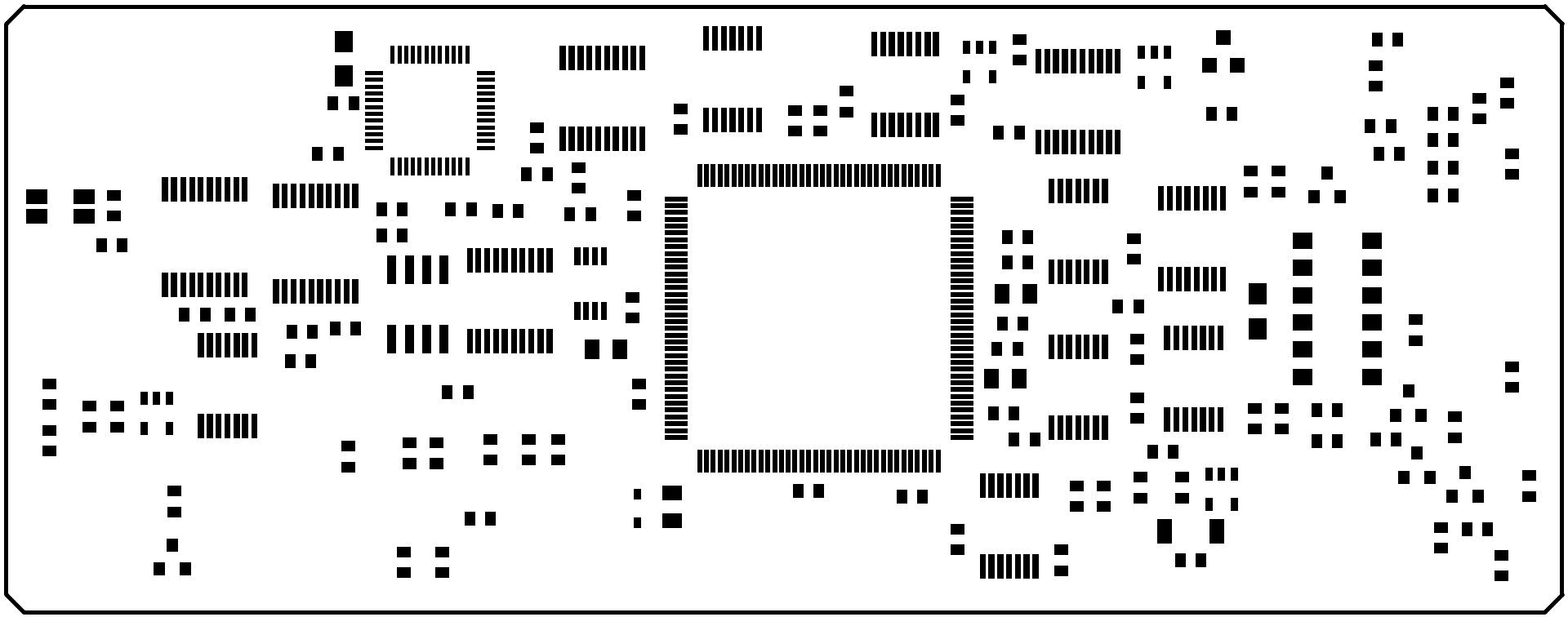
SOLDERMASK LAYER 1
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



SOLDERMASK LAYER 8
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



SOLDER PASTE MASK LAYER 1
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003



SOLDER PASTE MASK LAYER 8 (MUST BE MIRRORED)
WOODS HOLE OCEANOGRAPHIC INST.
uMODEM V1.1B OCT 28 2003