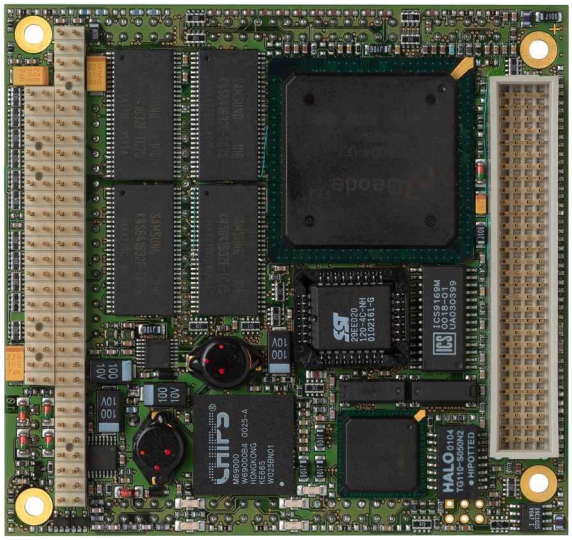
Cool SpaceRunner II

The Single Board Computer For Rugged Applications

Technical Manual



TME-104P-CS2-R1V6.DOC
Version 1.6 / August 02

Hans-Thoma-Str. 11
D-68163 Mannheim

http://www.lippert-at.com

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1 Motherboard functional specifications

The PC/104 "Cool SpaceRunner II" is a CPU-board for rugged applications. The CPU is an x86-compatible 64-bit microprocessor with sixth generation features and is available with speeds up to 300 MHz. The graphic interface fulfills the SVGA standard. It includes 2 Mbytes graphic memory and has a maximum resolution of 1280 x 1024, 16.7 million colors. Additionally the "Cool SpaceRunner II" does have a PanelLink interface. Memory is directly soldered and expandable up to 128 Mbytes. The board conforms to the official PC/104Plus Specification.

1.1 PC/104 "Cool SpaceRunner II" at a glance

CPU:
- National Geode™ MMX™ with I/O Companion CX5530A™

Cache Memory:
- 16 KB unified L1 Write-Back Cache
- No L2 cache subsystem can be installed

Main Memory:
- Supports a 64-bit memory up to 128MB SDRAM.

Extension slots:
- 1x 32-bit PC/104Plus slot
- 1x 16-bit PC/104 slot

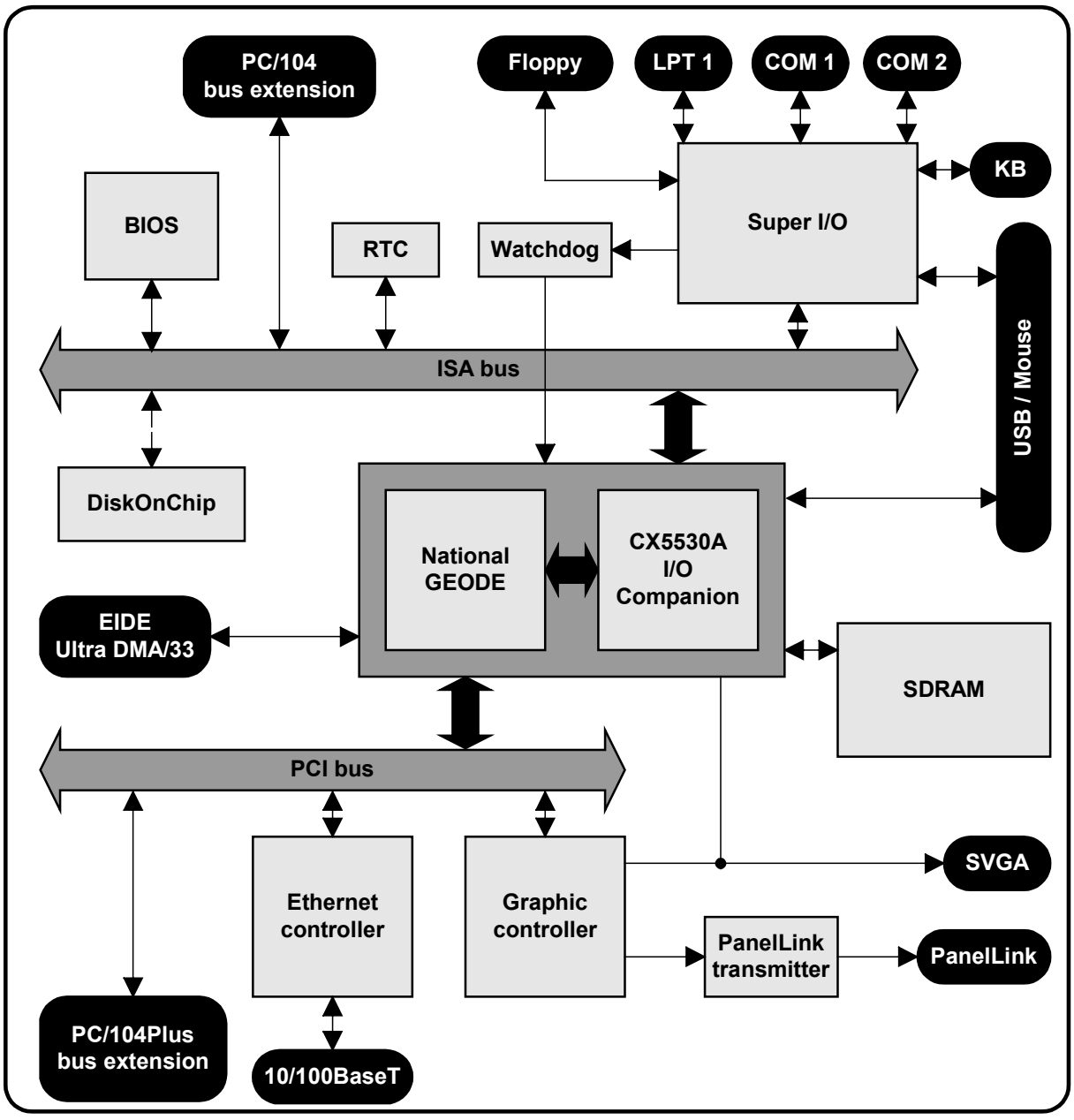
Interfaces:
- Power supply
- PS/2 Keyboard
- PS/2 Mouse
- one parallel port
- two serial ports
- USB
- IrDA
- Ethernet
- Floppy
- EIDE
- SVGA monitor
- PC/104 Bus
- PC/104+ Bus
- PanelLink

Other models are possible on high volumes.

Dimensions:
- 90.2mm x 95.9mm

Mounting:
- 4 mounting holes

1.2 Functional block diagram



1.3 Processor

The National Geode™ MMX™ is an advanced 64-bit x86 compatible processor offering high performance, fully accelerated 2D graphics, a 64-bit synchronous DRAM controller and a PCI bus controller, all on a single chip. In addition, it supports the MMX™ instruction set extension for the acceleration of multimedia applications. The processor is a split rail design with 3.3V I/O and 1,6 to 2.6V Core voltage and is offered in speeds up to 300 MHz. The core has integer and floating point execution units that are based on sixth-generation technology. The integer core contains a single, six-stage execution pipeline and offers advanced features such as operand forwarding, branch target buffers, and extensive write buffering. A 16Kbyte write-back L1 cache is accessed in a unique fashion that eliminates pipeline stalls to fetch operands that hit in the cache.
A tightly coupled synchronous DRAM memory controller supports graphics and system memory accesses. This tightly coupled memory subsystem eliminates the need for an external L2 cache. Software handler routines for XpressGRAPHICS™ and are included in the BIOS and provide compatible VGA.

1.4 I/O Companion

The Cx5530A™ I/O Companion is a PCI-to-ISA bridge (South Bridge), ACPI-compatible chipset that provides AT/ISA functionality. The device also contains state-of-art power management enabling notebook as well as "Deep Green" implementations. The integrated bus master EIDE controller supports two ATA-compatible devices. A Universal Serial Bus (USB) provides high speed, Plug & Play expansion for a variety of new consumer peripheral devices such as digital cameras.

1.5 Integrated Chipset features

- X86 compatibility and support of MMX™ instruction set extension
- fully 2D graphic acceleration
- synchronous memory interface
- PCI bus controller (PCI 2.1 compatible)
- ISA interface
- Ultra DMA/33 (ATA-4) support
- EIDE interface
- USB interface
- AT compatibility
- SMM power management
- full VGA and VESA video

1.6 On Board Power Supply

The on board power supply generates all necessary voltages from the single supply voltage of 5 volts. The generated voltage of 3.3 Volts that is available on the connectors „PC/104+" and „Flat Panel" must not be used to supply external electronic devices with high power consumption like other PC/104 boards or displays.

1.7 PC/104-Plus bus interface

The PC/104-Plus bus is a modification of the standard PCI PC bus. It incorporates all of the PC/104 features, with the added advantage of the high speed PCI bus.

The main features are:

- PC/104 Plus Bus slot fully compatible with PCI version 2.1 specifications.
- Integrated PCI arbitration interface (32 bit wide, 3.3V).
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- 66 MHz PCI clock.

The PC/104 "Cool SpaceRunner II " supports only signal levels at 3.3 Volt. Adapter boards on the PC/104-Plus bus must tolerate this voltage. Signal levels of 5 Volt are not allowed. The internal DC/DC converter does not supply the 3.3 Volt pins on the PC/104-Plus bus!

Because of the complete functionality on board, there are some restrictions for extension boards on the PC/104 Plus bus:

SLOT0: no restrictions are known for this slot.
SLOT1: only extension boards, which will not use busmaster function can operate on this slot number. If an extension board with busmaster function is used on this slot number, the system might hang during boot-time. This restriction is only valid, if the board is shipped with the onboard Ethernet controller (standard configuration).
SLOT2: no restrictions are known for this slot.
SLOT3: this slot is used by the onboard VGA controller and cannot be used for extension boards. This restriction is only valid, if the board is shipped with the onboard VGA controller (standard configuration).

Note: The PC/104 "Cool SpaceRunner II" supports only one busmaster extension board. This can be used only in SLOT0 or SLOT2.

1.8 PC/104 bus interface

The PC/104 bus is a modification of the industry standard (ISA) PC bus specified in IEEE P996. The PC/104 bus has different mechanics than IEEE P966 to allow the stacking of modules. The main features are:

- Supports programmable extra wait state for ISA cycles.
- Supports I/O recovery time for back to back I/O cycles.

The specification for the PC/104 bus and the PC/104-Plus bus are available from the PC/104 Consortium (http://www.PC104.org).

1.9 Super I/O

The onboard Super I/O (SMSC FDC37B78x) provides:

- PC-AT keyboard interface on IDC10 connector
- floppy disk interface on FFC connector
- COM1 and COM2 on IDC10 connectors
- LPT1 on IDC26 connector
- PS/2 mouse interface on IDC10 connector
- General purpose pins are used for the watchdog functions
- Real time clock

To use the watchdog function of the Super I/O it is necessary to program the registers. This can be done through the two I/O addresses 370h and 371h. The index register is located at I/O address 370h and the data register at I/O address 371h. To change the registers or to read them the Super I/O controller has to be in configuration mode. Therefore, the data byte 55h has to be written to the I/O address 370h. After configuration, writing AAh to I/O address 370h leaves the configuration mode. Reading from or writing to a register works as follows:

```
OUT (0x370, 0x55)
OUT (0x370, register-index)
OUT (0x371, register-data)      or      IN (0x371)
OUT (0x370, 0xAA)
```

On request there are the DOS programs **SMCW.EXE** (to write) and **SMCR.EXE** (to read) available. These Programs work as follows:

➔ ***hex-letters ' a ' to ' f ' have to be entered as small letters*** ←

To change a register enter:

```
SMCW <register-index (in hex)> <register-data (in hex)>
example:    SMC e2 0a
```

To read a register enter:

```
SMCR <register-index (in hex)>
example:    SMCR e2
output:     INDEX e2 VALUE a
```

The Super I/O controller is divided in functional groups. Before the value of a register of a functional group can be changed, this group has to be selected. This happens through writing the number of the corresponding functional group in the index-register 07. For example, the registers for the General Purpose Pins of the controller do have the functional group number 8. To select this group the following should be entered:

```
example:    SMCW 07 08
```

1.10 PS/2 keyboard interface

The keyboard interface is located on the IDC10 Header "KEYBOARD". To connect a standard PC-AT keyboard an adapter cable is available for this connector.

1.11 Speaker

The speaker signal is located on the IDC10 Header "KEYBOARD". A standard PC Speaker can be connected between the signal SPEAKER and VCC.

1.12 Reset-In Signal

The RESET-IN signal is located on the IDC10 Header "KEYBOARD". To reset the board the signal RESET-IN must be connected to GND.

1.13 Floppy disk interface

The floppy interface connector is built for slim line floppy disk drives. An adapter to connect a standard floppy drive is available.

1.14 Serial port COM1 and COM2

The serial ports are located on two IDC headers "COM1" and "COM2". Adapter cables with standard DB9 male connectors are available.
The serial ports are programmable in BIOS setup by pressing DEL at boot time. Entering **`Integrated Peripherals`** and then choosing **`Onboard Serial Port 1`** or **`Onboard Serial Port 2`**, configuration of the serial ports is accessible.

Configuring COM1, the following settings are possible :

- Auto
- 3F8 / IRQ4 (base address / interrupt channel)
- 2F8 / IRQ3 (base address / interrupt channel)
- 3E8 / IRQ4 (base address / interrupt channel)
- 2E8 / IRQ3 (base address / interrupt channel)

Configuring COM2, the following settings are possible :

- Disabled
- Auto
- 3F8 / IRQ4 (base address / interrupt channel)
- 2F8 / IRQ3 (base address / interrupt channel)
- 3E8 / IRQ4 (base address / interrupt channel)
- 2E8 / IRQ3 (base address / interrupt channel)

1.15 Parallel Port LPT1

The parallel port is located on an IDC26 header. An adapter cable with a standard DB25 female connector is available.
The parallel port is programmable in BIOS setup by pressing DEL at boot time. Entering **`Integrated Peripherals`** and then choosing **`Onboard Parallel Port`**, configuration of LPT1 is accessible.

Configuring LPT1, the following settings are possible :

- Disabled
- 3BC/IRQ7 (base address / interrupt channel)
- 378/IRQ7 (base address / interrupt channel)
- 278/IRQ5 (base address / interrupt channel)

While not disabled, **`Parallel Port Mode`** can be selected by choosing :

- Normal
- SPP
- EPP 1.7+SPP
- EPP 1.9+SPP
- ECP
- ECP+EPP 1.7
- ECP+EPP 1.9

If **`Parallel Port Mode`** is switched to **`ECP`** or **`ECP+EPP 1.x`**, **`ECP Mode Use DMA`** is accessible. DMA channel 1 or 3 can be selected.

1.16 PS/2 mouse interface

The PS/2 mouse signals MCLK and MDAT are located on the IDC10 header "KEYBOARD". The PS/2 mouse function is programmable in BIOS setup by pressing DEL at boot time. Entering **`BIOS features Setup`** and then choosing **`PS/2 mouse function control`** PS/2 mouse function can be disabled or enabled.

1.17 USB port

USB port is located on the IDC10 header "ETH/USB". To use USB, it has to be enabled in the BIOS. Entering **`Chipset Features Setup`** and then choosing **`USB Controller: Enabled`**.

It is possible to use an USB keyboard under DOS without special driver software. Therefore, USB legacy support has to be enabled in the BIOS. (note: not all keyboard manufacturers are supported)

Entering **`Chipset Features Setup`** and then choosing **`USB Controller: Enabled`** and also **`USB Legacy Support: Enabled.`**

1.18 EIDE port

An EIDE (**E**xtended **I**ntelligent **D**rive **E**lectronics) port is provided by the chipset to connect intelligent drives that integrate the controller (hard disk, CD-ROM etc.). This port supports LBA (Logic Block Addressing) that allows the use of hard disks larger than 512 Mbytes. To enhance the performance, this port supports DMA F type of transfer. The EIDE port is located on a standard 44-pin header (2mm) for 2,5" hard disks. An adapter cable is available to connect standard EIDE devices with a 40 pin IDC header.

1.19 DiskOnChip

The DiskOnChip is a single chip bootable FlashDisk designed to plug into a standard 32-pin DIL socket. It is mapped into an 8 Kbyte window in the upper memory address area of the PC. The address range can be selected in the bios, the DiskOnChip can also be enabled or disabled in the bios.

Entering **`Special Features Setup`** and then choosing **`DiskOnChip: Enabled`**

If enabled the following settings can be made:

`DiskOnChip Base Address: D000H, D400H, D800H, DC00H`

The address range is free for other AT96/ISA96-boards, if the DiskOnChip is not used.

The DiskOnChip contains a built-in copy of the M-Systems industry-standard TrueFFS software, which makes it operate as a standard disk drive. The DiskOnChip can contain the operating system inside to allow systems to boot without a hard disk. It can also be configured as the boot device in systems with a hard disk.

The DiskOnChip is a self-contained device. The installation of the DiskOnChip does not require any software installation. The design of the DiskOnChip allows full upward and downward compatibility. While available today in capacities of 2 to 144Mbytes, future DiskOnChip devices with higher densities will be fully compatible with standard DiskOnChip sockets. The basic design of the DiskOnChip actually supports an unlimited capacity.
If no hard disk is used, the DiskOnChip is automatically registered as drive C. If the DiskOnChip is used in combination with a hard disk, the letter of the drive is depending on the boot options in setup. If in boot options SCSI is selected as first boot device before drive C, the DiskOnChip gets drive letter C and the hard disk gets drive letter D. If in boot options C is selected as first boot device before SCSI, the DiskOnChip gets drive letter D and the hard disk gets drive letter C.

When installing or removing the DiskOnChip, be sure to touch a grounded surface first to discharge any static electricity from your body.

Setting DiskOnChip in its socket

- Align Pin 1 on the DiskOnChip with pin 1 of the socket.
- Carefully push the DiskOnChip into the socket until it is fully seated.
- Check to make sure the DiskOnChip is installed securely and there are no pins bent.

Caution: The DiskOnChip may be permanently damaged if installed incorrectly!

Install the DiskOnChip as drive C:

To install the DiskOnChip as drive C:\ on a system without hard disk, set the CMOS setup of drive C:\ to 'not installed' (indicating that no physical magnetic disk is installed) and reboot the computer. The DiskOnChip will install as drive C:\. The DiskOnChip needs to be formatted with the system files to make it bootable drive. See 'Configure the DiskOnChip as the BOOT device' below.

Install the DiskOnChip as drive D:

To install the DiskOnChip as drive D:\ on a system with a hard disk, just reboot the system and the DiskOnChip will install as drive D:\.

Configure the DiskOnChip as Boot device

In order to configure the DiskOnChip as the boot device, the operating system files need to be copied into it. Copying the operating system files into DiskOnChip should be done as if it is done to a hard disk. The following is an example of a typical initialization process:

- Set the DiskOnChip as a regular drive in your system (not a boot drive)
- Install a bootable floppy disk in drive A:\ and boot the system
- At the DOS prompt type SYS C:\ to transfer the DOS system files to the DiskOnChip (assuming the DiskOnChip is installed as drive C:\)
- Copy any files needed to the DiskOnChip
- Remove the floppy disk and reboot the system. The system will boot from DiskOnChip and will allow you to run and access any files that have been copied to DiskOnChip.

1.20 CRT / LCD Graphic-Controller

The graphic-controller CT69000 from Chips & Technologies combines state-of-art flat panel controller capabilities with low power, high performance integrated memory. It incorporates 2Mbytes of proprietary integrated SDRAM for the graphics/video frame buffer. The integrated SDRAM memory can support up to 83MHz operation, thus increasing the available memory bandwidth for the graphics subsystem. The result is support for additional high color / high-resolution graphics modes combined with real-time video acceleration. This additional bandwidth also allows more flexibility in the other graphics functions intensely used in Graphical User Interfaces (GUIs) such as Microsoft™ Windows™.
The CT69000 supports a wide variety of monochrome and color **S**ingle-Panel, **S**ingle-Drive (SS) and **D**ual-Panel, **D**ual-Drive (DD), standard and high resolution, passive STN and active matrix TFT/MIM LCD and EL panels. Up to 256 gray scales are supported on passive STN LCD's. Up to 16.7M different colors can be displayed on passive STN LCDs and up to 16.7M colors on 24-bit active matrix LCDs.

Vertical centering and stretching are provided for handling modes with less than 480 lines on 480-line panels. Horizontal and vertical stretching capabilities are also available for both text and graphics modes for optimal display of VGA text and graphics modes on 800x600, 1024x768 and 1280x1024 panels.
The CT69000 uses independent multimedia capture and display systems on-chip. The capture system places data in display memory and the display system places the data in a window on the screen.
The capture system can receive data from the system bus (PCI) in either RGB or YUV format. The input data can also be scaled down before storage in display memory. Capture of input data may also be double buffered for smoothing and to prevent image tearing. To better support MPEG2 (DVD) video decompression, the CT69000 includes a line buffer to directly support the native format of MPEG2 data of 720 pixels wide. The capture engine also supports image mirroring and rotation for camera support. This feature is important for applications such as video teleconferencing because it allows the image movements to appear on the display as it actually occurs. The image and movement is not a mirror image of what is actually taking place.
The display system can independently place either RGB or YUV data from anywhere in display memory into an on-screen window which can be any size and located at any pixel boundary (YUV is converted to RGB "on-the-fly" on output).
Non-rectangular windows are supported via color keying. The data can be fractionally zoomed on output up to 8x to fit the on-screen window and can be horizontally and vertically interpolated. Interlaced and non-interlaced data are both supported in the capture and display systems.
The internal logic of the CT69000 is optimized for 3.3V operation, bus and panel interfaces at 3.3V but can tolerate 5V operation.
The CT69000 graphics engine is designed to support high performance graphics and video acceleration for all supported display resolutions, display types and color modes. There is no compromise in performance operating in 8, 16 or 24 bpp color modes allowing true acceleration while displaying up to 16.7M colors.

Supported Display Modes

The following display modes are supported:

Resolution	Color (bpp)	Refresh Rates (Hz)
640x480	8	60, 75, 85
640x480	16	60, 75, 85
640x480	24	60, 75, 85
800x600	8	60, 75, 85
800x600	16	60, 75, 85
800x600	24	60, 75, 85
1024x768	8	60, 75, 85
1024x768	16	60, 75, 85
1280x1024	8	60

The CT69000 supports CRT and most kind of Displays like, STN DSTN, EL and TFT. The CT69000 can boot on CRT, LCD or simultaneous. Up to 16 different displays are supported in the VGA BIOS. This functions can be programmed in BIOS setup by pressing DEL at boot time. Entering **`Special Features Setup`** and then choosing:

`CT69000 Display Device: CRT, LCD` or **`simultaneous`**

The following panels are supported in the standard BIOS:

LCD Panel	Resolution	Type	Manufacturer	Part no.
#01	RESERVED			
#02	RESERVED			
#03	RESERVED			
#04	RESERVED			
#05	640 x 480	TFT Color	Sharp	LQ084V1DG21
#06	640 x 480	TFT Color	NEC	NL6448AC33-24
#07	1024 x 768	TFT Color	Sharp	LQ12X12
#08	800 x 600	TFT Color	Sharp	LQ121S1DG21
#09	RESERVED			
#10	RESERVED			
#11	RESERVED			
#12	RESERVED			
#13	RESERVED			
#14	RESERVED			
#15	RESERVED			
#16	RESERVED			

Note: The above table depends on the used VGA BIOS and may be changed for product improvement. The actual supported displays can be seen in the BIOS menu.

1.21 PanelLink

In addition to the standard display connection there is the opportunity to connect several display types through PanelLink. Displays can be used up to 15 meters away from the board. The range goes from VGA to High Refresh XGA (25-86MHz). The used PanelLink digital transmitter Sil 160A supports up to true color panels (24 bit/pixel, 16.7M colors) in one pixel clock mode and also features an inter-pair skew tolerance up to one full input clock cycle and a highly jitter tolerant PLL design. The signals are located on a 12 pin double row IDC header (2,54 mm).

1.22 Ethernet-Controller

The Ethernet-controller 82559ER from Intel is a fully integrated 10/100Base-TX LAN solution and consists of both the Media Access Controller (MAC) and the physical layer (PHY) interface combined into a single component solution.
The 32-bit PCI controller provides enhanced scatter-gather bus mastering capabilities and enables the 82559ER to perform high-speed data transfers over the PCI bus. Its bus master capabilities enable the component to process high level commands and perform multiple operations, which lowers CPU utilization by off-loading communication tasks from the CPU. Two large transmit and receive FIFO´s of 3 Kbytes each help prevent data underruns and overruns while waiting for bus accesses. This enables the 82559ER to transmit data with minimum interframe spacing (IFS).
The 82559ER can operate in either full duplex or half duplex mode. In full duplex mode the 82559 adheres with the IEEE 802.3x Flow Control specification. Half duplex performance is enhanced by a proprietary collision reduction mechanism.
The CSMA/CD unit of the 82559ER allows it to be connected to either a 10 or 100 Mbps Ethernet network. The CSMA/CD unit performs all of the functions of the 802.3 protocol such as frame formatting, frame stripping, collision handling, deferral to link traffic, etc. The CSMA/CD unit can also be placed in a full duplex mode, which allows simultaneous transmission and reception of frames.
The PHY unit of the 82559ER supports Auto-Negotiation for 10BaseT-/100BaseTX Half Duplex and 10BaseT-/100BaseTX Full Duplex.

The signals of the Ethernet interface are located on the IDC10 header "ETH/USB".

1.23 Watchdog

The board has two different independent watchdog systems, which are programmed through the Super I/O.

1.23.1 Short-time watchdog timer

A short-time watchdog is realized with a Maxim 691 Reset/Watchdog circuit. The trigger time of this watchdog is 400ms and accessible by the Super I/O controller through the functional group 8. To activate the short-time watchdog the contents of the register '0xE2' has to be set to '00'. To trigger this watchdog the contents of the register '0xE3' has to be changed within 400ms from '00' to '02' or vice versa. If there is no change of the register within 400ms, the watchdog releases and generates a full hardware reset.

program example:

```
SMCW 07 08    Activation of short time watchdog.
SMCW E2 00

SMCW E3 00    Triggering of the short time watchdog.
SMCW E3 02
SMCW E3 00
…
…
SMCW E3 00
SMCW E3 02
…
```

The status of the watchdog can be read through the register F6, Bit1 (Bit0 and Bit2-Bit7 are don´ t care) of the Super I/O. A low level at this pin indicates that a watchdog time-out has occurred.

1.23.2 Long-time watchdog timer

A long-time watchdog timer is implemented in the Super I/O. The watchdog time-out status bit may be mapped to an interrupt. It can also brought out as a hardware reset signal. Both options have to be programmed to the corresponding configuration registers of the Super I/O.

This watchdog timer has a time-out ranging from either 1 to 255 minutes with one-minute resolution or 1 to 255 seconds with one-second resolution. As soon as the watchdog timer is activated, it starts counting down from the value loaded. When the count value reaches zero the counter stops and sets the watchdog time-out status bit. Regardless of the current state of the watchdog timer, the time-out status bit can be directly set or cleared by the host CPU.
Three system events can reset the watchdog timer. These are a keyboard interrupt, a mouse interrupt or I/O reads/writes to address 0x201. The effect on the watchdog timer for each of these system events may be individually enabled or disabled. When a system event is enabled, the occurrence of this event will cause the watchdog timer to reload the stored value and reset the watchdog timer time-out status bit if set. If all three system events are disabled the watchdog timer will inevitably time out.
The watchdog timer may be configured to generate an interrupt on the rising edge of the time-out status bit. The watchdog timer interrupt is mapped to an interrupt channel through a configuration register. When mapped to an interrupt the interrupt request pin reflects the value of the watchdog timer time-out status bit.
The used registers of the Super-I/O are shown in the following table:

index-register	Data	action	program
0x07	0x08	select functional group 08	SMCW 07 08
0xf1 (default = 00)	0x00	timer unit in minutes	SMCW f1 00
0xf1	0x80	timer unit in seconds	SMCW f1 80
0xf2 (default = 00)	0x00	time-out disabled	SMCW f2 00
0xf2	0x01	time-out = 1 min/sec	SMCW f2 01
…	…	…	…
0xf2	0xff	time-out = 255 min/sec	SMCW f2 ff
0xf3 (default = 00)	Bit [0] = 0	WDT is not affected upon I/O read/write of I/O port 0x201	SMCW f3 x0
0xf3	Bit [0] = 1	WDT is reset upon I/O read/write of I/O port 0x201	SMCW f3 x1
0xf3	Bit [1] = 0	WDT is not affected by keyboard interrupts	SMCW f3 x0
0xf3	Bit [1] = 1	WDT is reset upon a keyboard interrupt	SMCW f3 x2
0xf3	Bit [2] = 0	WDT is not affected by mouse interrupts	SMCW f3 x0
0xf3	Bit [2] = 1	WDT is reset upon a mouse interrupt	SMCW f3 x4
0xf3	bit [3] = reserved	----------	----------
0xf3	bit [7..4] = 0	WDT interrupt mapping disable	SMCW f3 0x
0xf3	bit [7..4] = 1	WDT interrupt mapping to IRQ 1	SMCW f3 1x
0xf3	bit [7..4] = 2	Invalid	----------
0xf3	bit [7..4] = 3	WDT interrupt mapping to IRQ 3	SMCW f3 3x
0xf3	bit [7..4] = 4	WDT interrupt mapping to IRQ 4	SMCW f3 4x
…	…	…	…
0xf3	bit [7..4] = f	WDT interrupt mapping to IRQ 15	SMCW f3 fx
0xf4 (default = 00)	Bit [0] = 0	WD timer counting	SMCR/W f3 x0
0xf4	bit [0] = 1	WD timer occurred	SMCR/W f3 x1
0xf4	bit [2] = 1	forces time-out event (self-clearing)	SMCR/W f3 x4
0xf4	bit [1] , [7..3] = 0	Reserved	----------
0xe2	0x8a	hardware reset upon WDT time-out	SMCW e2 8a
0xf6	bit [1] = 0 bit [0] , [7..2] = don´ t care	WDT has generated a reset	SMCR f6

Program example:

```
SMCW 07 08      (select functional group)
SMCW f1 80      (timer unit in seconds)
SMCW f2 1e      (time-out in 30 timer units)
SMCW f3 02      (WDT reset upon keyboard interrupt)
SMCW e2 8a      (hardware reset upon WDT time-out)
```

The status if the watchdog has generated a reset can be read through the register F6, Bit1 (Bit0 and Bit2-Bit7 are don´ t care) of the Super I/O. A low level at this pin indicates that a watchdog time-out has occurred and the watchdog has generated a reset.

2 Hardware installation

The PC/104 "Cool SpaceRunner II" is delivered with a correct jumper setting for proper operation. The default jumper settings must not be changed by the customer. Improper jumper settings will cause system instability or system hang-ups.

Attention!

The board must not be connected or disconnected to PC/104 bus, PC/104Plus bus or peripherals (e.g. HDD, FDD, etc.) with power supply switched ON!

2.1 Adapter cable set

With the optional available cable set, standard PC devices can be easily connected to the board. The adapter cable set consists of the following items:

- adapter cable 3.5'' power supply connector female to 5.25'' power supply connector male for supplying the board with a standard PC power supply
- two adapter cables IDC10 female to DB9 male for serial port 1 and 2
- adapter cable IDC26 female to DB25 female for parallel port
- adapter cable IDC10 female to SUB-D HD15 female adapter for standard VGA monitor.
- adapter cable IDC44 / 2mm female to IDC44 / 2mm female to connect 2.5'' EIDE hard disks
- adapter cable IDC44 / 2mm female to IDC40 / 2,54mm female to connect 3,5'' EIDE hard disks
- flat foil cable 26p. plus PCB adapter to 34p. female 2 row 2.54mm grid (standard FDD connector)

The flat foil cable must be inserted in the FFC connector with the blank side on the top. Be careful not to damage the little safety lever at the floppy connector.

2.2 BIOS

The PC/104Plus "Cool SpaceRunner II" is delivered with a standard PC BIOS. By default, all setup settings are done to have a "ready to run" system, even without a BIOS setup backup battery. If the user wants to change some settings , the setup can be accessed by pressing the <DEL> key on power up. The BIOS is located in a flash prom and can be easily updated on board with software under DOS.

All changes in the setup of the BIOS are stored in the CMOS RAM of the real time clock. A copy of the CMOS RAM excluding date and time data is stored in the flash ROM. This means that even if the backup battery runs out of power, the CMOS settings are not lost. Only date and time will be set to a default value. For the power supply of the RTC the "Cool SpaceRunner II" has a 47mF GoldCap capacitor. This capacitor supplies the RTC for approximately 7 days with the necessary power. Additional connections, to connect an external battery, are located at the IDC10 header "KEYBOARD". To store the board the battery should be disconnected.

The default values of the BIOS can be automatically loaded at boot time. Therefore the key “ 0 / INSERT ” on the num pad has to be pressed before the system is turned on. While pressing this key and turning the system on, the default values will be loaded.

2.3 Software installation

For the PC/104Plus “Cool SpaceRunner II” are software drivers for Ethernet and graphic available. These drivers are delivered on request. For installation, follow the instructions on the driver disks.

3 Connectors

Connector position refer to chapter 5.2 Mechanical specifications

3.1 Power connector pin definition

Connector type: 3.5” FDD Power connector

signal name	pin	signal name	pin
+5 Volt	1	GND	2
GND	3	+ 12 Volt	4

3.2 COM1 port connector pin definition

Connector type: IDC10 pin header 2.54 mm

signal name	pin	signal name	pin
DCD	1	DSR	2
RXD	3	RTS	4
TXD	5	CTS	6
DTR	7	RI	8
GND	9	+5 Volt	10

3.3 COM2 port connector pin definition

Connector type: IDC10 pin header 2.54 mm

signal name	pin	Signal name	pin
DCD	1	DSR	2
RXD	3	RTS	4
TXD	5	CTS	6
DTR	7	RI	8
GND	9	+5 Volt	10

3.4 LPT 1 port connector pin definition

Connector type: IDC26 pin header 2.54 mm

signal name	pin	signal name	pin
Strobe	1	Auto LF	2
Data0	3	Error	4
Data1	5	Init	6
Data2	7	Select In	8
Data3	9	GND	10
Data4	11	GND	12
Data5	13	GND	14
Data6	15	GND	16
Data7	17	GND	18
ACK	19	GND	20
Busy	21	GND	22
Paper End	23	GND	24
Select	25	n.c.	26

3.5 Keyboard connector pin definition

Connector type: IDC10 pin header 2.54 mm

signal name	pin	Signal name	pin
Speaker	1	Mouse Clock	2
Reset-In (Power-Good)	3	Mouse Data	4
KB Data	5	KB Clock	6
GND	7	+5 Volt	8
Ext. Battery	9	Reset-In (Power-Good)	10

3.6 VGA connector pin definition

Connector type: IDC12 pin header 2.54 mm

signal name	pin	Signal name	pin
Red	1	GND	2
Green	3	GND	4
Blue	5	GND	6
HSYNC	7	GND	8
VSYNC	9	GND	10
GND	11	GND	12

3.7 10/100BaseT connector pin definition

Connector type: IDC10 pin header 2.54 mm

signal name	pin	signal name	pin
TX+	1	TX-	2
RX+	3	PE	4
PE	5	RX-	6
USB+	7	USB-	8
VCC	9	GND	10

3.8 EIDE connector pin definition

Connector type: IDC44 pin header 2.00 mm

signal name	pin	signal name	pin
/Reset	1	GND	2
Data7	3	Data8	4
Data6	5	Data9	6
Data5	7	Data10	8
Data4	9	Data11	10
Data3	11	Data12	12
Data2	13	Data13	14
Data1	15	Data14	16
Data0	17	Data15	18
GND	19	n.c.	20
DRQ0	21	GND	22
Write	23	GND	24
Read	25	GND	26
Ready	27	GND	28
DACK0	29	GND	30
IRQ	31	/CS16	32
Address1	33	GND	34
Address0	35	Address2	36
CS1	37	CS3	38
LED	39	GND	40
+5 Volt	41	+5 Volt	42
GND	43	n.c.	44

3.9 Floppy connector pin definition

Connector type: FFC 26 pin 1.00 mm

signal name	pin	signal name	pin
+5 Volt	1	Index	2
+5 Volt	3	Drive Select 0	4
+5 Volt	5	Disk change	6
n.c.	7	n.c.	8
n.c.	9	Motor On 0	10
n.c.	11	Direction	12
n.c.	13	Step	14
GND	15	Write Data	16
GND	17	Write Gate	18
GND	19	Track 0	20
GND	21	Write Protect	22
GND	23	Read Data	24
GND	25	Head Select	26

3.10 PanelLink connector pin definition

Connector type: IDC 12-pin header 2.54 mm

Signal name	pin	signal name	pin
+5 Volt	1	TX1+	2
TX1-	3	GND	4
TX0+	5	TX0-	6
GND	7	TX2+	8
TX2-	9	GND	10
TXC+	11	TXC-	12

3.11 PC/104-Plus bus pin definition

pin	A	B	C	D
1	GND	Reserved	+5 Volt	AD00
2	VI/O	AD02	AD01	+5 Volt
3	AD05	GND	AD04	AD03
4	C/BE0	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	+3.3 Volt	C/BE1	AD15	+3.3 Volt
9	SERR	GND	SB0	PAR
10	GND	PERR	+3.3 Volt	SDONE
11	STOP	+3.3 Volt	LOCK	GND
12	+3.3 Volt	TRDY	GND	DEVSEL
13	FRAME	GND	IRDY	+3.3 Volt
14	GND	AD16	+3.3 Volt	C/BE2
15	AD18	+3.3 Volt	AD17	GND
16	AD21	AD20	GND	AD19
17	+3.3 Volt	AD23	AD22	+3.3 Volt
18	IDSEL0	GND	IDSEL	IDSEL2
19	AD24	C/BE3	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5 Volt	AD28	AD27
22	+5 Volt	AD30	GND	AD31
23	REQ0	GND	REQ1	VI/O
24	GND	REQ2	+5 Volt	GNT0
25	GNT1	VI/O	GNT2	GND
26	+5 Volt	CLK0	GND	CKL1
27	CLK2	+5 Volt	CLK3	GND
28	GND	INTD	+5 Volt	RST
29	+12 Volt	INTA	INTB	INTC
30	-12 Volt	Reserved	Reserved	GND

All VIO pins are connected to 3.3 Volt by default.
-12 Volt is not supported on this board.

3.12 PC/104 bus pin definition

pin	D	C
0	GND	GND
1	MEMCS16	SBHE
2	IOCS16	LA23
3	IRQ10	LA22
4	IRQ11	LA21
5	IRQ12	LA20
6	IRQ13	LA19
7	IRQ14	LA18
8	DACK0	LA17
9	DRQ0	MEMR
10	DACK5	MEMW
11	DRQ5	SD8
12	DACK6	SD9
13	DRQ6	SD10
14	DACK7	SD11
15	DRQ7	SD12
16	+5 Volt	SD13
17	MASTER	SD14
18	GND	SD15
19	GND	GND

pin	A	B
1	IOCHCK	GND
2	D7	RSTDRV
3	D6	+5 Volt
4	D5	IRQ9
5	D4	-5 Volt
6	D3	DRQ2
7	D2	-12 Volt
8	D1	ENDXFR
9	D0	+12 Volt
10	IOCHRDY	GND / KEY
11	AEN	SMEMW
12	A19	SMEMR
13	A18	IOW
14	A17	IOR
15	A16	DACK3
16	A15	DRQ3
17	A14	DACK1
18	A13	DRQ1
19	A12	REFRESH
20	A11	SYSCLK
21	A10	IRQ7
22	A9	IRQ6
23	A8	IRQ5
24	A7	IRQ4
25	A6	IRQ3
26	A5	DACK2
27	A4	TC
28	A3	BALE
29	A2	+5 Volt
30	A1	OSC
31	A0	GND
32	GND	GND

-5 Volt and –12 Volt are not supported on this board.

4 Motherboard software specifications

4.1 System address map

This section describes the mapping of the CPU memory and I/O address spaces. Also covered in this section are the PCI configuration space mapping.

Memory address map

Address Range (Dec)	Address Range (Hex)	Size	Description
1024K – XXXXXK	100000 - XXXXXX	31K – 127K	Extended Memory
960K – 1024K	0F0000 – 0FFFFF	64K	System Bios
800K – 960K	0C7C00 – 0EFFFF	160K	unused
768K – 800K	0C0000 – 0C7BFF	32K	Graphic Bios
704K – 768K	0B0000 – 0BFFFF	64K	Text Memory
640K – 704K	0A0000 – 0AFFFF	64K	Graphic Memory
0K – 640K	0 – 9FFFF	640K	Conventional Memory

I/O address map

The system chip set implements a number of registers in I/O address space. These registers occupy the following map in the I/O space (depending on enabled or disabled functions in the BIOS other or more resources may be used)

.

Address Range (Hex)	Size (Hex)	Description
0000-000F	16 Bytes	DMA Controller 1 (8237)
0020-0021	2 Bytes	Interrupt Controller 1 (8259)
0022-0023	2 Bytes	ST486 Specific Registers
0040-0043	4 Bytes	Timer Controller (8254)
0060	1 Bytes	Keyboard Controller Data Byte
0061	1 Byte	NMI, Speaker Control
0064	1 Byte	Kbd Ctlr, CMD,STAT Byte
0070, bit 7	1 bit	Enable
0070, bit6:0	7 bits	Real Time Clock Address
0078	1 Byte	internal
0079	1 Byte	Watchdog
0080-008F	16 Bytes	DMA Page Registers
00A0-00A1	2 Bytes	Interrupt Controller 2 (8259)
00C0-00DE	31 Bytes	DMA Controller 1 (8237)
00F0	1 Byte	Reset Numeric Error
0102	1 Byte	VGA Setup Register
0170-0177	8 Bytes	Secondary IDE Channel
01F0-01F7	8 Bytes	Primary IDE Channel
0201	1 Byte	Super I/O
0278-027B	4 Bytes	Parallel Port 2 (Bidir)
02F8-02FF	8 Bytes	Serial Port 2
0378-037F	8 Bytes	Parallel Port 1
03B4, 03B5, 03BA	3 bytes	VGA Registers
03D4, 03D5, 03DA	3 Bytes	VGA Registers
03C0-03CF	16 Bytes	VGA Registers
03F0-03F5	6 Bytes	Floppy Controller Registers
03F6	1 Byte	IDE Command Port
03F7 (Write)	1 Byte	Floppy Command Port
03F7, bit 7	1 bit	Floppy Disk Change
03F7, bits 6:0	7 bits	IDE Status Port
03F8-03FF	8 Bytes	Serial Port 2
0CF8	1 Byte	PCI Configuration Address Register
0CFC-0CFF	8 Bytes	PCI Configuration Data Registers
046E8	1 Byte	VGA Add-in mode enable Register
C000-C0FF	256 Bytes	PCI Configuration Registers

4.2 Interrupts and DMA channels

Interrupts

IRQ	System Resource
NMI	Parity Error
0	Timer
1	Keyboard
2	Interrupt Controller 2
3	Serial Port 2
4	Serial Port 1
5	User available (PC/104 or -Plus)
6	Floppy
7	Parallel Port 1
8	Real Time Clock
9	User available (PC/104 or -Plus)
10	User available (PC/104 or -Plus)
11	Ethernet Controller
12	PS/2 Mouse
13	Math coprocessor
14	EIDE
15	EIDE, if the Secondary IDE controller is disabled in BIOS setup, IRQ15 can be used on the PC/104 or -Plus bus.

DMA channels

DMA	data width	System Resource
0	8 bits	User available
1	8 bits	User available
2	8 bits	Floppy
3	8 bits	Parallel Port
4		Reserved, Cascade Channel
5	16 bits	User Available
6	16 bits	User Available
7	16 bits	User Available

Note :Depending on enabled or disabled functions in the BIOS other or more resources may be used

5 Technical characteristics

5.1 Electrical specifications

Supply voltage: +5 Volt

Supply voltage ripple: +/- 5 %

Supply current: depending on CPU frequency
approx. 0.8 A at 200 MHz (CPU GX1 1,8V)
approx. 1.1 at 300 MHz (CPU GX1 2,0V)

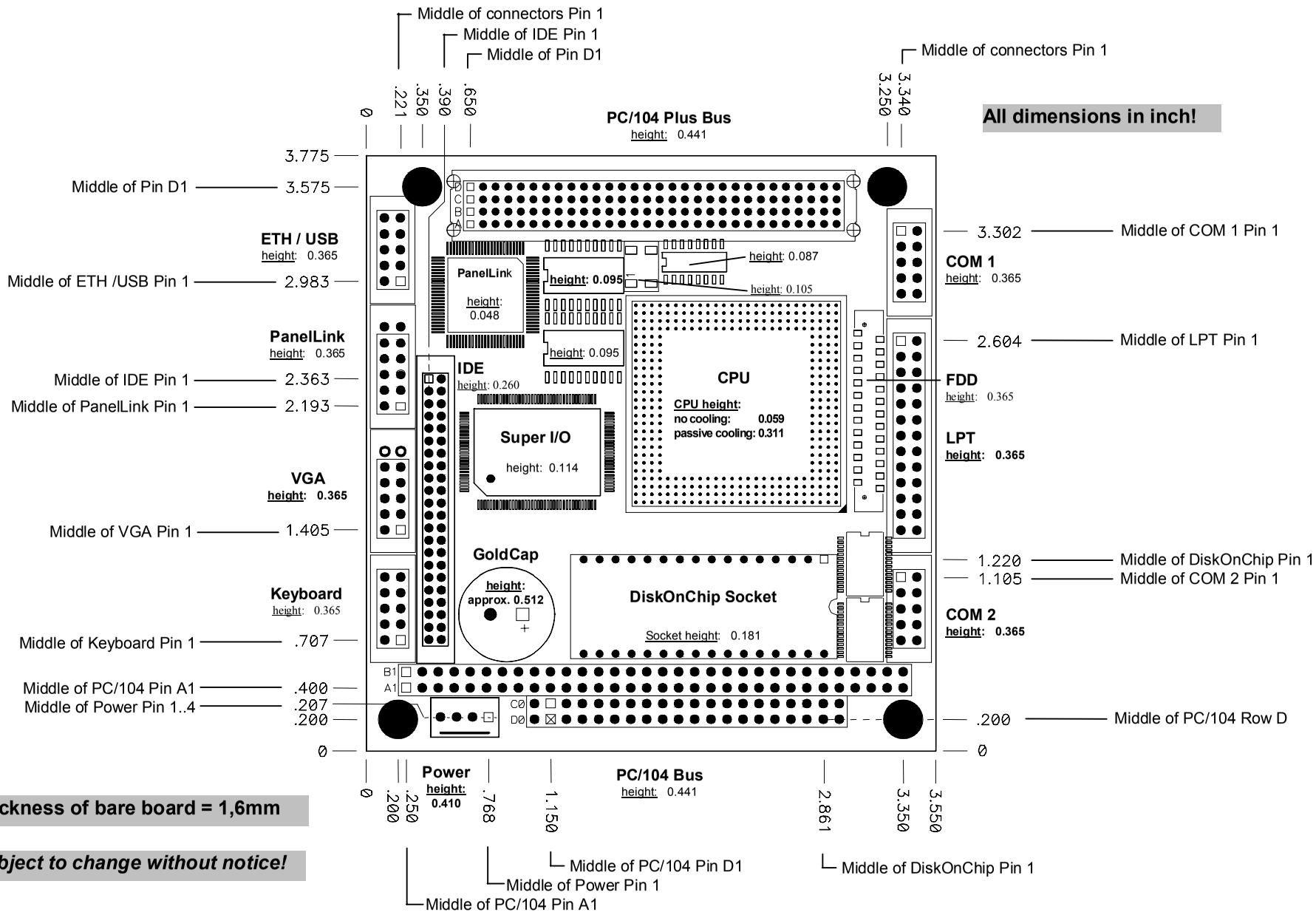
5.2 Mechanical specification

Dimensions (LxW) : 90.2mm x 95.9mm

Height : 15mm

Weight : 115g (including DiskOnChip 48Mbyte)

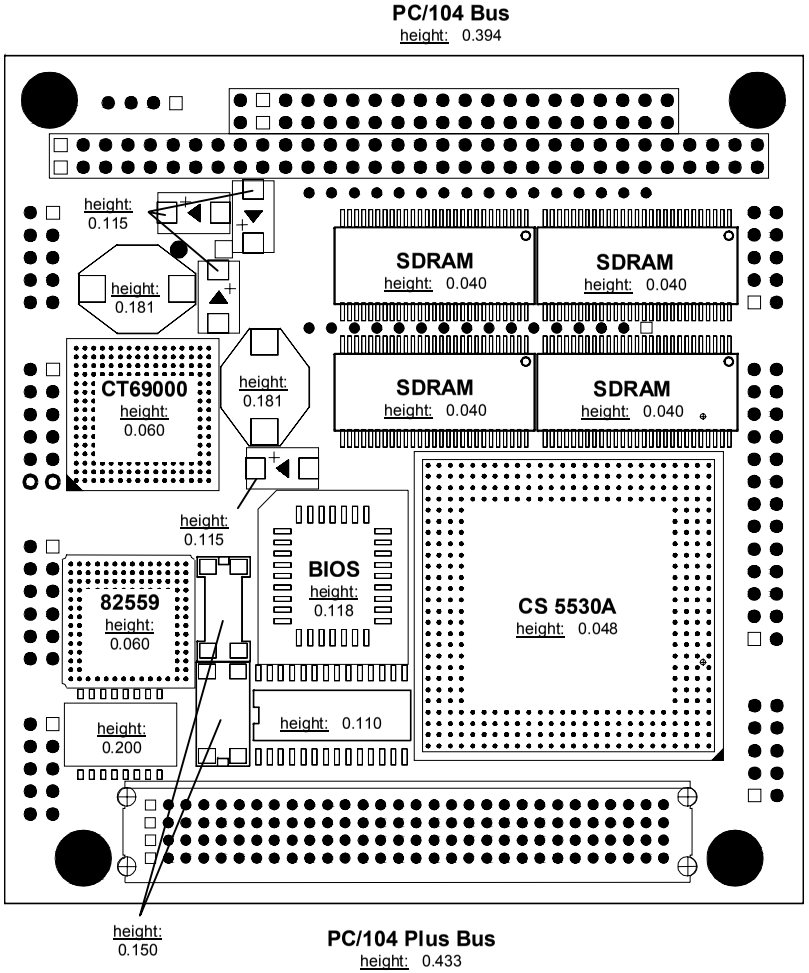
Mechanical Dimensions Top Layer:



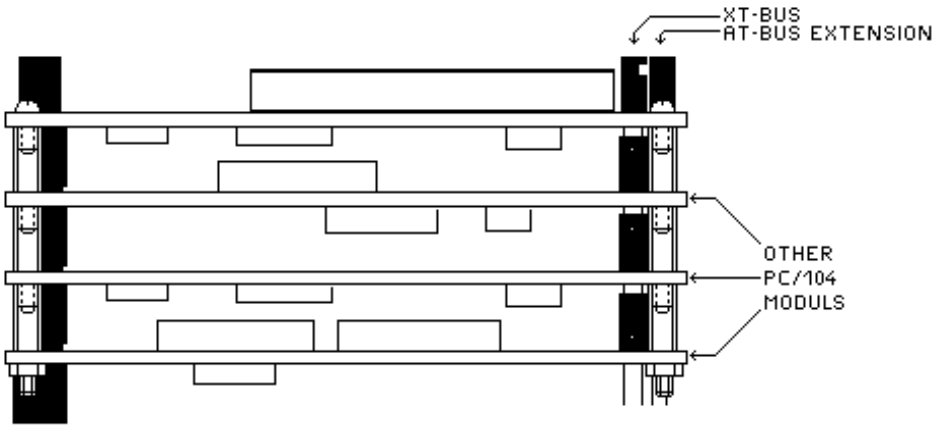
Thickness of bare board = 1,6mm

Subject to change without notice!

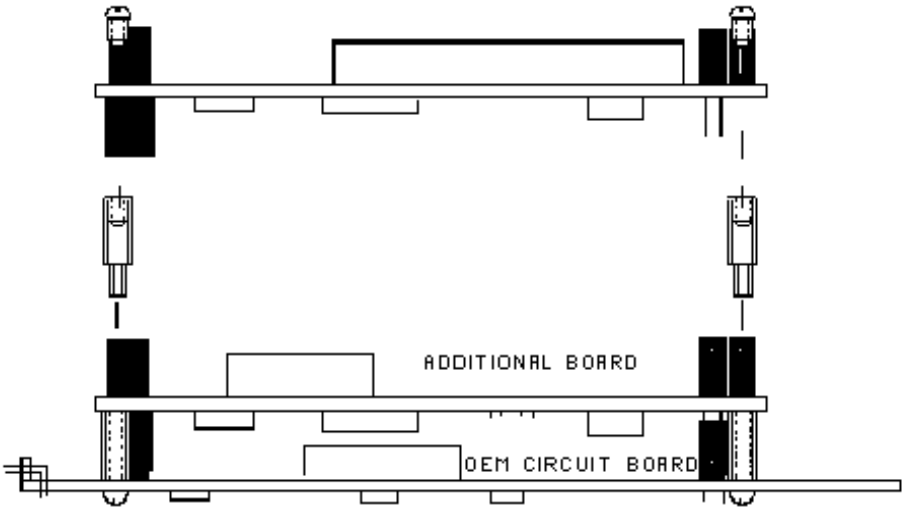
Mechanical Dimensions Bottom Layer:



Self-stacking system (standard) :



Customized system :



5.3 Environment specifications

Temperature range:	-40..85 °C
Temperature change:	max. 10K / 30 minutes
Humidity (relative):	10..90 %
Pressure:	450..1100 hPa

6 Options

- Graphic driver software
- Ethernet driver software
- Sound driver software
- Compact flash cards
- Adapter cable set (including standard PC connectors for COM 1 and 2, LPT, Keyboard, flat foil cable adapter for 3,5" Floppy, VGA adapter cable, cable for 2,5'' hard disk drives and Power supply)
- Adapter cable for Ethernet, Sound, USB, PS/2 Mouse

7 Document History

Filename	Date	Edited by	Alteration to preceding revision
TME-104P-CS2-R1V0	08/10/01	B. Reiss	Draft
TME-104P-CS2-R1V1	06/12/01	B. Reiss	Chapter 4 completed
TME-104P-CS2-R1V2	14/03/02	B. Reiss	- Description of chapter 1.23.1 (short time watchdog) corrected. - Insert chapter 1.19 (DiskOnChip)
TME-104P-CS2-R1V3	28/03/02	P.Kannegießer	Remove unused items from the display description.
TME-104P-CS2-R1V3	16/05/02	B. Reiss	"Preliminary" removed
TME-104P-CS2-R1V4	12/06/02	B. Reiss	- Correction of supported panels table. - Correction of 10/100BaseT connector pin definition.
TME-104P-CS2-R1V5	15/08/02	B. Reiss	Correction of EIDE connector type in Chapter 3.8
TME-104P-CS2-R1V6	22/08/02	B. Reiss	- Correction of VGA connector in drawing "Mechanical Dimensions Top Layer" and "Mechanical Dimensions Bottom Layer" - IDE interface pin 28 changed to GND