*i*Coupler® Digital Isolator

ADuM1100*

FEATURES

- High Data Rate: DC–100 Mbps (NRZ)
- Compatible with 3.3 V and 5.0 V Operation/ Level Translation
- 125°C Max Operating Temperature
- Low Power Operation
  - 5 V Operation:
    - 1.0 mA Max @ 1 Mbps
    - 4.5 mA Max @ 25 Mbps
    - 16.8 mA Max @ 100 Mbps
  - 3.3 V Operation:
    - 0.4 mA Max @ 1 Mbps
    - 3.5 mA Max @ 25 Mbps
    - 7.1 mA Max @ 50 Mbps
- Small Footprint: Standard 8-Lead SOIC Package
- High Common-Mode Transient Immunity: >25 kV/μs
- Safety and Regulatory Information:
  - UL Recognized
    - 2500 V rms for 1 Minute per UL 1577
  - CSA Component Acceptance Notice #5A
  - VDE Certificate of Conformity (Pending)
    - DIN EN 60747-5-2 (VDE 0884 Rev. 2): 2002–04
    - DIN EN 60950 (VDE 0805): 2001–12; EN 60950: 2000
    - V_{IORM} = 560 V_{PEAK}

APPLICATIONS

- Digital Fieldbus Isolation
- Opto-Isolator Replacement
- Computer-Peripheral Interface
- Microprocessor System Interface
- General Instrumentation and Data Acquisition Applications

GENERAL DESCRIPTION

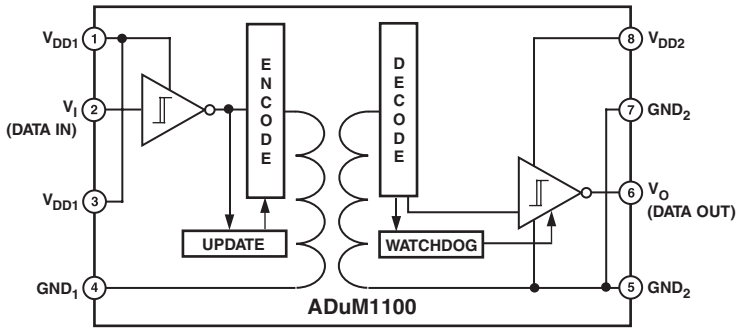
The ADuM1100 is a digital isolator based on Analog Devices' *i*Coupler technology. Combining high speed CMOS and monolithic air core transformer technology, this isolation component provides outstanding performance characteristics superior to alternatives such as optocoupler devices.

Configured as a pin compatible replacement for existing high speed optocouplers, the ADuM1100 supports data rates as high as 25 Mbps and 100 Mbps.

The ADuM1100 operates with either voltage supply ranging from 3.0 V to 5.5 V, boasts propagation delay of <18 ns and edge asymmetry of <2 ns, and is compatible with temperatures up to 125°C. It operates at very low power, less than 0.9 mA of quiescent current (sum of both sides), and a dynamic current of less than 160 μA per Mbps of data rate. Unlike common transformer implementations, the ADuM1100 provides dc correctness with a patented refresh feature that continuously updates the output signal.

The ADuM1100 is offered in three grades. The ADuM1100AR and ADuM1100BR can be operated to a maximum temperature of 100°C and support data rates up to 25 Mbps and 100 Mbps, respectively. The ADuM1100UR can be operated to a maximum temperature of 125°C and supports data rates up to 100 Mbps.

FUNCTIONAL BLOCK DIAGRAM



FOR PRINCIPLES OF OPERATION, SEE METHOD OF OPERATION, DC CORRECTNESS, AND MAGNETIC FIELD IMMUNITY SECTION.

*Protected by U.S. Patent 5,952,849. Additional patents pending.

REV. B

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ADuM1100–SPECIFICATIONS

ELECTRICAL SPECIFICATIONS, 5 V OPERATION[1]

($4.5\ V \le V_{DD1} \le 5.5\ V$, $4.5\ V \le V_{DD2} \le 5.5\ V$. All Min/Max specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at $T_A = 25°C$, $V_{DD1} = V_{DD2} = 5\ V$.)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current	$I_{DD1(Q)}$		0.3	0.8	mA	V_I = 0 V or V_{DD1}
Output Supply Current	$I_{DD2(Q)}$		0.01	0.06	mA	V_I = 0 V or V_{DD1}
Input Supply Current (25 Mbps) (See TPC 1)	$I_{DD1(25)}$		2.2	3.5	mA	12.5 MHz Logic Signal Frequency
Output Supply Current[2] (25 Mbps) (See TPC 2)	$I_{DD2(25)}$		0.5	1.0	mA	12.5 MHz Logic Signal Frequency
Input Supply Current (100 Mbps) (See TPC 1)	$I_{DD1(100)}$		9.0	14	mA	50 MHz Logic Signal Frequency, ADuM1100BR/UR Only
Output Supply Current[2] (100 Mbps) (See TPC 2)	$I_{DD2(100)}$		2.0	2.8	mA	50 MHz Logic Signal Frequency, ADuM1100BR/UR Only
Input Current	I_I	–10	+0.01	+10	µA	$0 \le V_{IN} \le V_{DD1}$
Logic High Output Voltage	V_{OH}	V_{DD2} – 0.1	5.0		V	I_O = –20 µA, $V_I = V_{IH}$
		V_{DD2} – 0.8	4.6		V	I_O = –4 mA, $V_I = V_{IH}$
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	I_O = +20 µA, $V_I = V_{IL}$
			0.03	0.1	V	I_O = +400 µA, $V_I = V_{IL}$
			0.3	0.8	V	I_O = +4 mA, $V_I = V_{IL}$
SWITCHING SPECIFICATIONS						
For ADuM1100AR						
Minimum Pulsewidth[3]	PW			40	ns	C_L = 15 pF, CMOS Signal Levels
Maximum Data Rate[4]		25			Mbps	C_L = 15 pF, CMOS Signal Levels
For ADuM1100BR/ADuM1100UR						
Minimum Pulsewidth[3]	PW		6.7	10	ns	C_L = 15 pF, CMOS Signal Levels
Maximum Data Rate[4]		100	150		Mbps	C_L = 15 pF, CMOS Signal Levels
For All Grades						
Propagation Delay Time to Logic Low Output[5, 6] (See TPC 3)	t_{PHL}		10.5	18	ns	C_L = 15 pF, CMOS Signal Levels
Propagation Delay Time to Logic High Output[5, 6] (See TPC 3)	t_{PLH}		10.5	18	ns	C_L = 15 pF, CMOS Signal Levels
Pulsewidth Distortion $\lvert t_{PLH} - t_{PHL} \rvert$[6]	PWD		0.5	2	ns	C_L = 15 pF, CMOS Signal Levels
Change Versus Temperature[7]			3		ps/°C	C_L = 15 pF, CMOS Signal Levels
Propagation Delay Skew (Equal Temperature)[6, 8]	t_{PSK1}			8	ns	C_L = 15 pF, CMOS Signal Levels
Propagation Delay Skew (Equal Temperature, Supplies)[6, 8]	t_{PSK2}			6	ns	C_L = 15 pF, CMOS Signal Levels
Output Rise/Fall Time	t_R, t_F		3		ns	C_L = 15 pF, CMOS Signal Levels
Common-Mode Transient Immunity at Logic Low/High Output[9]	$\lvert CM_L \rvert$, $\lvert CM_H \rvert$	25	35		kV/µs	V_I = 0 or V_{DD1}, V_{CM} = 1000 V, Transient Magnitude = 800 V
Input Dynamic Power Dissipation Capacitance[10]	C_{PD1}		35		pF	
Output Dynamic Power Dissipation Capacitance[10]	C_{PD2}		8		pF	

See Notes on page 5.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS, 3.3 V OPERATION[1]

(3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V. All Min/Max specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V.)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current	$I_{DD1(Q)}$		0.1	0.3	mA	V_I = 0 V or V_{DD1}
Output Supply Current	$I_{DD2(Q)}$		0.005	0.04	mA	V_I = 0 V or V_{DD1}
Input Supply Current (25 Mbps) (See TPC 1)	$I_{DD1(25)}$		2.0	2.8	mA	12.5 MHz Logic Signal Frequency
Output Supply Current[2] (25 Mbps) (See TPC 2)	$I_{DD2(25)}$		0.3	0.7	mA	12.5 MHz Logic Signal Frequency
Input Supply Current (50 Mbps) (See TPC 1)	$I_{DD1(50)}$		4.0	6.0	mA	25 MHz Logic Signal Frequency, ADuM1100BR/UR Only
Output Supply Current[2] (50 Mbps) (See TPC 2)	$I_{DD2(50)}$		1.2	1.6	mA	25 MHz Logic Signal Frequency, ADuM1100BR/UR Only
Input Current	I_I	–10	+0.01	+10	μA	0 ≤ V_{IN} ≤ V_{DD1}
Logic High Output Voltage	V_{OH}	V_{DD2} – 0.1	3.3		V	I_O = –20 μA, V_I = V_{IH}
		V_{DD2} – 0.5	3.0		V	I_O = –2.5 mA, V_I = V_{IH}
Logic Low Output Voltage	V_{OL}		0.0	0.1	V	I_O = 20 μA, V_I = V_{IL}
			0.04	0.1	V	I_O = 400 μA, V_I = V_{IL}
			0.3	0.4	V	I_O = 2.5 mA, V_I = V_{IL}
SWITCHING SPECIFICATIONS						
For ADuM1100AR						
Minimum Pulsewidth[3]	PW			40	ns	C_L = 15 pF, CMOS Signal Levels
Maximum Data Rate[4]		25			Mbps	C_L = 15 pF, CMOS Signal Levels
For ADuM1100BR/ADuM1100UR						
Minimum Pulsewidth[3]	PW		10	20	ns	C_L = 15 pF, CMOS Signal Levels
Maximum Data Rate[4]		50	100		Mbps	C_L = 15 pF, CMOS Signal Levels
For All Grades						
Propagation Delay Time to Logic Low Output[5, 6] (See TPC 4)	t_{PHL}		14.5	28	ns	C_L = 15 pF, CMOS Signal Levels
Propagation Delay Time to Logic High Output[5, 6] (See TPC 4)	t_{PLH}		15.0	28	ns	C_L = 15 pF, CMOS Signal Levels
Pulsewidth Distortion $\lvert t_{PLH} - t_{PHL} \rvert$[6]	PWD		0.5	3	ns	C_L = 15 pF, CMOS Signal Levels
Change Versus Temperature[7]			10		ps/°C	C_L = 15 pF, CMOS Signal Levels
Propagation Delay Skew (Equal Temperature)[6, 8]	t_{PSK1}			15	ns	C_L = 15 pF, CMOS Signal Levels
Propagation Delay Skew (Equal Temperature, Supplies)[6, 8]	t_{PSK2}			12	ns	C_L = 15 pF, CMOS Signal Levels
Output Rise/Fall Time	t_R, t_F		3		ns	C_L = 15 pF, CMOS Signal Levels
Common-Mode Transient Immunity at Logic Low/High Output[9]	$\lvert CM_L \rvert$, $\lvert CM_H \rvert$	25	35		kV/μs	V_I = 0 or V_{DD1}, V_{CM} = 1000 V, Transient Magnitude = 800 V
Input Dynamic Power Dissipation Capacitance[10]	C_{PD1}		47		pF	
Output Dynamic Power Dissipation Capacitance[10]	C_{PD2}		14		pF	

See Notes on page 5.

Specifications subject to change without notice.

ELECTRICAL SPECIFICATIONS, MIXED 5 V/3 V or 3 V/5 V OPERATION[1]

(5 V/3 V operation: 4.5 V ≤ V_{DD1} ≤ 5.5 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V. 3 V/5 V operation: 3.0 V ≤ V_{DD1} ≤ 3.6 V, 4.5 V ≤ V_{DD2} ≤ 5.5 V. All Min/Max specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, V_{DD2} = 5 V or V_{DD1} = 5 V, V_{DD2} = 3.3 V.)

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
DC SPECIFICATIONS						
Input Supply Current, Quiescent	$I_{DDI(Q)}$					
5 V/3 V Operation			0.3	0.8	mA	
3 V/5 V Operation			0.1	0.3	mA	
Output Supply Current, Quiescent	$I_{DDO(Q)}$					
5 V/3 V Operation			0.005	0.04	mA	
3 V/5 V Operation			0.01	0.06	mA	
Input Supply Current, (25 Mbps)	$I_{DDI(25)}$					
5 V/3 V Operation			2.2	3.5	mA	12.5 MHz Logic Signal Frequency
3 V/5 V Operation			2.0	2.8	mA	12.5 MHz Logic Signal Frequency
Output Supply Current, (25 Mbps)	$I_{DDO(25)}$					
5 V/3 V Operation			0.3	0.7	mA	12.5 MHz Logic Signal Frequency
3 V/5 V Operation			0.5	1.0	mA	12.5 MHz Logic Signal Frequency
Input Supply Current, (50 Mbps)	$I_{DDI(50)}$					
5 V/3 V Operation			4.5	7.0	mA	25 MHz Logic Signal Frequency
3 V/5 V Operation			4.0	6.0	mA	25 MHz Logic Signal Frequency
Output Supply Current, (50 Mbps)	$I_{DDO(50)}$					
5 V/3 V Operation			1.2	1.6	mA	25 MHz Logic Signal Frequency
3 V/5 V Operation			1.0	1.5	mA	25 MHz Logic Signal Frequency
Input Currents	I_{IA}	–10	+0.01	+10	μA	$0 \le V_{IA}, V_{IB}, V_{IC}, V_{ID} \le V_{DD1}$ or V_{DD2}
Logic High Output Voltage,	V_{OH}	V_{DD2} – 0.1	3.3		V	I_O = –20 μA, $V_I = V_{IH}$
5 V/3 V Operation		V_{DD2} – 0.5	3.0		V	I_O = –2.5 mA, $V_I = V_{IH}$
Logic Low Output Voltage,	V_{OL}		0.0	0.1	V	I_O = 20 μA, $V_I = V_{IL}$
5 V/3 V Operation			0.04	0.1	V	I_O = 400 μA, $V_I = V_{IL}$
			0.3	0.4	V	I_O = 2.5 mA, $V_I = V_{IL}$
Logic High Output Voltage,	V_{OH}	V_{DD2} – 0.1	5.0		V	I_O = –20 μA, $V_I = V_{IH}$
3 V/5 V Operation		V_{DD2} – 0.8	4.6		V	I_O = –4 mA, $V_I = V_{IH}$
Logic Low Output Voltage,	V_{OL}		0.0	0.1	V	I_O = 20 μA, $V_I = V_{IL}$
3 V/5 V Operation			0.03	0.1	V	I_O = 400 μA, $V_I = V_{IL}$
			0.3	0.8	V	I_O = 4 mA, $V_I = V_{IL}$
SWITCHING SPECIFICATIONS						
For ADuM1100AR						
Minimum Pulsewidth[3]	PW			40	ns	C_L = 15 pF, CMOS Signal Levels
Maximum Data Rate[4]		25			Mbps	C_L = 15 pF, CMOS Signal Levels
For ADuM1100BR/ADuM1100UR						
Minimum Pulsewidth[3]	PW			20	ns	C_L = 15 pF, CMOS Signal Levels
Maximum Data Rate[4]		50			Mbps	C_L = 15 pF, CMOS Signal Levels
For All Grades						
Propagation Delay Time to Logic Low/High Output[5, 6]	t_{PHL}, t_{PHL}					
5 V/3 V Operation (See TPC 5)			13	21	ns	C_L = 15 pF, CMOS Signal Levels
3 V/5 V Operation (See TPC 6)			16	26	ns	C_L = 15 pF, CMOS Signal Levels
Pulsewidth Distortion, $\lvert t_{PLH} - t_{PHL} \rvert$[6]	PWD					
5 V/3 V Operation			0.5	2	ns	C_L = 15 pF, CMOS Signal Levels
3 V/5 V Operation			0.5	3	ns	C_L = 15 pF, CMOS Signal Levels
Change Versus Temperature						
5 V/3 V Operation			3		ps/°C	C_L = 15 pF, CMOS Signal Levels
3 V/5 V Operation			10		ps/°C	C_L = 15 pF, CMOS Signal Levels
Propagation Delay Skew (Equal Temperature)[6, 8]	t_{PSK1}					
5 V/3 V Operation				12	ns	C_L = 15 pF, CMOS Signal Levels
3 V/5 V Operation				15	ns	C_L = 15 pF, CMOS Signal Levels
Propagation Delay Skew (Equal Temperature, Supplies)[6, 8]	t_{PSK2}					
5 V/3 V Operation				9	ns	C_L = 15 pF, CMOS Signal Levels
3 V/5 V Operation				12	ns	C_L = 15 pF, CMOS Signal Levels
Output Rise/Fall Time (10%–90%)	t_R, t_f		3		ns	C_L = 15 pF, CMOS Signal Levels

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
SWITCHING SPECIFICATIONS (continued)						
Common Mode Transient Immunity at Logic Low/High Output[8]	$\|CM_L\|$, $\|CM_H\|$	25	35		kV/μs	V_I = 0 or V_{DD1}, V_{CM} = 1000 V, Transient Magnitude = 800 V
Input Dynamic Power Dissipation Capacitance[10]	C_{PD1}					
5 V/3 V Operation			35		pF	
3 V/5 V Operation			47		pF	
Output Dynamic Power Dissipation Capacitance[10]	C_{PD2}					
5 V/3 V Operation			8		pF	
3 V/5 V Operation			14		pF	

NOTES

[1]All voltages are relative to their respective ground.

[2]Output supply current values are with no output load present. The supply current drawn at a given signal frequency when an output load is present is given by: $I_{DD2(L)} = I_{DD2} + V_{DD2} \times f \times C_L$, where I_{DD2} is the unloaded output supply current, f is the input signal frequency, and C_L is the output load capacitance.

[3]The minimum pulsewidth is the shortest pulsewidth at which the specified pulsewidth distortion is guaranteed.

[4]The maximum data rate is the fastest data rate at which the specified pulsewidth distortion is guaranteed.

[5]t_{PHL} is measured from the 50% level of the falling edge of the V_I signal to the 50% level of the falling edge of the V_O signal. t_{PLH} is measured from the 50% level of the rising edge of the V_I signal to the 50% level of the rising edge of the V_O signal.

[6]Since the input thresholds of the ADuM1100 are at voltages other than the 50% level of typical input signals, the measured propagation delay and pulsewidth distortion may be affected by slow input rise/fall times. See the Propagation Delay-Related Parameters section and Figures 3–7 for information on the impact of given input rise/fall times on these parameters.

[7]Pulsewidth distortion change versus temperature is the absolute value of the change in pulsewidth distortion for a 1°C change in operating temperature.

[8]t_{PSK1} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that will be measured between units at the same operating temperature and output load within the recommended operating conditions. t_{PSK2} is the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} that will be measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

[9]CM_H is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O > 0.8\ V_{DD2}$. CM_L is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_O < 0.8$ V. The common-mode voltage slew rates apply to both rising and falling edges. The transient magnitude is the range over which the common-mode is slewed.

[10]The Dynamic Power Dissipation Capacitance is given by:
$C_{PDi} = (I_{DDi(100)} - I_{DDi(Q)})/(V_{DDi} \times f)$, where i = 1 or 2 and f is the input signal frequency.
The supply current consumptions at a given frequency and output load are calculated as follows:
$I_{DD1} = C_{PD1} \times V_{DD1} \times f + I_{DD1(Q)}$; $I_{DD2(L)} = (C_{PD2} + C_L) \times V_{DD2} \times f + I_{DD2(Q)}$, where C_L is the output load capacitance.

Specifications subject to change without notice.

PACKAGE CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output)[1]	R_{I-O}		10^{12}		Ω	
Capacitance (Input-Output)[1]	C_{I-O}		1		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
Input IC Junction-to-Case Thermal Resistance	θ_{JCI}		46		°C/W	Thermocouple Located at Center Underside of Package
Output IC Junction-to-Case Thermal Resistance	θ_{JCO}		41		°C/W	
Package Power Dissipation	P_{PD}			240	mW	

NOTES

[1]Device considered a 2-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.

[2]Input capacitance is measured at Pin 2 (V_I).

REGULATORY INFORMATION

The ADuM1100 has been approved by the following organizations:

UL	CSA	VDE (Pending)
Recognized under 1577 Component Recognition Program[1] File E214100	Approved under CSA Component Acceptance Notice #5A, C22.2 No. 1-98, C22.2 No. 14-95, and C22.2 No. 950-95 File 205078	Certified according to: DIN EN 60747-5-2 (VDE 0884 Rev. 2): 2002–4[2] DIN EN 60950 (VDE 0805): 2001–12; EN60950: 2000

NOTES

[1]In accordance with UL 1577, each ADuM1100 is proof tested by applying an insulation test voltage ≥ 3000 V rms for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ μA).

[2]In accordance with VDE 0884, each ADuM1100 is proof tested by applying an insulation test voltage ≥ 1050 V_{PEAK} for 1 second (partial discharge detection limit ≤ 5 pC).

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Parameter	Symbol	Value	Unit	Conditions
Minimum External Air Gap (Clearance)	L(I01)	4.90 min	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	4.01 min	mm	Measured from input terminals to output terminals, shortest distance path along body
Minimum Internal Gap (Internal Clearance)		0.016 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

VDE 0884 INSULATION CHARACTERISTICS (APPROVAL PENDING)

Description	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110			
For Rated Mains Voltage ≤ 150 V rms		I–IV	
For Rated Mains Voltage ≤ 300 V rms		I–III	
For Rated Mains Voltage ≤ 400 V rms		I–II	
Climatic Classification		40/125/21	
Pollution Degree (DIN VDE 0110, Table I)		2	
Maximum Working Insulation Voltage	V_{IORM}	560	V_{PEAK}
Input to Output Test Voltage, Method b1			
$V_{IORM} \times 1.875 = V_{PR}$, 100% Production Test, $t_M = 1$ sec, Partial Discharge < 5 pC	V_{PR}	1050	V_{PEAK}
Input to Output Test Voltage, Method a	V_{PR}	672	V_{PEAK}
After Environmental Tests Subgroup 1)			
$V_{IORM} \times 1.6 = V_{PR}$, $t_M = 60$ sec, Partial Discharge < 5 pC	V_{PR}	896	V_{PEAK}
After Input and/or Safety Test Subgroup 2/3)			
$V_{IORM} \times 1.2 = V_{PR}$, $t_M = 60$ sec, Partial Discharge < 5 pC	V_{PR}	672	V_{PEAK}
Highest Allowable Overvoltage (Transient Overvoltage, $t_{TR} = 10$ sec)	V_{TR}	4000	V_{PEAK}
Safety-Limiting Values (Maximum Value Allowed in the Event of a Failure,			
See Thermal Derating Curve, Figure 1)			
Case Temperature	T_S	150	°C
Input Current	$I_{S, INPUT}$	160	mA
Output Current	$I_{S, OUTPUT}$	170	mA
Insulation Resistance at T_S, $V_{IO} = 500$ V	Rs	$>10^9$	Ω

NOTE

This isolator is suitable for "basic isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

The * marking on the package denotes VDE 0884 approval for 560 V_{PEAK} working voltage.

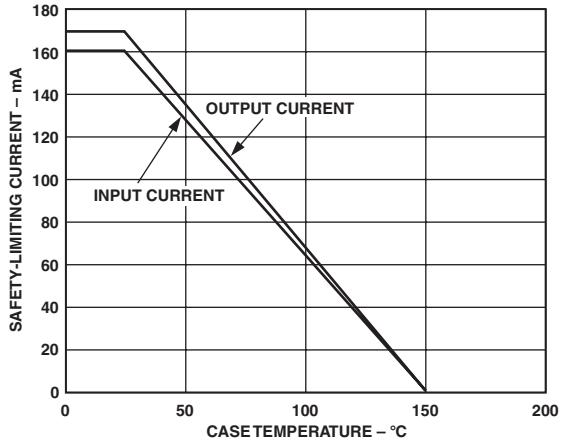


Figure 1. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per VDE 0884

ABSOLUTE MAXIMUM RATINGS[1]

Parameter	Symbol	Min	Max	Unit
Storage Temperature	T_S	–55	+150	°C
Ambient Operating Temperature	T_A	–40	+125	°C
Supply Voltages[2]	V_{DD1}, V_{DD2}	–0.5	+6.5	V
Input Voltage[2]	V_I	–0.5	V_{DD1} + 0.5	V
Output Voltage[2]	V_O	–0.5	V_{DD2} + 0.5	V
Average Current, Per Pin[3]				
Temperature ≤ 100°C		–25	+25	mA
Temperature ≤ 125°C				
Input Current		–7	+7	mA
Output Current		–20	+20	mA
ESD (Human Body Model)		–2.0	+2.0	kV
Lead Solder Temperature (Hand Soldering)	Heating at Lead Tip 275°C ±10°C for 20 Seconds			
Solder Reflow Temperature Profile	JEDEC Standard 20A			

NOTES
[1] Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute maximum ratings apply individually only, not in combination. Ambient temperature = 25°C, unless otherwise noted.
[2] All voltages are relative to their respective ground.
[3] See Figure 1 for information on maximum allowable current for various temperatures.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Operating Temperature				
ADuM1100AR and ADuM1100BR	T_A	–40	+100	°C
ADuM1100UR	T_A	–40	+125	°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	3.0	5.5	V
Logic High Input Voltage, 5 V Operation[1, 2] (See TPCs 7 and 8)	V_{IH}	2.0	V_{DD1}	V
Logic Low Input Voltage, 5 V Operation[1, 2] (See TPCs 7 and 8)	V_{IL}	0.0	0.8	V
Logic High Input Voltage, 3.3 V Operation[1, 2] (See TPCs 7 and 8)	V_{IH}	1.5	V_{DD1}	V
Logic Low Input Voltage, 3.3 V Operation[1, 2] (See TPCs 7 and 8)	V_{IL}	0.0	0.5	V
Input Signal Rise and Fall Times			1.0	ms

NOTES
[1]All voltages are relative to their respective ground.
[2]Input switching thresholds have 300 mV of hysteresis.

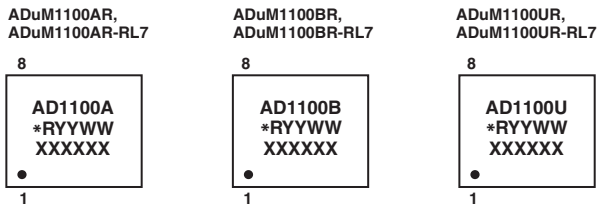
See the Method of Operation, DC Correctness, and Magnetic Field Immunity section and Figures 8 and 9 for information on immunity to external magnetic fields.

Table I. Truth Table (Positive Logic)

V_I Input	V_{DD1} State	V_{DD2} State	V_O Output
H	Powered	Powered	H
L	Powered	Powered	L
X	Unpowered	Powered	H*
X	Powered	Unpowered	X*

*V_O returns to V_I state within 1 μs of power restoration.

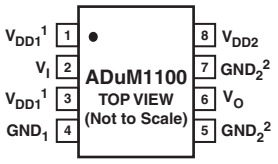
Note: Package branding is as follows:



where

*	= VDE 0884 mark (pending)
R	= Package Designator (R denotes SOIC)
YYWW	= Date Code
XXXXXX	= Lot Code

PIN CONFIGURATION



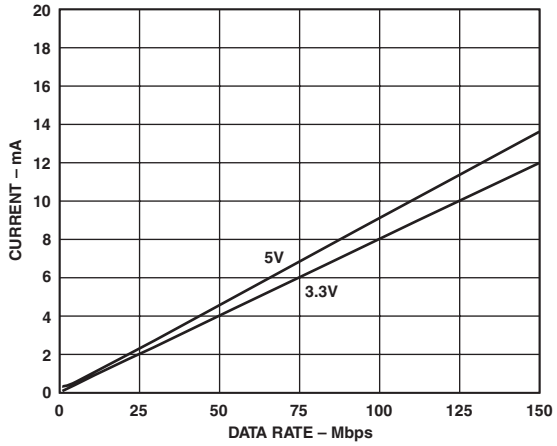
NOTES
[1]PIN 1 AND PIN 3 ARE INTERNALLY CONNECTED. EITHER OR BOTH MAY BE USED FOR V_{DD1}.
[2]PIN 5 AND PIN 7 ARE INTERNALLY CONNECTED. EITHER OR BOTH MAY BE USED FOR GND_2.

ORDERING GUIDE

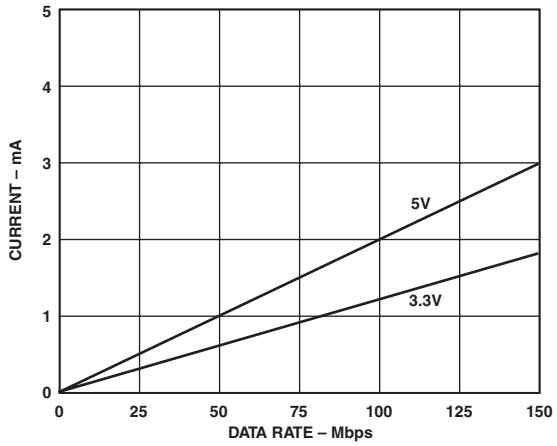
Model	Temperature Range	Max Data Rate (Mbps)	Min Pulse-width (ns)	Package Description	Package Option
ADuM1100AR	–40°C to +100°C	25	40	8-Lead SOIC	R-8
ADuM1100BR	–40°C to +100°C	100	10	8-Lead SOIC	R-8
ADuM1100UR	–40°C to +125°C	100	10	8-Lead SOIC	R-8
ADuM1100AR-RL7	–40°C to +100°C	25	40	8-Lead SOIC, 1000 Piece Reel	R-8
ADuM1100BR-RL7	–40°C to +100°C	100	10	8-Lead SOIC, 1000 Piece Reel	R-8
ADuM1100UR-RL7	–40°C to +125°C	100	10	8-Lead SOIC, 1000 Piece Reel	R-8

CAUTION

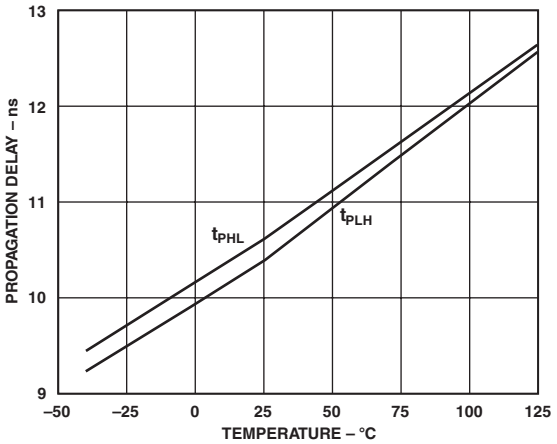
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADuM1100 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



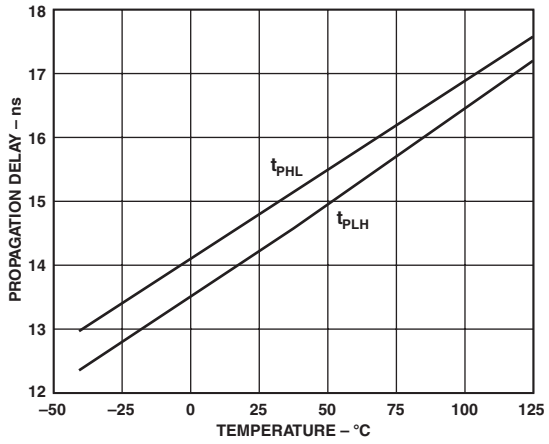
TPC 1. Typical Input Supply Current vs. Logic Signal Frequency for 5 V and 3.3 V Operation



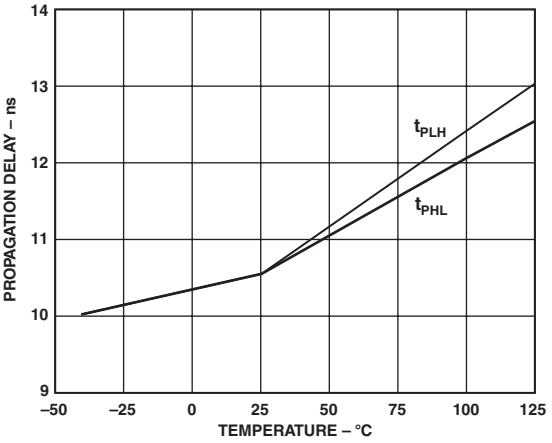
TPC 2. Typical Output Supply Current vs. Logic Signal Frequency for 5 V and 3.3 V Operation



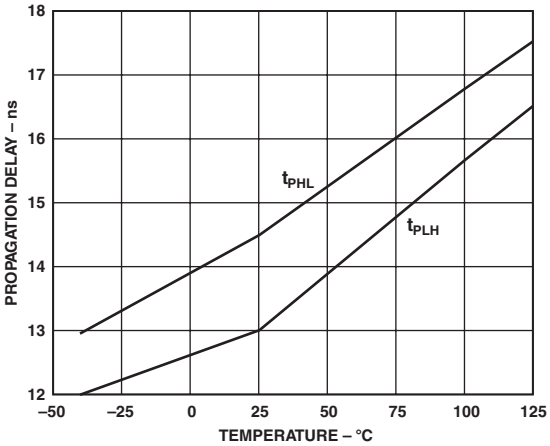
TPC 3. Typical Propagation Delays vs. Temperature, 5 V Operation



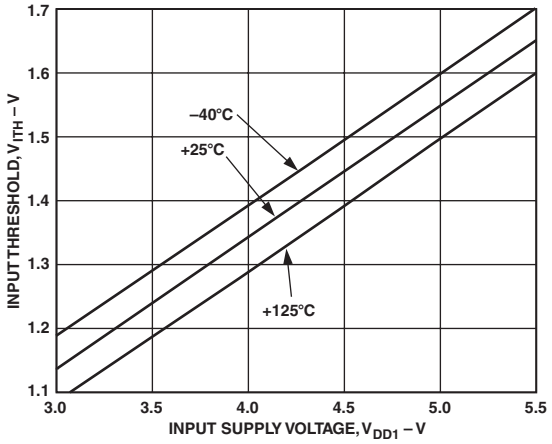
TPC 4. Typical Propagation Delays vs. Temperature, 3.3 V Operation



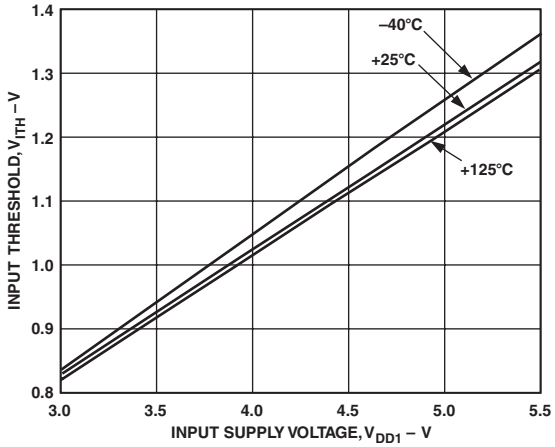
TPC 5. Typical Propagation Delays vs. Temperature, 5 V/3 V Operation



TPC 6. Typical Propagation Delays vs. Temperature, 3 V/5 V Operation



TPC 7. Typical Input Voltage Switching Threshold, Low-to-High Transition



TPC 8. Typical Input Voltage Switching Threshold, High-to-Low Transition

APPLICATION INFORMATION

PC Board Layout

The ADuM1100 digital isolator requires no external interface circuitry for the logic interfaces. A bypass capacitor is recommended at the input and output supply pins. The input bypass capacitor may most conveniently be connected between Pins 3 and 4 (Figure 2). Alternatively, the bypass capacitor may be located between Pins 1 and 4. The output bypass capacitor may be connected between Pins 7 and 8 or Pins 5 and 8. The capacitor value should be between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the power supply pins should not exceed 20 mm.

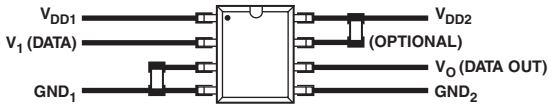


Figure 2. Recommended Printed Circuit Board Layout

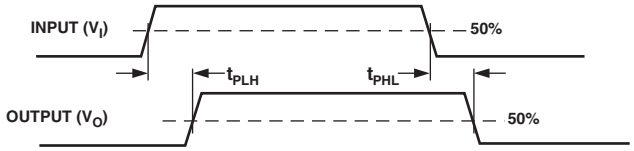


Figure 3. Propagation Delay Parameters

Propagation Delay-Related Parameters

Propagation delay time is a parameter that describes the length of time it takes for a logic signal to propagate through a component. Propagation delay time to logic low output and propagation delay time to logic high output refer to the duration between an input signal transition and the respective output signal transition (Figure 3).

Pulsewidth distortion is the maximum difference between t_{PLH} and t_{PHL} and provides an indication of how accurately the input signal's timing is preserved in the component's output signal. Propagation delay skew is the difference between the minimum and maximum propagation delay values among multiple ADuM1100 components operated at the same operating temperature and having the same output load.

Depending on the input signal rise/fall time, the measured propagation delay based on the input 50% level can vary from the true propagation delay of the component (as measured from its input switching threshold). This is due to the fact that the input threshold, as is the case with commonly used optocouplers, is at a different voltage level than the 50% point of typical input signals. This propagation delay difference is given by:

$$\Delta_{LH} = t'_{PLH} - t_{PLH} = \left(t_r / 0.8V_1\right)\left(0.5V_1 - V_{ITH(L-H)}\right)$$

$$\Delta_{HL} = t'_{PHL} - t_{PHL} = \left(t_f / 0.8V_1\right)\left(0.5V_1 - V_{ITH(H-L)}\right)$$

where:

t_{PLH}, t_{PHL} = propagation delays as measured from the input 50% level.

t'_{PLH}, t'_{PHL} = propagation delays as measured from the input switching thresholds.

t_r, t_f = input 10%–90% rise/fall time.

V_I = amplitude of input signal (0 to V_I levels assumed).

$V_{ITH(L-H)}$, $V_{ITH(H-L)}$ = input switching thresholds.

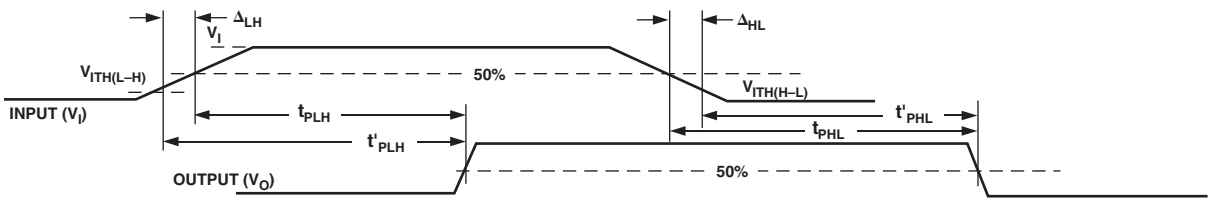


Figure 4. Impact of Input Rise/Fall Time on Propagation Delay

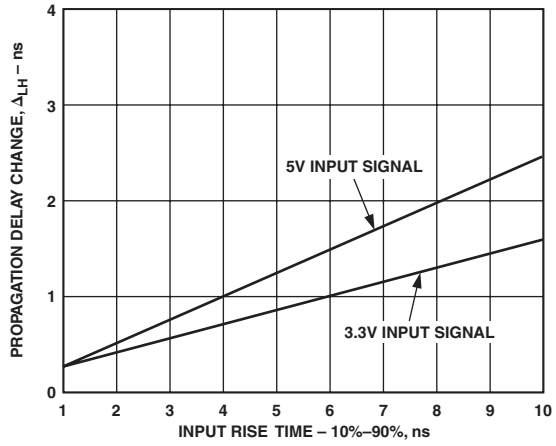


Figure 5. Typical Propagation Delay Change Due to Input Rise Time Variation (for V_{DD1} = 3.3 V and 5 V)

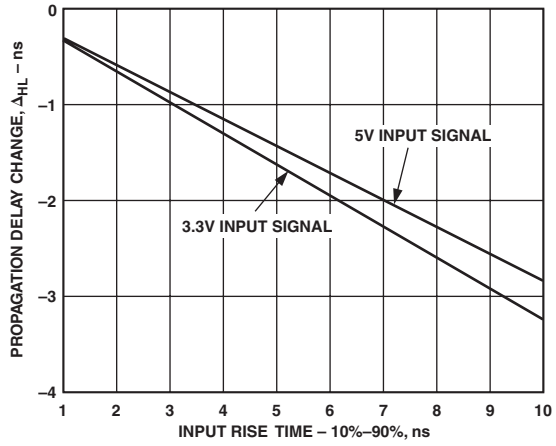


Figure 6. Typical Propagation Delay Change Due to Input Fall Time Variation (for V_{DD1} = 3.3 V and 5 V)

The impact of slower input edge rates can also affect the measured pulsewidth distortion as based on the input 50% level. This impact may either increase or decrease the apparent pulsewidth distortion depending on the relative magnitudes of t_{PHL}, t_{PLH}, and PWD. The case of interest here is the condition that leads to the largest increase in pulsewidth distortion. The change in this case is given by:

$$\Delta_{PWD} = PWD' - PWD = \Delta_{LH} - \Delta_{HL} =$$
$$\left(t/0.8V_1\right)\left(V - V_{ITH(L-H)} - V_{ITH(H-L)}\right), \left(for\ t = t_r = t_f\right)$$

where

$$PWD = \left|t_{PLH} - t_{PHL}\right|$$
$$PWD' = \left|t'_{PLH} - t'_{PHL}\right|$$

This adjustment in pulsewidth distortion is plotted as a function of input rise/fall time in Figure 7.

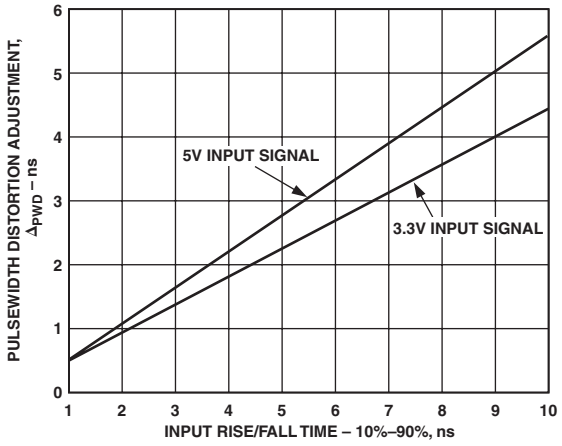


Figure 7. Typical Pulsewidth Distortion Adjustment Due to Input Rise/Fall Time Variation (at V_{DD1} = 3.3 V and 5 V)

Method of Operation, DC Correctness, and Magnetic Field Immunity

Referring to the functional block diagram, the two coils act as a pulse transformer. Positive and negative logic transitions at the isolator input cause narrow (2 ns) pulses to be sent via the transformer to the decoder. The decoder is bistable and therefore either set or reset by the pulses indicating input logic transitions. In the absence of logic transitions at the input for more than 2 µs, a periodic "update" pulse of the appropriate polarity is sent to ensure "dc correctness" at the output. If the decoder receives none of these "update" pulses for more than about 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a logic high state by the watchdog timer circuit.

The limitation on the ADuM1100's magnetic field immunity is set by the condition in which induced voltage in the transformer's "receiving" coil is sufficiently large to either falsely set or reset the decoder. The analysis that follows defines the conditions under which this may occur. The ADuM1100's 3.3 V operating condition is examined as it represents the most susceptible mode of operation.

The pulses at the transformer output are greater than 1.0 V in amplitude. The decoder has sensing thresholds at about 0.5 V, therefore establishing a 0.5 V margin in which induced voltages can be tolerated. The induced voltage induced across the "receiving" coil is given by:

$$V = \left(-d\beta/dt\right)\Sigma\pi r_n^2; n = 1, 2, \ldots, N$$

where

β = magnetic flux density (Gauss).
N = number of turns in receiving coil.
r_n = radius of nth turn in receiving coil (cm).

Given the geometry of the receiving coil in the ADuM1100 and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated as shown in Figure 8.

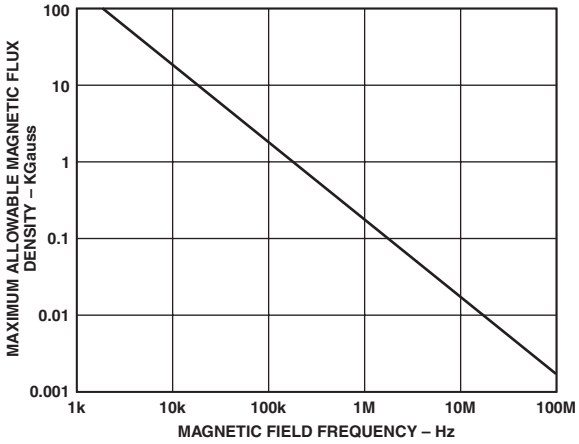


Figure 8. Maximum Allowable External Magnetic Field

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 KGauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and will not cause a faulty output transition. Similarly, if such an event were to occur during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances away from the ADuM1100 transformers. Figure 9 expresses these allowable current magnitudes as a function of frequency for selected distances. As can be seen, the ADuM1100 is extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For the 1 MHz example noted above, one would have to place a current of 1 kA 5 mm away from the ADuM1100 to affect the component's operation.

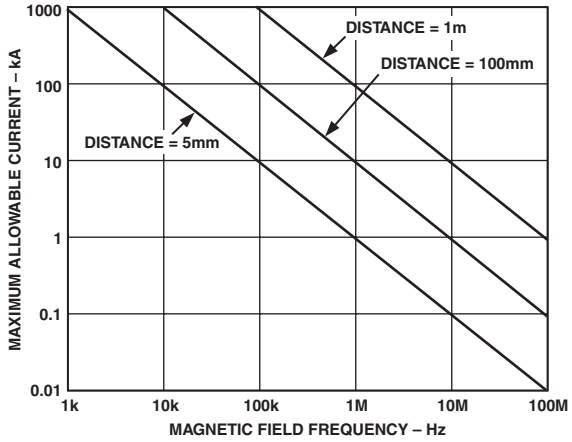


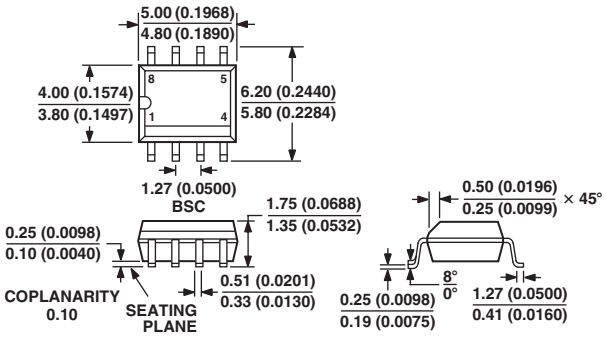
Figure 9. Maximum Allowable Current for Various Current-to-ADuM1100 Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce sufficiently large error voltages to trigger the thresholds of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

OUTLINE DIMENSIONS

8-Lead Standard Small Outline Package [SOIC]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches).



COMPLIANT TO JEDEC STANDARDS MS-012AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN

Revision History

Location	Page
1/03—Data Sheet changed from REV. A to REV. B.	
Added ADuM1100UR Grade	Universal
Changed ADuM1100AR/ADuM1100BR to ADuM1100	Universal
Changes to FEATURES	1
Changes to GENERAL DESCRIPTION	1
Changes to SPECIFICATIONS	2
Added Electrical Specifications, Mixed 5 V/3 V or 3 V/5 V Operation table	4
Updated REGULATORY INFORMATION	6
Changes to VDE 0884 INSULATION CHARACTERISTICS	6
Changes to ABSOLUTE MAXIMUM RATINGS	7
Changes to Package Branding	8
Updated TPCs 3–8	9
Deleted *i*Coupler in Field Bus Networks section	11
Changes to Figure 8	12
Added a new Figure 9 and related text	12
11/02—Data Sheet changed from REV. 0 to REV. A.	
Edits to FEATURES	1
Edits to REGULATORY INFORMATION	4
Edits to VDE 0884 INSULATION CHARACTERISTICS	5
Added Revision History	12
Updated OUTLINE DIMENSIONS	12

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