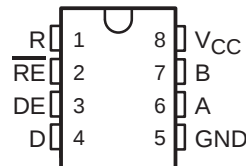


SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040H – AUGUST 1987 – REVISED JUNE 2000

- Meet or Exceed the Requirements of TIA/EIA-422-B, TIA/EIA-485-A[†] and ITU Recommendations V.11 and X.27
- Operate at Data Rates up to 35 Mbaud
- Four Skew Limits Available:
SN65ALS176 . . . 15 ns
SN75ALS176 . . . 10 ns
SN75ALS176A . . . 7.5 ns
SN75ALS176B . . . 5 ns
- Designed for Multipoint Transmission on Long Bus Lines in Noisy Environments
- Low Supply-Current Requirements
. . . 30 mA Max
- Wide Positive and Negative Input/Output Bus-Voltage Ranges
- Thermal Shutdown Protection
- Driver Positive and Negative Current Limiting
- Receiver Input Hysteresis
- Glitch-Free Power-Up and Power-Down Protection
- Receiver Open-Circuit Fail-Safe Design

D OR P PACKAGE
(TOP VIEW)



description

The SN65ALS176 and SN75ALS176 series differential bus transceivers are designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet TIA/EIA-422-B, TIA/EIA-485-A, and ITU Recommendations V.11 and X.27.

The SN65ALS176 and SN75ALS176 series combine a 3-state, differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form a differential input/output (I/O) bus port that is designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$. This port features wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The SN65ALS176 is characterized for operation from -40°C to 85°C . The SN75ALS176 series is characterized for operation from 0°C to 70°C .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

[†] These devices meet or exceed the requirements of TIA/EIA-485-A, except for the Generator Contention Test (para. 3.4.2) and the Generator Current Limit (para. 3.4.3). The applied test voltage ranges are -6 V to 8 V for the SN75ALS176, SN75ALS176A, and SN75ALS176B and -4 V to 8 V for the SN65ALS180.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

Copyright © 2000, Texas Instruments Incorporated

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B

DIFFERENTIAL BUS TRANSCEIVERS

SLLS040H – AUGUST 1987 – REVISED JUNE 2000

AVAILABLE OPTIONS

T _A	t _{sk(lim)} [†]	PACKAGED DEVICES	
		SMALL OUTLINE (D) [‡]	PLASTIC DIP (P)
0°C to 70°C	10 7.5 5	SN75ALS176D SN75ALS176AD SN75ALS176BD	SN75ALS176P SN75ALS176AP SN75ALS176BP
–40°C to 85°C	15	SN65ALS176D	SN65ALS176P

[†] This is the maximum range that the driver or receiver delay times vary over temperature, V_{CC}, and process (device to device).

[‡] The D package is available taped and reeled. Add the suffix R to the device type (e.g., SN75ALS176DR).

Function Tables

DRIVER

INPUT D	ENABLE DE	OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

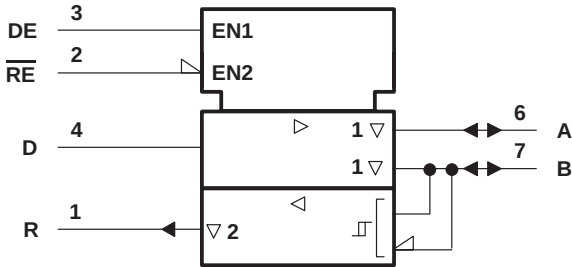
H = high level, L = low level, X = irrelevant,
Z = high impedance

RECEIVER

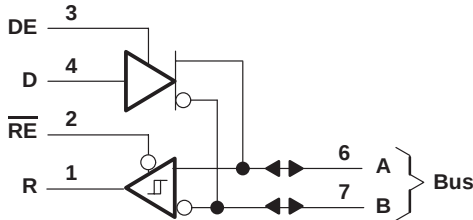
DIFFERENTIAL INPUTS A–B	ENABLE $\overline{\text{RE}}$	OUTPUT R
V _{ID} ≥ 0.2 V	L	H
–0.2 V < V _{ID} < 0.2 V	L	?
V _{ID} ≤ –0.2 V	L	L
X	H	Z
Inputs open	L	H

H = high level, L = low level, X = irrelevant,
Z = high impedance

logic symbol[§]

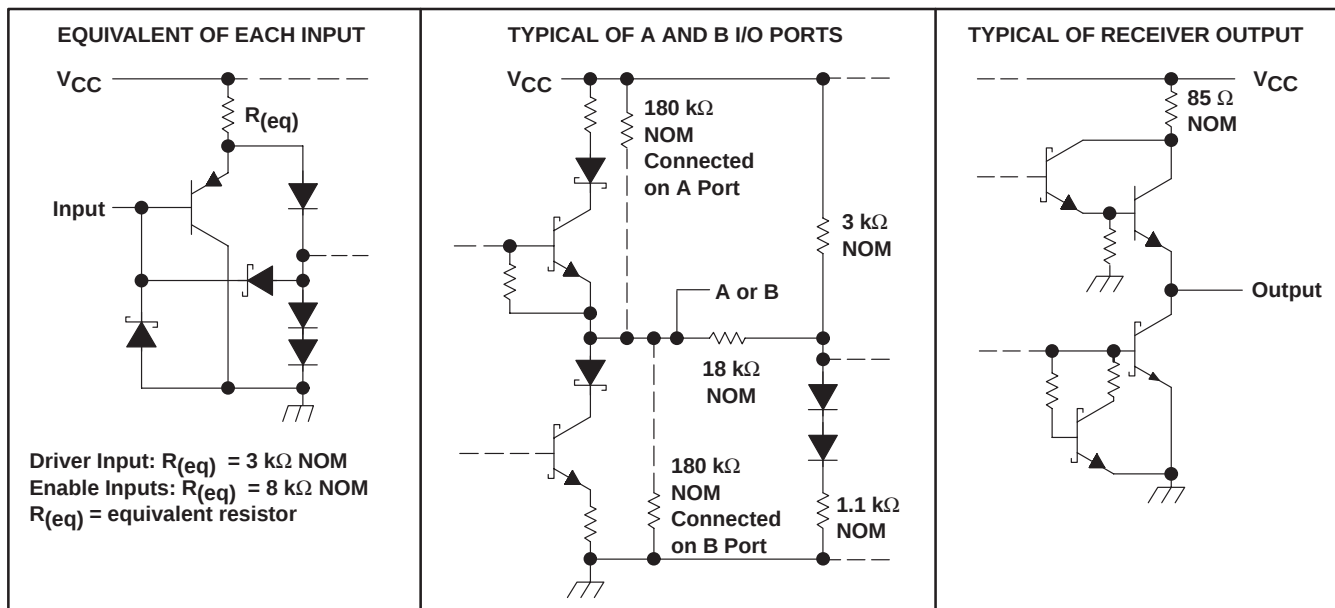


logic diagram (positive logic)



[§] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage, V _{CC} (see Note 1)	7 V
Voltage range at any bus terminal	–7 V to 12 V
Enable input voltage, V _I	5.5 V
Package thermal impedance, θ_{JA} (see Note 2): D package	97°C/W
P package	85°C/W
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. All voltage values, except differential I/O bus voltage, are with respect to network ground terminal.
 2. The package thermal impedance is calculated in accordance with JESD 51.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B

DIFFERENTIAL BUS TRANSCEIVERS

SLLS040H – AUGUST 1987 – REVISED JUNE 2000

recommended operating conditions (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Supply voltage, V _{CC}		4.75	5	5.25	V
Input voltage at any bus terminal (separately or common mode), V _I or V _{IC}		12			V
		−7			
High-level input voltage, V _{IH}	D, DE, and $\overline{RE}$	2			V
Low-level input voltage, V _{IL}	D, DE, and $\overline{RE}$	0.8			V
Differential input voltage, V _{ID} (see Note 3)		±12			V
High-level output current, I _{OH}	Driver	−60			mA
	Receiver	−400			μA
Low-level output current, I _{OL}	Driver	60			mA
	Receiver	8			
Operating free-air temperature, T _A	SN65ALS176	−40		85	°C
	SN75ALS176 series	0		70	

NOTE 3: Differential input/output bus voltage is measured at the noninverting terminal A with respect to the inverting terminal B.



POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040H – AUGUST 1987 – REVISED JUNE 2000

DRIVER SECTION

electrical characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IK} Input clamp voltage	$I_I = -18 \text{ mA}$				-1.5	V
V_O Output voltage	$I_O = 0$		0		6	V
$ V_{OD1} $ Differential output voltage	$I_O = 0$		1.5		6	V
$ V_{OD2} $ Differential output voltage	$R_L = 100 \Omega$,	See Figure 1	$1/2 V_{OD1}$ or $2^{\S}$			V
	$R_L = 54 \Omega$,	See Figure 1	1.5	2.5	5	V
V_{OD3} Differential output voltage	$V_{test} = -7 \text{ V to } 12 \text{ V}$,	See Figure 2	1.5		5	V
$\Delta V_{OD} $ Change in magnitude of differential output voltage¶	$R_L = 54 \Omega$ or 100Ω ,	See Figure 1			± 0.2	V
V_{OC} Common-mode output voltage	$R_L = 54 \Omega$ or 100Ω ,	See Figure 1			3 -1	V
$\Delta V_{OC} $ Change in magnitude of common-mode output voltage¶	$R_L = 54 \Omega$ or 100Ω ,	See Figure 1			± 0.2	V
I_O Output current	Outputs disabled (see Note 4)	$V_O = 12 \text{ V}$			1	mA
		$V_O = -7 \text{ V}$			-0.8	
I_{IH} High-level input current	$V_I = 2.4 \text{ V}$				20	μA
I_{IL} Low-level input current	$V_I = 0.4 \text{ V}$				-400	μA
I_{OS} Short-circuit output current#	$V_O = -4 \text{ V}$	SN65ALS176			-250	mA
	$V_O = -6 \text{ V}$	SN75ALS176			-250	
	$V_O = 0$				-150	
	$V_O = V_{CC}$				250	
	$V_O = 8 \text{ V}$				250	
I_{CC} Supply current	No load	Outputs enabled		23	30	mA
		Outputs disabled		19	26	

† The power-off measurement in TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.

‡ All typical values are at $V_{CC} = 5 \text{ V}$ and $T_A = 25^\circ\text{C}$.

§ The minimum V_{OD2} with a $100\text{-}\Omega$ load is either $1/2 V_{OD1}$ or 2 V , whichever is greater.

¶ $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC} , respectively, that occur when the input is changed from one logic state to the other.

Duration of the short circuit should not exceed one second for this test.

NOTE 4: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B

DIFFERENTIAL BUS TRANSCEIVERS

SLLS040H – AUGUST 1987 – REVISED JUNE 2000

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

SN65ALS176

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
t _d (OD) Differential output delay time	R _L = 54 Ω, C _L = 50 pF, See Figure 3			15	ns
t _{sk} (p) Pulse skew [‡]	R _L = 54 Ω, C _L = 50 pF, See Figure 3		0	2	ns
t _{sk} (lim) Pulse skew [§]	R _L = 54 Ω, C _L = 50 pF, See Figure 3			15	ns
t _t (OD) Differential output transition time	R _L = 54 Ω, C _L = 50 pF, See Figure 3		8		ns
t _{PZH} Output enable time to high level	R _L = 110 Ω, C _L = 50 pF, See Figure 4			80	ns
t _{PZL} Output enable time to low level	R _L = 110 Ω, C _L = 50 pF, See Figure 5			30	ns
t _{PHZ} Output disable time from high level	R _L = 110 Ω, C _L = 50 pF, See Figure 4			50	ns
t _{PLZ} Output disable time from low level	R _L = 110 Ω, C _L = 50 pF, See Figure 5			30	ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] Pulse skew is defined as the |t_{pLH} – t_{pHL}| of each channel of the same device.

[§] Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER	TEST CONDITIONS	MIN	TYP [†]	MAX	UNIT
t _d (OD) Differential output delay time	R _L = 54 Ω, C _L = 50 pF, See Figure 3	3	8	13	ns
		4	7	11.5	
		5	8	10	
t _{sk} (p) Pulse skew [‡]	R _L = 54 Ω, C _L = 50 pF, See Figure 3		0	2	ns
t _{sk} (lim) Pulse skew [§]	R _L = 54 Ω, C _L = 50 pF, See Figure 3			10	ns
				7.5	
				5	
t _t (OD) Differential output transition time	R _L = 54 Ω, C _L = 50 pF, See Figure 3		8		ns
t _{PZH} Output enable time to high level	R _L = 110 Ω, C _L = 50 pF, See Figure 4		23	50	ns
t _{PZL} Output enable time to low level	R _L = 110 Ω, C _L = 50 pF, See Figure 5		14	20	ns
t _{PHZ} Output disable time from high level	R _L = 110 Ω, C _L = 50 pF, See Figure 4		20	35	ns
t _{PLZ} Output disable time from low level	R _L = 110 Ω, C _L = 50 pF, See Figure 5		8	17	ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] Pulse skew is defined as the |t_{pLH} – t_{pHL}| of each channel of the same device.

[§] Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

SYMBOL EQUIVALENTS

DATA-SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V _O	V _{0a} , V _{0b}	V _{0a} , V _{0b}
V _{OD1}	V ₀	V ₀
V _{OD2}	V _t (R _L = 100 Ω)	V _t (R _L = 54 Ω)
V _{OD3}	None	V _t (test termination measurement 2)
Δ V _{OD}	V _t – V _{tl}	V _t – V _{tl}
V _{OC}	V _{os}	V _{os}
Δ V _{OC}	V _{os} – V _{os}	V _{os} – V _{os}
I _{OS}	I _{sa} , I _{sb}	None
I _O	I _{xa} , I _{xb}	I _{ia} , I _{ib}



SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040H – AUGUST 1987 – REVISED JUNE 2000

RECEIVER SECTION

electrical characteristics over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
V_{IT+} Positive-going input threshold voltage	$V_O = 2.7\text{ V}$,	$I_O = -0.4\text{ mA}$			0.2	V
V_{IT-} Negative-going input threshold voltage	$V_O = 0.5\text{ V}$,	$I_O = 8\text{ mA}$	$-0.2^{\ddagger}$			V
V_{hys} Hysteresis voltage ($V_{IT+} - V_{IT-}$)				60		mV
V_{IK} Enable-input clamp voltage	$I_I = -18\text{ mA}$				-1.5	V
V_{OH} High-level output voltage	$V_{ID} = 200\text{ mV}$, See Figure 6	$I_{OH} = -400\text{ }\mu\text{A}$,	2.7			V
V_{OL} Low-level output voltage	$V_{ID} = -200\text{ mV}$, See Figure 6	$I_{OL} = 8\text{ mA}$,			0.45	V
I_{OZ} High-impedance-state output current	$V_O = 0.4\text{ V to }2.4\text{ V}$				± 20	μA
V_I Line input current	Other input = 0 V (see Note 5)	$V_I = 12\text{ V}$			1	mA
		$V_I = -7\text{ V}$			-0.8	
I_{IH} High-level-enable input current	$V_{IH} = 2.7\text{ V}$				20	μA
I_{IL} Low-level-enable input current	$V_{IL} = 0.4\text{ V}$				-100	μA
r_I Input resistance			12	20		$\text{k}\Omega$
I_{OS} Short-circuit output current	$V_{ID} = 200\text{ mV}$,	$V_O = 0$	-15		-85	mA
I_{CC} Supply current	No load	Outputs enabled		23	30	mA
		Outputs disabled		19	26	

[†] All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.

[‡] The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.

NOTE 5: This applies for power on and power off. Refer to TIA/EIA-485-A for exact conditions.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B

DIFFERENTIAL BUS TRANSCEIVERS

SLLS040H – AUGUST 1987 – REVISED JUNE 2000

switching characteristics over recommended ranges of supply voltage and operating free-air temperature range (unless otherwise noted)

SN65ALS176

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
t _{pd}	Propagation time	V _{ID} = –1.5 V to 1.5 V, See Figure 7	C _L = 15 pF,			25	ns
t _{sk(p)}	Pulse skew [§]	V _{ID} = –1.5 V to 1.5 V, See Figure 7	C _L = 15 pF,		0	2	ns
t _{sk(lim)}	Pulse skew [¶]	R _L = 54 Ω, See Figure 3	C _L = 50 pF,			15	ns
t _{PZH}	Output enable time to high level	C _L = 15 pF,	See Figure 8		11	18	ns
t _{PZL}	Output enable time to low level	C _L = 15 pF,	See Figure 8		11	18	ns
t _{PHZ}	Output disable time from high level	C _L = 15 pF,	See Figure 8			50	ns
t _{PLZ}	Output disable time from low level	C _L = 15 pF,	See Figure 8			30	ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[§] Pulse skew is defined as the |t_{PLH} – t_{PHL}| of each channel of the same device.

[¶] Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

SN75ALS176, SN75ALS176A, SN75ALS176B

PARAMETER		TEST CONDITIONS		MIN	TYP [†]	MAX	UNIT
t _{pd}	Propagation time	V _{ID} = –1.5 V to 1.5 V, See Figure 7	C _L = 15 pF,	9	14	19	ns
				10.5	14	18	
				11.5	13	16.5	
t _{sk(p)}	Pulse skew [‡]	V _{ID} = –1.5 V to 1.5 V, See Figure 7	C _L = 15 pF,		0	2	ns
t _{sk(lim)}	Pulse skew [§]	R _L = 54 Ω, See Figure 3	C _L = 50 pF,			10	ns
						7.5	
						5	
t _{PZH}	Output enable time to high level	C _L = 15 pF,	See Figure 8		7	14	ns
t _{PZL}	Output enable time to low level	C _L = 15 pF,	See Figure 8		20	35	ns
t _{PHZ}	Output disable time from high level	C _L = 15 pF,	See Figure 8		20	35	ns
t _{PLZ}	Output disable time from low level	C _L = 15 pF,	See Figure 8		8	17	ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] Pulse skew is defined as the |t_{PLH} – t_{PHL}| of each channel of the same device.

[§] Skew limit is the maximum difference in propagation delay times between any two channels of any two devices.

PARAMETER MEASUREMENT INFORMATION

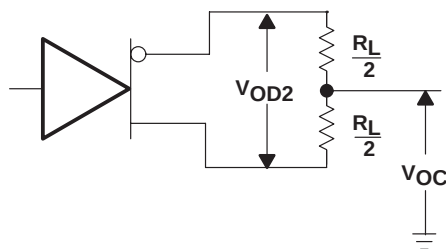


Figure 1. Driver V_{OD2} and V_{OC}

PARAMETER MEASUREMENT INFORMATION

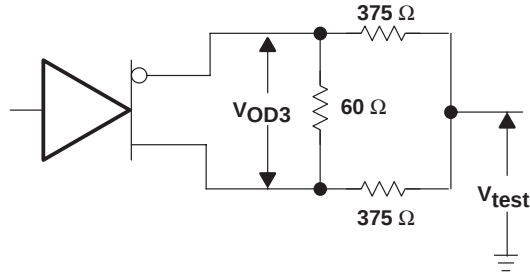
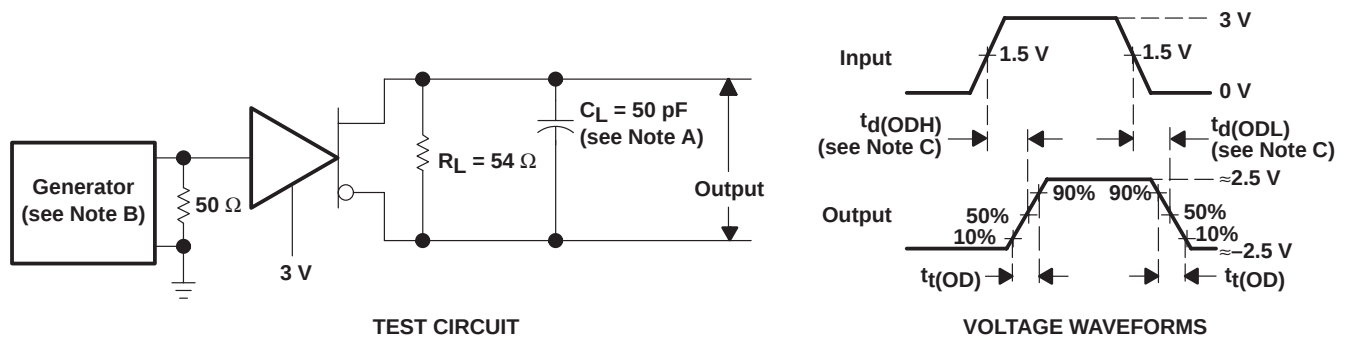
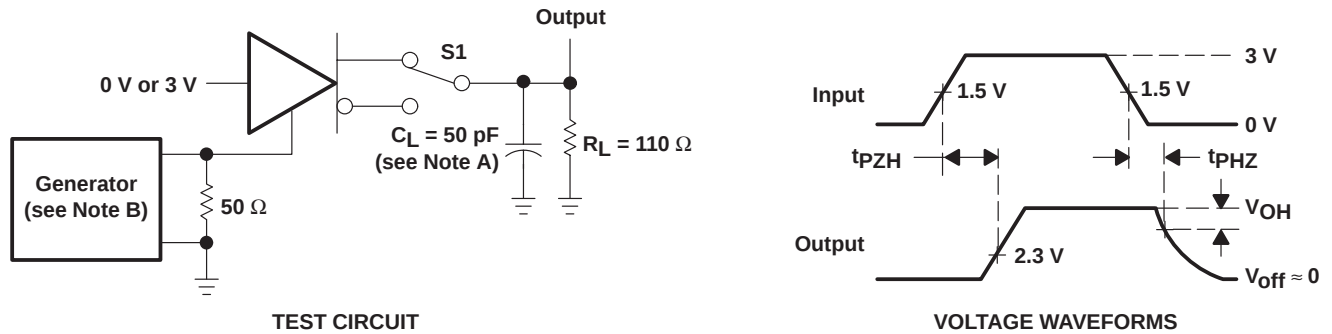


Figure 2. Driver V_{OD3}



- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.
C. $t_d(OD) = t_d(ODH)$ or $t_d(ODL)$

Figure 3. Driver Test Circuit and Voltage Waveforms



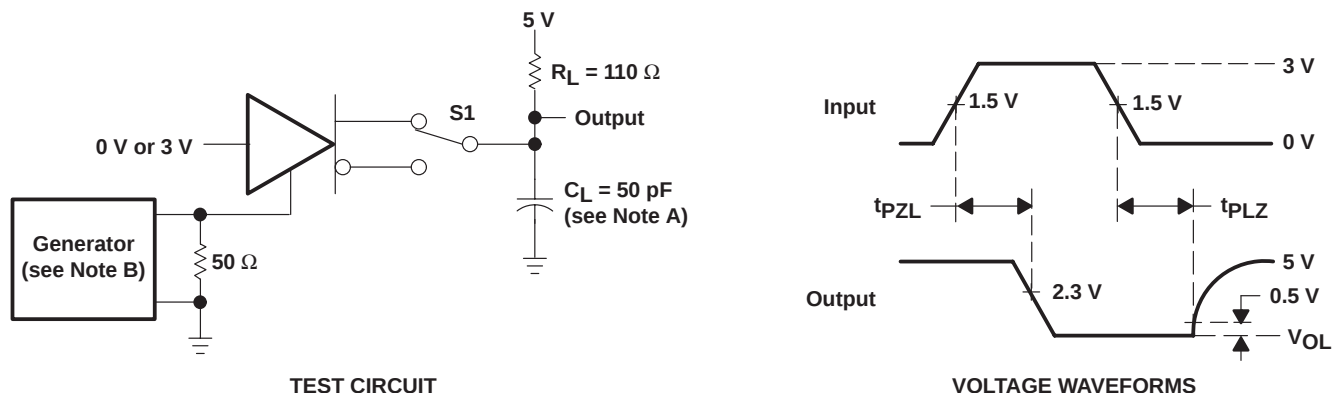
- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 4. Driver Test Circuit and Voltage Waveforms

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040H – AUGUST 1987 – REVISED JUNE 2000

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.

Figure 5. Driver Test Circuit and Voltage Waveforms

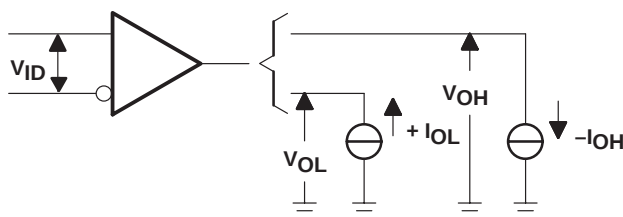
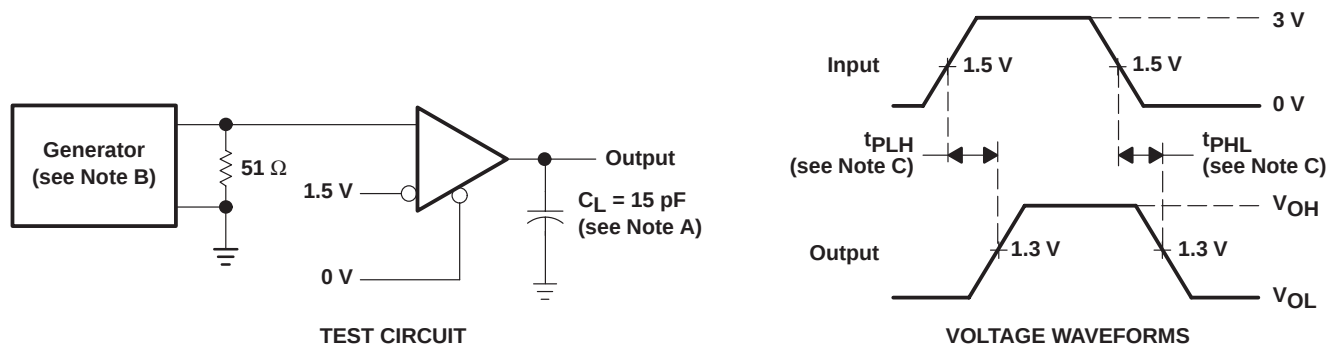


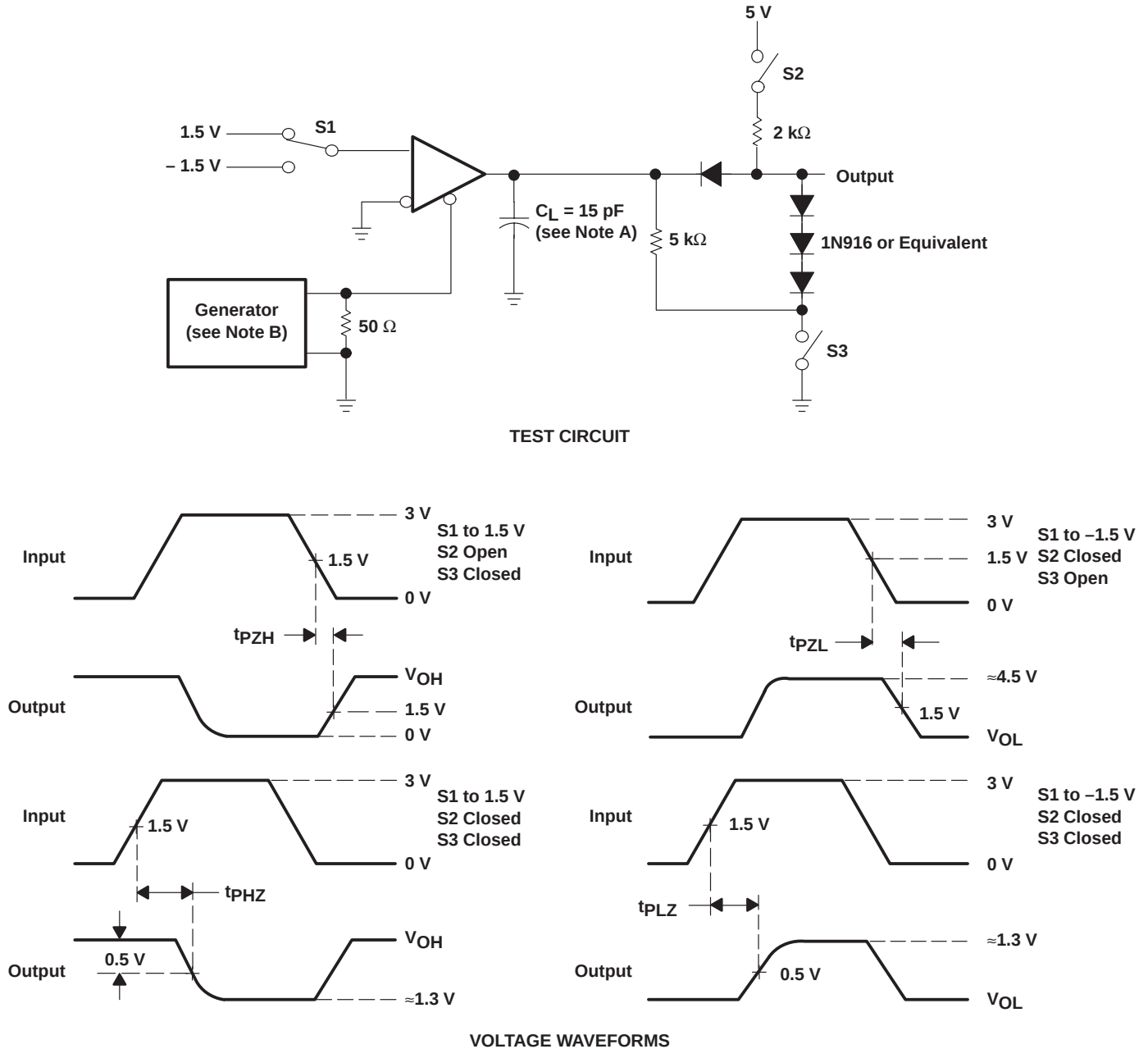
Figure 6. Receiver V_{OH} and V_{OL} Test Circuit



- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: $PRR \leq 1$ MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_0 = 50 \Omega$.
C. $t_{pd} = t_{PLH}$ or t_{PHL}

Figure 7. Receiver Test Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, $t_r \leq 6$ ns, $t_f \leq 6$ ns, $Z_O = 50 \Omega$.

Figure 8. Receiver Test Circuit and Voltage Waveforms

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B
DIFFERENTIAL BUS TRANSCEIVERS

SLLS040H – AUGUST 1987 – REVISED JUNE 2000

TYPICAL CHARACTERISTICS†

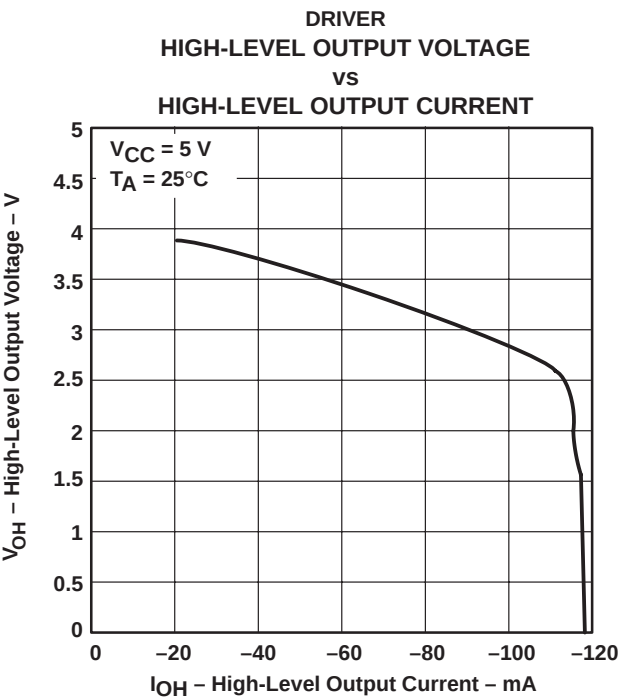


Figure 9

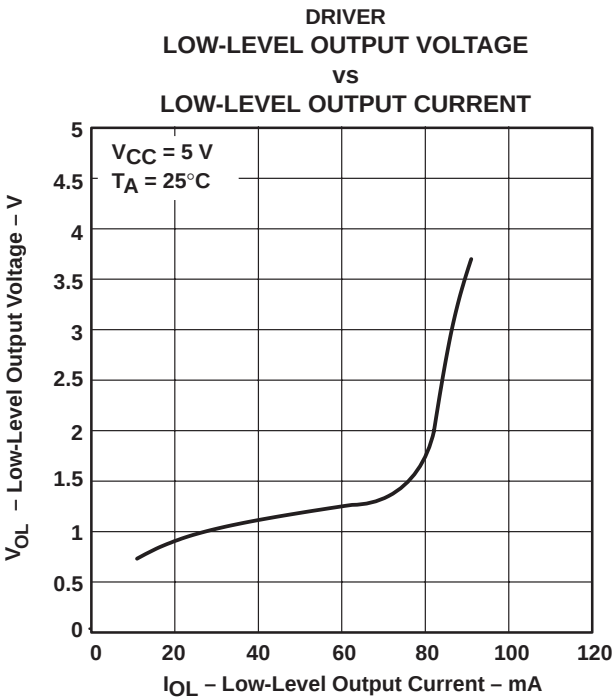


Figure 10

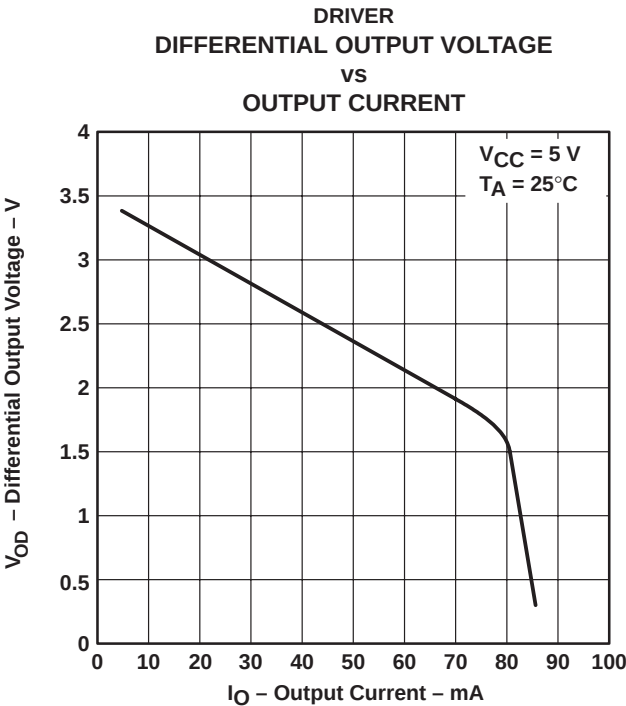


Figure 11

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B DIFFERENTIAL BUS TRANSCEIVERS

SLLS040H – AUGUST 1987 – REVISED JUNE 2000

RECEIVER TYPICAL CHARACTERISTICS†

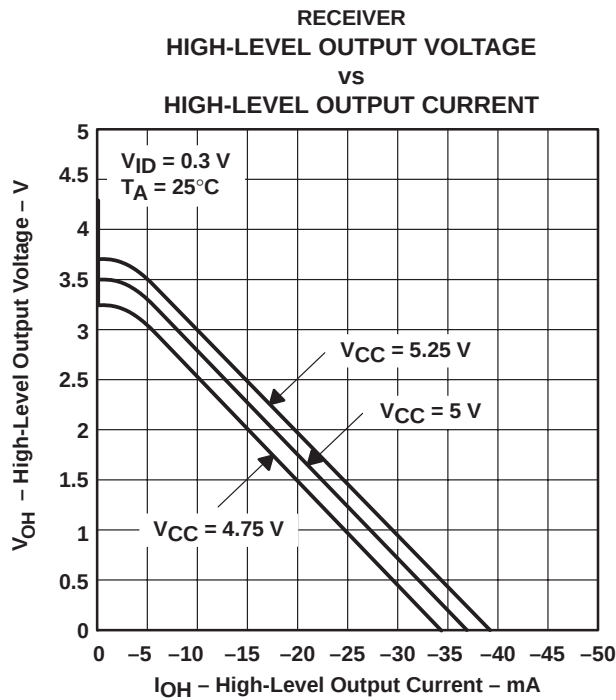


Figure 12

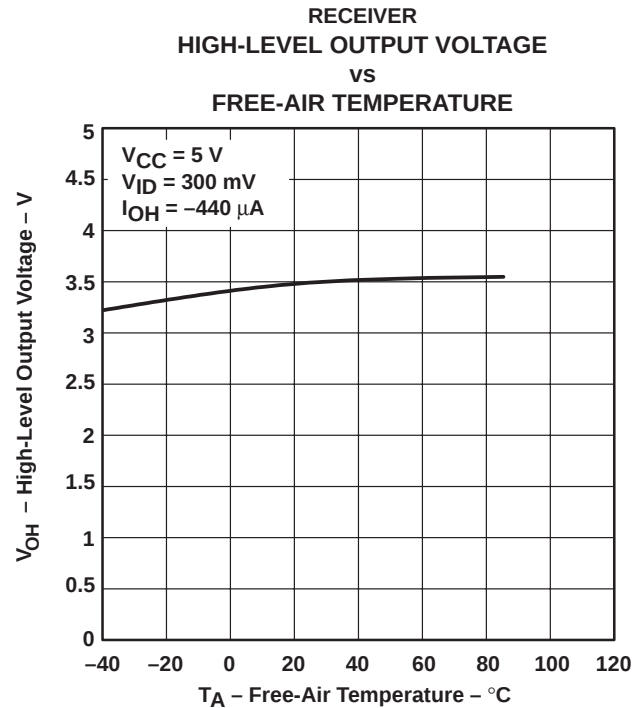


Figure 13

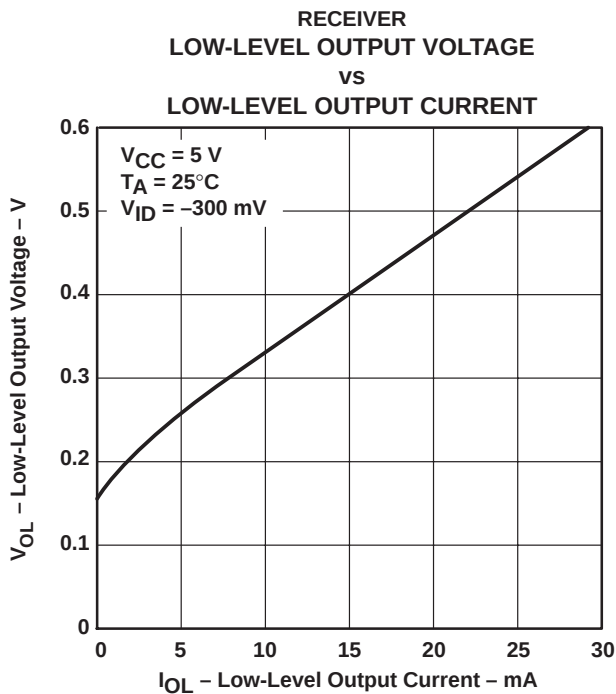


Figure 14

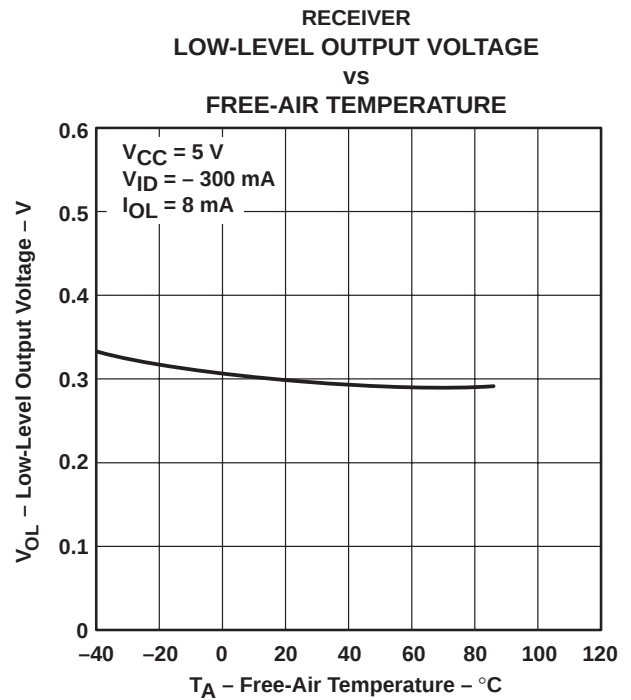


Figure 15

† Operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

SN65ALS176, SN75ALS176, SN75ALS176A, SN75ALS176B
DIFFERENTIAL BUS TRANSCEIVERS

SLLS040H – AUGUST 1987 – REVISED JUNE 2000

TYPICAL CHARACTERISTICS†

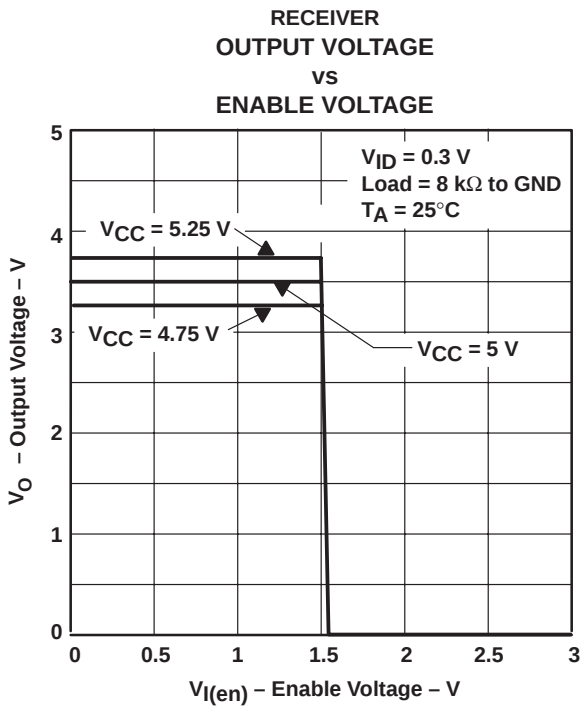


Figure 16

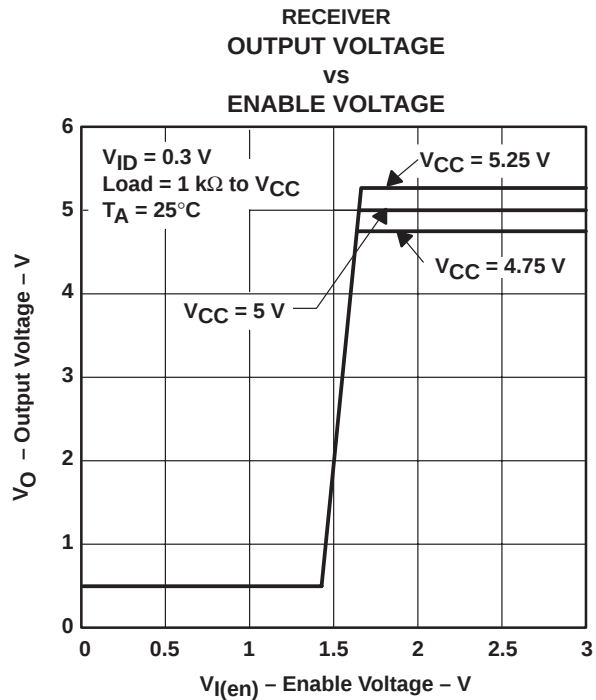
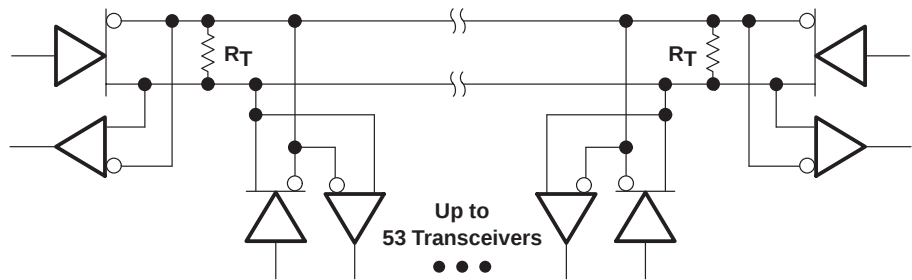


Figure 17

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

APPLICATION INFORMATION



NOTE A: The line should terminate at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 18. Typical Application Circuit

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN65ALS176D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65ALS176DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65ALS176DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN65ALS176DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65ALS176DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN65ALS176DRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN65ALS176P	OBSOLETE	PDIP	P	8		TBD	Call TI	Call TI
SN75ALS176AD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS176ADE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS176ADR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS176ADRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS176AP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75ALS176APE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75ALS176BD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS176BDE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS176BDG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN75ALS176BDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS176BDRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS176BDRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1YEAR
SN75ALS176BP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75ALS176BPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75ALS176D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS176DE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS176DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN75ALS176DRE4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN75ALS176P	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC
SN75ALS176PE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	Level-NC-NC-NC

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

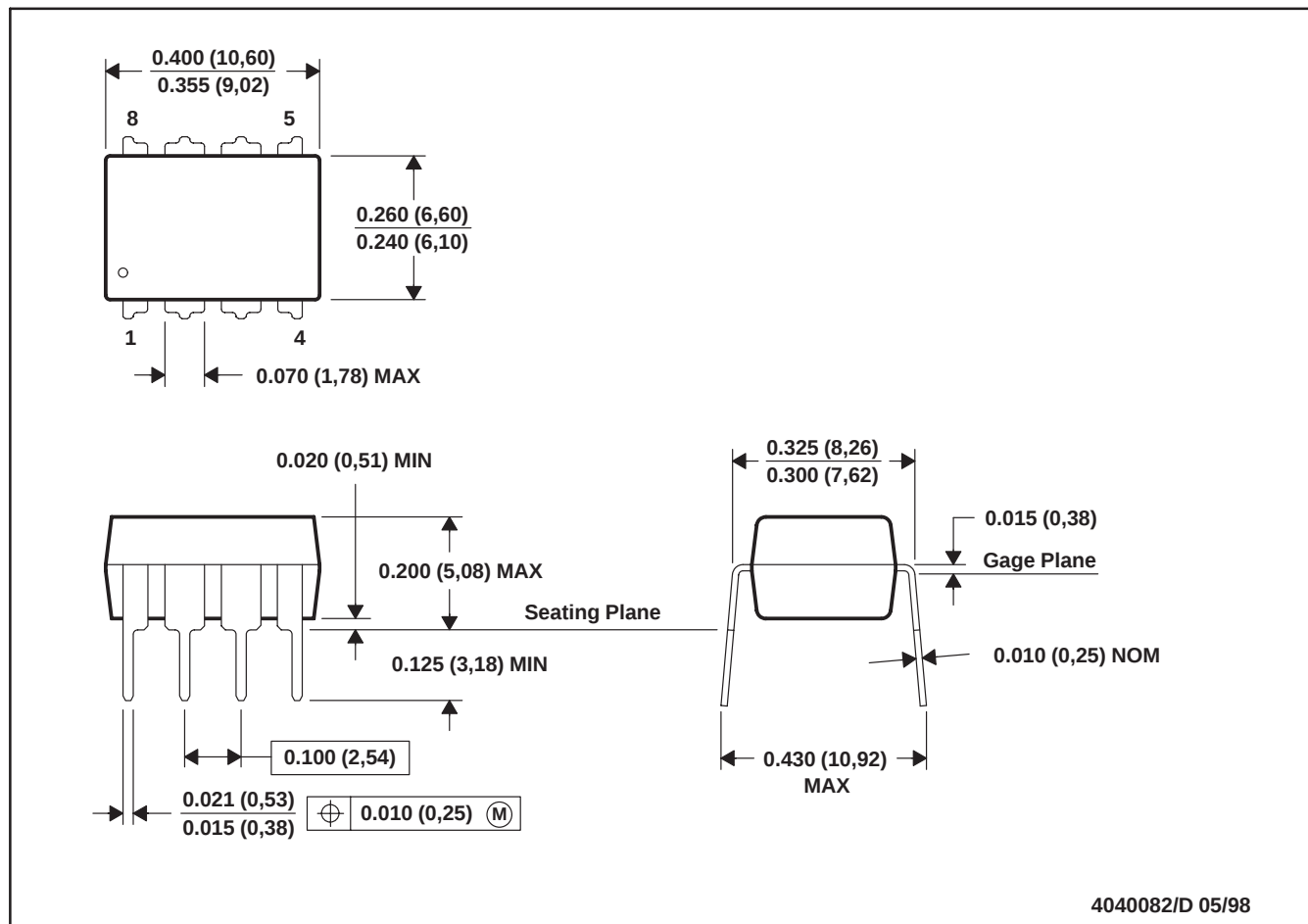
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE

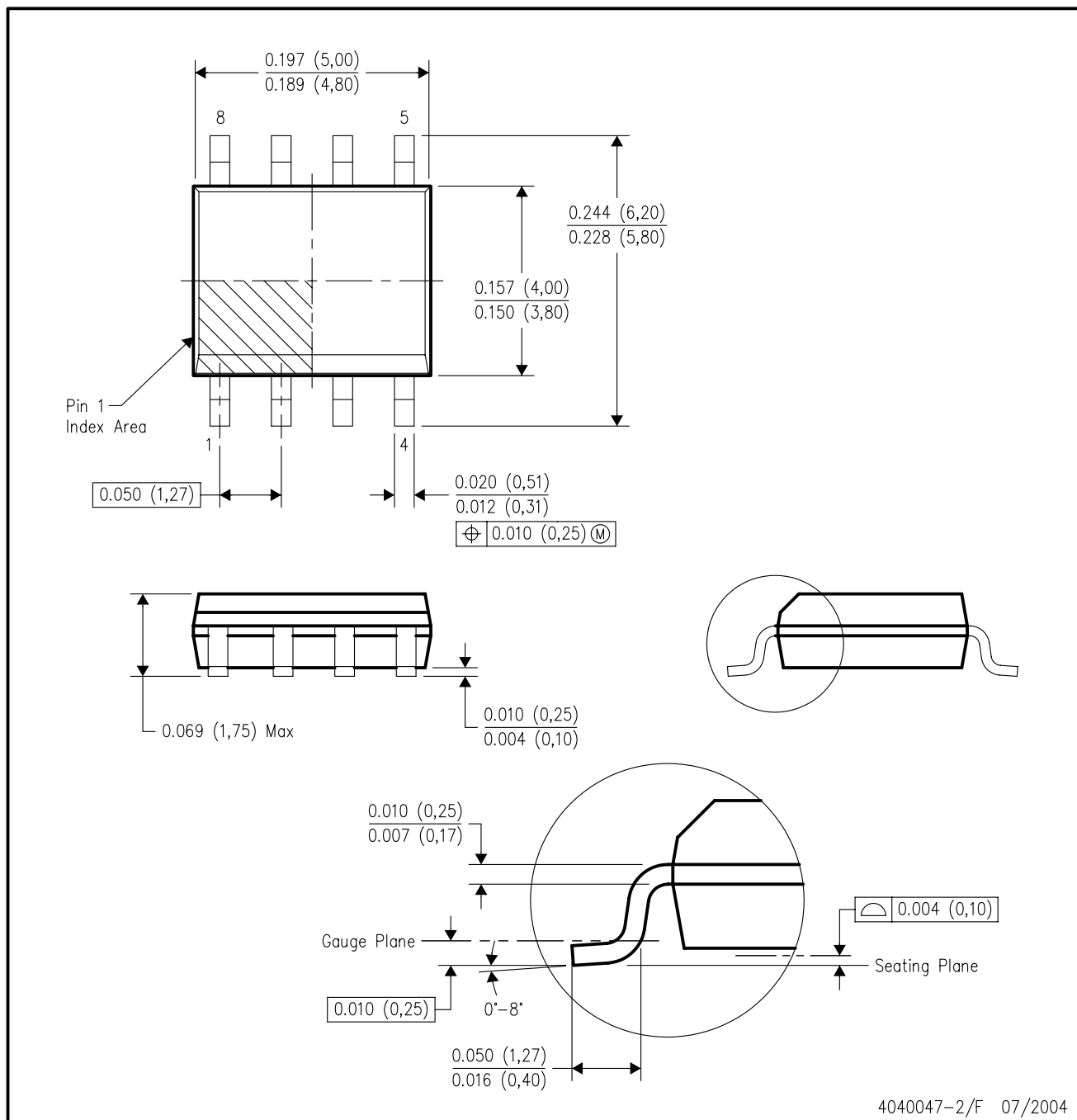


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MS-001

For the latest package information, go to http://www.ti.com/sc/docs/package/pkg_info.htm

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-012 variation AA.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		Applications	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
		Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265

Copyright © 2005, Texas Instruments Incorporated