

MOPS/cdGX1

Product Manual

Document Revision 1.6

CONTENTS

<u>1.</u>	<u>USER INFORMATION</u>	1
1.1	<u>ABOUT THIS MANUAL</u>	1
1.2	<u>COPYRIGHT NOTICE</u>	1
1.3	<u>TRADEMARKS</u>	2
1.4	<u>STANDARDS</u>	2
1.5	<u>WARRANTY</u>	2
1.6	<u>TECHNICAL SUPPORT</u>	3
<u>2.</u>	<u>INTRODUCTION</u>	4
<u>3.</u>	<u>SPECIFICATIONS</u>	5
3.1	<u>FUNCTIONAL SPECIFICATIONS</u>	5
3.2	<u>MECHANICAL SPECIFICATIONS</u>	7
3.3	<u>ELECTRICAL SPECIFICATIONS</u>	7
3.4	<u>ENVIRONMENTAL SPECIFICATIONS</u>	7
<u>4.</u>	<u>CPU, CHIPSET, AND SUPER I/O</u>	9
4.1	<u>CPU</u>	9
4.2	<u>CHIPSET</u>	9
4.3	<u>SUPER I/O</u>	10
<u>5.</u>	<u>SYSTEM MEMORY</u>	11
5.1	<u>CONNECTOR (X1)</u>	11
<u>6.</u>	<u>ISA EXPANSION</u>	12
6.1	<u>CONNECTORS (X2A AND X2B)</u>	12
6.2	<u>CONFIGURATION</u>	13
6.3	<u>ADAPTER CARD MOUNTING</u>	13
<u>7.</u>	<u>USB INTERFACE</u>	14
7.1	<u>CONNECTORS (X6 AND X7)</u>	14
7.2	<u>CONFIGURATION</u>	14
<u>8.</u>	<u>SERIAL-COMMUNICATION INTERFACE</u>	15
8.1	<u>CONNECTORS (X11 AND X12)</u>	15
8.2	<u>CONFIGURATION</u>	15
<u>9.</u>	<u>PARALLEL-COMMUNICATION INTERFACE</u>	16
9.1	<u>CONNECTOR (X15)</u>	16
9.2	<u>CONFIGURATION</u>	17

<u>10. KEYBOARD AND FRONT-PANEL INTERFACE</u>	18
<u>10.1 CONNECTOR (X10)</u>	18
<u>10.2 CONFIGURATION</u>	18
<u>10.3 SIGNAL DESCRIPTIONS</u>	19
<u>10.4 ADAPTER CABLE PINOUT</u>	20
<u>11. PS/2-MOUSE INTERFACE</u>	21
<u>11.1 CONNECTOR (X20)</u>	21
<u>11.2 CONFIGURATION</u>	21
<u>12. FLOPPY-DRIVE INTERFACE</u>	22
<u>12.1 CONNECTOR (X13)</u>	22
<u>12.2 CONFIGURATION</u>	23
<u>13. IDE-CONTROLLER INTERFACE</u>	24
<u>13.1 IDE CONNECTOR (X5)</u>	24
<u>13.2 CONFIGURATION</u>	25
<u>13.3 COMPACTFLASH CONNECTOR (X14)</u>	25
<u>14. CHIPDISK-IDE INTERFACE</u>	26
<u>14.1 CONNECTOR (X5)</u>	27
<u>14.2 CONFIGURATION</u>	27
<u>14.3 SIGNAL DESCRIPTIONS</u>	27
<u>15. ETHERNET-CONTROLLER INTERFACE</u>	30
<u>15.1 CONNECTOR (X17 AND X18)</u>	31
<u>15.2 CONFIGURATION</u>	31
<u>15.3 ETHERNET TECHNICAL SUPPORT</u>	31
<u>16. GRAPHICS-CONTROLLER INTERFACE</u>	32
<u>16.1 FLAT PANEL LVDS (JILI) CONNECTOR (X16)</u>	32
<u>16.2 CONFIGURATION</u>	32
<u>16.3 VGA CONNECTOR (X9)</u>	33
<u>16.4 CONFIGURATION</u>	33
<u>17. OPERATING SYSTEMS</u>	34
<u>18. POWER</u>	35
<u>18.1 VBAT (SYSTEM BATTERY CONNECTION)</u>	35
<u>18.2 CONNECTOR (X2C)</u>	35
<u>19. WATCHDOG TIMER</u>	36
<u>19.1 CONFIGURATION</u>	36

<u>20.</u>	<u>APPENDIX A: SYSTEM-RESOURCE ALLOCATIONS</u>	37
20.1	<u>I/O PORT ASSIGNMENTS</u>	37
20.2	<u>INTERRUPT REQUEST LINES</u>	37
20.3	<u>DIRECT MEMORY ACCESS (DMA) CHANNELS</u>	38
20.4	<u>UPPER MEMORY AREA MAP</u>	38
20.5	<u>PCI DEVICES</u>	38
<u>21.</u>	<u>APPENDIX B: BIOS OPERATION</u>	39
21.1	<u>CONFIGURING THE SYSTEM BIOS</u>	39
21.2	<u>MAIN MENU</u>	41
21.3	<u>ADVANCED MENU</u>	43
21.4	<u>SECURITY MENU</u>	49
21.5	<u>POWER MENU</u>	50
21.6	<u>SETUP BOOT MENU</u>	51
21.7	<u>EXIT MENU</u>	54
21.8	<u>UPDATING OR RESTORING BIOS USING PHOENIX PHLASH</u>	54
<u>22.</u>	<u>APPENDIX C: BLOCK DIAGRAM</u>	57
<u>23.</u>	<u>APPENDIX D: MECHANICAL DIMENSIONS</u>	58
23.1	<u>TOP</u>	58
23.2	<u>BOTTOM</u>	58
<u>24.</u>	<u>APPENDIX E: CONNECTOR LAYOUT</u>	59
24.1	<u>CONNECTOR LAYOUT</u>	59
24.2	<u>CONNECTOR TABLE</u>	59
<u>25.</u>	<u>APPENDIX F: JIDA STANDARD</u>	60
25.1	<u>OBTAINING INFORMATION ABOUT BOARDS THAT USE THE JIDA STANDARD</u>	60
<u>26.</u>	<u>APPENDIX G: PC ARCHITECTURE INFORMATION</u>	61
26.1	<u>BUSES</u>	61
26.2	<u>GENERAL PC ARCHITECTURE</u>	62
26.3	<u>PORTS</u>	62
26.4	<u>PROGRAMMING</u>	63
<u>27.</u>	<u>APPENDIX H: DOCUMENT-REVISION HISTORY</u>	64

1. USER INFORMATION

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Before contacting Kontron Embedded Modules technical support, please consult our Web site for the latest product documentation, utilities, and drivers. If the information does not help solve the problem, contact us by telephone.

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2. INTRODUCTION

The MOPSlcdGX1 provides a complete embedded solution and offers the latest in features and technology. The board uses the National GX1 CPU.

PC/AT subsystems found in desktop units are built into the MOPSlcdGX1. Subsystems include:

- CPU
- System ROM (BIOS)
- Direct memory access (DMA)
- Counters
- Interrupt controllers
- Keyboard
- Motherboard speaker
- Floppy-drive interface
- Integrated Drive Electronics (IDE) hard-disk interface
- Serial ports (COM1 and COM2)
- Parallel port (LPT1)
- Integrated memory controller with up to 4MB unified memory architecture (UMA) for VGA

Additional subsystems integrated into the MOPSlcdGX1 enhance its PC/AT functionality. Subsystems include:

- PS/2 style mouse
- Universal serial bus (USB) ports
- Up to two peripheral component interconnect (PCI) Fast Ethernet chips

3. SPECIFICATIONS

3.1 Functional Specifications

- National Semiconductor Geode GX1 processor
- Bus
 - ◆ 200MHz (33Mhz bus clock)
 - ◆ 266MHz (33Mhz bus clock)
 - ◆ 300MHz (33Mhz bus clock)
- Geode I/O Companion Multifunction South Bridge (CS5530A) chipset
- Winbond W83977AF Super I/O
- 16KB-integrated cache
- Memory
 - ◆ One SO-DIMM socket for 8/16/32/64/128/256MB SDRAM module
- Two serial ports
 - ◆ COM1 and COM2
 - ◆ Transistor-to-transistor logic (TTL) signals only
- One parallel port
 - ◆ LPT1
 - ◆ Extended capabilities port (ECP) and enhanced parallel port (EPP) with bi-directional capability
- Floppy-drive interface
- One PCI Bus Master IDE port support for up to two IDE devices
 - ◆ Ultra 33 DMA mode
 - ◆ Programmable input/output (PIO) modes up to Mode 4 timing
 - ◆ Multiword DMA Mode 0, 1, 2 with independent timing

- Onboard CompactFlash socket
 - ◆ Type 1 only for commercial compact flashes
 - ◆ Master on secondary IDE
 - ◆ Located on bottom of MOPSlcdGX1 board
- USB
 - ◆ Two USB 1.0 ports (OHCI)
 - ◆ USB legacy-keyboard support
- Two Davicom 9102A PCI Ethernet chips
 - ◆ 10BASE-T/100BASE-T LAN
 - ◆ Fast Ethernet, network-interface card (NIC) controller
- Onboard VGA integrated in Geode I/O Companion Multifunction South Bridge (CS5530A) chipset
 - ◆ 2D-graphics accelerator and display controller
 - ◆ Cathode ray tube (CRT) and liquid crystal display (LCD) panel support
 - ◆ Low voltage differential signaling (LVDS): 110MHz channel that uses the JUMPtec Intelligent LVDS Interface (JILI)
 - ◆ Digital signals: using JUMPtec Intelligent Digital Interface (JIDI)
 - ◆ Resolution up to 1280 x 1024 x 8 x 16bpp
 - ◆ Up to 4MB Video RAM based on UMA
- Phoenix Flash BIOS (512KB)
- NV-EEPROM for CMOS setup
- Keyboard controller
- PS/2 mouse interface
- Watchdog timer (WDT)
- Real-time clock (requires external battery)

3.2 Mechanical Specifications

- Mechanical: 96mm x 90mm (3.8" x 3.6")
- Mounting: Two pieces of 2x32 pin-male and 2x20 pin-male connector

3.3 Electrical Specifications

3.3.1 Supply Voltage

When operating a LCD panel, make sure you use a stable power supply, using the following volts:

- 5V DC +/- 5%

3.3.2 Supply Voltage Ripple

- 100mV peak to peak 0-20 MHz

3.3.3 Supply Current

- Typical: 1.2A
- Maximum: 1.2A

3.3.4 External RTC Battery

- External real-time clock (RTC) battery voltage: 2.2 - 3.5V (typ. 3.0V)
- External RTC battery quiescent current: max. 2.4uA

3.4 Environmental Specifications

3.4.1 Temperature

- Operating: 0 to + 60°C((*)with appropriate airflow))
- Nonoperating: -10 to + 85 ° C

(*) The maximum operating temperature is the maximum measurable temperature on any spot on the modules' surface. It is the user's responsibility to maintain this temperature within the above specification.

3.4.2 Humidity

- Operating: 10% to 90% (noncondensing)
- Nonoperating: 5% to 95% (noncondensing)

4. CPU, CHIPSET, AND SUPER I/O

4.1 CPU

National Semiconductor Geode GX1 processor features include:

- Support for Intel's MultiMedia eXtensions (MMX) instruction set extension for acceleration of multimedia applications
- 16KB unified L1 cache
- Advanced Power Management (APM 1.2) for legacy power management
- PCI host controller
- 2D-graphics accelerator and display controller
- Synchronous dynamic random access memory (SDRAM) interface tightly coupled to CPU core and graphics subsystem for maximum efficiency

4.2 Chipset

Geode I/O Companion Multifunction South Bridge (CS5530A) features include:

- 3.3V or 5.0V, PCI-bus compatible
- 5.0V-tolerant I/O interfaces
- PCI-2.1 compliant
- Support for PCI initiator to Industry Standard Architecture (ISA) and ISA master-to-PCI cycle translations
- PCI master for audio I/O and IDE controllers
- PCI-to-ISA interrupt mapper/translator distributed DMA supported
- Two 8259A-equivalent interrupt controllers
- 8254-equivalent timer
- Two 8237-equivalent DMA controllers

- Boot-read only memory (ROM) and keyboard-chip select
- Two controllers with support for up to three IDE devices
- Independent timing for master and slave devices for both channels
- PCI bus master burst reads and writes
- Ultra DMA/33 support
- Two independent USB interfaces
 - ◆ Open-host controller interface (OpenHCI)
 - ◆ Second-generation design

4.3 Super I/O

The Winbond W83977AF Super I/O integrates the following:

- Disk-drive adapter
- Serial port (Universal Asynchronous Receiver/Transmitter [UART])
- Parallel port
- Configurable plug-and-play (PNP) registers for the whole chip

Other features include:

- PNP 1.0A compatible
- Supports 13 interrupt request (IRQ) lines, 4 DMA channels, full 16-bit address decoding
- Sharing ISA-bus IRQs

5. SYSTEM MEMORY

5.1 Connector (X1)

The MOPSlcdGX1 uses only small outline dual inline memory modules (SO-DIMMs). One socket is available for 3.3-volt (power level), unbuffered synchronous dynamic random access memory (SDRAM) of 8, 16, 32, 64, 128, or 256MB.

To find the location of Connector X1 on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

6. ISA EXPANSION

For expansion, the MOPSlcdGX1 provides a PC/104 socket. This industry-standard bus provides ISA bus signals.

6.1 Connectors (X2a and X2b)

X2b is a 64-pin, dual-row socket connector with 0.1" x 0.1" pitch. The connector implements standard, 8-bit, ISA-bus signals. X2a is a 40-pin connector of the same style and implements 16-bit expansion signals on the ISA bus.

To find the location of Connectors X2a and X2b on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

ISA Lower/X2a				ISA Upper/X2b			
Pin #	Signal	Pin #	Signal	Pin #	Signal	Pin #	Signal
A1	IOCHK#	B1	GND	C0	GND	D0	GND
A2	SD7	B2	RESDRV	C1	BHE#	D1	MEMCS16#
A3	SD6	B3	VCC (***)	C2	LA23	D2	IOCS16#
A4	SD5	B4	IRQ9	C3	LA22	D3	IRQ10
A5	SD4	B5	-5V	C4	LA21	D4	IRQ11
A6	SD3	B6	DREQ2	C5	LA20	D5	IRQ12
A7	SD2	B7	-12V	C6	LA19	D6	IRQ15
A8	SD1	B8	WS0#	C7	LA18	D7	IRQ14
A9	SD0	B9	+12V	C8	LA17	D8	DACK0#
A10	IOCHRDY	B10	GND (*)	C9	MEMR#	D9	DREQ0
A11	AEN	B11	SMEMW#	C10	MEMW#	D10	DACK5#
A12	SA19	B12	SMEMR#	C11	SD8	D11	DREQ5
A13	SA18	B13	IOW#	C12	SD9	D12	DACK6#
A14	SA17	B14	IOR#	C13	SD10	D13	DREQ6
A15	SA16	B15	DACK3#	C14	SD11	D14	DACK7#
A16	SA15	B16	DREQ3	C15	SD12	D15	DREQ7
A17	SA14	B17	DACK1#	C16	SD13	D16	VCC (***)
A18	SA13	B18	DREQ1	C17	SD14	D17	IMASTER (**)
A19	SA12	B19	REFSH#	C18	SD15	D18	GND
A20	SA11	B20	SYSCLK	C19	KEY(*)	D19	GND
A21	SA10	B21	IRQ7				
A22	SA9	B22	IRQ6				
A23	SA8	B23	IRQ5				
A24	SA7	B24	IRQ4				
A25	SA6	B25	IRQ3				
A26	SA5	B26	DACK2#				
A27	SA4	B27	TC				
A28	SA3	B28	ALE				
A29	SA2	B29	VCC (***)				
A30	SA1	B30	OSC				
A31	SA0	B31	GND				
A32	GND	B32	GND				

Notes:

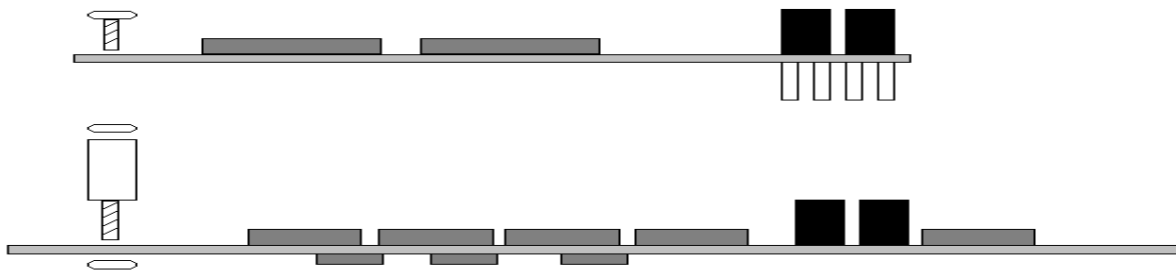
- (*) Key pin for PC/104; GND for PC/104+ specification
 - (**) Not supported on MOPSlcdGX1.
 - (***) To protect external power lines of peripheral devices, make sure that
 - the wires have the right diameter to withstand maximum available current
 - the enclosure of the peripheral device fulfils fire-protecting requirements of IEC/EN 60950.
-

6.2 Configuration

Refer to the [PCI Configuration Submenu](#) in the [Appendix B: BIOS Operation](#) chapter for information on configuraton.

6.3 Adapter Card Mounting

PC/104 adapter cards are mounted in a stack-through manner. Adapter cards are designed with plugs on their undersides that mate with the PC/104 socket connectors of the MOPSlcdGX1. PC/104 adapters can support the socket-connector version on their topside and allow further stacking of adapters.



7. USB INTERFACE

The MOPSlcdGX1 comes with two USB ports, which you can expand by adding external hubs. You can connect up to 127 USB peripherals on each hub.

For more information on USB interfaces, please see the [Appendix G: PC Architecture Information](#) chapter.

7.1 Connectors (X6 and X7)

To find the location of Connectors X6 and X7 on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

Pin	Pin Function
1	+5V
2	USB-
3	USB+
4	GND

Use power contacts on Pin 1 and Pin 4 for internal USB devices only.

Note: Use a fuse to power on external USB connectors.

7.2 Configuration

Refer to the [I/O Device Configuration Submenu](#) in the [Appendix B: BIOS Operation](#) chapter for information on configuraton.

8. SERIAL-COMMUNICATION INTERFACE

The MOPSLcdGX1 has two 16550-compatible serial ports:

- COMA
- COMB

The line drivers used for COMA and COMB conform to the IEEE RS232C standard.

For more information on serial-communication interfaces, please see the [Appendix G: PC Architecture Information](#) chapter.

8.1 Connectors (X11 and X12)

To find the location of Connectors X11 and X12 on the MOPSLcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

COMA (X11) and COMB (X12) (RS232C)				
Pin	Signal Name	In / Out	DSUB-25 (need adapter)	DSUB-9 (need adapter)
1	DCD	In	8	1
2	DSR	In	6	6
3	RxD	In	3	2
4	RTS	Out	4	7
5	TxD	Out	2	3
6	CTS	In	5	8
7	DTR	Out	20	4
8	RI	In	22	9
9	GND	--	7	5
10	VCC (*)	--	--	--

8.2 Configuration

Refer to the [I/O Device Configuration Submenu](#) in the [Appendix B: BIOS Operation](#) chapter for information on configuraton.

9. PARALLEL-COMMUNICATION INTERFACE

The MOPSlcdGX1 supports one parallel port in either extended capabilities port (ECP) or enhanced parallel port (EPP) mode.

For more information on parallel-communication interfaces, please see the [Appendix G: PC Architecture Information](#) chapter.

9.1 Connector (X15)

To find the location of Connector X15 on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

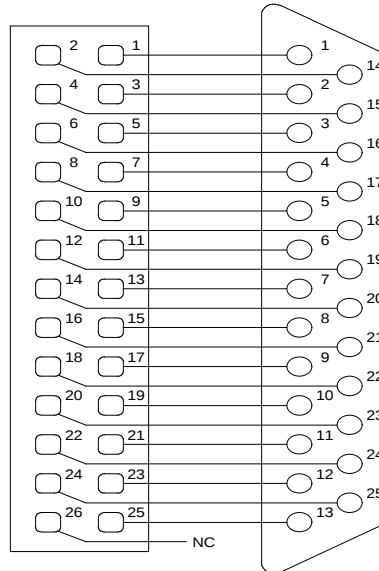
Parallel Port LPT 1 (X15)				
Pin	Signal Name	Function	In / Out	DSUB-25 (need adapter)
1	Strobe#		Out	1
3	Data 0		I/O	2
5	Data 1		I/O	3
7	Data 2		I/O	4
9	Data 3		I/O	5
11	Data 4		I/O	6
13	Data 5		I/O	7
15	Data 6		I/O	8
17	Data 7		I/O	9
19	ACK#		In	10
21	BUSY		In	11
23	PAPER out		In	12
25	SEL out		In	13
2	AUTOFD#		Out	14
4	ERROR#		In	15
6	INIT#		Out	16
8	SEL in		Out	17
26	VCC (*)	+ 5 V	--	NC
10,12	GND	Signal Ground	--	18 - 25
14,16	GND	Signal Ground	--	18 - 25
18,20	GND	Signal Ground	--	18 - 25
22,24	GND	Signal Ground	--	18 - 25

Note: (*) To protect external power lines of peripheral devices, make sure that

- the wires have the right diameter to withstand maximum available current
- the enclosure of the peripheral device fulfils fire-protecting requirements of IEC/EN 60950.

9.1.1 Adapter Cable

You can use an adapter cable to change from the 26-pin header style of the MOPSLcdGX1 to the more common 25-pin female D-sub.



26-pin Header to 25-pin D-Subconversion

9.2 Configuration

The MOPSLcdGX1 parallel ports are bi-directional. The bi-directional functions are compatible with those of a PS/2 style parallel port. The functionality is always available and does not conflict with normal printer use. The parallel-port mode, I/O addresses, and IRQs are defined in the PhoenixBIOS Setup Utility.

Refer to the [I/O Device Configuration Submenu](#) in the [Appendix B: BIOS Operation](#) chapter for information on configuraton.

10. KEYBOARD AND FRONT-PANEL INTERFACE

The keyboard and front-panel interface consists of the following:

- Keyboard
- Reset
- Battery
- Speaker

For more information on keyboard and front-panel interfaces, please see the [Appendix G: PC Architecture Information](#) chapter.

10.1 Connector (X10)

To find the location of Connector X10 on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

Pin	Signal Name	Function	5-pin Diode Keyboard Adapter	6-pin Minidin Keyboard Adapter (PS2)
1	SPKR	Speaker output		
2	GND	Ground		
3	RESIN	Reset input 1		
4	KLOCK#	Keyboard lock		
5	KDATA	Keyboard data	2	1
6	KCLK	Keyboard clock	1	5
7	GND	Ground	4	3
8	VCC (*)	+5V	5	4
9	VBAT	VBAT input (max. 3,3V)		
10	POWERGOOD	Reset input 2		

Note: (*)To protect external power lines of peripheral devices, make sure that:

- wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the fire protecting requirements of IEC/EN 60950.

10.2 Configuration

Refer to the [Keyboard Features Submenu](#) in the [Appendix B: BIOS Operation](#) chapter for information on configuraton.

10.3 Signal Descriptions

10.3.1 KLOCK# (Keyboard Lock)

- Input on CPU modules
- Output on other modules
- Input to keyboard controller: input port 1, bit 7

10.3.2 RESIN (Reset Input 1)

- Input on CPU modules
- Open collector output on all other modules
- When POWERGOOD goes high, it starts the reset generator on the CPU module to pull the onboard reset line high after a valid reset period. You also can use this pin as a low active hardware reset for modules.

10.3.3 SPKR (Speaker Output)

- Open-collector output on modules that can drive a loudspeaker.
- Input on modules that connect an 8-Ohm loudspeaker to this pin.
- An 8-Ohm loudspeaker is connected between SPEAKER and GND. Connect just one loudspeaker to this pin. The CPU usually drives this pin. However, other modules also can use this signal to drive the system loudspeaker.

10.3.4 KDATA (Keyboard Data)

- Bi-directional I/O pin on CPU modules
- Keyboard data signal

10.3.5 KCLK (Keyboard Clock)

- Bi-directional I/O pin on CPU modules
- Keyboard clock signal

10.3.6 VBAT (System Battery Connection)

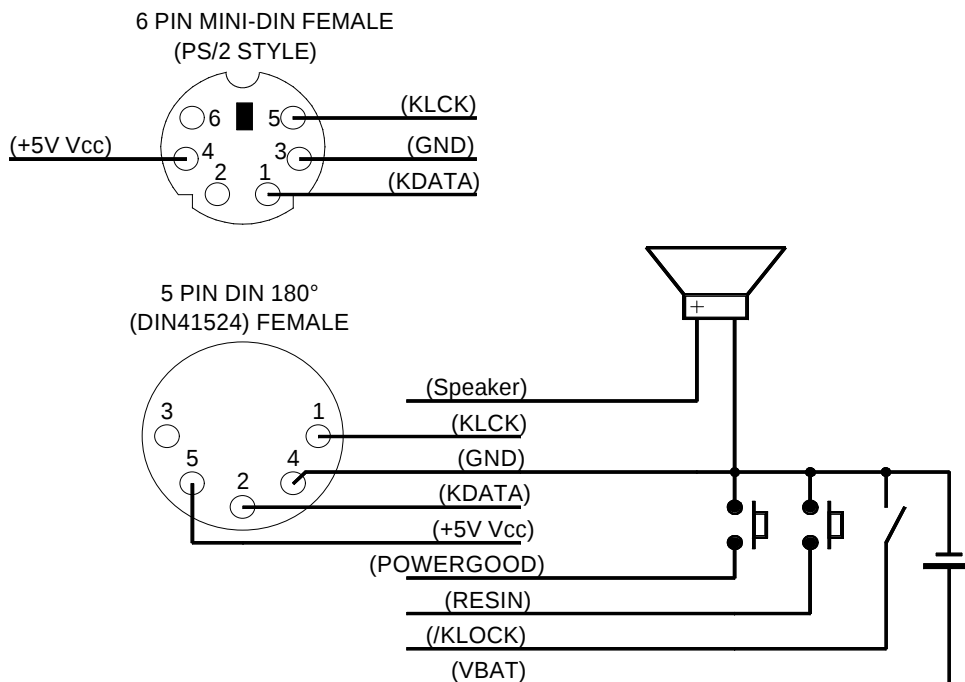
- This pin connects a system battery to all modules.
- The battery voltage has to be higher than 2.85V and lower than 3.15V. Kontron Embedded Modules recommends a 3V battery (for example, CR2032).

Note: There is no battery needed to hold CMOS-setup data. Your configuration information is saved in an onboard Ferroelectric Random Access Memory (FRAM.) However, you need a battery to run the CMOS date and time when power consumption is off.

10.3.7 POWERGOOD (Reset Input 2)

- Input on CPU modules
- Open collector output on all other modules
- When POWERGOOD goes high, it starts the reset generator on the CPU module to pull the onboard reset line high after a valid reset period. You also can use this pin as a low active hardware reset for modules.

10.4 Adapter Cable Pinout



11. PS/2-MOUSE INTERFACE

11.1 Connector (X20)

To find the location of Connector X20 on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

Pin	Signal Name	Function
1	MSDAT	PS/2 mouse data
2	VCC*	Power 5V
3	GND	Power ground
4	MSCLK	PS/2 mouse clock

Note: (*)To protect the external power lines of peripheral devices, make sure that:

- wires have the right diameter to withstand the maximum available current.
- the enclosure of the peripheral device fulfils the requirements for fire protection as recommended in IEC/EN 60950.

11.2 Configuration

Refer to the [Advanced Menu](#) in the [Appendix B: BIOS Operation](#) chapter for information on configuraton.

12. FLOPPY-DRIVE INTERFACE

The floppy-drive interface can support one 3.5" drive, using the adapter cable ADA-Floppy 2, (Kontron Embedded Modules part number 96001-0000-00-0).

The board can support the following drive capacities:

- 720K
- 1.44M
- 2.88M

For more information on floppy-drive interfaces, please see the [Appendix G: PC Architecture Information](#) chapter.

12.1 Connector (X13)

To find the location of Connector X13 on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

Signal	Function	Pin	Signal	Function
VCC (*)	+ 5V	2	IDX	Index
VCC (*)	+ 5V	4	DS0	Drive select 0
VCC (*)	+ 5V	6	DCHNG#	Disk change
NC	-	8	NC	-
NC	-	10	Mo0	Motor on
NC	-	12	DIR	Direction select
NC	-	14	STEP	Step
GND	Ground	16	WD	Write data
GND	Ground	18	WG	Write gate
GND	Ground	20	TR00	Track 00
GND	Ground	22	WP	Write protect
GND	Ground	24	RD	Read data
GND	Ground	26	SIDE	Side one select

Note: (*)To protect the external power lines of peripheral devices, make sure that:

- wires have the right diameter to withstand the maximum available current
- the enclosure of the peripheral device fulfils the requirements for fire protection as outlined in IEC/EN 60950.

12.2 Configuration

Specify the drive type using the PhoenixBIOS Setup Utility.

Choices for the 3.5" drive type include:

- 720KB
- 1.44MB
- 2.44MB
- None

You can disable the floppy-disk interface from the PhoenixBIOS Setup Utility.

Refer to the [Advanced Menu](#) in the [Appendix B: BIOS Operation](#) chapter for information on configuraton.

13. IDE-CONTROLLER INTERFACE

PCI-bus devices serve as primary and secondary IDE hosts on the MOPSlcdGX1. BIOS automatically configures them, but you can disable them by using the BIOS Setup Utility. Resources used by primary and secondary IDE host adapters are compatible with the PC/AT.

The IDE controller supports the following modes:

- Ultra 33 DMA mode
- PIO modes up to Mode-4 timing
- Multiword DMA Mode 0, 1, 2 with independent timing

Use a master/slave daisy chain when connecting two devices to a single adapter.

For more information on IDE-controller interfaces, please see the [Appendix G: PC Architecture Information](#) chapter.

13.1 IDE Connector (X5)

The IDE connector is a 44-pin, dual in-line, 2mm-pitch, male header.

To find the location of Connector X5 on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

IDE Connector for 2.5 " Hard Disk (X5)			
Pin	Signal	Pin	Signal
1	RESET#	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	NC
21	NC	22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27	RDY	28	NC
29	ACK	30	GND
31	IRQ14	32	NC
33	SA1	34	NC
35	SA 0	36	SA2

IDE Connector for 2.5 " Hard Disk (X5)			
Pin	Signal	Pin	Signal
37	CS0#	38	CS1#
39	NC	40	GND
41	VCC	42	VCC
43	GND	44	NC

13.2 Configuration

You can connect one or two IDE drives to the header by using an appropriate flat-ribbon cable.

1. Configure the first drive as master.
2. Configure the second drive (at the end of the cable) as slave.
3. Consult your disk-drive manual for instructions.

The IDE interface offers several potential configuration settings. Refer to the [I/O Device Configuration Submenu](#) in the [Appendix B: BIOS Operation](#) chapter for information on configuraton.

13.3 CompactFlash Connector (X14)

A CompactFlash socket for commercial CompactFlashes (Type I) is integrated on the bottom side of the MOPSlcdGX1 board.

13.3.1 Configuration

You can use the CompactFlash card as a master device on the secondary IDE port.

Refer to the [I/O Device Configuration Submenu](#) in the [Appendix B: BIOS Operation](#) chapter for information on configuraton.

14. CHIPDISK-IDE INTERFACE

As an option, you can add Kontron Embedded Modules' *chipDISK-IDE* to the MOPSlcdGX1 board. However, the boards support just two IDE drives on the interface. You can use one *chipDISK-IDE* and one hard disk or CD-ROM.

The *chipDISK-IDE* provides high-capacity, solid-state, Flash memory that is electrically compatible with an IDE disk drive. *ChipDISK-IDE* modules provide up to 192 MB of formatted storage capacity. A *chipDISK* has no mechanical parts.

The Flash Chipset (FCS) on *chipDISK-IDE* consists of two chips:

- A highly integrated flash controller
- One to three memory modules

The *chipDISK-IDE* controller provides a true IDE compatible interface to the host computer. The controller manages interfacing to the host system, data storage and retrieval, as well as electrical connectivity checks (ECC), defect handling and diagnostics and power management. The controller manages all defects and errors and makes the Flash memory appear as perfect memory to the host. After the *chipDISK* has been configured, it appears to the host as an IDE disk drive. The *chipDISK-IDE* is an IDE-compatible disk, which you plug into a 2.5"-IDE connector. Features include:

- Direct plug in for 2.5" IDE connectors
- Very low power CMOS operation and ultra low power standby modes
- 5V +/- 10% supply voltage
- No formatting and installation software needed
- 50-bit Reed Solomon ECC
- Automatic error correction and retry
- Automatic sleep mode
- 0°C to 60°C operating temperature range
- 44-pin, 2mm-IDE connector

See the *chipDISK-IDE* manual on the Kontron Embedded Modules Web site for more information.

14.1 Connector (X5)

To find the location of Connector X5 on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

Pin	Signal	Pin	Signal
1	Reset#	2	GND
3	D7	4	D8
5	D6	6	D9
7	D5	8	D10
9	D4	10	D11
11	D3	12	D12
13	D2	14	D13
15	D1	16	D14
17	D0	18	D15
19	GND	20	
21		22	GND
23	IOW#	24	GND
25	IOR#	26	GND
27		28	
29		30	GND
31	IRQ	32	IOCS16#
33	HA1	34	PDIAG#
35	HA0	36	HA2
37	IDECS0	38	IDEC/S1
39	SLV/ACT	40	GND
41	VCC	42	VCC
43	GND	44	

14.2 Configuration

Refer to the [Main Menu](#) in the [Appendix B: BIOS Operation](#) chapter for information on configuraton.

14.3 Signal Descriptions

14.3.1 Reset#

Input low active

Reset signal from the host system that is active low during power up and inactive thereafter.

14.3.2 GND / VCC

Power ground.

14.3.3 D[0:15]

Input / output

16-bit bi-directional data bus between the host and the drive. The lower eight bits, D0:D7, are used for register and error-correction code (ECC) access. All 16 bits are used for data transfers.

14.3.4 IOW#

Input low active

Write strobe, the rising edge of which clocks data from the host data bus, D0:D15, into a register of the *chipDISK*.

14.3.5 IOR#

Input low active

Read strobe, which when low enables data from a register of the *chipDISK* onto the host data bus, D0:D15.

14.3.6 IRQ

Output tri state

Interrupt to the host system.

The interrupt is enabled only when:

- *chipDISK* is selected
- Host activates the —IEN bit as active high
- Drive is not selected

This output is in a high impedance state regardless of the state of the IRQ bit. The interrupt is set when the IRQ bit is set by the *chipDISK*. IRQ is reset to zero by a host read of the status register or a write to the command register.

14.3.7 IOCS16#

Output tri state

Indication to the host system that the 16 bit data register has been addressed and that the *chipDISK* is prepared to send or receive a 16-bit data word.

14.3.8 PDIAG#

Input / output

Passed Diagnostic. Output by the *chipDISK* if it is the slave drive. Input to the *chipDISK* if it is the master drive. This low active signal indicates to a master that the slave has passed its internal diagnostic command. This signal is only high during the execution of the internal diagnostic command.

14.3.9 HA[0:2]

Input

Binary-coded address used to select the individual registers in the task file of the *chipDISK*.

14.3.10 IDECS0

Input

Chip-select input from the host system. Used to select some of the host-accessible registers.

14.3.11 IDECS1

Input

Chip-select input from the host system. Used to select three of the registers in the task file.

14.3.12 SLVI/ACT

Output

Signal from the *chipDISK* to:

- Drive a LED whenever the *chipDISK* is accessed
- Indicate a second drive present

This signal is active low when the *chipDISK* is busy.

15. ETHERNET-CONTROLLER INTERFACE

The MOPSlcdGX1 on-board Ethernet interfaces uses two Davicom DM9102A PCI Fast Ethernet Controllers. The network controllers support a 10/100Base-T interface. The device auto-negotiates the use of a 10Mbit/sec or 100Mbit/sec connection.

All major network-operating systems and several real-time and embedded-operating systems support the interface.

The DM9102A provides:

- Integrated Fast Ethernet MAC, Physical Layer, and transceiver in one chip
- Compliance with PCI specification 2.2
- PCI bus-master architecture
- EEPROM 93C46 interface supports node-ID, access-configuration information
- Compliance with IEEE 802.3u 100Base-TX and 802.3 10Base-T
- Compliance with IEEE 802.3u auto-negotiation protocol for automatic link-type selection
- Full-duplex/half-duplex capability
- Supports IEEE 802.3x full duplex flow control
- Digital-clock recovery circuit using advanced digital algorithm to reduce jitter
- High-performance 100Mbps-clock generator and data-recovery circuit
- Provides loopback mode for easy system diagnostics

15.1 Connector (X17 and X18)

To find the location of Connectors X17 and X18 on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

15.1.1 Connector Pinout

Pin#	Signal Name	Function	In/Out
1	TXD+ ¹	100/10BASE-T Transmit	Differential Output
2	TXD- ¹	100/10BASE-T Transmit	Differential Output
3	RXD+ ²	100/10BASE-T Receive	Differential Input
4	NC	Unused Pin	
5	NC	Unused Pin	
6	RXD- ²	100/10BASE-T Receive	Differential Input
7	NC	Unused Pin	
8	NC	Unused Pin	

Notes:

¹TXD+, TXD- Differential output pair drives 10 and 100Mb/s Manchester-encoded data to the 100/10BASE-T transmit lines.

²RXD+, RXD- Differential input pair receives 10 and 100Mb/s Manchester-encoded data from the 100/10BASE-T receive lines.

15.2 Configuration

You can configure the on-board PCI Ethernet interface via the PhoenixBIOS Setup Utility. You can assign it to an available I/O and IRQ location.

Refer to the [Ethernet Configuration Submenu](#) in the [Appendix B: BIOS Operation](#) chapter for additional information on configuraton.

15.3 Ethernet Technical Support

You can solve some Ethernet problems by using the latest drivers for the DAVICOM DM9102A controller. Kontron Embedded Modules provides you with the latest tested drivers, which can differ from newer ones.

For further technical support, contact either Kontron Embedded Modules or get support information and download software updates from DAVICOM.

16. GRAPHICS-CONTROLLER INTERFACE

The Geode I/O Companion Multifunction South Bridge (CS5530A) chipset incorporates extensions to the GX1 processor's display subsystem. These include:

- Video accelerator
 - ◆ Buffers and formats input luminance-bandwidth-chrominance (YUV) video data from processor
 - ◆ 8-bit interface to the GXLV processor
 - ◆ X & Y scaler with bilinear filter
 - ◆ Color space converter (YUV to RGB)
- Video Overlay Logic
 - ◆ Color key
 - ◆ Data switch for graphics and video data
 - ◆ Gamma RAM
 - ◆ Brightness and contrast control
- Display Interface
 - ◆ Integrated RGB Video digital-to-analog converters (DACs)
 - ◆ VESA DDC2B/DPMS support
 - ◆ Flat-panel interface (simultaneous operation of CRT and LCD)
- Supported Resolutions (CRT and LCD)
 - ◆ The display controller on the MOPSlcdGX1 supports resolutions for CRT and LCD panels (only JILI) up to 1280x1024x8 bpp and 1024x768x16 bpp.
 - ◆ On the flat panel digital interface (JIDI), displays up to 640x480x18 bpp can be used.

16.1 Flat Panel LVDS (JILI) Connector (X16)

The user interface for flat panels is the JUMPtec Intelligent LVDS Interface (JILI). The implementation of this subsystem complies with the JILI Specification.

To find the location of Connector X16 on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

16.2 Configuration

For information on configuring JILI, call Kontron Embedded Modules for documentation and information.

16.3 VGA Connector (X9)

To find the location of Connector X9 on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

Pin	Signal Name	Function	DSUB15 (Need Adapter)
1	RED	Analog Video Red	1
2	GREEN	Analog Video Green	2
3	BLUE	Analog Video Blue	3
4	GND	Signal Ground	5, 6, 7, 8, 10
5	VSYNC	Vertical Sync	14
6	HSYNC	Horizontal Sync	13

16.4 Configuration

Refer to the [Advanced Chipset Control Submenu](#) in the [Appendix B: BIOS Operation](#) chapter for information on configuraton.

17. OPERATING SYSTEMS

The MOPSlcdGX1 is compatible with the following operating systems (OS):

- DOS
- Linux
- Most PC-compatible RTOS
- Windows CE, Window 9x, and Windows NT

18. POWER

The MOPSlcdGX1 uses +5V-only modules. You have the choice of using +12V, -12V, and -5V, which may be necessary for other boards in the PC/104 system.

Power consumption of all available power pins on the MOPSlcdGX1 is limited to 5A in total (1A per pin, with two pins on the power connector, two pins on the XT-bus, and one pin on the AT-bus) and at GND up to 8A. Systems consuming more than 2A should not be served over the power connector only. Systems consuming more than 5A must provide power supply through an additional connector on another board.

Note: The MOPSlcdGX1 is not a replacement for a backplane. Use all power pins on the PC/104 connector for power supply to the MOPSlcdGX1, and additional I/O cards. It is not acceptable to use only the power pins of the PC/104 connector for power supply of the full PC/104 stack.

18.1 VBAT (System Battery Connection)

Pin 3 connects a system battery to all modules.

The battery voltage has to be higher than 2.2V and lower than 3.5V. Kontron Embedded Modules recommends a 3V battery (for example, CR2032).

Your configuration is automatically saved in an onboard dynamic random access memory (DRAM). You do need a battery to save the CMOS date and time when the power is off.

18.2 Connector (X2c)

To find the location of Connector X2c on the MOPSlcdGX1 board, please see the [Appendix E: Connector Layout](#) chapter.

Power Connector (X2c)	
Pin	Signal
1	GND
2	+5V
3	VBAT
4	+12V
5	-5V
6	-12V
7	GND
8	+5V

19. WATCHDOG TIMER

The watchdog-timer (WDT) feature is implemented in the Winbond W83977A Super I/O device. You can configure the WDT from the BIOS setup utility to start after a set amount of time after power-on boot. The application software will strobe the WDT to prevent its timeout. Upon timeout, the WDT resets and restarts the system. This provides a way to recover from program crashes or lockups.

19.1 Configuration

You can program the timeout period for the WDT in ranges from 15 seconds to 30 hours and 15 minutes.

Refer to the [Watchdog Settings Submenu](#) in the [Appendix B: BIOS Operation](#) chapter for additional information on configuraton.

Contact Kontron Embedded Modules for information on programming and operating the WDT.

20. APPENDIX A: SYSTEM-RESOURCE ALLOCATIONS

20.1 I/O Port Assignments

Devices on the MOPSlcdGX1 use I/O addresses common to the PC/AT.

20.2 Interrupt Request Lines

The following table describes the allocation of the 16 hardware-interrupt lines for the MOPSlcdGX1.

IRQ #	Primary Use	Available	Comment
0	Timer0	No	
1	Keyboard	No	
2	Cascade	No	
3	COM2	No	Note (1)
4	COM1	No	Note (1)
5	Sound	No	Note (1)
6	FDC	No	Note (1)
7	LPT1	No	Note (1)
8	RTC	No	
9	Free	Yes	
10	Free	Yes	
11	Free	Yes	
12	PS/2 Mouse	No	Note (1)
13	FPU	No	
14	IDE0	No	Note (1)
15	IDE1	No	Note (1)

Notes: ¹ If the "Used For" device is disabled in setup, the corresponding interrupt is available for other devices.

20.3 Direct Memory Access (DMA) Channels

DMA #	Used For	Available
0		Yes
1	Sound	No
2	FDC	No
3	LPT	No
4	Cascade	No
5	Sound	No
6		Yes
7		Yes

Note: ¹ If the “Used For” device is disabled in setup, the corresponding interrupt is available for other devices.

20.4 Upper Memory Area Map

Upper Memory	Use	Available
C0000h – CBFFFh	VGA BIOS	No
CC000h – DFFFFh		Yes
E0000h – E5FFFh*		Yes
E6000h – F0000h	System BIOS	No

Note: *The availability of Upper Memory depends upon the BIOS revision. You can check the actual UMA ceiling from the Summary Screen. To do this, enable the Summary Screen from the BIOS setup.

20.5 PCI Devices

PCI Device #	IDSEL #	Use	Device/Vendor ID
South Bridge	REQ0 / GNT0	-	Required for CS5530A
Ethernet1	REQ1 / GNT1	INTA	REQ1/GNT1 available if a CPU board without Ethernet is used
Ethernet2	REQ2 / GNT2	INTB	REQ2/GNT2 available if a CPU board without Ethernet is used
USB Controller	-	INTA	Integrated in CS5530A

21. APPENDIX B: BIOS OPERATION

The MOPSlcdGX1 comes equipped with Phoenix BIOS 4.0, Release 6.1, which is located in the onboard Flash. The BIOS version displays onscreen during the POST at boot. The device has an 8-bit access. The shadow RAM feature offers faster access (16 bit). You can update the BIOS using a Flash utility. For complete Phoenix BIOS 4.0 information, visit the Phoenix Technologies Web site.

21.1 Configuring the System BIOS

The PhoenixBIOS setup utility allows you to change system behavior by modifying the BIOS configuration. Setup-utility menus allow you to make changes and turn features on or off.

BIOS-setup menus represent those found in most models of the MOPSlcdGX1. The BIOS setup utility for specific models can differ slightly.

Note: Selecting incorrect values can cause system boot failure. Load setup-default values to recover by pressing <F9>.

21.1.1 Starting the Setup Utility

To start the PhoenixBIOS setup utility, press <F2> when the following string appears during bootup.

Press <F2> to enter Setup

The Main Menu then appears.

Several sections comprise the **Setup Screen**.

Setup Screen	Location	Function
Menu Bar	Top	Lists and selects all top level menus
Legend Bar	Bottom	Lists setup navigation keys
Item Specific Help Window	Right	Help for selected item
Menu Window	Left Center	Selection fields for current menu
General Help Window	Overlay (center)	Help for selected menu

Menu Bar

The menu bar at the top of the window lists menus. Use the left/right arrow keys to make a selection.

Legend Bar

Use the keys listed in the legend bar on the bottom to make your selections or exit the current menu. The table below describes the legend keys and their alternates.

Key	Function
<F1> or <Alt-H>	General Help window
<Esc>	Exit menu
← or → Arrow key	Select a menu
↑ or ↓ Arrow key	Select fields in current menu
<Tab> or <Shift-Tab>	Cycle cursor up and down
<Home> or <End>	Move cursor to top or bottom of current window
<PgUp> or <PgDn>	Move cursor to next or previous page
<F5> or <->	Select previous value for the current field
<F6> or <+> or <Space>	Select next value for the current field
<F9>	Load the default configuration values for this menu
<F10>	Save and exit
<Enter>	Execute command or select submenu
<Alt-R>	Refresh screen

Selecting an Item

Use the ↑ or ↓ key to move the cursor to the field you want. Then use the + and - keys to select a value for that field. The **Save Value** commands in the **Exit** menu save the values displayed in all the menus.

Displaying Submenus

Use the ← or → key to move the cursor to the submenu you want. Then press <Enter>. A pointer (►) indicates submenus.

Item Specific Help Window

The Help window on the right side of each menu displays the Help text for the selected item. It updates as you move the cursor to each field.

General Help Window

Pressing <F1> or <ALT-F1> on a menu brings up the General Help window that describes legend keys and alternates. Press <Esc> to exit the General Help window.

21.2 Main Menu

Feature	Option	Description
System Time	HH:MM:SS	Sets the system time. Use <Enter> to move to MM or SS.
System Date	MM/DD/YYYY	Set the system date. Use <Enter> to move to DD or YYYY.
Legacy Diskette A	360 kB, 5 ¼" 1.2 MB, 5 ¼" 720 kB, 3 ½" 1.44/1.25 MB, 3 ½" 2.88 MB, 3 ½" Disabled	Select the type of floppy disk drive.
Legacy Diskette B	360 kB, 5 ¼" 1.2 MB, 5 ¼" 720 kB, 3 ½ " 1.44/1.25 MB, 3 ½ " 2.88 MB, 3 ½ " Disabled	Select the type of floppy disk drive.
▸ Primary Master	Autodetected drive	Displays result of PM autotyping.
▸ Primary Slave	Autodetected drive	Displays result of PS autotyping.
▸ Compact Flash	Autodetected drive	Displays result of SM autotyping.
System Memory	N/A	Displays amount of conventional memory detected during bootup.
Extended Memory	N/A	Displays amount of extended memory detected during bootup.

Note: In the **Option** column, **bold** shows default settings.

21.2.1 Primary Master, Primary Slave, and CompactFlash Submenus

Feature	Option	Description
Type	None User Auto CD-ROM ATAPI Removable Other ATAPI	None = Autotyping is unable to supply the drive type or end user has selected None, disabling any drive that may be installed. User = End user supplies hdd information. Auto = Autotyping, drive supplies information.
Cylinders	1 to 65,536	Number of cylinders.
Heads	1 to 256	Number of read/write heads.
Sectors	1 to 63	Number of sectors per track.
Maximum Capacity	N/A	Displays calculated size of the drive in CHS
Total Sectors	N/A	Displays total number of sectors in LBA
Maximum Capacity	N/A	Displays calculated size of drive in LBA
Multisector Transfer	Disabled Standard 2 sectors	Any selection except Disabled determines the number of sectors transferred per block.

Feature	Option	Description
	4 sectors 8 sectors 16 sectors	Standard is one sector per block.
LBA Mode Control	Disabled Enabled	Enabling LBA causes Logical Block Addressing to be used in place of CHS.
32-Bit I/O	Disabled Enabled	Enables 32-bit communication between CPU and IDE card. Requires PCI or Local Bus.
Transfer Mode	Standard Fast PIO 1 Fast PIO 2 Fast PIO 3 Fast PIO 4 FPIO3 / DMA1 FPIO4 / DMA2	Selects the method for transferring the data between the hard disk and system memory. Autotype the drive to select the optimum transfer mode.
SMART Device Monitoring	Disabled Enabled	Enables SMART warnings of imminent failure of drive.

Note: In the **Option** column, **bold** shows default settings.

21.3 Advanced Menu

Feature	Option	Description
▸ Advanced Chipset Control	Submenu	Opens Advanced Chipset Control submenu.
Plug & Play (PNP) OS	Yes No	If your system has a PNP OS, such as Win9X, select Yes to let the OS configure PNP devices not required for boot. No makes BIOS configure them.
Secured Setup Configuration	Yes No	Yes prevents a Plug and Play OS from changing system settings.
Reset Configuration Data	No Yes	Yes erases all configuration data in ESCD, which stores the configuration settings for plug-in devices. Select Yes when required to restore the manufacturer's defaults.
▸ PCI Configuration	Submenu	Opens PCI Configuration submenu.
PS/2 Mouse	Autodetect Enabled Disabled	Selecting Disabled prevents installed PS/2 mouse from functioning but frees up IRQ12. Selecting Autodetect frees IRQ12 if no mouse detected.
▸ Keyboard Features	Submenu	Opens keyboard features submenu.
▸ I/O Device Configuration	Submenu	Opens I/O Device Configuration submenu.
Large Disk Access Mode	DOS Other	Select DOS if you have DOS. Select Other if you have another OS, such as UNIX. A large disk has more than 1024 cylinders, more than 16 heads, or more than 63 sectors per track.
Halt On Errors	No Yes	Determines if post errors cause the system to halt.

Note: In the **Option** column, **bold** shows default settings.

21.3.1 Advanced Chipset Control Submenu

Feature	Option	Description
Video Resolution	Low Medium High Super	Determines the UMA memory size for VGA. Higher resolution means more VGA memory and less system memory. Super = 4MB, High = 2.125 MB, Medium = 1.5 MB, Low = 1.25 MB
Multiple Monitor Support	Motherboard Disable Motherboard Primary Adapter Primary	Motherboard Primary enables motherboard graphics for VGA, Adapter Primary enables an external adapter or VGA, Motherboard Disable does not allocate graphics resources.
Display Mode	CRT only LCD only Simultan	Determines display mode.

Note: In the **Option** column, **bold** shows default settings. If Motherboard Disable is enabled and you want to Defaults. To load the Setup Defaults during boot up, press <F2> until you hear a beep and then <F9><Enter> and <F10> <Enter>.

21.3.2 PCI Configuration Submenu

Feature	Option	Description
PCI/PNP ISA UMB Region Exclusion	Submenu	Opens UMB Region Exclusion submenu.
PCI/PNP ISA IRQ Resource Exclusion	Submenu	Opens IRQ Exclusion submenu.
PCI/PNP ISA DMA Resource Exclusion	Submenu	Opens DMA Exclusion submenu.
ISA graphics device installed	No Yes	PCI devices may need to know if an ISA graphics device is installed in the system to enable card to function correctly.

Note: In the **Option** column, **bold** shows default settings.

21.3.3 PCI/PNP ISA UMB Region Exclusion Submenu

Feature	Option	Description
C800 - CBFF	Available Reserved	Reserves specified block of upper memory for legacy ISA devices.
CC00 - CFFF	Available Reserved	Reserves specified block of upper memory for legacy ISA devices.
D000 – D3FF	Available Reserved	Reserves specified block of upper memory for legacy ISA devices.
D400 – D7FF	Available Reserved	Reserves specified block of upper memory for legacy ISA devices.
D800 - DBFF	Available Reserved	Reserves specified block of upper memory for legacy ISA devices.
DC00 - DFFF	Available Reserved	Reserves specified block of upper memory for legacy ISA devices. (Reserved if legacy USB enabled.)

Note: In the **Option** column, **bold** shows default settings.

21.3.4 PCI/PNP ISA IRQ Exclusion Submenu

Feature	Option	Description
IRQ3	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ4	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ5	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ7	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ9	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ10	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ11	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ12	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices.
IRQ14	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices. (Visible if primary IDE disabled).
IRQ15	Available Reserved	Reserves the specified IRQ for use by legacy ISA devices. (Visible if secondary IDE disabled).

Note: In the **Option** column, **bold** shows default settings.

21.3.5 PCI/PNP ISA DMA Exclusion Submenu

Feature	Option	Description
DMA 0	Available Reserved	Reserves specified DMA for legacy ISA devices.
DMA 1	Available Reserved	Reserves specified DMA for legacy ISA devices.
DMA 2	Available Reserved	Reserves specified DMA for legacy ISA devices.
DMA 3	Available Reserved	Reserves specified DMA for legacy ISA devices.
DMA 5	Available Reserved	Reserves specified DMA for legacy ISA devices.
DMA 6	Available Reserved	Reserves specified DMA for legacy ISA devices.
DMA 7	Available Reserved	Reserves specified DMA for legacy ISA devices.

Note: In the **Option** column, **bold** shows default settings.

21.3.6 Keyboard Features Submenu

Feature	Option	Description
Numlock	Auto On Off	On or Off turns NumLock on or off at bootup. Auto turns NumLock on if it finds a numeric keypad.
Key Click	Disabled Enabled	Turns audible key click on.
Keyboard auto-repeat rate	30/sec , 26.7/sec, 21.8/sec, 13.3/sec, 10/sec, 6/sec, 2/sec	Sets the number of times to repeat a keystroke per second if you hold the key down.
Keyboard auto-repeat delay	¼ sec, ½ sec , ¾ sec, 1 sec	Sets the delay time after the key is held down before it begins to repeat the keystroke.

Note: In the **Option** column, **bold** shows default settings.

21.3.7 Ethernet Configuration Submenu

Feature	Option	Description
Onboard Ethernet 1	Enabled Disabled	Enable/Disable onboard Ethernet controller 1
Onboard Ethernet 2	Enabled Disabled	Enable/Disable onboard Ethernet controller 2

Note: In the **Option** column, **bold** shows default settings.

21.3.8 I/O Device Configuration Submenu

Feature	Option	Description
Local Bus IDE adapter	Disabled Primary Secondary Both	Enables onboard PCI IDE device.
Onboard FDC	Disabled Enabled	Enables onboard FDC controller.
External FDC	Disabled Enabled	Enables external FDC controller.
Base I/O address	Primary Secondary	Selects base address of the FDC controller. (Primary = 3F0h, Secondary = 370)
Floppy Drive Swap	Disabled Enabled	Determines whether to swap the Floppy A & B drives.
Serial Port A Serial Port B	Disabled Enabled Auto	Disabled turns off the port. Enabled requires end user to enter the base I/O address and IRQ. Auto makes the BIOS or OS configure the port, depending on PNP OS setting.
Serial Port C Serial Port D	Disabled Enabled Auto	Disabled turns off port. Enabled requires end user to enter base I/O address and IRQ. Auto makes BIOS or OS configure the port, depending on PNP OS setting.
Base I/O address	3F8h, 2F8h, 3E8h, 2E8h	Select I/O base of port.
IRQ (Port A and B)	IRQ 3, IRQ 4	Select IRQ of Port A and B
IRQ (port C and D)	IRQ 10, IRQ 11	Select IRQ of Port C and D
Onboard LPT	Disabled Enabled Auto	Disabled turns off the port. Enabled requires end user to enter base I/O address and the IRQ. Auto makes the BIOS or OS configure the port, depending on PNP OS setting.
External LPT	Disabled Enabled Auto	Disabled turns off the port. Enabled requires end user to enter base I/O address and the IRQ. Auto makes the BIOS or OS configure the port, depending on PNP OS setting.
Mode	Output only Bi-directional ECP EPP	Set the mode for the parallel port.
Base I/O address	378h, 278h, 3BCh	Select I/O base of port.
IRQ	IRQ 5, IRQ 7	Select IRQ of parallel port.
DMA	DMA1, DMA3	Select DMA channel of port if in ECP mode.
Mode	Output only Bi-directional EPP	Sets the mode for the parallel port on the backplane. ECP is not supported.
Base I/O address	378h , 278h, 3BCh	Select I/O base of LPT port on backplane.

Feature	Option	Description
IRQ	<i>IRQ 5, IRQ 7</i>	Select IRQ of parallel port on backplane.
USB Host Controller	Disabled Enabled	Enable or disable onboard USB controller.
USB BIOS Legacy Support	Disabled Enabled	Enable or disable support for USB keyboard and mice. Enable for use with non-USB aware OSes such as UNIX and DOS.
Watchdog Settings	Submenu	Opens WDT Settings submenu.

Notes:

The options noted in *italics* are only visible if an additional I/O controller (SMSC669) is on the OEM backplane.

Options noted in **bold** and **bold italics** are default settings.

The FDC and LPT settings marked with an asterisk (*) are mutually exclusive. Drive swap is enabled automatically to get to Drive A.

If legacy USB is enable, IRQ1 and IRQ2 do not wake the system from standby or suspend state; the UMB region DC000h-E3FFFh is reserved.

21.3.9 Watchdog Settings Submenu

Feature	Option	Description
Mode	Disabled Reset	Select watchdog operation mode.
Timeout	15s, 45s, 1:15m, 2:15m, 5:15m, 10:15m, 30:15m	Max. trigger period.

Note: In the **Option** column, **bold** shows default settings.

21.4 Security Menu

Feature	Option	Description
Set User Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives restricted access to setup.
Set Supervisor Password	Up to seven alphanumeric characters	Pressing <Enter> displays the dialog box for entering the user password. In related systems, this password gives full access to setup.
Password on boot	Disabled Enabled	Enabled requires a password on boot. Requires prior setting of the supervisor password. If supervisor password is set and this option is disabled, BIOS assumes user is booting.
Diskette access	User Supervisor	Enabled requires supervisor password to access floppy disk.
Fixed disk boot sector	Normal Write protected	Write-protect the boot sector on the hard disk for virus protection. Requires a password to format or Fdisk the hard disk.
Virus check reminder	Disabled Daily Weekly Monthly	Displays a message during boot-up asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with Y. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and monthly on the first boot of the month.
System backup reminder	Disabled Daily Weekly Monthly	Displays a message during boot-up asking (Y/N) if you backed up the system or scanned for viruses. Message returns on each boot until you respond with Y. Daily displays the message on the first boot of the day, Weekly on the first boot after Sunday, and monthly on the first boot of the month.

Notes: In the **Option** column, **bold** shows default settings.

Enabling Supervisor Password requires a password for entering Setup.

Passwords are not case sensitive.

User and Supervisor passwords are related.

You can only create a User password if a Supervisor password is first created.

21.5 Power Menu

A power-management system reduces the amount of energy used after specified periods of inactivity. The setup menu supports:

- Full-on state
- Standby state with partial power reduction
- Suspend state with full power reduction

Feature	Option	Description
Power Savings	Disabled Enabled	Disabled turns off all power management.
Standby Timeout	Off, 1min, 2min, 4min , 5min, 10min, 20min, 30min, 1hour	Inactivity period required to put system in Standby mode (partial power shutdown).
Auto Suspend Timeout	Off, 1min, 2min, 4min , 5min, 10min, 20min, 30min, 1hour	Inactivity period required after Standby to Suspend mode (maximum power shutdown).
Hard Disk Timeout	Off , 1min, 2min, 4min, 5min, 10min, 20min, 30min, 1hour	Inactivity period of hard disk required before standby (motor off).
Activity Event	Submenu	Opens Activity Event submenu.

Note: In the **Option** column, **bold** shows default settings.

21.5.1 Activity Event Submenu

Feature	Option	Description
IRQ1	Yes No	Wakes up system on IRQ1 (Keyboard).
IRQ12	Yes No	Wakes up system on IRQ1 (PS/2 Mouse).
IRQ3, 4, 5, 7, 9, 10, 11	Yes No	Wakes up system on IRQ.

Note: If legacy USB is enabled, IRQ1 and IRQ12 do not wake system from standby or suspend state.

21.6 Setup Boot Menu

Feature	Option	Description
Floppy Check	Disabled Enabled	Enabled verifies floppy type on boot. Disabled speeds boot.
Summary Screen	Disabled Enabled	Displays system configuration on boot.
QuickBoot Mode	Disabled Enabled	Allows the system to skip certain tests while booting. This will decrease the time needed to boot the system.
Dark Boot	Disabled Enabled	Enables the QuietBoot feature.
Boot Device Priority	Submenu	Opens Boot Device Priority submenu.
Onboard LAN RPL ROM	Disabled Enabled	Enables the remote boot BIOS extension for the onboard LAN controller.

Notes: In the Option column, **bold** represents the default settings.

If the onboard LAN RPL ROM is enabled, the LAN-boot ROM asks during bootup which LAN-boot option to use.

21.6.1 QuietBoot

Upon turn on or reset, QuietBoot displays a black screen as the default or a graphical logo instead of a text-based POST screen, which displays diagnostic messages.

The graphical logo is visible until just before the OS-load unless:

- <Esc> is pressed to display the POST screen
- <F2> is pressed to enter Setup
- POST issues an error message
- BIOS or option ROM requests keyboard input

21.6.2 MultiBoot

Multiboot allows you to select the following boot device:

- Hard disk
- Floppy disk
- CD-ROM

- Network card

You can make the selections from the BIOS utility setup, or by selecting the boot device in the **BootFirst Menu**.

MultiBoot consists of the following menus:

- Setup Boot
- Boot Device Priority
- Removable Devices
- Hard Drive
- Network Boot Priority
- Boot First

21.6.3 Boot Device Priority Submenu

This menu allows you to select the order of the devices from which the BIOS attempts to boot the OS. During POST, if BIOS is unsuccessful at booting from one device, it will try the next one on the list.

The items on this menu each may represent the first of a class of items. For example, if you have more than one hard disk drive, Hard Drive represents the first of such drives as specified in the Hard Drive menu described below.

To change the order, select the device you want to change and press <-> to decrease or <+> to increase priority.

Feature	Option	Description
▸ Hard Drive	Boot priority and submenu	Sets boot priority of Hard Disks as described in the respective submenu.
▸ Removable Devices	Boot priority and submenu	Sets boot priority of Removable Devices as described in the respective submenu.
ATAPI CD-ROM Drive	Boot priority	Sets boot priority of ATAPI CD-ROM Drives.
▸ Network Boot	Boot priority and submenu	Sets boot priority of Network Adapters as described in respective submenu.

Hard Drive Submenu

If there is more than one bootable hard drive, select **Hard Drive** and press <Enter> to display Fixed Disk Menu and choose a boot priority.

Removable Devices Submenu

If there is more than one Removable Media drive, select **Removable Devices** and press <Enter> to display the Removable Media menu and choose which drive is represented in the boot-order menu.

Note: The standard 1.44MB floppy drive is referenced as Legacy Floppy Drives.

Network Boot Submenu

If there is more than one bootable network adapter in the system, select **Network Boot** and press <Enter> to display available network adapters and choose the boot priority.

21.6.4 Boot First Menu

Display the **Boot First Menu** by pressing <Esc> during POST. In response, the BIOS displays the message `Entering Boot Menu` and then displays the Boot Menu at the end of POST.

Use the menu to select a following option:

- Override the existing boot sequence (for this boot only) by selecting another boot device. If the specified device does not load the OS, the BIOS reverts to previous boot sequence.
- Enter Setup.
- Press <Esc> to continue with the existing boot sequence.

21.7 Exit Menu

Feature	Option	Description
Exit Saving Changes	Saves selections and exits setup. The next time the system boots, the BIOS configures the system according to the Setup selection stored in CMOS.	Exit saving changes.
Exit Discarding Changes	Exits Setup without storing in CMOS any new selections you may have made. The selections previously in effect remain in effect.	Exit discarding changes.
Load Setup Defaults	Displays default values for all the Setup menus.	Load setup defaults.
Discard Changes	If, during a Setup session, you change your mind about changes you have made and have not yet saved the values to CMOS, you can restore the values you saved to CMOS.	Discard changes.
Save Changes	Saves all the selection without exiting Setup. You can return to the other menus to review and change your selection.	Save changes.

21.8 Updating or Restoring BIOS Using Phoenix Phlash

Phoenix Phlash allows you to update BIOS using a floppy disk without having to install a new ROM chip. Phoenix Phlash is a utility for flashing a BIOS to the Flash ROM installed on the MOPSlcdGX1.

Use Phoenix Phlash to:

- Update the current BIOS with a newer version
- Restore a corrupt BIOS

21.8.1 Flashing a BIOS

Use the following procedure to update or restore a BIOS.

1. Download the Phoenix Phlash compressed file, CRISPGX1.ZIP, from the Kontron Embedded Modules Web site. It contains the following files:

File	Purpose
MAKEBOOT.EXE	Creates the custom boot sector on the Crisis Recovery Diskette.
CRISBOOT.BIN	Serves as the Crisis Recovery boot sector code.
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH.EXE	Programs the flash ROM.
WINCRISIS.EXE	Creates the Crisis Recovery Diskette from Windows.
WINCRISIS.HLP	Serves as the help file of WINCRISSES.EXE.
PLATFORM.BIN	Performs platform-dependent functions.
BIOS.ROM	Serves as the actual BIOS image to be programmed into Flash ROM.

2. Install Phoenix Phlash on a hard disk by unzipping the content of CRISPGX1.ZIP into a local directory such as C:\PHLASH.
3. Create a Crisis Recovery Diskette by inserting a blank diskette into Drive A: or B: and execute WINCRISIS.EXE. This copies four files onto the diskette.

File	Purpose
MINIDOS.SYS	Allows the system to boot in Crisis Recovery Mode.
PHLASH.EXE	Programs the flash ROM.
PLATFORM.BIN	Performs platform-dependent functions.
BIOS.ROM	Serves as the actual BIOS image to be programmed into Flash ROM.

4. If the BIOS image (BIOS.ROM) changes due to an update or bug fix, copy the new BIOS.ROM image (PGX1R119.ROM) onto the diskette.

Phoenix Phlash runs in one of two modes:

- ☛ Command line mode
- ☛ Crisis recovery mode

5. Use the command line mode to update or replace a BIOS. To execute Phlash in this mode, move to the Crisis Recovery Disk and type:

```
PHLASH PGX1R110.ROM
```

Phoenix Phlash will update the BIOS. Phlash can fail if the system uses memory managers. If this occurs, the utility displays the following message:

```
Cannot flash when memory managers are present.
```

If you have a high-memory manager present, type:

```
PHLASH/X PGX1R110.ROM
```

21.8.2 Preventing Problems When Updating or Restoring BIOS

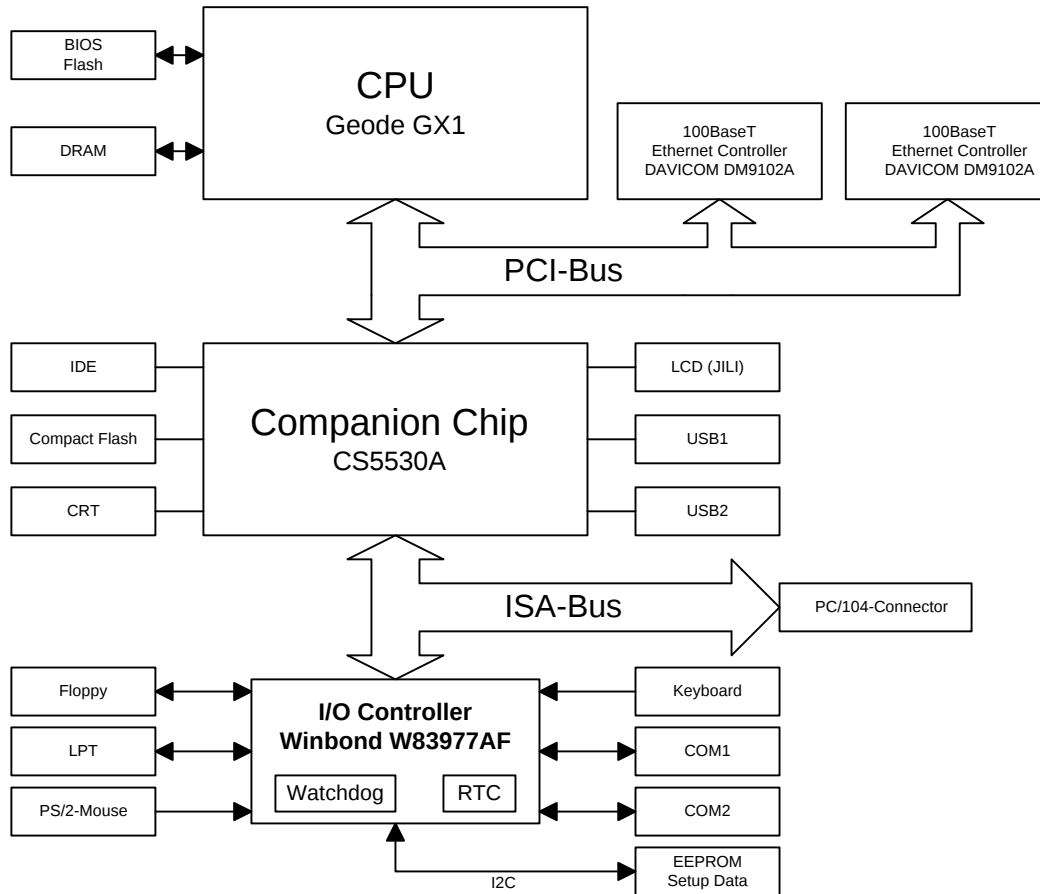
Updating the BIOS represents a potential hazard. Power failures or fluctuations that occur when you update the Flash ROM can damage the BIOS code, making the system unbootable.

To prevent this hazard, many systems come with a boot-block Flash ROM. The boot-block region contains a fail-safe recovery routine. If the boot-block code finds a corrupted BIOS (checksum fails), it boots into the crisis recovery mode and loads a BIOS image from a crisis diskette (see above).

Additionally, the end user can insert an update key into the LPT port to force initiating the boot block recovery routine.

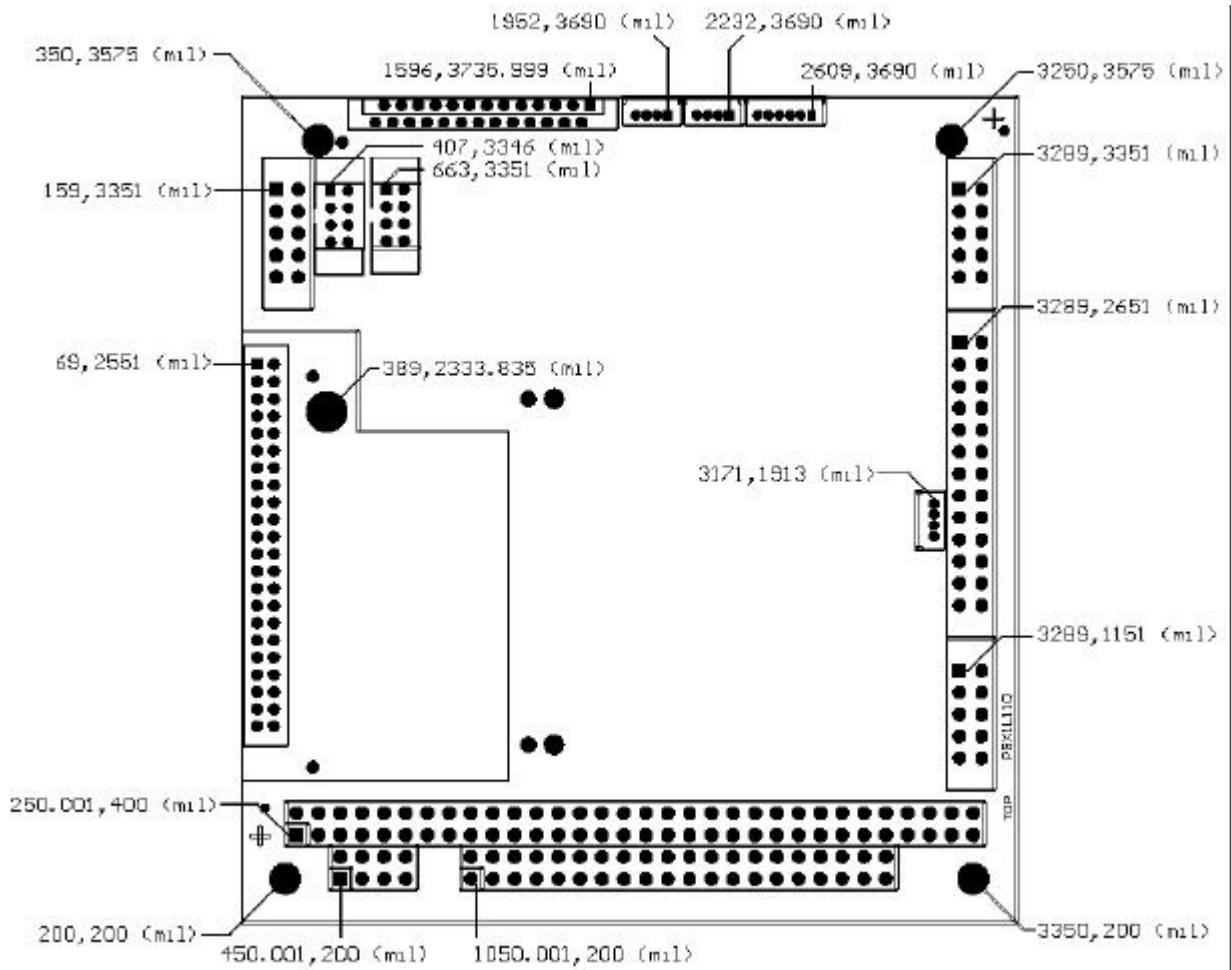
For further information on the update key and the crisis diskette, see Application Note JAP0034, which is available on the Kontron Embedded Modules Web site.

22. APPENDIX C: BLOCK DIAGRAM

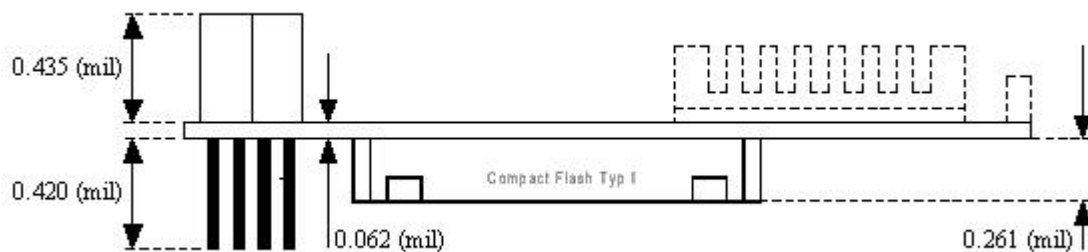


23. APPENDIX D: MECHANICAL DIMENSIONS

23.1 Top

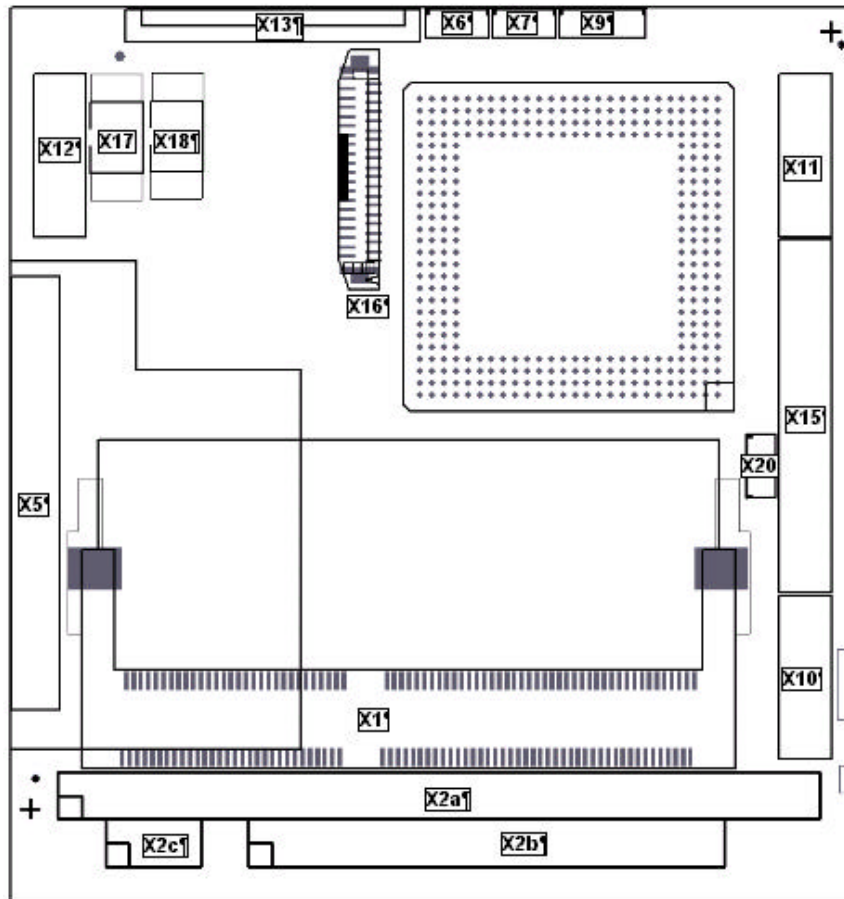


23.2 Bottom



24. APPENDIX E: CONNECTOR LAYOUT

24.1 Connector Layout



24.2 Connector Table

Connector	Device	Connector	Device
X1	SO-DIMM memory	X11	COM1
X2a	PC/104 ISA-lower	X12	COM2
X2b	PC/104 ISA-upper	X13	Floppy
X2c	Power connector	X14	CompactFlash socket (bottom of board)
X5	IDE hard-disk drive or Kontron Embedded Modules <i>chipDISK</i>	X15	Parallel port
X6	USB	X16	JIL
X7	USB	X17	Ethernet 1
X9	VGA	X18	Ethernet 2
X10	Keyboard	X20	PS/2 mouse

25. APPENDIX F: JIDA STANDARD

Every board with an on-board BIOS extension supports the following function calls, which supply information about the board. Jump^{tec} Intelligent Device Architecture (JIDA) functions are called via Interrupt 15h. Functions include:

- AH=Eah
- AL=function number
- DX=4648h (security word)
- CL=board number (starting with 1)

The interrupt returns a CL≠0 if a board with the number specified in CL does not exist. CL will equal 0 if the board number exists. In this case, the content of DX determines if the operation was successful. DX=6B6Fh indicates success; other values indicate an error.

25.1 Obtaining Information about Boards that Use the JIDA Standard

To obtain information about the installed boards that follow the JIDA standard, use the following procedure.

1. Call Get BIOS ID with CL=1.
The name of the first device installed will be returned. If you see the result **Board exists** (CL=0), increment CL, and call **Get BIOS ID** again.
2. Repeat until you see **Board not present** (CL≠0).
You now know the names of boards that follow the JIDA standard.
3. You can find out more information about a specific board by calling the appropriate inquiry function with the board's number in CL.

Note: Association between board and board number may change because of configuration changes. Do not rely on associations between board and board number. Use the above procedure to determine the association between board and board number.

Refer to the JIDA manual in the jidai110.zip folder for further information on implementing and using JIDA calls with C sample code.

26. APPENDIX G: PC ARCHITECTURE INFORMATION

The following sources of information can help you better understand PC architecture.

26.1 Buses

26.1.1 ISA, Standard PS/2 - Connectors

- *AT Bus Design: Eight and Sixteen-Bit ISA, E-ISA and EISA Design*, Edward Solari, Annabooks, 1990, ISBN 0-929392-08-6
- *AT IBM Technical Reference Vol 1&2*, 1985
- *ISA & EISA Theory and Operation*, Edward Solari, Annabooks, 1992, ISBN 0929392159
- *ISA Bus Specifications and Application Notes*, Jan. 30, 1990, Intel
- *ISA System Architecture, Third Edition*, Tom Shanley and Don Anderson, Addison-Wesley Publishing Company, 1995, ISBN 0-201-40996-8
- *Personal Computer Bus Standard P996*, Draft D2.00, Jan. 18, 1990, IEEE Inc
- *Technical Reference Guide, Extended Industry Standard Architecture Expansion Bus*, Compaq 1989

26.1.2 PCI/104

- **Embedded PC 104 Consortium**
The consortium provides information about PC/104 and PC/104-Plus technology. You can search for information about the consortium on the Web.
- **PCI SIG**
The PCI-SIG provides a forum for its ~900 member companies, who develop PCI products based on the specifications that are created by the PCI-SIG. You can search for information about the SIG on the Web.
- *PCI & PCI-X Hardware and Software Architecture & Design*, Fifth Edition, Edward Solari and George Willse, Annabooks, 2001, ISBN 0-929392-63-9.
- *PCI System Architecture*, Tom Shanley and Don Anderson, Addison-Wesley, 2000, ISBN 0-201-30974-2.

26.2 General PC Architecture

- *Embedded PCs*, Markt&Technik GmbH, ISBN 3-8272-5314-4 (German)
- *Hardware Bible*, Winn L. Rosch, SAMS, 1997, 0-672-30954-8
- *Interfacing to the IBM Personal Computer*, Second Edition, Lewis C. Eggebrecht, SAMS, 1990, ISBN 0-672-22722-3
- *The Indispensable PC Hardware Book*, Hans-Peter Messmer, Addison-Wesley, 1994, ISBN 0-201-62424-9
- *The PC Handbook: For Engineers, Programmers, and Other Serious PC Users, Sixth Edition*, John P. Choisser and John O. Foster, Annabooks, 1997, ISBN 0-929392-36-1

26.3 Ports

26.3.1 RS-232 Serial

- EIA-232-E standard
The EIA-232-E standard specifies the interface between (for example) a modem and a computer so that they can exchange data. The computer can then send data to the modem, which then sends the data over a telephone line. The data that the modem receives from the telephone line can then be sent to the computer. You can search for information about the standard on the Web.
- *RS-232 Made Easy: Connecting Computers, Printers, Terminals, and Modems*, Martin D. Seyer, Prentice Hall, 1991, ISBN 0-13-749854-3
- National Semiconductor
The Interface Data Book includes application notes. Type “232” as a search criteria to obtain a list of application notes. You can search for information about the data book on National Semiconductor’s Web site.

26.3.2 Serial ATA

Serial AT Attachment (ATA) Working Group

This X3T10 standard defines an integrated bus interface between disk drives and host processors. It provides a common point of attachment for systems manufacturers and the system. You can search for information about the working group on the Web.

We recommend you also search the Web for information on *4.2 I/O cable*, if you use hard disks in a DMA3 or PIO4 mode.

26.3.3 USB

USB Specification

USB Implementers Forum, Inc. is a non-profit corporation founded by the group of companies that developed the Universal Serial Bus specification. The USB-IF was formed to provide a support organization and forum for the advancement and adoption of Universal Serial Bus technology. You can search for information about the standard on the Web.

26.4 Programming

- *C Programmer's Guide to Serial Communications*, Second Edition, Joe Campbell, SAMS, 1987, ISBN 0-672-22584-0
- *Programmer's Guide to the EGA, VGA, and Super VGA Cards*, Third Edition, Richard Ferraro, Addison-Wesley, 1990, ISBN 0-201-57025-4
- *The Programmer's PC Sourcebook*, Second Edition, Thom Hogan, Microsoft Press, 1991, ISBN 1-55615-321-X
- *Undocumented PC, A Programmer's Guide to I/O, CPUs, and Fixed Memory Areas*, Frank van Gilluwe, Second Edition, Addison-Wesley, 1997, ISBN 0-201-47950-8

27. APPENDIX H: DOCUMENT-REVISION HISTORY

Version	Date	Edited by	Changes
1.6	25.02.03	VGG	Add environment note
1.5	07.01.03	FK	Updates USB chapter information.
1.4	23.09.02	FK	Updated pin table for PS/2 Mouse Interface chapter.
1.3	23.07.02	FK	Updated Upper Memory Area Map table.
1.2	20.06.02	FK	Updated information on supply voltage, interrupt-request lines, and the Setup Boot Menu.
1.1	06.05.02	MD	Updated BIOS chapter.
1.0	08.04.02	FK and JL	Initial release of manual.
0.3	04.04.02	FK and JL	Updated manual throughout.
0.2	27.03.02	JL	Formatted and edited manual.
0.1	14.03.02	FK	Created manual.