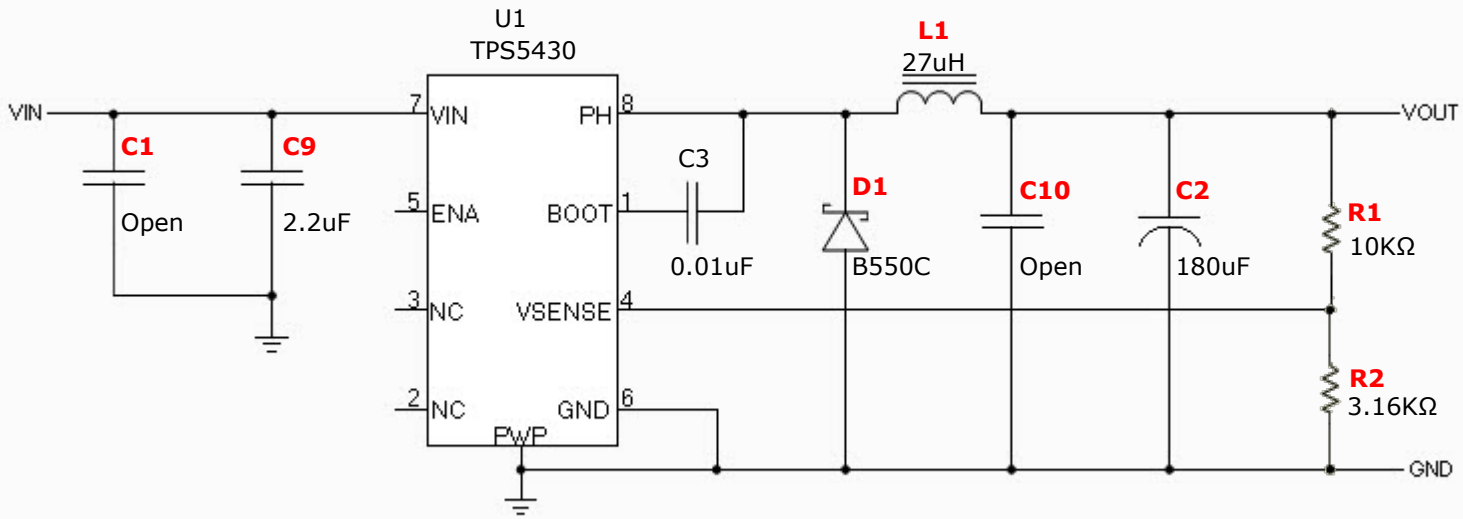
SwitcherPro Design Report
Schematic

Design Name: Wakey 5 V **Part:** TPS5430

VinMin: 20V **VinMax:** 34V **Vout:** 5V **Iout:** 3A



SwitcherPro Design Report
Analysis - Main

Design Name: Wakey 5 V **Part:** TPS5430

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Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Input Voltage Volts - V	20.00	-	34.00	-	-	-	-	-	-
Input Ripple mVp-p - mVp-p	-	-	-	-	-	680	-	-	685.8
UVLO(Start) Volts - V	-	-	-	-	-	-	-	5.30	-
UVLO(Stop) Volts - V	-	-	-	-	-	-	-	-	-
Switching Frequency KHz - KHz	-	-	-	-	500	-	-	-	-
Slow Start ms - ms	-	-	-	-	8.00	-	-	-	-
Estimated PCB Area mm² - mm²	-	-	-	-	-	-	-	698	-
Max Component Height mm - mm	-	-	-	-	-	25	-	-	12

SwitcherPro Design Report
Analysis - Output1

Design Name: Wakey 5 V **Part:** TPS5430

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Parameter Units-Symbol	User Input Minimum	User Input Nominal	User Input Maximum	Default Input Minimum	Default Input Nominal	Default Input Maximum	Calculated Minimum	Calculated Nominal	Calculated Maximum
Output Voltage Volts - V	-	5.000	-	-	-	-	4.908	-	5.266
Output Ripple mVp-p - mVp-p	-	-	-	-	-	100	-	-	2.1
Output Current Amps - A	-	-	3.000	0.100	-	-	-	-	-
Inductor Peak to Peak Current Amps - A	-	-	-	-	-	-	0.368	-	0.427
Current Limit Threshold Amps - A	-	-	-	-	4.500	-	-	-	-
Gain Margin dB - dB	-	-	-	-10	-	-	-	-16	-
Phase Margin Deg. - Deg.	-	-	-	60	-	-	-	38	-
Upper FET RDSon mOhms - mΩ	-	-	-	-	-	-	112	-	112
Duty Cycle % - %	-	-	-	-	-	-	16.2	-	27.5
On Time Min (switch) ns - ns	-	-	-	-	-	-	269.9	-	687.0
Cross Over Frequency KHz - KHz	-	-	-	-	-	-	-	12	-

SwitcherPro Design Report
Stress Results

Design Name: Wakey 5 V **Part:** TPS5430

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Device	Rated Voltage	Calculated Voltage	Rated Current (RMS)	Calculated Current (RMS)	Error Message	Power	Calculated Max Temp
C9 (High Freq. Input Cap)	100V	34.2V	2.55A	1.34A	-	4mW	-
C2 (Bulk Output Cap)	6.3V	5.03V	4A	0.12A	-	76uW	-
L1 (Output Inductor)	-	-	4.3A	3A	-	171mW	-
D1 (Catch Diode)	50V	34.2V	5A	2.51A	-	1.2W	85°C
U1 (Converter)	40V	34.2V	4A	1.57A	-	951mW	47°C

SwitcherPro Design Report
Efficiency

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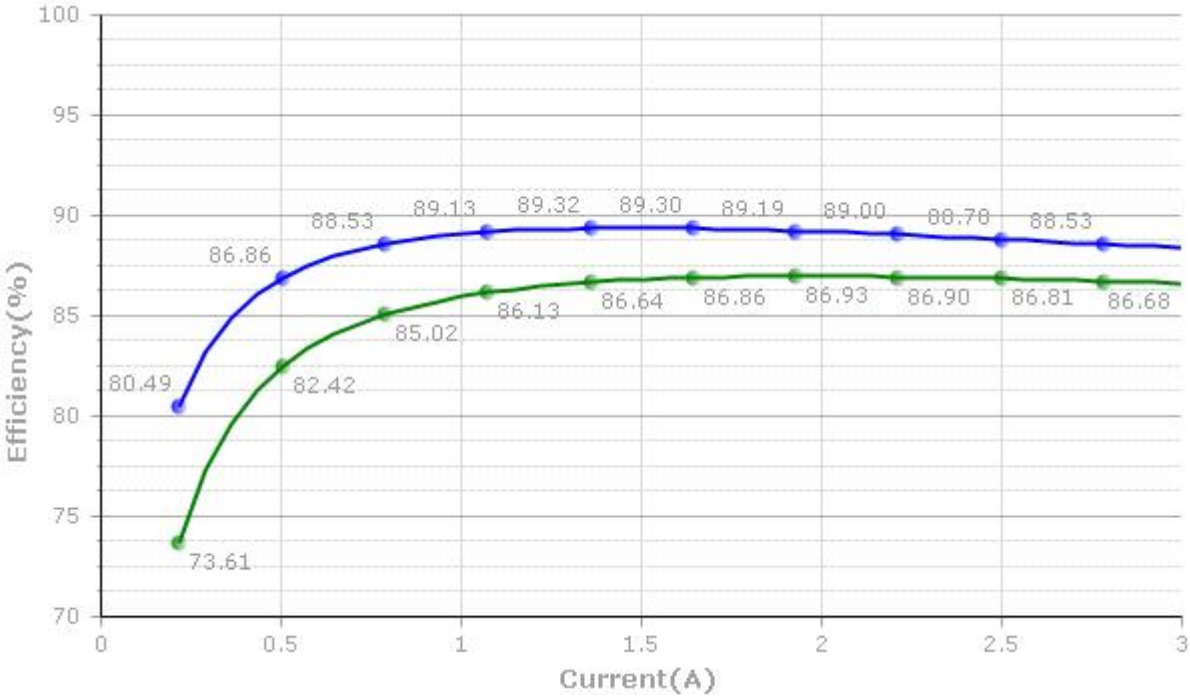

Efficiency For Vin Max
Efficiency For Vin Min

SwitcherPro Design Report
Loop Response

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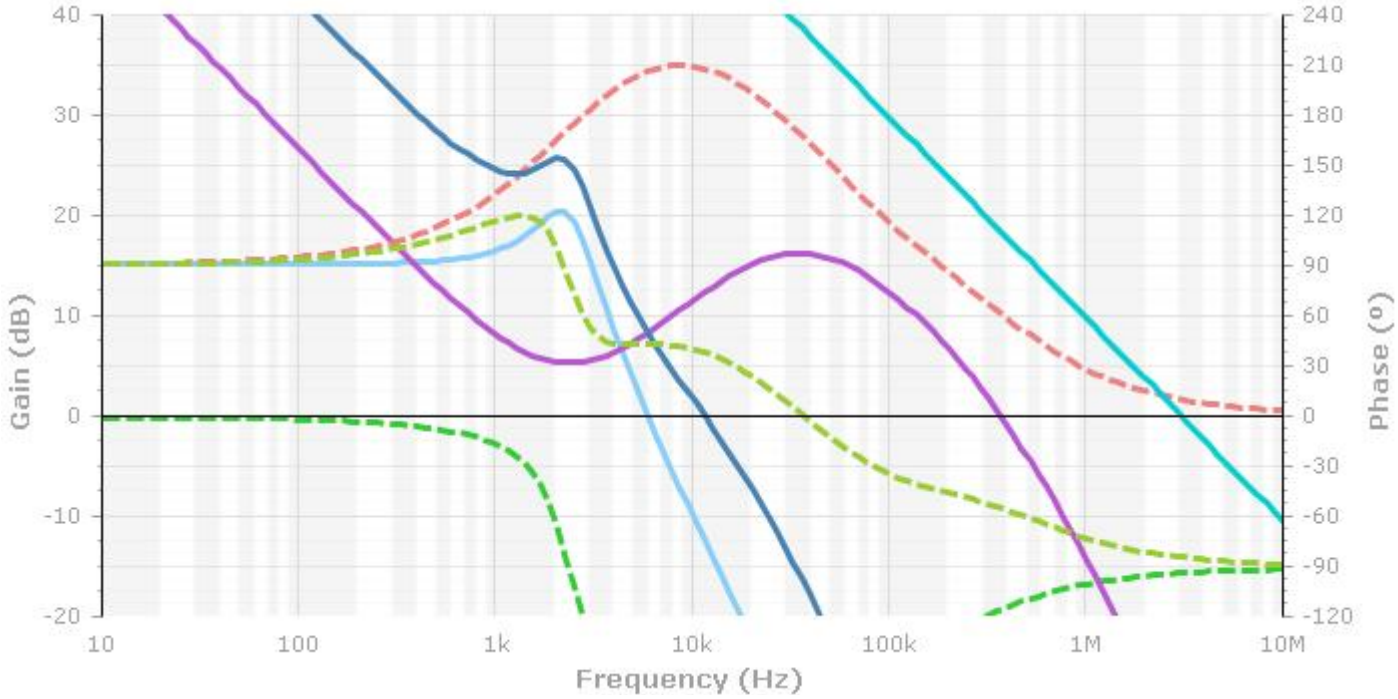
VinMin: 20V **VinMax:** 34V **Vout:** 5V **Iout:** 3A



This graph was generated using the following conditions: Nominal Switching Freq, Minimum Vin, Maximum Load,and Maximum Capacitor ESR. To customize conditions use the 'What If Analysis' form

- Power Stage Gain
- Power Stage Phase
- Compensation Gain
- Compensation Phase
- Error Amp Gain
- Total Gain
- Total Phase

SwitcherPro Design Report
Bill of Materials

Design Name: Wakey 5 V **Part:** TPS5430

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Name	Quantity	Part Number	Description	Manufacturer	Package	Area(mm²)	Height(mm)
C2	1	EEFSE0J181R	Capacitor, NA, 180uF, 6.3V, 20%	Panasonic	EEFSDE	32	4
C3	1	Standard	Capacitor, Ceramic, 0.01uF, 20V, 1%	Standard	0603	2	1
C9	1	GRM32ER72A225KA35L	Capacitor, Ceramic, 2.2uF, 100V, 10%	Murata Manufacturing	1210	8	8
D1	1	B550C	Diode, Schottky, 50V, 5A	Diodes Inc	SMC	44.22	2.62
L1	1	PCH-45-273	Inductor, 27uH, 4.3A, 19mΩ	CoilCraft	Unshielded	252.218	11.506
R1	1	Standard	Resistor, SurfaceMount, 10KΩ, 100mW, 1%	Standard	0603	2	1
R2	1	Standard	Resistor, SurfaceMount, 3.16KΩ, 100mW, 1%	Standard	0603	2	1
U1	1	TPS5430	IC, Converter, 8 pins	Texas Instruments, Inc.	DDA	30	2

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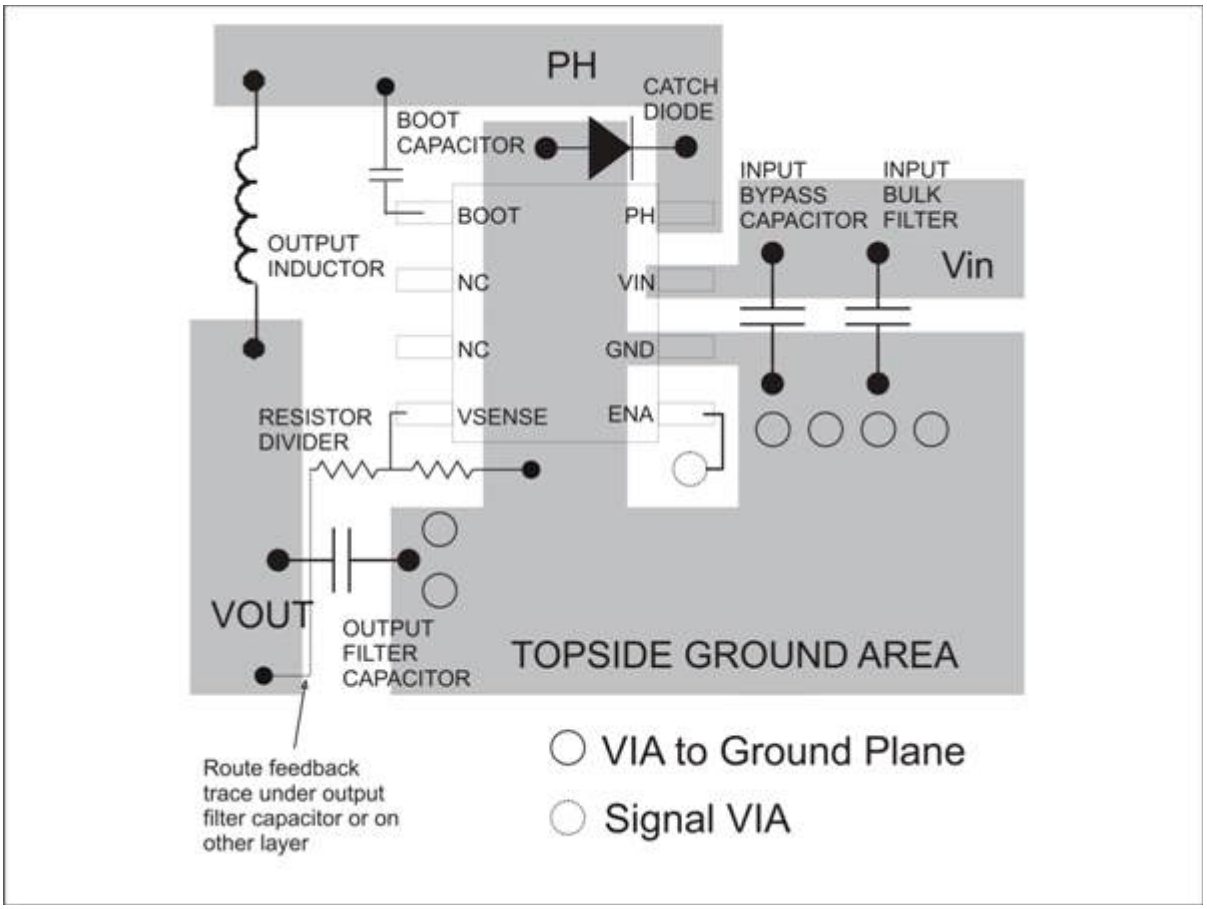

TPS543x/TPS5450

The VIN pins should be connected together on the printed circuit board (PCB) and bypassed with a low ESR ceramic bypass capacitor. Care should be taken to minimize the loop area formed by the bypass capacitor connections, the VIN pins, and the TPS543x/50 ground pin. The best way is to extend the top side ground area from under the device adjacent to the VIN trace, and place the bypass capacitor as close as possible to the VIN pins. The minimum recommended bypass capacitance is 10 uF ceramic with a X5R or X7R dielectric.

There should be an area of ground one the top layer directly under the IC, with an exposed area for connection to the PowerPAD. Use vias to connect this ground area to any internal ground planes. Use additional vias at the ground side of the input and output filter capacitors as well. The GND pin should be tied to the PCB ground by connecting it to the ground area under the device as shown.

The PH pin should be routed to the output inductor catch diode and boot capacitor. Since the PH connection is the switching node, inductor should be located very close to the PH pins and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The catch diode should also be placed close to the device to minimize the output current loop area. Connect the boot capacitor between the phase node and the BOOT pin as shown. Keep the boot capacitor close to the IC and minimize the conductor trace lengths The component placements and connections shown work well, but other connection routings may also be effective.

Connect the output filter capacitor(s) as shown between the VOUT trace and GND. It is important to keep the loop formed by the PH pins, Lout, Cout and PGND as small as is practical.

Connect the VOUT trace the VSENSE pin using the resistor divider network to set the output voltage. Do not route this trace too close to the PH trace. Do to the size of the IC package and the device pin-out, the trace may need to be routed under the output capacitor. Alternately, the routing may be done on an alternate layer if a trace under the output capacitor is not desired.

If the grounding scheme shown is utilized, it will be necessary to use a via connection to a different layer to route to the ENA pin.