EP9301 User's Guide

Release 1.00

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DS636UM2

Revision	Date	Changes
1	12 December 2003	Initial Release
2	12 February 2004	Updated ChipID, SysCfg and DeviceCfg register information. Added ExtensionID register information to the Security section.

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Preface

About the EP9301 User's Guide

This Guide describes the architecture, hardware and operation of the Cirrus Logic EP9301. It is intended to be used in conjunction with the EP9301 Datasheet, which contains the full electrical specifications for the device.

How to Use this Guide

Subject Matter	Location
AC'97	Chapter 18 - AC'97 Controller
ARM920T Processor	Chapter 2 - ARM920T Core and Advanced High-Speed Bus (AHB)
Boot ROM, Hardware and Software	Chapter 3 - Boot ROM
Booting From SROM or SyncFlash	Chapter 10 - SDRAM, SyncROM, and SyncFLASH Controller
Buses - AMBA, AHB, APB	Chapter 2 - ARM920T Core and Advanced High-Speed Bus (AHB)
DMA Controller	Chapter 7 - DMA Controller
EP9301 Block Diagram	Chapter 2 - ARM920T Core and Advanced High-Speed Bus (AHB)
Ethernet	Chapter 6 - 1/10/100 Mbps Ethernet LAN Controller
GPIO	Chapter 21 - GPIO Interface
HDLC	Chapter 11 - UART1 With HDLC and Modem Control Signals
I^2S	Chapter 17 - I^2S Controller
Infra-Red Interface	Chapter 13 - IrDA
Interrupt Registers	Chapter 5 - Vectored Interrupt Controller
Interrupts	Chapter 5 - Vectored Interrupt Controller
IrDA	Chapter 13 - IrDA
MAC	Chapter 6 - 1/10/100 Mbps Ethernet LAN Controller
Memory Map	Chapter 1 - Introduction
Modem	Chapter 11 - UART1 With HDLC and Modem Control Signals
Power Management	Chapter 4 - System Controller
Programming Clocks	Chapter 4 - System Controller
Real Time Clock	Chapter 16 - Real Time Clock With Software Trim
Register List	Chapter 1 - Introduction

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Subject Matter	Location
RTC	Chapter 16 - Real Time Clock With Software Trim
SDRAM	Chapter 10 - SDRAM, SyncROM, and SyncFLASH Controller
Security	Chapter 22 - Security
SMC	Chapter 9 - Static Memory Controller
SSP	Chapter 19 - Synchronous Serial Port
Static Memory Controller	Chapter 9 - Static Memory Controller
System Configuration	Chapter 4 - System Controller
System Registers	Chapter 4 - System Controller
Timers	Chapter 14 - Timers
Touch Screen	Chapter 20 - Analog-to-Digital Converter (ADC) Interface
UART	Chapter 11 - UART1 With HDLC and Modem Control Signals Chapter 12 - UART2
USB	Chapter 8 - Universal Serial Bus Host Controller
Vectored Interrupt Registers	Chapter 5 - Vectored Interrupt Controller
Vectored Interrupts	Chapter 5 - Vectored Interrupt Controller
Watchdog Timer	Chapter 15 - Watchdog Timer

Related Documents from Cirrus Logic

1. EP9301 Datasheet, document number - DS636PP1

Reference Documents

1. ARM920T Technical Reference Manual
2. AMBA Specification (Rev. 2.0), ARM IHI 0011A, ARM Limited.
3. AHB Example AMBA System (Addendum 01), ARM DDI 0170A, ARM Limited.
4. The coprocessor instruction assembler notation can be referenced from ARM programming manuals or the Quick Reference Card, document number ARM QRC 0001D.
5. The MAC engine is compliant with the requirements of ISO/IEC 8802-3 (1993), Sections 3 and 4.
6. OpenHCI - Open Host Controller interface Specification for USB, Release 1.0a; Compaq, Microsoft, National Semiconductor.
7. ARM Coprocessor Quick Reference Card, document number ARM QRC 0001D.

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8. Information Technology, AT Attachment with Packet Interface - 5 (ATA/ATAPI-5) ANSI NCITS document T13 1321D, Revision 3, 29 February 2000

9. OpenHCI - Open Host Controller Interface Specification for USB, Release: 1.0a, Released - 09/14/99 2:33 PM

10. ARM PrimeCell PL190-Rel1v1 Revision 1.7 Technical Reference Manual DDI0181C

11. Audio Codec '97, Revision 2.3, April 2002, Intel Corporation

Notational Conventions

This document uses the following conventions:

- Internal and external Signal Names, and Pin Names use mixed upper and lower case alphanumeric, and are shown in bold font: **RDLED**.
- Register Bit Fields are named using upper and lower case alphanumeric: that is, SBOOT, LCSn1.
- Registers are named using mixed upper and lower case alphanumeric: that is, SysCfg or PxDDR. (Where there are multiple registers with similar names, a lower case "x" is used as a place holder. For example, in the PxDDR registers, x represents a letter between A and H, indicating the specific port being discussed.)

Caution: In the Internal Register Map in Table 2-7 on page 7-47, some memory locations are listed as **Reserved**. These memory locations should not be used. Reading from these memory locations will yield invalid data. Writing to these memory locations may cause unpredictable results.

(An example register description is shown below. This description is used for the following examples.)

A specific bit may be specified in one of two ways:

By *register name[bit number]*: *SysCfg[29]*,
or by *register name.bit field[bit number]*: *SysCfg.REV[1]*

Both of these representations refer to the same bit.

The following:

SysCfg[8], or
SysCfg.SBOOT

also refer to the same bit.

Hexidecimal numbers are referred to as *0x0000_0000*.

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Binary numbers are referred to as *0000_0000b*.

Register Example

Note: This is only and example. For actual SysCfg register information, see "SysCfg" on page 97.

SysCfg

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REV				RSVD											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD							SBOOT	LCSn7	LCSn6	LASDO	LEEDA	LEECLK	RSVD	LCSn2	LCSn1

Address:

0x8093_009C - Read/Write, Software locked

Default:

0x0000_0000

Definition:

System Configuration Register. Provides various system configuration options.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

REV: Revision, reads chip Version number: 0 - Rev A, 1 - Rev B, 2 - Rev C, 3 - Rev D.

SBOOT: Serial Boot Flag. This bit is read-only.
1 hardware detected Serial Boot selection,
0 hardware detected Normal Boot.

LCSn7, LCSn6: Latched version of CSn7 and CSn6 respectively. These are used to define the external bus width for the boot code boot.

LASDO: Latched version of ASDO pin. Used to select synchronous versus asynchronous boot device.

LEEDA: Latched version of EEDAT pin.

LEECLK: Define Internal or external boot:
1 Internal
0 External

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LCSn2, LCSn1: Define Watchdog startup action:

0	0	Watchdog disabled, Reset duration disabled
0	1	Watchdog disabled, Reset duration active
1	0	Watchdog active, Reset duration disabled
1	1	Watchdog active, Reset duration active

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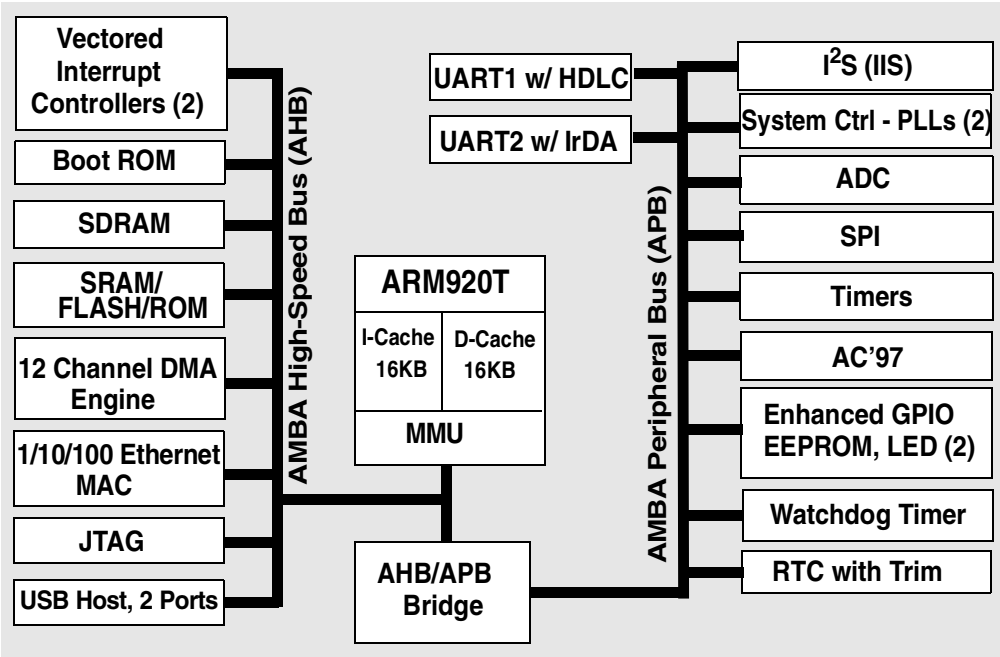
Chapter 1 Introduction

1.1 Introduction

The EP9301 is a highly integrated system-on-chip processor that paves the way for a multitude of next-generation consumer and industrial electronic products. Designers of digital media servers and jukeboxes, telematic control systems, thin clients, set-top boxes, point-of-sale terminals, industrial controls, biometric security systems, and GPS devices will benefit from the EP9301's integrated architecture and advanced features. In fact, with amazingly agile performance provided by a 166 MHz ARM920T processor, and featuring an incredibly wide breadth of peripheral interfaces, the EP9301 is well suited to an even broader range of high volume applications. Furthermore, by enabling or disabling the EP9301's peripheral interfaces, designers can reduce development costs and accelerate time-to-market by creating a single platform that can be easily modified to deliver a variety of differentiated end products.

Figure 1-1. EP9301 Block Diagram



1.2 EP9301 Features

The EP9301 system-on-chip processor has the following features:

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- 166 MHz ARM920T Processor
  - 16 KByte data cache and 16 KByte instruction cache
  - MMU enabling Linux® and Windows® CE
  - 66 MHz system bus
- MaverickKey™ IDs for Digital Rights Management or Design IP Security
  - 32-bit unique ID
  - 128-bit random ID

Integrated Peripheral Interfaces

- 1/10/100 Mbps Ethernet MAC
- Two-port USB 2.0 Full Speed host (OHCI)
- Two UARTs (16550 Type)
- IrDA interface, slow and fast mode
- Analog-to-Digital Converter (ADC)
- Serial Peripheral Interface (SPI) port
- AC ‘97 interface
- I2S interface, up to 2 channels
- External Memory Options
  - 16-bit SDRAM interface, up to four banks
  - 16/8-bit SRAM/Flash/ROM interface (I/F)
  - Serial EEPROM interface

Internal Peripherals

- Real-Time clock with software trim
- 12 DMA channels for data transfer that maximizes system performance
- Boot ROM
- Dual PLLs control all clock domains
- Watchdog timer
- Two general purpose 16-bit timers
- General purpose 32-bit timer
- 40-bit debug timer
- General-Purpose I/Os
  - 16 enhanced GPIOs including interrupt capability

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- 31 additional optional GPIOs multiplexed on peripherals
- Available in 208-pin LQFP package

1.3 EP9301 Applications

The EP9301 can be used in a variety of applications, such as:

- Digital media servers
- Integrated home media gateways
- Digital audio jukeboxes
- Portable audio/video players
- Streaming audio/video players
- Telematic control systems
- Set-top boxes
- Point-of-sale terminals
- Thin clients
- Internet TVs
- Biometric security systems
- Industrial controls
- GPS & fleet management systems
- Educational toys
- Voting machines
- Medical equipment

1.4 Overview of EP9301 Features

1.4.1 High-Performance ARM920T Processor Core

The EP9301 features an advanced ARM920T processor design with an MMU that supports Linux®, Windows® CE, and many other embedded operating systems. The ARM920T's 32-bit microcontroller architecture, with a five-stage pipeline, delivers impressive performance at very low power. The included 16 KByte instruction cache and 16 KByte data cache provide zero-cycle latency to the current program and data, or can be locked to provide guaranteed no-latency access to critical instructions and data. For applications with instruction memory size restrictions, the ARM920T's compressed Thumb® instruction set provides a space-efficient design that maximizes external instruction memory usage.

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1.4.2 MaverickKey™ Unique ID Secures Digital Content and OEM Designs

MaverickKey unique hardware programmed IDs provide an excellent solution to the growing concern over secure Web content and commerce. With Internet security playing an important role in the delivery of digital media such as books or music, traditional software methods are quickly becoming unreliable. The MaverickKey unique IDs provide OEMs with a method of utilizing specific hardware IDs for DRM (Digital Rights Management) mechanisms.

MaverickKey uses a specific 32-bit ID and a 128-bit random ID that are programmed into the EP9301 through the use of laser probing technology. These IDs can then be used to match secure copyrighted content with the ID of the target device that the EP9301 is powering, and then deliver the copyrighted information over a secure connection. In addition, secure transactions can benefit by matching device IDs to server IDs.

MaverickKey IDs can also be used by OEMs and design houses to protect against design piracy by presetting ranges for unique IDs. For more information on securing your design using MaverickKey, please contact your Cirrus Logic sales representative.

1.4.3 Integrated Two-port USB 2.0 Full Speed Host with Transceivers

The EP9301 integrates two USB 2.0 Full Speed host ports. Fully compliant to the OHCI USB 2.0 Full Speed specification (12 Mbps), the host ports can be used to provide connections to a number of external devices including mass storage devices, external portable devices such as audio players or cameras, printers, or USB hubs. Naturally, the two-port USB host also supports the USB 2.0 Low Speed standard. This provides the opportunity to create a wide array of flexible system configurations.

1.4.4 Integrated Ethernet MAC Reduces BOM Costs

The EP9301 integrates a 1/10/100 Mbps Ethernet Media Access Controller (MAC) on the device. With a simple connection to an MII-based external PHY, an EP9301-based system has easy, high-performance, cost-effective Internet capability.

1.4.5 Multiple Booting Mechanisms Increase Flexibility

The processor includes a 16 KByte boot ROM to set up standard configurations. Optionally, the processor may be booted from FLASH memory, over the SPI serial interface, or through the UART. This boot flexibility makes it easy to design user-controlled, field-upgradable systems. See Chapter 3 on page 59, for additional details.

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1.4.6 Abundant General Purpose I/Os Build Flexible Systems

The EP9301 includes both enhanced and standard general-purpose I/O pins (GPIOs). The 16 different enhanced GPIOs may individually be configured as inputs, outputs, or interrupt-enabled inputs. There are an additional 31 standard GPIOs that may individually be used as inputs, outputs, or open-drain pins. The standard GPIOs are multiplexed with peripheral function pins, so the number available depends on the utilization of peripherals. Together, the enhanced and standard GPIOs facilitate easy system design with external peripherals not integrated on the EP9301.

1.4.7 General-Purpose Memory Interface (SDRAM, SRAM, ROM and FLASH)

The EP9301 features a unified memory address model in which all memory devices are accessed over a common address/data bus. Memory accesses are performed via the high-speed processor bus. The SRAM memory controller supports 8 and 16-bit devices and accommodates an internal boot ROM concurrently with a 16-bit SDRAM memory.

1.4.8 12-Bit Analog-to-Digital Converter (ADC) Functionality

The EP9301 includes a 12-bit ADC, which can be used for general ADC functionality. The interface performs all sampling, averaging, ADC range checking, and control for a wide variety of applications. To improve system performance, the converter only interrupts the processor when a meaningful change occurs.

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Chapter 2

ARM920T Core and Advanced High-Speed Bus (AHB)

2

2.1 Introduction

This section discusses the ARM920T processor core and the Advanced High-Speed Bus (AHB).

2.2 Overview: ARM920T Processor Core

The ARM920T is a Harvard architecture processor core with separate 16 kbyte instruction and data caches with an 8-word line length used in the EP9301. The processor core utilizes a five-stage pipeline consisting of fetch, decode, execute, data memory access, and write stages.

2.2.1 Features

Key features include:

- ARM V4T (32-bit) and Thumb (16-bit compressed) instruction sets
- 32-bit Advanced Micro-Controller Bus Architecture (AMBA)
- 16 kbyte Instruction Cache with lockdown
- 16 kbyte Data Cache (programmable write-through or write-back) with lockdown
- Write Buffer
- MMU for Microsoft Windows CE and Linux operating systems
- Translation Look-aside Buffers (TLB) with 64 Data and 64 Instruction Entries
- Programmable Page Sizes of 64 kbyte, 4 kbyte, and 1 kbyte
- Independent lockdown of TLB Entries
- JTAG Interface for Debug Control

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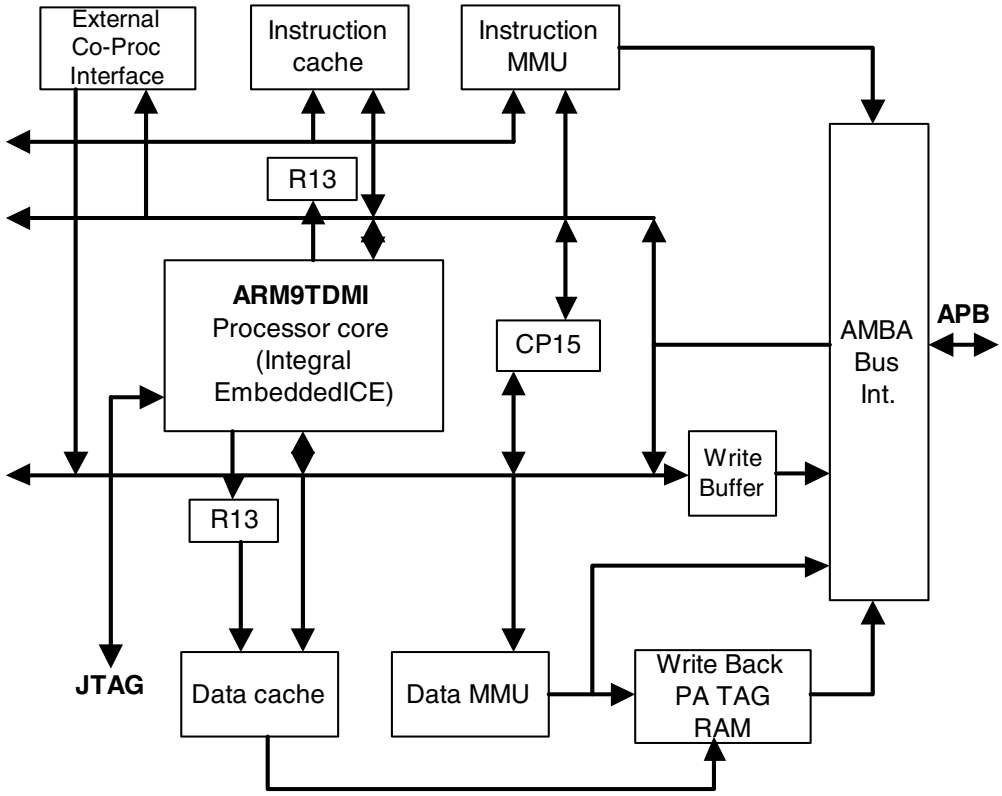
2.2.2 Block Diagram

2

Figure 2-1. ARM920T Block Diagram



2.2.3 Operations

The ARM920T core follows a Harvard architecture and consists of an ARM9TDMI core, MMU, instruction and data cache. The core supports both the 32-bit ARM and 16-bit Thumb instruction sets.

The internal bus structure (AMBA) includes both an internal high speed and external low speed bus. The high speed bus AHB (Advanced High-performance Bus) contains a high speed internal bus clock to synchronize coprocessor, MMU, cache, DMA controller, and memory modules. AMBA includes a AHB/APB bridge to the lower speed APB (Advanced Peripheral Bus). The APB bus connects to lower speed peripheral devices such as UARTs and GPIOs.

The MMU provides memory address translation for all memory and peripherals designed to remap memory devices and peripheral address locations. Sections, large, small and tiny pages are programmable to map memory in 1 Mbyte, 64 kbyte, 4 kbyte, 1 kbyte size blocks. To increase system

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performance, a 64-entry translation look-aside buffer will cache 64 address locations before a TLB miss occurs.

A 16 kbyte instruction and a 16 kbyte data cache are included to increase performance for cache-enabled memory regions. The 64-way associative cache also has lock-down capability. Cached instructions and data also have access to a 16-word data and 4-word instruction write buffer to allow cached instructions to be fetched and decoded while the write buffer sends the information to the external bus.

The ARM920T core supports a number of coprocessors by means of a specific pipeline architecture interface.

2.2.3.1 ARM9TDMI Core

ARM9TDMI core is responsible for executing both 32-bit ARM and 16-bit Thumb instructions. Each provides a unique advantage to a system design. Internally, the instructions enter a 5-stage pipeline. These stages are:

- Instruction Fetch
- Instruction Decode
- Execute
- Data Memory Access
- Register Write

All instructions are fully interlocked. This mechanism will delay the execution stage of a instruction if data in that instruction comes from a previous instruction that is not available yet. This simply insures that software will function identically across different implementations.

For memory access instructions, the base register used for the access will be restored by the processor in the event of an Abort exception. The base register will be restored to the value contained in the processor register before execution of the instruction.

The ARM9TDMI core memory interface includes a separate instruction and data interface to allow concurrent access of instructions and data to reduce the number of CPI (cycles per instruction). Both interfaces use pipeline addressing. The core can operate in big and little endian mode. Endianess affects both the address and the data interfaces.

The memory interface executes four types of memory transfers: sequential, non-sequential, internal, and coprocessor. It will also support uni- and bi-directional transfer modes.

The core provides a debug interface called JTAG (Joint Testing Action Group). This interface provides debug capability with five external control signals:

- **TDO** - Test Data Out

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- **TDI** - Test Data In
- **TMS** - Test Mode Select
- **TCK** - Test Clock
- **nTRST** - Test Reset

There are six scan chains (0 through 5) in the ARM9TDMI controlled by the JTAG Test Access Port (TAP) controller. Details on the individual scan chain function and bit order can be found in the ARM920T Technical Reference Manual.

2.2.3.2 Memory Management Unit

The MMU provides the translation and access permissions for the address and data ports for the ARM9TDMI core. The MMU is controlled by page tables stored in system memory and accessed using the CP15 register 1. The main features of the MMU are as follows:

- Address Translation
- Access Permissions and Domains
- MMU Cache and Write Buffer Access

2.2.3.2.1 Address Translation

The virtual address from the ARM920T core is modified by R13 internally to create a modified virtual address. The MMU then translates the modified virtual address from R13 by the CP15 register 3 into a physical address to access external memory or a device. The MMU looks for the physical address from the Translation Table Base (TTB) in system memory. It will also update the TLB cache.

The TLB is two 64-entry caches, one for data and one for instruction. If the physical address for the current virtual address is not found in the TLB (miss), the processor will go to external memory and look for the TTB in system memory. The internal translation table walks hardware steps through the page table setup in external memory for the appropriate physical address.

When the physical address is acquired, the TLB is updated. When the address is found in the TLB, system performance will increase since it will take additional cycles to access memory and update the TLB.

Translation of system memory is done by breaking up the memory into different size blocks called sections, large pages, small pages, and tiny pages. System memory and registers can be remapped by the MMU. The block sizes are as follows:

- Section - 1 Mbyte
- Large Page - 64 kbyte

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- Small Page - 16 kbyte
- Tiny Page - 1 kbyte

2.2.3.2.2 Access Permission and Domains

Access to any section or page of memory is dependent on its domain. The page table in external memory also contains access permissions for all sub-divisions of external memory. Access to specific instructions or data has three possible states, assuming access is permitted:

- *Client*: Access permissions based on the section or page table descriptor
- *Manager*: Ignore access permissions in the section or page table descriptor
- *No access*: any attempted access generates a domain fault

2.2.3.2.3 MMU Enable

Enabling the MMU allows for system memory control, but is also required if the data cache and the write buffer are to be used. These features are enabled for specific memory regions, as defined in the system page table. MMU enable is done via CP15 register 1. The procedure is as follows:

1. Program the Translation Table Base (TTB) and domain access control registers.
2. Create level 1 and level 2 pages for the system and enable the cache and the write buffer.
3. Enable MMU - bit 0 of CP15 register 1.

2.2.3.3 Cache and Write Buffer

Cache configuration is 64-way set associative. There is a separate 16 kbyte instruction and data cache. The cache has the following characteristics:

- 8 words per line with 1 valid bit and 2 dirty bits per line for allowing half-line write-backs.
- Write-through and write-back capable, selectable per memory region defined by the MMU.
- Pseudo random or round robin replacement algorithms for cache misses. This is determined by the RR bit (bit 14 in CP15 register 1). An 8-word line is reloaded on a cache miss.
- Independent cache lock-down with granularity of 1/64th of total cache size or 256 bytes for both instructions and data. Lock-down of the cache will prevent an eight-word cache line fill of that region of cache.
- For compatibility with Windows CE and to reduce latency, physical addresses stored for data cache entries are stored in the PA TAG RAM to

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be used for cache line write-back operations without need of the MMU, which prevents a possible TLB miss that would degrade performance.

- Write Buffer is a 4-word instruction x 16-word data buffer. If enabled, writes are sent to buffer directly from cache or from the CPU in the event of a cache miss or cache not enabled.

2.2.3.3.1 Instruction Cache Enable

- At reset, the cache is disabled.
- A write to CP15 register 1, bit 12, will enable or disable the Instruction Cache. If the Instruction Cache (I-Cache) is enabled without the MMU enabled, all accesses are treated as cacheable.
- If disabled, current contents are ignored. If re-enabled before a reset, contents will be unchanged but may not be coherent with main memory. If so, contents must be flushed before re-enabling.

2.2.3.3.2 Data Cache Enable

- A write to CP15 register 1, bit 0, will enable or disable the Data Cache (D-Cache)/Write Buffer.
- D-Cache must only be enabled when the MMU is enabled. All data accesses are subject to MMU and permission checks.
- If disabled, current contents are ignored. If re-enabled before a reset, contents will be unchanged but may not be coherent with main memory. Depending on system software, a clean and invalidate action may be required before re-enabling.

2.2.3.3.3 Write Buffer Enable

- The Write bugger is enabled by the page table entries in the MMU. The Write buffer is not enabled unless MMU is enabled.

2.2.4 AMBA AHB Bus Interface Overview

The AMBA AHB is designed for use with high-performance, high clock frequency system modules. The AHB acts as the high-performance system backbone bus. AHB supports the efficient connection of processors, on-chip memories and off-chip external memory interfaces with low-power peripheral functions. AHB is also specified to ensure ease of use in an efficient design flow using synthesis and automated test techniques. Figure 2-2 shows a typical AMBA AHB System.

AHB (Advanced High-Performance Bus) connects with devices that require greater bandwidth, such as DMA controllers, external system memory, and coprocessors. The AMBA AHB bus has the following characteristics:

- Burst Transactions

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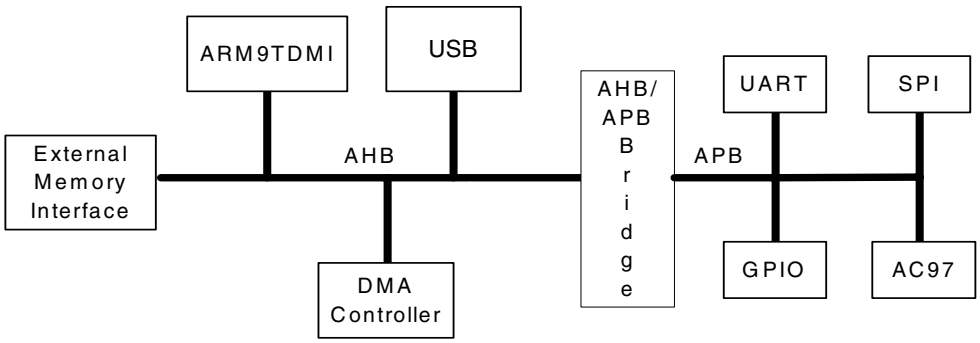
- Split Transactions
- Bus Master hand-over to devices, that is, DSP or DMA controller
- Single clock edge operations

APB (Advanced Peripheral Bus) is a lower bandwidth lower power bus which provides the following:

- Low Power Operations
- Latched address and control
- Simple Interface

Figure 2-2. Typical AMBA AHB System



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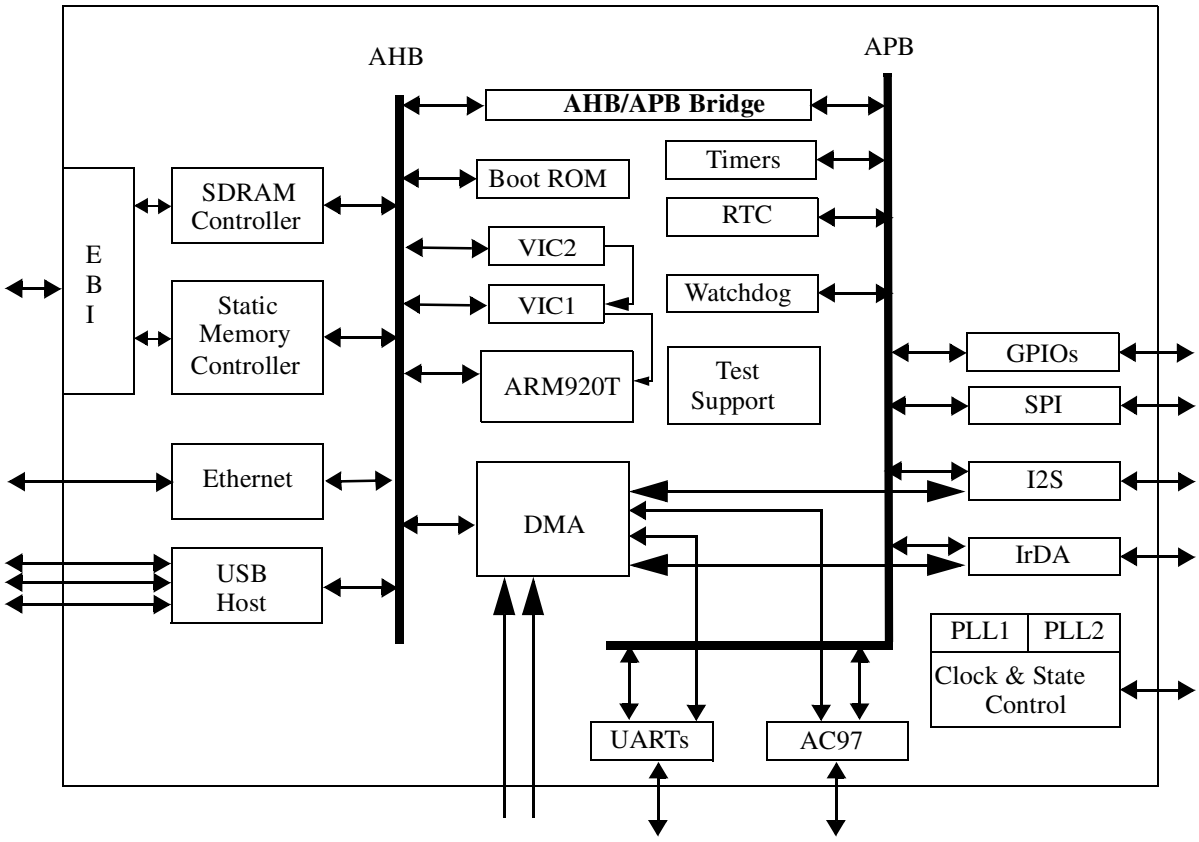
2.2.5 EP9301 AHB Implementation Details

2

Peripherals that have high bandwidth or latency requirements are connected to the EP9301 processor using the AHB bus. These include the external memory interface, Vectored Interrupt Controllers (VIC1, VIC2), DMA, USB host, Ethernet MAC and the bridge to the APB interface. The AHB/APB Bridge transparently converts the AHB access into the slower speed APB accesses. All of the control registers for the APB peripherals are programmed using the AHB/APB bridge interface. The main AHB data and address lines are configured using a multiplexed bus. This removes the need for three state buffers and bus holders and simplifies bus arbitration. Figure 2-3 shows the main data paths in the EP9301 AHB implementation.

Figure 2-3. EP9301 Main Data Paths



Before an AMBA-to-AHB transfer can commence, the bus master must be granted access to the bus. This process is started by the master asserting a request signal to the arbiter. Then the arbiter indicates when the master will be granted use of the bus. A granted bus master starts an AMBA-to-AHB transfer by driving the address and control signals. These signals provide information on the address, direction and width of the transfer, as well as indicating whether the transfer forms part of a burst.

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Two different forms of burst transfers are allowed:

- Incrementing bursts, which do not wrap at address boundaries
- Wrapping bursts, which wrap at particular address boundaries.

A write data bus is used to move data from the master to a slave, while a read data bus is used to move data from a slave to the master. Every transfer consists of:

- An address and control cycle
- One or more cycles for the data.

In normal operation a master is allowed to complete all the transfers in a particular burst before the arbiter grants another master access to the bus. However, in order to avoid excessive arbitration latencies, it is possible for the arbiter to break up a burst, and, in such cases, the master must re-arbitrate for the bus in order to complete the remaining transfers in the burst.

2.2.6 Memory and Bus Access Errors

There are several possible sources of access errors.

- Reads to reserved or undefined register memory addresses will return indeterminate data. Writes to reserved or undefined memory addresses are generally ignored, but this behavior is not guaranteed. Many register addresses are not fully decoded, so aliasing may occur. Addresses and memory ranges listed as **Reserved** should not be accessed; access behavior to these regions is not defined.
- Access to non-existent registers or memory may result in a bus error.
- Any access in the APB control register space will complete normally, as these devices have no means of signaling an error.
- Access to non-existent AHB/APB registers may result in a bus error, depending on the device and nature of the error. Device specific access rules are defined in the device descriptions.
- External memory access is controlled by the Static Memory Controller (SMC) and the Synchronous Dynamic RAM (SDRAM) controller. In general, access to non-existent external memory will complete normally, with reads returning random false data.

2.2.7 Bus Arbitration

The arbitration mechanism is used to ensure that only one master has access to the bus it controls at any one time. The arbiter performs this function by observing a number of different requests to use the bus and deciding which is currently the highest priority master requesting the bus.

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The arbitration scheme can be broken down into three main areas:

- The main AHB system bus arbiter
- The SDRAM slave interface arbiter
- The EBI bus arbiter

2.2.7.1 Main AHB Bus Arbiter

This arbiter controls the bus master arbitration for the AHB bus. The AHB bus has several Master interfaces. These are:

- ARM920T
- DMA controller
- USB host (USB1, 2)
- Ethernet MAC

These interfaces have an order of priority that is linked closely with the power saving modes. The power saving modes of Halt and Standby force the arbiter to grant the default bus master, in this case, the ARM920T.

In summary, the order of priority of the bus masters, from highest to lowest, is shown in Table 2-1.

Table 2-1: AHB Arbiter Priority Scheme

Priority Number	PRIOR 00 (Reset value)	PRIOR 01	PRIOR 10	PRIOR 11
1	MAC	MAC	DMA	DMA
2	USB	USB	USB	MAC
3	DMA	ARM920T	MAC	USB
4	ARM920T	DMA	ARM920T	ARM920T

The priority of the Arbiter can be programmed in the BusMstrArb register in the Clock and State Controller. The Arbiter can also be programmed to degrant one of the following masters: DMA, USB Host or Ethernet MAC, if an interrupt (IRQ or FIQ) is pending or being serviced. This prevents one of these masters from blocking important interrupt service routines. These masters are prevented from accessing the bus, and their bus requests are masked, until the IRQ/FIQ is removed (by the Interrupt Service Routine), at which point their bus requests will be recognized. The default is to program the Arbiter so that it does *not* degrant any of these masters.

In normal operation, when the ARM920T is granted the bus and a request to enter Halt mode is received, the ARM920T is de-granted from the AHB bus. Any other master requesting the bus in Halt mode (according to the priority) will be granted the bus. In the case of the entry into Standby, the dummy master will be granted the bus, which simply performs IDLE transfers. In this

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way, all the masters except the ARM920T can be used during Halt mode, but are shutdown during an entry into Standby.

2.2.7.2 EBI Bus Arbiter

This arbiter is used to arbitrate between accesses from the SDRAM controller and the Static Memory controller. The priority is given to accesses from the SDRAM controller.

2.3 AHB Decoder

The AHB decoder contains the memory map for all the AHB masters/slaves and the APB bridge. When a particular address range is selected, the appropriate signal is generated. It is defined in Table 2-2.

(For additional information, see “Reference Documents”, on Page 4.)

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Table 2-2: AHB Peripheral Address Range

Address Range	Register Width	Peripheral Type	Peripheral
0x800D_0000 - 0x800F_FFFF	-	-	Reserved
0x800C_0000 - 0x800C_FFFF	32	AHB	VIC2
0x800B_0000 - 0x800B_FFFF	32	AHB	VIC1
0x800A_0000 - 0x800A_FFFF	-	-	Reserved
0x8009_0000 - 0x8009_FFFF	32	AHB	Boot ROM physical address
0x8008_0000 - 0x8008_FFFF	32	AHB	SRAM Controller
0x8007_0000 - 0x8007_FFFF	-	-	Reserved
0x8006_0000 - 0x8006_FFFF	32	AHB	SDRAM Controller
0x8005_0000 - 0x8005_FFFF	-	-	Reserved
0x8004_0000 - 0x8004_FFFF	-	-	Reserved
0x8003_0000 - 0x8003_FFFF	-	-	Reserved
0x8002_0000 - 0x8002_FFFF	32	AHB	USB Host
0x8001_0000 - 0x8001_FFFF	32	AHB	Ethernet MAC
0x8000_0000 - 0x8000_FFFF	32	AHB	DMA

Note: Due to decoding optimization, the AHB peripheral registers are aliased throughout each peripherals register bank. Do not program access to an unspecified register within the bank.

2.3.1 AHB Bus Slave

An AHB slave responds to transfers initiated by bus masters within the system. The slave uses signals from the decoder to determine when it should respond to a bus transfer. All other signals required for the transfer, such as the address and control information, are generated by the bus master.

2.3.2 AHB to APB Bridge

The AHB to APB bridge is an AHB slave, providing an interface between the high-speed AHB and the low-power APB. Read and write transfers on the AHB are converted into equivalent transfers on the APB. As the APB is not pipelined. Wait states are added during transfers to and from the APB when the AHB is required to wait for the APB.

The main sections of this module are:

- AHB slave bus interface
- APB transfer state machine, which is independent of the device memory map
- APB output signal generation.

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2.3.2.1 Function and Operation of APB Bridge

The APB bridge responds to transaction requests from the currently granted AHB master. The AHB transactions are then converted into APB transactions.

If an undefined location is accessed, operation of the system continues as normal, but no peripherals are selected. The APB bridge acts as the only master on the APB.

The APB memory map is shown in Table 2-3.

Table 2-3: APB Peripheral Address Range

Address Range	Register Width	Peripheral Type	Peripheral
0x8095_0000 - 0x9000_FFFF	-	-	Reserved
0x8094_0000 - 0x8094_FFFF	16	APB	Watchdog Timer
0x8093_0000 - 0x8093_FFFF	32	APB	Syscon
0x8092_0000 - 0x8092_FFFF	32	APB	Real time clock
0x8091_0000 - 0x8091_FFFF	-	-	Reserved
0x8090_0000 - 0x8090_FFFF	-	-	Reserved
0x808F_0000 - 0x808F_FFFF	-	-	Reserved
0x808E_0000 - 0x808E_FFFF	-	-	Reserved
0x808D_0000 - 0x808D_FFFF	8	APB	UART2
0x808C_0000 - 0x808C_FFFF	32	APB	UART1
0x808B_0000 - 0x808B_FFFF	32	APB	IrDA
0x808A_0000 - 0x808A_FFFF	16	APB	SPI
0x8089_0000 - 0x8089_FFFF	-	-	Reserved
0x8088_0000 - 0x8088_FFFF	32	APB	AAC
0x8087_0000 - 0x8087_FFFF	-	-	Reserved
0x8086_0000 - 0x8086_FFFF	-	-	Reserved
0x8085_0000 - 0x8085_FFFF	-	-	Reserved
0x8084_0000 - 0x8084_FFFF	16	APB	GPIO
0x8083_0000 - 0x8083_FFFF	32	APB	Security
0x8082_0000 - 0x8082_FFFF	32	APB	I2S
0x8081_0000 - 0x8081_FFFF	32	APB	Timers
0x8080_0000 - 0x8080_FFFF	-	-	Reserved
0x8010_0000 - 0x807F_FFFF	-	-	Reserved

Note: Due to decoding optimization, the APB peripheral registers are aliased throughout each peripherals register bank. Do not program access to an unspecified register within the bank.

2.3.3 APB Bus Slave

An APB slave responds to transfers initiated by bus masters within the system. The slave uses signals from the decoder to determine when it should respond to a bus transfer. All other signals required for the transfer, such as the address and control information, are generated by the APB bridge.

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2.3.4 Register Definitions

ARM has thirty seven 32-bit internal registers, some are modal, some are banked. If operating in Thumb mode, the processor must switch to ARM mode before taking an exception. The return instruction will restore the processor to Thumb state. Most tasks are executed out of User mode.

User:	Unprivileged normal operating mode
FIQ:	Fast interrupt (high priority) mode when FIQ is asserted
IRQ:	Interrupt request (normal) mode when IRQ is asserted
Supervisor:	Software interrupt instruction (SWI) or reset will cause entry into this mode
Abort:	Memory access violation will cause entry into this mode
Undef:	Undefined instructions
System:	Privileged mode. Uses same registers as user mode

Table 2-4 illustrates the use of all registers for the following ARM920T operating modes. Each will bank or store a specific number of registers. Banked register information is not shared between modes. FIQs bank the fewest number of registers which increases performance.

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Table 2-4: Register Organization Summary

	Privileged Modes						
		Exception Modes					
User	**System**	**Supervisor**	**Abort**	**Undefined**	**IRQ**	**FIQ**	
r0	r0	r0	r0	r0	r0	r0	Thumb state low registers
r1	r1	r1	r1	r1	r1	r1	
r2	r2	r2	r2	r2	r2	r2	
r3	r3	r3	r3	r3	r3	r3	
r4	r4	r4	r4	r4	r4	r4	
r5	r5	r5	r5	r5	r5	r5	
r6	r6	r6	r6	r6	r6	r6	
r7	r7	r7	r7	r7	r7	r7	
r8	r8	r8	r8	r8	r8	r8_fiq	Thumb state high registers
r9	r9	r9	r9	r9	r9	r9_fiq	
r10	r10	r10	r10	r10	r10	r10_fiq	
r11	r11	r11	r11	r11	r11	r11_fiq	
r12	r12	r12	r12	r12	r12	r12_fiq	
r13(sp)	r13	r13_svc	r13_abt	r13_und	r13_irq	r13_fiq	
r14(lr)	r14	r14_svc	r14_abt	r14_und	r14_irq	r14_fiq	
r15(pc)	pc	pc	pc	pc	pc	pc	
cpsr	cpsr	cpsr	cpsr	cpsr	cpsr	cpsr	
		spsr_svc	spsr_abt	spsr_und	spsr_irq	spsr_fiq	

Note: Colored areas represent banked registers.

User mode in Thumb state generally limits access to r0-r7. There are six instructions that allow access to the high registers. For these 6 exceptions, the processor must revert to ARM state. These exceptions are:

- r0-r12: General purpose read/write 32-bit registers
- r13 (sp): Stack Pointer
- r14 (lr): Link Register
- r15 (pc): Program Counter
- cpsr: Current Program Status Register (contains condition codes and operating modes)
- spsr: Saved Program Status Register (saves CPSR when exception

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occurs)

The ARM920T core has 16 coprocessor registers for control over the core. Updates to the coprocessor registers are written using the CP15 instruction. Table 2-5 describes the CP15 ARM920T registers.

Table 2-5: CP15 ARM920T Register Description

Register	Description
0	**ID Code:** (Read/Only) This register returns a 32-bit device code. ID Code data represents the core type, revision, part number etc. Access to this register is done with the following instruction: MRC p15 0, Rd, c0, c0, 0 **Cache Code:** This will also return cache type, size and length of both I-Cache and D-Cache, size, and associativity. This is accessed with: MRC p15 0, Rd, c0, c0, 1
1	**Control Register:** (Read/Write) Use this register to enable MMU, instruction and data cache, round robin replacement 'RR'-bit, system protection, ROM protection, clocking mode. Read/Write Instructions: MRC p15, 0, Rd, c1, c0, 0 - Read control register - value stored in Rd MCR p15, 0, Rd, c1, c0, 0 - Write control register - value first loaded into Rd
2	**Translation Base Table:** (Read/Write) This register contains the start address of the first level translation table. Upper18 bits represent the pointer to table base. Lower 14 bits should be 0 for a write, unpredictable if read. MRC p15, 0, Rd, c2, c0, 0 - Read TTB MCR p15, 0, Rd, c2, c0, 0 - Write TTB
3	**Domain Access Control:** (Read/Write) This register specifies permissions for all 16 domains. MRC p15, 0, Rd, c3, c0, 0 MCR p15, 0, Rd, c3, c0, 0
4	**Reserved:** Do not access. Unpredictable behavior may result.
5	**Fault Status:** (Read/Write) This register indicates type of fault and domain of last data abort. MRC p15, 0, Rd, c5, c0, 0 - read data FSR value MCR p15, 0, Rd, c5, c0, 0 - write data FSR value
6	**Fault Address:** (Read/Write) This register contains address of the last data access abort. MRC p15, 0, Rd, c6, c0, 0 - read data FAR data MCR p15, 0, Rd, c6, c0, 0 - write data FAR data
7	**Cache Operation:** (Write/Only) This register will configure or perform a clean (flush) of the cache and write buffer when written to. An example: MRC p15, 0, Rd, c7, c7, 0 - Invalidate I/D-cache MRC p15, 0, Rd, c7, c5, 0 - Invalidate I-Cache
8	**TLB Operation:** (Write/Only) This register can configure or clean (flush) when written to: MRC p15, 0, Rd, c8, c7, 0 - Invalidate TLB
9	**Cache Lockdown:** (Read/Write) Prevents certain cache-line fills from being overwritten (locked). MRC p15, 0, Rd, c9, c0, 1- Write lockdown base pointer for D-Cache MRC p15, 0, Rd, c9, c0, 1 - Write lockdown base pointer for I-Cache

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Table 2-5: CP15 ARM920T Register Description (Continued)

Register	Description
10	**TLB Lockdown:** (Read/Write) Prevents TLB entries from being erased during a table walk. MRC p15, 0, Rd, c10, c0, 1- Write lockdown base pointer for data TLB entry MRC p15, 0, Rd, c10, c0, 1 - Write lockdown base pointer for instruction TLB entry
11,12,14	**Reserved**
13	**FCSE PID Register:** (Read/Write) Addresses by the ARM9TDMI core in a range from 0 to 32 MB are translated by this register to A + FCSE*32MB and remapped. If turned off, straight address map to the MMU results.
15	**Test Register Only:** Reads or writes will cause unpredictable behavior.

2.3.5 Memory Map

The overall memory map for the device is shown in Table 2-6.

If internal Boot Mode is selected and the register BootModeClr has been written, the address range 0x0000_0000 -> 0x0000_FFFF is occupied by the internal Boot ROM until the internal Boot Code is completed and then the map reverts back to either Synchronous or Asynchronous memory in this address space.

NOTE: Some memory locations are listed as **Reserved**. These memory locations should not be used. Reading from these memory locations will yield invalid data. Writing to these memory locations may cause unpredictable results.

Table 2-6: Global Memory Map for the Two Boot Modes

Address Range	Sync Memory Boot	Async Memory Boot
	ASD0 Pin = 1	ASD0 Pin = 0
0xF000_0000 - 0xFFFF_FFFF	Async memory (nCS0)	Sync memory (nSDCE3)
0xE000_0000 - 0xEFFF_FFFF	Sync memory (nSDCE2)	Sync memory (nSDCE2)
0xD000_0000 - 0xDFFF_FFFF	Sync memory (nSDCE1)	Sync memory (nSDCE1)
0xC000_0000 - 0xCFFF_FFFF	Sync memory (nSDCE0)	Sync memory (nSDCE0)
0x9000_0000 - 0xBFFF_FFFF	Not Used	Not Used
0x8080_0000 - 0x8FFF_FFFF	APB mapped registers	APB mapped registers
0x8010_0000 - 0x807F_FFFF	Reserved	Reserved
0x8000_0000 - 0x800F_FFFF	AHB mapped registers	AHB mapped registers
0x7000_0000 - 0x7FFF_FFFF	Async memory (nCS7)	Async memory (nCS7)
0x6000_0000 - 0x6FFF_FFFF	Async memory (nCS6)	Async memory (nCS6)
0x5000_0000 - 0x5FFF_FFFF	Reserved	Reserved
0x4000_0000 - 0x4FFF_FFFF	Reserved	Reserved
0x3000_0000 - 0x3FFF_FFFF	Async memory (nCS3)	Async memory (nCS3)
0x2000_0000 - 0x2FFF_FFFF	Async memory (nCS2)	Async memory (nCS2)
0x1000_0000 - 0x1FFF_FFFF	Async memory (nCS1)	Async memory (nCS1)
0x0001_0000 - 0x0FFF_FFFF	Sync memory (nSDCE3)	Async memory (nCS0)

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Table 2-6: Global Memory Map for the Two Boot Modes (Continued)

Address Range	Sync Memory Boot	Async Memory Boot
	ASD0 Pin = 1	**ASD0 Pin = 0**
0x0000_0000 - 0x0000_FFFF	Sync memory (nSDCE3) or Internal Boot ROM if INTBOOT selected	Async memory (nCS0) or Internal Boot ROM if INTBOOT selected

Note: The shaded areas are the memory areas dedicated to system registers. Details of these registers are in Table 2-7.

2.3.6 Internal Register Map

Registers are set to their default state by the **RSTOn** pin and by the **PRSTn** pin inputs. Some state conserving registers are reset only by the **PRSTn** pin. All registers are read/write unless specified otherwise.

2.3.6.1 Memory Access Rules

Any memory address not specifically assigned to a register should be avoided. Reads to register memory addresses labelled Reserved, Unused or Undefined will return indeterminate data. Writes to register memory addresses labelled Reserved, Unused or Undefined are generally ignored, but this behavior is not guaranteed. Many register addresses are not fully decoded, so aliasing may occur. Addresses and memory ranges listed as Reserved (RSVD) should not be accessed; access behavior to these regions is not defined.

The SW Lock field identifies registers with a software lock. The software lock prevents the register from being written unless a proper unlock operation is performed immediately prior to writing the target register. Any register whose accidental alteration could cause system damage is controlled with a software lock. Each peripheral with software lock capability has its own software lock register.

Within a register definition, a reserved bit, indicated the name RSVD, means the bit is not accessible. Software should mask the RSVD bits when doing bit reads. RSVD bits will ignore writes, that is writing a zero or a one does not matter.

Register bits identified as NC must be treated in a specific manner for reads and writes; see the register description for each register for information on how to read and write register bits identified as NC. Register bits identified as NC are functionally alive but have an undocumented or a “don’t care” operating function. The register description will provide information on how to handle NC bits.

Unless specified otherwise, all registers can be accessed as a byte, half-word, or word.

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CAUTION: Some memory locations are listed as **Reserved**. These memory locations should not be used. Reading from these memory locations will yield invalid data. Writing to these memory locations may cause unpredictable results.

Table 2-7: Internal Register Map

Address	Register Name	Register Description	SW Lock
0x8000_xxxx	**DMA**	**DMA Control Registers**	
0x8000_0000 - 0x8000_003C	M2P Channel 0 Registers (Tx)	Memory-to-Peripheral Channel 0 Registers (Tx)	N
0x8000_0040 - 0x8000_007C	M2P Channel 1 Registers (Rx)	Memory-to-Peripheral Channel 1 Registers (Rx)	N
0x8000_0080 - 0x8000_00BC	M2P Channel 2 Registers (Tx)	Memory-to-Peripheral Channel 2 Registers (Tx)	N
0x8000_00C0 - 0x8000_00FC	M2P Channel 3 Registers (Rx)	Memory-to-Peripheral Channel 3 Registers (Rx)	N
0x8000_0100 - 0x8000_013C	M2M Channel 0 Registers	Memory-to-Memory Channel 0 Registers	N
0x8000_0140 - 0x8000_017C	M2M Channel 1 Registers	Memory-to-Memory Channel 1 Registers	N
0x8000_0180 - 0x8000_01FC		Reserved	
0x8000_0200 - 0x8000_023C	M2P Channel 5 Registers (Rx)	Memory-to-Peripheral Channel 5 Registers (Rx)	N
0x8000_0240 - 0x8000_027C	M2P Channel 4 Registers (Tx)	Memory-to-Peripheral Channel 4 Registers (Tx)	N
0x8000_0280 - 0x8000_02BC	M2P Channel 7 Registers (Rx)	Memory-to-Peripheral Channel 7 Registers (Rx)	N
0x8000_02C0 - 0x8000_02FC	M2P Channel 6 Registers (Tx)	Memory-to-Peripheral Channel 6 Registers (Tx)	N
0x8000_0300 - 0x8000_033C	M2P Channel 9 Registers (Rx)	Memory-to-Peripheral Channel 9 Registers (Rx)	N
0x8000_0340 - 0x8000_037C	M2P Channel 8 Registers (Tx)	Memory-to-Peripheral Channel 8 Registers (Tx)	N
0x8000_0380	DMAChArb	DMA Channel Arbitration Register	N
0x8000_03C0	DMAGIInt	DMA Global Interrupt Register	N
0x8000_03C4 - 0x8000_FFFC		Reserved	
0x8001_xxxx	**Ethernet MAC**	**Ethernet MAC Control Registers**	
0x8001_0000	RXCtl	MAC Receiver Control Register	N
0x8001_0004	TXCtl	MAC Transmitter Control Register	N
0x8001_0008	TestCtl	MAC Test Control Register	N
0x8001_0010	MIICmd	MAC MII Command Register	N
0x8001_0014	MIIData	MAC MII Data Register	N
0x8001_0018	MIISts	MAC MII Status Register	N
0x8001_0020	SelfCtl	MAC Self Control Register	N
0x8001_0024	IntEn	MAC Interrupt Enable Register	N
0x8001_0028	IntStsP	MAC Interrupt Status Preserve Register	N
0x8001_002C	IntStsC	MAC Interrupt Status Clear Register	N
0x8001_0030 - 0x8001_0034		Reserved	
0x8001_0038	DiagAd	MAC Diagnostic Address Register	N
0x8001_003C	DiagDa	MAC Diagnostic Data Register	N
0x8001_0040	GT	MAC General Timer Register	N
0x8001_0044	FCT	MAC Flow Control Timer Register	N
0x8001_0048	FCF	MAC Flow Control Format Register	N
0x8001_004C	AFP	MAC Address Filter Pointer Register	N
0x8001_0050 - 0x8001_0055	IndAd	MAC Individual Address Register, (shares address space with HashTbl)	N

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Table 2-7: Internal Register Map (Continued)

Address	Register Name	Register Description	SW Lock
0x8001_0050 - 0x8001_0057	HashTbl	MAC Hash Table Register, (shares address space with IndAd)	N
0x8001_0060	GlIntSts	MAC Global Interrupt Status Register	N
0x8001_0064	GlIntMsk	MAC Global Interrupt Mask Register	N
0x8001_0068	GlIntROSts	MAC Global Interrupt Read Only Status Register	N
0x8001_006C	GlIntFrc	MAC Global Interrupt Force Register	N
0x8001_0070	TXCollCnt	MAC Transmit Collision Count Register	N
0x8001_0074	RXMissCnt	MAC Receive Miss Count Register	N
0x8001_0078	RXRuntCnt	MAC Receive Runt Count Register	N
0x8001_0080	BMCtl	MAC Bus Master Control Register	N
0x8001_0084	BMSts	MAC Bus Master Status Register	N
0x8001_0088	RXBCA	MAC Receive Buffer Current Address Register	N
0x8001_0090	RXDQBAdd	MAC Receive Descriptor Queue Base Address Register	N
0x8001_0094	RXDQBLen	MAC Receive Descriptor Queue Base Length Register	N
0x8001_0096	RXDQCurLen	MAC Receive Descriptor Queue Current Length Register	N
0x8001_0098	RXDCurAdd	MAC Receive Descriptor Current Address Register	N
0x8001_009C	RXDEnq	MAC Receive Descriptor Enqueue Register	N
0x8001_00A0	RXStsQBAdd	MAC Receive Status Queue Base Address Register	N
0x8001_00A4	RXStsQBLen	MAC Receive Status Queue Base Length Register	N
0x8001_00A6	RXStsQCurLen	MAC Receive Status Queue Current Length Register	N
0x8001_00A8	RXStsQCurAdd	MAC Receive Status Queue Current Address Register	N
0x8001_00AC	RXStsEnq	MAC Receive Status Enqueue Register	N
0x8001_00B0	TXDQBAdd	MAC Transmit Descriptor Queue Base Address Register	N
0x8001_00B4	TXDQBLen	MAC Transmit Descriptor Queue Base Length Register	N
0x8001_00B6	TXDQCurLen	MAC Transmit Descriptor Queue Current Length Register	N
0x8001_00B8	TXDQCurAdd	MAC Transmit Descriptor Current Address Register	N
0x8001_00BC	TXDEnq	MAC Transmit Descriptor Enqueue Register	N
0x8001_00C0	TXStsQBAdd	MAC Transmit Status Queue Base Address Register	N
0x8001_00C4	TXStsQBLen	MAC Transmit Status Queue Base Length Register	N
0x8001_00C6	TXStsQCurLen	MAC Transmit Status Queue Current Length Register	N
0x8001_00C8	TXStsQCurAdd	MAC Transmit Status Queue Current Address Register	N
0x8001_00D0	RXBufThrshld	MAC Receive Buffer Threshold Register	N
0x8001_00D4	TXBufThrshld	MAC Transmit Buffer Threshold Register	N
0x8001_00D8	RXStsThrshld	MAC Receive Status Threshold Register	N
0x8001_00DC	TXStsThrshld	MAC Transmit Status Threshold Register	N
0x8001_00E0	RXDThrshld	MAC Receive Descriptor Threshold Register	N
0x8001_00E4	TXDThrshld	MAC Transmit Descriptor Threshold Register	N
0x8001_00E8	MaxFrmLen	MAC Maximum Frame Length Register	N
0x8001_00EC	RXHdrLen	MAC Receive Header Length Register	N
0x8001_0100 - 0x8001_010C		Reserved	
0x8001_4000 - 0x8001_50FF	MACFIFO	MAC FIFO RAM	N
0x8002_xxxx	**USB**	**USB Registers**	N
0x8002_0000	HcRevision	USB Host Controller Revision	N

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Table 2-7: Internal Register Map (Continued)

Address	Register Name	Register Description	SW Lock
0x8002_0004	HcControl	USB Host Controller Control	N
0x8002_0008	HcCommandStatus	USB Host Controller Command Status	N
0x8002_000C	HcInterruptStatus	USB Host Controller Interrupt Status	N
0x8002_0010	HcInterruptEnable	USB Host Controller Interrupt Enable	N
0x8002_0014	HcInterruptDisable	USB Host Controller Interrupt Disable	N
0x8002_0018	HcHCCA	USB Host Controller HCCA	N
0x8002_001C	HcPeriodCurrentED	USB Host Controller Period CurrentED	N
0x8002_0020	HcControlHeadED	USB Host Controller Control HeadED	N
0x8002_0024	HcControlCurrentED	USB Host Controller Control CurrentED	N
0x8002_0028	HcBulkHeadED	USB Host Controller Bulk HeadED	N
0x8002_002C	HcBulkCurrentED	USB Host Controller Bulk CurrentED	N
0x8002_0030	HcDoneHead	USB Host Controller Done Head	N
0x8002_0034	HcFmInterval	USB Host Controller Fm Interval	N
0x8002_0038	HcFmRemaining	USB Host Controller Fm Remaining	N
0x8002_003C	HcFmNumber	USB Host Controller Fm Number	N
0x8002_0040	HcPeriodicStart	USB Host Controller Periodic Start	N
0x8002_0044	HcLSThreshold	USB Host Controller LS Threshold	N
0x8002_0048	HcRhDescriptorA	USB Host Controller Root Hub Descriptor A	N
0x8002_004C	HcRhDescriptorB	USB Host Controller Root Hub Descriptor B	N
0x8002_0050	HcRhStatus	USB Host Controller Root Hub Status	N
0x8002_0054	HcRhPortStatus[1]	USB Host Controller Root Hub Port Status 1	N
0x8002_0058	HcRhPortStatus[2]	USB Host Controller Root Hub Port Status 2	N
0x8002_005C	HcRhPortStatus[3]	USB Host Controller Root Hub Port Status 3	N
0x8002_0080	USBCtrl	USB Configuration Control	N
0x8002_0084	USBHCI	USB Host Controller Interface Status	N
0x8006_xxxx	**SDRAM**	**SDRAM Registers**	N
0x8006_0000		Reserved	
0x8006_0004	GlConfig	Control and status bits used in configuration	N
0x8006_0008	RefrshTimr	Set the period between refresh cycles	N
0x8006_000C	BootSts	Reflect the state of the boot mode option pins	N
0x8006_0010	SDRAMDevCfg0	Device configuration 0	N
0x8006_0014	SDRAMDevCfg1	Device configuration 1	N
0x8006_0018	SDRAMDevCfg2	Device configuration 2	N
0x8006_001C	SDRAMDevCfg3	Device configuration 3	N
0x8008_xxxx	**SMC**	**SMC Control Registers**	
0x8008_0000	SMCBCR0	Bank config Register 0 (used to program characteristics of the SRAM/ROM memory)	N
0x8008_0004	SMCBCR1	Bank config Register 1 (used to program characteristics of the SRAM/ROM memory)	N
0x8008_0008	SMCBCR2	Bank config Register 2 (used to program characteristics of the SRAM/ROM memory)	N

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Table 2-7: Internal Register Map (Continued)

Address	Register Name	Register Description	SW Lock
0x8008_000C	SMCBCR3	Bank config Register 3 (used to program characteristics of the SRAM/ROM memory)	N
0x8008_0010 - 0x8008_0014		Reserved	
0x8008_0018	SMCBCR6	Bank config Register 6 (used to program characteristics of the SRAM/ROM memory)	N
0x8008_001C	SMCBCR7	Bank config Register 7 (used to program characteristics of the SRAM/ROM memory)	N
0x8008_0020 - 0x8008_FFFC		Reserved	
0x8009_xxxx	**Boot ROM**	**Boot ROM Memory Locations**	
0x8009_0000		Boot ROM Start	N
0x8009_3FFF		Boot ROM End	N
0x800B_xxxx	**VIC1**	**Vectored Interrupt Controller 1 Registers**	
0x800B_0000	VIC1IRQStatus	IRQ status Register	N
0x800B_0004	VIC1FIQStatus	FIQ status Register	N
0x800B_0008	VIC1RawIntr	Raw interrupt status Register	N
0x800B_000C	VIC1IntSelect	Interrupt select Register	N
0x800B_0010	VIC1IntEnable	Interrupt enable Register	N
0x800B_0014	VIC1IntEnClear	Interrupt enable clear Register	N
0x800B_0018	VIC1SoftInt	Software interrupt Register	N
0x800B_001C	VIC1SoftIntClear	Software interrupt clear Register	N
0x800B_0020	VIC1Protection	Protection enable Register	N
0x800B_0030	VIC1VectAddr	Vector address Register	N
0x800B_0034	VIC1DefVectAddr	Default vector address Register	N
0x800B_0100	VIC1VectAddr0	Vector address 0 Register	N
0x800B_0104	VIC1VectAddr1	Vector address 1 Register	N
0x800B_0108	VIC1VectAddr2	Vector address 2 Register	N
0x800B_010C	VIC1VectAddr3	Vector address 3 Register	N
0x800B_0110	VIC1VectAddr4	Vector address 4 Register	N
0x800B_0114	VIC1VectAddr5	Vector address 5 Register	N
0x800B_0118	VIC1VectAddr6	Vector address 6 Register	N
0x800B_011C	VIC1VectAddr7	Vector address 7 Register	N
0x800B_0120	VIC1VectAddr8	Vector address 8 Register	N
0x800B_0124	VIC1VectAddr9	Vector address 9 Register	N
0x800B_0128	VIC1VectAddr10	Vector address 10 Register	N
0x800B_012C	VIC1VectAddr11	Vector address 11 Register	N
0x800B_0130	VIC1VectAddr12	Vector address 12 Register	N
0x800B_0134	VIC1VectAddr13	Vector address 13 Register	N
0x800B_0138	VIC1VectAddr14	Vector address 14 Register	N
0x800B_013C	VIC1VectAddr15	Vector address 15 Register	N
0x800B_0200	VIC1VectCntl0	Vector control 0 Register	N
0x800B_0204	VIC1VectCntl1	Vector control 1 Register	N

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Table 2-7: Internal Register Map (Continued)

Address	Register Name	Register Description	SW Lock
0x800B_0208	VIC1VectCntl2	Vector control 2 Register	N
0x800B_020C	VIC1VectCntl3	Vector control3 Register	N
0x800B_0210	VIC1VectCntl4	Vector control 4 Register	N
0x800B_0214	VIC1VectCntl5	Vector control 5 Register	N
0x800B_0218	VIC1VectCntl6	Vector control 6 Register	N
0x800B_021C	VIC1VectCntl7	Vector control 7 Register	N
0x800B_0220	VIC1VectCntl8	Vector control 8 Register	N
0x800B_0224	VIC1VectCntl9	Vector control 9 Register	N
0x800B_0228	VIC1VectCntl10	Vector control 10 Register	N
0x800B_022C	VIC1VectCntl11	Vector control 11 Register	N
0x800B_0230	VIC1VectCntl12	Vector control 12 Register	N
0x800B_0234	VIC1VectCntl13	Vector control 13 Register	N
0x800B_0238	VIC1VectCntl14	Vector control 14 Register	N
0x800B_023C	VIC1VectCntl15	Vector control 15 Register	N
0x800B_0FE0	VIC1PeriphID0	Peripheral identification Register bits 7:0	N
0x800B_0FE4	VIC1PeriphID1	Peripheral identification Register bits 15:8	N
0x800B_0FE8	VIC1PeriphID2	Peripheral identification Register bits 23:16	N
0x800B_0FEC	VIC1PeriphID3	Peripheral identification Register bits 31:24	N
0x800B_0FF0 - 0x800B_0FFC		Reserved	N
0x800C_xxxx	**VIC2**	**Vectored Interrupt Controller 2 Registers**	
0x800C_0000	VIC2IRQStatus	IRQ status Register	N
0x800C_0004	VIC2FIQStatus	FIQ status Register	N
0x800C_0008	VIC2RawIntr	Raw interrupt status Register	N
0x800C_000C	VIC2IntSelect	Interrupt select Register	N
0x800C_0010	VIC2IntEnable	Interrupt enable Register	N
0x800C_0014	VIC2IntEnClear	Interrupt enable clear Register	N
0x800C_0018	VIC2SoftInt	Software interrupt Register	N
0x800C_001C	VIC2SoftIntClear	Software interrupt clear Register	N
0x800C_0020	VIC2Protection	Protection enable Register	N
0x800C_0030	VIC2VectAddr	Vector address Register	N
0x800C_0034	VIC2DefVectAddr	Default vector address Register	N
0x800C_0100	VIC2VectAddr0	Vector address 0 Register	N
0x800C_0104	VIC2VectAddr1	Vector address 1 Register	N
0x800C_0108	VIC2VectAddr2	Vector address 2 Register	N
0x800C_010C	VIC2VectAddr3	Vector address 3 Register	N
0x800C_0110	VIC2VectAddr4	Vector address 4 Register	N
0x800C_0114	VIC2VectAddr5	Vector address 5 Register	N
0x800C_0118	VIC2VectAddr6	Vector address 6 Register	N
0x800C_011C	VIC2VectAddr7	Vector address 7 Register	N
0x800C_0120	VIC2VectAddr8	Vector address 8 Register	N
0x800C_0124	VIC2VectAddr9	Vector address 9 Register	N
0x800C_0128	VIC2VectAddr10	Vector address 10 Register	N

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Table 2-7: Internal Register Map (Continued)

Address	Register Name	Register Description	SW Lock
0x800C_012C	VIC2VectAddr11	Vector address 11 Register	N
0x800C_0130	VIC2VectAddr12	Vector address 12 Register	N
0x800C_0134	VIC2VectAddr13	Vector address 13 Register	N
0x800C_0138	VIC2VectAddr14	Vector address 14 Register	N
0x800C_013C	VIC2VectAddr15	Vector address 15 Register	N
0x800C_0200	VIC2VectCntl0	Vector control 0 Register	N
0x800C_0204	VIC2VectCntl1	Vector control 1 Register	N
0x800C_0208	VIC2VectCntl2	Vector control 2 Register	N
0x800C_020C	VIC2VectCntl3	Vector control3 Register	N
0x800C_0210	VIC2VectCntl4	Vector control 4 Register	N
0x800C_0214	VIC2VectCntl5	Vector control 5 Register	N
0x800C_0218	VIC2VectCntl6	Vector control 6 Register	N
0x800C_021C	VIC2VectCntl7	Vector control 7 Register	N
0x800C_0220	VIC2VectCntl8	Vector control 8 Register	N
0x800C_0224	VIC2VectCntl9	Vector control 9 Register	N
0x800C_0228	VIC2VectCntl10	Vector control 10 Register	N
0x800C_022C	VIC2VectCntl11	Vector control 11 Register	N
0x800C_0230	VIC2VectCntl12	Vector control 12 Register	N
0x800C_0234	VIC2VectCntl13	Vector control 13 Register	N
0x800C_0238	VIC2VectCntl14	Vector control 14 Register	N
0x800C_023C	VIC2VectCntl15	Vector control 15 Register	N
0x800C_0FE0	VIC2PeriphID0	Peripheral identification Register bits 7:0	N
0x800C_0FE4	VIC2PeriphID1	Peripheral identification Register bits 15:8	N
0x800C_0FE8	VIC2PeriphID2	Peripheral identification Register bits 23:16	N
0x800C_0FEC	VIC2PeriphID3	Peripheral identification Register bits 31:24	N
0x800C_0FF0 - 0x800C_0FFC		Reserved	N
0x8081_xxxx	**TIMER**	**Timer Registers**	
0x8081_0000	Timer1Load	Contains the initial value of the timer	N
0x8081_0004	Timer1Value	Gives the current value of the timer	N
0x8081_0008	Timer1Control	Provides enable/disable and mode configurations for the timer	N
0x8081_000C	Timer1Clear	Clears an interrupt generated by the timer	N
0x8081_0020	Timer2Load	Contains the initial value of the timer	N
0x8081_0024	Timer2Value	Gives the current value of the timer	N
0x8081_0028	Timer2Control	Provides enable/disable and mode configurations for the timer	N
0x8081_002C	Timer2Clear	Clears an interrupt generated by the timer	N
0x8081_0060 - 0x8081_0064		Reserved	
0x8081_0080	Timer3Load	Contains the initial value of the timer	N
0x8081_0084	Timer3Value	Gives the current value of the timer	N
0x8081_0088	Timer3Control	Provides enable/disable and mode configurations for the timer	N
0x8081_008C	Timer3Clear	Clears an interrupt generated by the timer	N

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Table 2-7: Internal Register Map (Continued)

Address	Register Name	Register Description	SW Lock
0x8082_xxxx	**I2S**	**I2S Registers**	N
0x8082_0000	I2STXClkCfg	Transmitter clock configuration Register	N
0x8082_0004	I2SRXClkCfg	Receiver clock configuration Register	N
0x8082_0008	I2SGISts	I2S Global Status Register. This reflects the status of the 3 RX FIFOs and the 3 TX FIFOs	N
0x8082_000C	I2SGICtrl	I2S Global Control Register	N
0x8082_0010	I2STX0Lft	Left Transmit data Register for channel 0	N
0x8082_0014	I2STX0Rt	Right Transmit data Register for channel 0	N
0x8082_0018	I2STX1Lft	Left Transmit data Register for channel 1	N
0x8082_001C	I2STX1Rt	Right Transmit data Register for channel 1	N
0x8082_0020	I2STX2Lft	Left Transmit data Register for channel 2	N
0x8082_0024	I2STX2Rt	Right Transmit data Register for channel 2	N
0x8082_0028	I2STXLinCtrlData	Transmit Line Control Register	N
0x8082_002C	I2STXCtrl	Transmit Control Register	N
0x8082_0030	I2STXWrdLen	Transmit Word Length	N
0x8082_0034	I2STX0En	TX0 Channel Enable	N
0x8082_0038	I2STX1En	TX1 Channel Enable	N
0x8082_003C	I2STX2En	TX2 Channel Enable	N
0x8082_0040	I2SRX0Lft	Left Receive data Register for channel 0	N
0x8082_0044	I2SRX0Rt	Right Receive data Register for channel 0	N
0x8082_0048	I2SRX1Lft	Left Receive data Register for channel 1	N
0x8082_004C	I2SRX1Rt	Right Receive data Register for channel 1	N
0x8082_0050	I2SRX2Lft	Left Receive data Register for channel 2	N
0x8082_0054	I2SRX2Rt	Right Receive data Register for channel 2	N
0x8082_0058	I2SRXLinCtrlData	Receive Line Control Register	N
0x8082_005C	I2SRXCtrl	Receive Control Register	N
0x8082_0060	I2SRXWrdLen	Receive Word Length	N
0x8082_0064	I2SRX0En	RX0 Channel Enable	N
0x8082_0068	I2SRX1En	RX1 Channel Enable	N
0x8082_006C	I2SRX2En	RX2 Channel Enable	N
0x8083_xxxx	**SECURITY**	**Security Registers**	
0x8083_2714	ExtensionID	Contains the Part ID for EP93XX devices	N
Contact Cirrus Logic for details regarding implementation of device Security measures.			
0x8084_xxxx	**GPIO**	**GPIO Control Registers**	
0x8084_0000	PADR	GPIO Port A Data Register	N
0x8084_0004	PBDR	GPIO Port B Data Register	N
0x8084_0008	PCDR	GPIO Port C Data Register	N
0x8084_000C	PDDR	GPIO Port D Data Register	N
0x8084_0010	PADDR	GPIO Port A Data Direction Register	N
0x8084_0014	PBDDR	GPIO Port B Data Direction Register	N

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Table 2-7: Internal Register Map (Continued)

Address	Register Name	Register Description	SW Lock
0x8084_0018	PCDDR	GPIO Port C Data Direction Register	N
0x8084_001C	PDDDR	GPIO Port D Data Direction Register	N
0x8084_0020	PEDR	GPIO Port E Data Register	N
0x8084_0024	PEDDR	GPIO Port E Data Direction Register	N
0x8084_0028 - 0x8084_002C		Reserved	
0x8084_0030	PFDR	GPIO Port F Data Register	N
0x8084_0034	PFDDR	GPIO Port F Data Direction Register	N
0x8084_0038	PGDR	GPIO Port G Data Register	N
0x8084_003C	PGDDR	GPIO Port G Data Direction Register	N
0x8084_0040	PHDR	GPIO Port H Data Register	N
0x8084_0044	PHDDR	GPIO Port H Data Direction Register	N
0x8084_0048		Reserved	
0x8084_004C	GPIOFIntType1	Register controlling type, level or edge, of interrupt generated by the pins of Port F	N
0x8084_0050	GPIOFIntType2	Register controlling polarity, high/low or rising/falling, of interrupt generated by Port F	N
0x8084_0054	GPIOFEOI	GPIO Port F End Of Interrupt Register	N
0x8084_0058	GPIOFIntEn	Interrupt Enable for Port F	N
0x8084_005C	IntStsF	GPIO Interrupt Status Register. Contains status of Port F interrupts after masking.	N
0x8084_0060	RawIntStsF	Raw Interrupt Status Register. Contains raw interrupt status of Port F before masking.	N
0x8084_0064	GPIOFDB	GPIO F Debounce Register	N
0x8084_0068 - 0x8084_008C		Reserved	
0x8084_0090	GPIOAIntType1	Register controlling type, level or edge, of interrupt generated by the pins of Port A	N
0x8084_0094	GPIOAIntType2	Register controlling polarity, high/low or rising/falling, of interrupt generated by Port A	N
0x8084_0098	GPIOAEOI	GPIO Port A End Of Interrupt Register	N
0x8084_009C	GPIOAIntEn	Controlling the generation of interrupts by the pins of Port A	N
0x8084_00A0	IntStsA	GPIO Interrupt Status Register. Contains status of Port A interrupts after masking.	N
0x8084_00A4	RawIntStsA	Raw Interrupt Status Register. Contains raw interrupt status of Port A before masking.	N
0x8084_00A8	GPIOADB	GPIO A Debounce Register	N
0x8084_00AC	GPIOBIntType1	Register controlling type, level or edge, of interrupt generated by the pins of Port B	N
0x8084_00B0	GPIOBIntType2	Register controlling polarity, high/low or rising/falling, of interrupt generated by Port B	N
0x8084_00B4	GPIOBEOI	GPIO Port B End Of Interrupt Register	N
0x8084_00B8	GPIOBIntEn	Controlling the generation of interrupts by the pins of Port B	N
0x8084_00BC	IntStsB	GPIO Interrupt Status Register. Contains status of Port B interrupts after masking.	N
0x8084_00C0	RawIntStsB	Raw Interrupt Status Register. Contains raw interrupt status of Port B before masking.	N
0x8084_00C4	GPIOBDB	GPIO B Debounce Register	N

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Table 2-7: Internal Register Map (Continued)

Address	Register Name	Register Description	SW Lock
0x8084_00C8	EEDrive	EEPROM pin drive type control. Defines the driver type for the EECLK and EEDAT pins	N
0x8088_xxxx	**AC'97**	**AC'97 Control Registers**	
0x8088_0000	AC97DR	Data read or written from/to FIFO	N
0x8088_0004	AC97RXCR	Control Register for receive	N
0x8088_0008	AC97TXCR	Control Register for transmit	N
0x8088_000C	AC97SR	Status Register	N
0x8088_0010	AC97RISR	Raw interrupt status Register	N
0x8088_0014	AC97ISR	Interrupt Status	N
0x8088_0018	AC97IE	Interrupt Enable	N
0x8088_001C		Reserved	
0x8088_0080	AC97S1Data	Data received/transmitted on SLOT1	N
0x8088_0084	AC97S2Data	Data received/transmitted on SLOT2	N
0x8088_0088	AC97S12Data	Data received/transmitted on SLOT12	N
0x8088_008C	AC97RGIS	Raw Global interrupt status Register	N
0x8088_0090	AC97GIS	Global interrupt status Register	N
0x8088_0094	AC97IM	Interrupt mask Register	N
0x8088_0098	AC97EOI	End Of Interrupt Register	N
0x8088_009C	AC97GCR	Main Control Register	N
0x8088_00A0	AC97Reset	RESET control Register	N
0x8088_00A4	AC97SYNC	SYNC control Register	N
0x8088_00A8	AC97GCIS	Global channel FIFO interrupt status Register	N
0x808A_xxxx	**SPI**	**SPI Control Registers**	
0x808A_0000	SSP1CR0	SPI1 Control Register 0	N
0x808A_0004	SSP1CR1	SPI1 Control Register 1	N
0x808A_0008	SSP1DR	SPI1 Data Register	N
0x808A_000C	SSP1SR	SPI1 Status Register	N
0x808A_0010	SSP1CPSR	SPI1 Clock Prescale Register	N
0x808A_0014	SSP1IIR	SPI1 Interrupt/Interrupt Clear Register	N
0x808B_xxxx	**IrDA**	**IrDA Control Registers**	
0x808B_0000	IrEnable	IrDA Interface Enable	N
0x808B_0004	IrCtrl	IrDA Control Register	N
0x808B_0008	IrAdrMatchVal	IrDA Address Match Value Register	N
0x808B_000C	IrFlag	IrDA Flag Register	N
0x808B_0010	IrData	IrDA Transmit and Receive FIFOs	N
0x808B_0014	IrDataTail	IrDA Data Tail Register	N
0x808B_0018 - 0x808B_001C		Reserved	
0x808B_0020	IrRIB	IrDA Receive Information Buffer	N
0x808B_0024	IrTR0	IrDA Test Register, Received byte count	N

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Table 2-7: Internal Register Map (Continued)

Address	Register Name	Register Description	SW Lock
0x808B_0088	MIIR	IrDA MIR Interrupt Register	N
0x808B_008C - 0x808B_018C		Reserved	
0x808C_xxxx	**UART1**	**UART1 Control Registers**	
0x808C_0000	UART1Data	UART1 Data Register	N
0x808C_0004	UART1RXSts	UART1 Receive Status Register	N
0x808C_0008	UART1LinCtrlHigh	UART1 Line Control Register - High Byte	N
0x808C_000C	UART1LinCtrlMid	UART1 Line Control Register - Middle Byte	N
0x808C_0010	UART1LinCtrlLow	UART1 Line Control Register - Low Byte	N
0x808C_0014	UART1Ctrl	UART1 Control Register	N
0x808C_0018	UART1Flag	UART1 Flag Register	N
0x808C_001C	UART1IntIDIntClr	UART1 Interrupt ID and Interrupt Clear Register	N
0x808C_0020		Reserved	
0x808C_0028	UART1DMACtrl	UART1 DMA Control Register	N
0x808C_0100	UART1ModemCtrl	UART1 Modem Control Register	N
0x808C_0104	UART1ModemSts	UART1 Modem Status Register	N
0x808C_0114 - 0x808C_0208		Reserved	
0x808C_020C	UART1HDLCCtrl	UART1 HDLC Control Register	N
0x808C_0210	UART1HDLCAddMtchVal	UART1 HDLC Address Match Value	N
0x808C_0214	UART1HDLCAddMask	UART1 HDLC Address Mask	N
0x808C_0218	UART1HDLCRXInfoBuf	UART1 HDLC Receive Information Buffer	N
0x808C_021C	UART1HDLCSts	UART1 HDLC Status Register	N
0x808D_xxxx	**UART2**	**UART2 Control Registers**	
0x808D_0000	UART2Data	UART2 Data Register	N
0x808D_0004	UART2RXSts	UART2 Receive Status Register	N
0x808D_0008	UART2LinCtrlHigh	UART2 Line Control Register - High Byte	N
0x808D_000C	UART2LinCtrlMid	UART2 Line Control Register - Middle Byte	N
0x808D_0010	UART2LinCtrlLow	UART2 Line Control Register - Low Byte	N
0x808D_0014	UART2Ctrl	UART2 Control Register	N
0x808D_0018	UART2Flag	UART2 Flag Register	N
0x808D_001C	UART2IntIDIntClr	UART2 Interrupt ID and Interrupt Clear Register	N
0x808D_0020	UART2IrLowPwrCntr	UART2 IrDA Low-power Counter Register	N
0x808D_0028	UART2DMACtrl	UART2 DMA Control Register	N
0x8092_xxxx	**RTC**	**RTC Control Registers**	
0x8092_0000	RTCData	RTC Data Register	N
0x8092_0004	RTCMatch	RTC Match Register	N
0x8092_0008	RTCSts	RTC Status/EOI Register	N
0x8092_000C	RTCLoad	RTC Load Register	N
0x8092_0010	RTCCtrl	RTC Control Register	N
0x8092_0108	RTCSWComp	RTC Software Compensation	N

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Table 2-7: Internal Register Map (Continued)

Address	Register Name	Register Description	SW Lock
0x8093_xxxx	**Syscon**	**System Control Registers**	
0x8093_0000	PwrSts	Power/state control state	N
0x8093_0004	PwrCnt	Clock/debug control status	N
0x8093_0008	Halt	Enter IDLE mode	N
0x8093_000C	Stby	Enter Standby mode	N
0x8093_0018	TEOI	Write to clear Watchdog interrupt	N
0x8093_001C	STFClr	Write to clear Nbflg, rstflg, pfflg and cldflg	N
0x8093_0020	ClkSet1	Clock speed control 1	N
0x8093_0024	ClkSet2	Clock speed control 2	N
0x8093_0040	ScratchReg0	Scratch Register 0	N
0x8093_0044	ScratchReg1	Scratch Register 1	N
0x8093_0050	APBWait	APB wait	N
0x8093_0054	BusMstrArb	Bus Master Arbitration	N
0x8093_0058	BootModeClr	Boot Mode Clear Register	N
0x8093_0080	DeviceCfg	Device configuration	Y
0x8093_0084	VidClkDiv	Video Clock Divider	Y
0x8093_0088	MIRClkDiv	MIR Clock Divider.	Y
0x8093_008C	I2SClkDiv	I2S Audio Clock Divider	
0x8093_0090	KeyTchClkDiv	Keyscan/Touch Clock Divider	Y
0x8093_0094	ChipID	Chip ID Register	Y
0x8093_009C	SysCfg	System Configuration	Y
0x8093_00C0	SysSWLock	Syscon Software Lock Register	N
0x8094_xxxx	**WATCHDOG**	**Watchdog Control Register**	N
0x8094_0000	Watchdog	Watchdog Timer Register	N
0x8094_0004	WDStatus	Watchdog Status Register	N
0x8095_0000 - 0x8FFF_FFFF		Reserved	

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Chapter 3

Boot ROM

3

3.1 Introduction

The Boot ROM allows a program or OS to boot from the following devices:

- SPI EEPROM
- FLASH/SyncFLASH or SROM
- Serial port

3.1.1 Boot ROM Hardware Operational Overview

The Boot ROM is an AHB slave device containing a 16 kbyte mask-programmed ROM. The AHB slave always operates with one wait state, so all data reads from the ROM use 2 HCLK cycles.

The ROM contains 3 code sections. The lower 8 kbytes contain the system boot code. The next 4 kbytes contain the first secure code block, and the top 4 kbytes contain the second secure code block. In non-secure boot, the lower 8 kbytes are accessible. In secure boot, one of the two secure code blocks is accessible. See Chapter 22, “Security,” for details.

On system reset, the ARM920T begins executing code at address zero. The system follows the Hardware Configuration controls to select the boot device that appears at address zero. If Internal Boot is selected, the Boot ROM is mapped to address zero and the ARM920T will execute the Boot ROM code.

3.1.1.1 Memory Map

The Boot ROM base address (ROM base) is fixed in the EP9301 at 0x8009_0000. It will alias on 16 kbyte intervals. When internal boot is active, the Boot ROM is double decoded and appears at its normal address space and at address zero. (The Boot ROM writes the BootModeClr in order to remap address 0x0 to be external memory while the Boot ROM code continues execution at 0x8009_0000.)

3.1.2 Boot ROM Software Operational Overview

The Boot ROM is a 16 kbyte mask-programmed ROM that controls the source of the first off-chip code executed by the EP9301. The code within the Boot ROM supports the following sources for the EP9301 initialization program:

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- UART1: Code is downloaded through UART1 into an on chip buffer and executed.
- SPI Serial ROM: Code is copied from an SPI Serial ROM into an on-chip buffer and executed.
- FLASH: Code present in FLASH memory is executed directly.

Note that the code retrieved via UART1 and the SPI Serial ROM is not intended to be a complete operating system image. It is intended to be a small (up to 2 kbyte) loader that will, in turn, retrieve a complete operating system image. This small loader can retrieve this complete image through UART1 or the SPI Serial ROM (just as the Boot ROM did) or it can be more sophisticated and retrieve it through the IrDA, USB, or Ethernet interfaces.

The Boot ROM code disables the ARM920T's MMU, so any loader program that is downloaded sees physical addresses. The loader is free to initialize the page tables and start the MMU and caches if needed.

The Boot ROM code also does not enable interrupts or timers, so that the system delivered to the user is in a known safe state and is ready for an operating system or for user code to be loaded.

3.1.2.1 Image Header

One of ASCII strings, "CRUS" or "SURC" must be present as a HeaderID prefixed to an executable image. This HeaderID must be present in images copied from the SPI serial ROM and from images programmed into FLASH.

3.1.2.2 Boot Algorithm

Following are the steps in the software boot process:

1. Remap memory.
2. Turn the green LED off and the red LED on.
3. Disable the watchdog.
4. Read the Boot State
5. Set up the Clocks to run from external clocks
6. Based on the Boot State memory width, do the following:
   A. initialize the SDRAM and FLASH memory interfaces for slow (maximum compatibility) operation.
   B. Initialize SRAM interfaces for slow operation as well.
   C. Perform minimal memory tests.
7. Based on the contents of the SysCfg register, start serial download.
   A. Initialize UART1 to 9600 baud, 8 bits, no parity, 1 stop bit.

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B. Output a “<” character.

C. Read 2048 (decimal count) characters from UART1 and store these in the internal Boot buffer (alias for the Ethernet Mac buffer)

D. Output a “>” to signify 2048 characters have been read.

E. Turn on Green LED

F. Jump to the start of the internal Boot Buffer.

8. If it is not Serial Download, attempt to read from SPI serial ROM, and then do the following:

   A. Check if the first 4 bytes from the serial ROM are equal to “CRUS” or to “SURC” in ASCII, verifying the HeaderID.

   B. Read the next 2048 (decimal count) bytes into the Internal Boot Buffer.

   C. Turn on Green LED

   D. Jump to the start of the Internal Boot Buffer.

9. Attempt to read the “CRUS” or “SURC” in ASCII in FLASH memory at (FLASH Base + 0x0000), verifying the HeaderID. This is read in for each FLASH Chip select, then do the following:

   A. Turn on Green LED

   B. Jump to the start of FLASH memory plus four bytes.

10. Attempt to read the “CRUS” or “SURC” in ASCII in FLASH memory at (FLASH Base + 0x1000), verifying the HeaderID. This is read in for each FLASH Chip select, and then do the following:

    A. Turn on Green LED

    B. Jump to the start of FLASH memory.

11. Attempt to read the “CRUS” or “SURC” HeaderID in ASCII in memory at 0xC000_0000 and 0xF000_0000, verifying the HeaderID. This is read in for SDRAM or SyncFLASH boot.

    A. Turn on Green LED

    B. Jump to memory location 0xC000_0004 or 0xF000_0004.

12. Attempt to read the “CRUS” or “SURC” HeaderID in ASCII in memory at 0xC000_1000 and 0xF000_1000, verifying the HeaderID. This is read in for SDRAM or SyncFLASH boot.

    A. Turn on Green LED

    B. Jump to memory location 0xC000_0000 or 0xF000_0000 .

13. Copy dummy vectors into low SDRAM

    A. Flash Green LED

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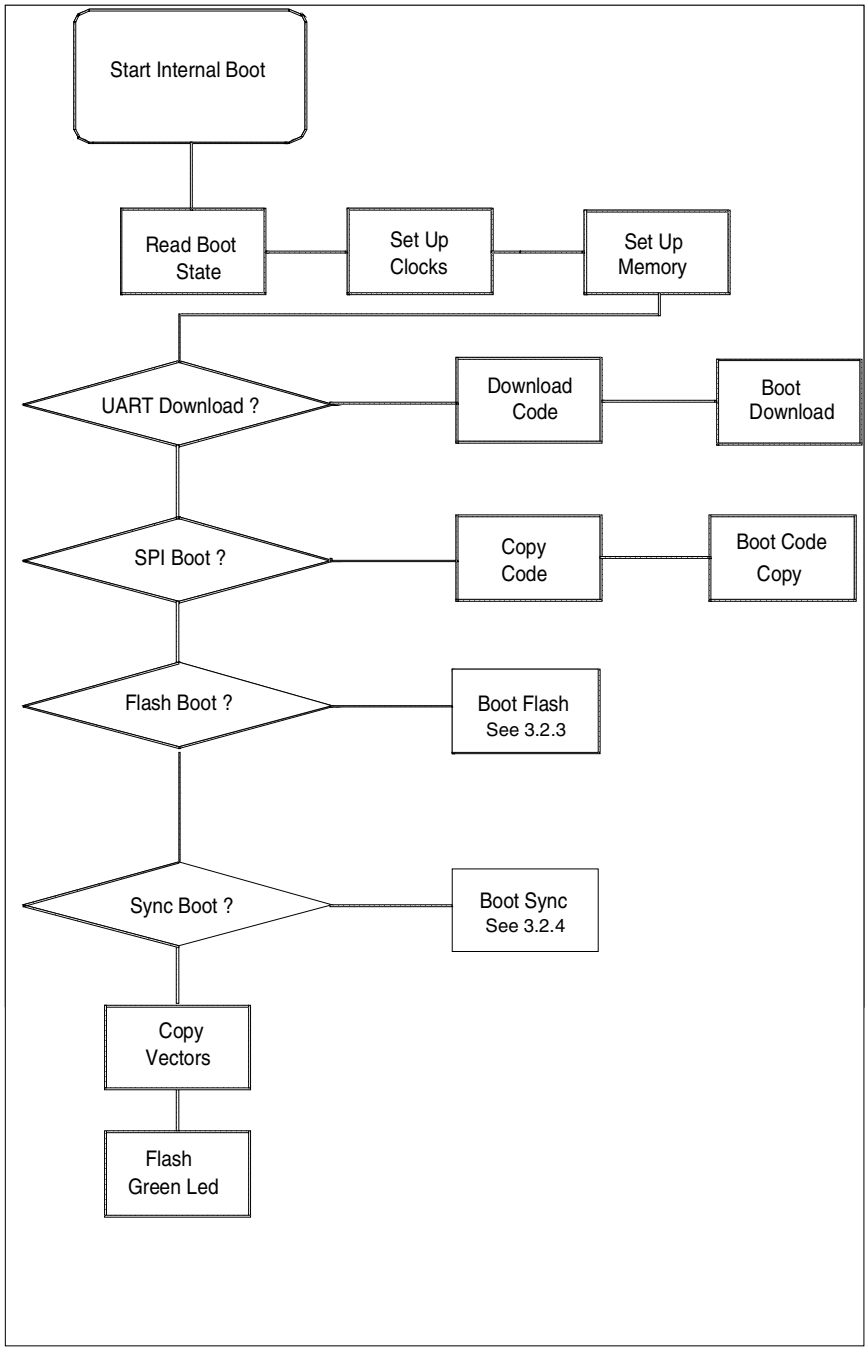
3.1.2.3 Flowchart

Figure 3-1 provides a flow chart for operation of the Boot ROM software.

Figure 3-1. Flow Chart of Boot ROM Software



3.2 Boot Options

Table 3-1 show configuration settings that are common to all boot modes.

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Table 3-1: Boot Configuration Options (Normal Boot)

EECLK	EEDAT	LBOOT1	LBOOT0	ASDO	CSn[7:6]	Boot Configuration
0	1	0	0	1	0 0 0 1	External boot from Sync memory space selected by DevCfg3 through the SDRAM Controller. The media type must be either SROM or SyncFLASH. The selection of the SRAM width is determined by latched **CSn[7:6]** value: 16-bit SFLASH 16-bit SROM
0	1	0	0	0	0 0 0 1	External boot from Async memory space selected by nCS0 through Synchronous Memory Controller. The selection of the SRAM width is determined by latched **CSn[7:6]** value: 8-bit SRAM 16-bit SRAM
1	1	0	1	x	01	16-bit serial boot
1	1	0	0	1	0 0 0 1	Internal boot from on-chip ROM. The selection of the ROM width is determined by latched **CSn[7:6]** value: 16-bit 16-bit
1	1	0	0	0	0 0 0 1	Internal boot from on-chip ROM. The selection of the ROM width is determined by latched **CSn[7:6]** value: 8-bit 16-bit

3.2.1 UART Boot

Make sure that the test pins are configured for internal boot mode. **EEDAT** and **LBOOT0** should be pulled high and **LBOOT1** should be pulled low as shown in Table 4-1 on page 69. UART 1 is configured at 9600 bps, 8-bits, No Parity, No flow control. The code performs the following steps:

1. A single “<“ is output by UART 1.
2. The “CRUS” or “SURC” signature is read.
3. 2048 characters are received by UART 1 and copied to the Ethernet buffer at address 0x8001_4000.
4. The processor will jump to 0x8001_4000. The processor will be in ARM SVC mode when the jump occurs.

3.2.2 SPI Boot

To boot from an SPI memory device, make sure that the test pins are configured for internal boot mode. **EEDAT** should be pulled high and **LBOOT1** and **LBOOT0** should be pulled low as shown in Table 4-1 on page 69.

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To boot from FLASH, put the “CRUS” or “SURC” signature at the first location in the SPI memory. The code will be copied from the SPI memory to the Ethernet buffer at address 0x8001_1000 with a length of 2048 bytes. Code execution will start at 0x8001_4000 (Mac base + 0x4000). Processor will be in ARM SVC mode. At this point the user can use the code in the MAC RAM to load the rest of the SPI memory data.

3.2.3 FLASH Boot

To enable FLASH boot, make sure that the pins are configured for normal boot mode, as shown in Table 3-1. Also make sure that the FLASH word size is correct as shown in Table 3-1.

To boot from FLASH, put the “CRUS” or “SURC” HeaderID at one of the following locations (this location will be referred to as FLASH base + 0x0):

0x1000_0000
0x2000_0000
0x3000_0000
0x6000_0000
0x7000_0000

Code execution will start at address (FLASH base + 0x4). Processor will be in ARM SVC mode.

Alternatively, to boot from FLASH put the “CRUS” or “SURC” HeaderID at one of the following locations (this location will be referred to as FLASH base + 0x1000):

0x1000_1000
0x2000_1000
0x3000_1000
0x6000_1000
0x7000_1000

Code execution will start at address (FLASH base + 0x0). The processor will be in ARM SVC mode.

3.2.4 SDRAM or SyncFLASH Boot

To enable SDRAM or SyncFLASH boot, make sure that the pins are configured for normal boot mode, as shown in Table 3-1. If booting with SyncFLASH, make sure the SDRAM or SyncFLASH word size is correct, as shown in Table 3-1. If booting with a 16-bit SDRAM device, follow the suggested software sequence of commands, as shown in Figure 3-2.

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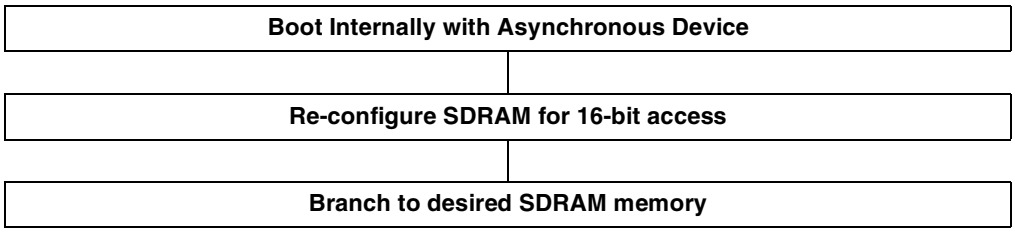
Figure 3-2. Flow chart of Boot Sequence for 16-bit SDRAM Devices



To boot from SDRAM or SyncFLASH, put the “CRUS” or “SURC” HeaderID at one of the following locations (this is Base + 0x0):

0xC000_0000
0xF000_0000

Code execution will start at address (Base + 0x4). Processor will be in ARM SVC mode.

Alternatively, to boot from SDRAM or SyncFLASH, put the “CRUS” or “SURC” HeaderID at one of the following locations (this is Base + 0x1000):

0xC000_1000
0xF000_1000

Code execution will start at address (Base + 0x0). The processor will be in ARM SVC mode.

3.2.5 Synchronous Memory Operation

If running from Synchronous memory, before issuing a software reset, perform the following procedure:

1. Run from SDRAM.
2. Perform a software reset (because of the SWRST bit in DEVCFG).
3. Run the internal boot code and boot to FLASH.
4. Set the PLL back to use the external clock.
5. Set up the SDRAM.
6. Load the programs to SDRAM.
7. Run from SDRAM.

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Chapter 4

System Controller

4.1 Introduction

The System Controller (Syscon) provides the EP9301 central clock and control resources. These central resources are:

- Clock control
- Power management
- System configuration management.

These resources are controlled by a set of software-locked registers which can be used to prevent accidental accesses. Syscon generates the various bus and peripheral clocks as well as controls the system startup configuration.

4.1.1 System Startup

System startup begins with the assertion of a reset signal. There are five different categories of reset events in the device. In order of decreasing effect, the reset events are:

- **PRSTn** (external pin for power-on reset)
- **RSTOn** (external pin for user reset)
- Three-key reset (externally generated, behaves like user reset)
- Watchdog reset (internally generated)
- Software reset (internally generated)

During the time that any reset is active, the system is halted until it exits the reset state.

When the device starts with an external **PRSTn** or **RSTOn**, certain hardware configurations are determined, and some system configuration information will be recorded so that software can access it. See the details in “System Reset” on page 67 and “Hardware Configuration Control” on page 68.

4.1.2 System Reset

The device system reset consists of several events and signals. It has four levels of reset control. They are:

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- Power-on-reset, controlled by **PRSTn** pin. It resets the entire chip with no exceptions.
- User reset, controlled by **RSTOn** pin. While active, it resets the entire chip, except certain system variables such as RTC, SDRAM refresh control/global configuration, and the registers in the Syscon.

Note: If PLLs are enabled, user reset does NOT disable or reset the PLLs. They retain their frequency settings.

- Three-key reset. When F2, F4, and F7 are pressed, a user reset (above) occurs.
- Software reset and watchdog reset. They perform the functions of the user reset (above), but are under software control.

Watchdog and PwrSts registers contain the information regarding which reset event occurred. Note that only the Watchdog timer contains information about a user-generated 3-key reset.

4.1.3 Hardware Configuration Control

The Hardware Configuration controls provide a mechanism to place the system into various boot configurations. In addition, one of several external boot memory options can be selected at system wake up.

The Hardware Configuration controls are defined by a set of device pins that are latched into configuration control bits on the assertion of chip reset on the rising edge of the **PRSTn** or **RSTOn** pin. The different hardware configuration bits define watchdog behavior, boot mode (internal or external), boot synchronicity, and external boot width. The latched pins are:

CSn[1] - Disable Watchdog reset timer
CSn[2] - Disable Watchdog reset duration
CSn[3] - Should be pulled upto “1”
EECLK - Select internal or external boot
EEDAT - Should be pulled upto “1”
BOOT[1:0] - Select boot mode
ASDO - Select synchronous or asynchronous boot
CSn[7:6] - Select external boot width

The latched version of these signals have an “L” prefix, and are readable by software in the SysCfg register.

The Hardware Control configurations are as show in Table 4-1.

The normal boot function is described in Chapter 3, Boot ROM.

Serial boot is functionally identical to normal boot except that the SBoot bit in the SysCfg register is set. This mode is available for a software configuration option that is readable by the boot code.

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In either normal boot or serial boot mode, once the chip starts up, it will begin to execute the instruction at logical address 0x0000_0000. Various configuration options are provided to select the different memory elements for booting from location 0. The options are listed in Table 4-1.

Table 4-1: Boot Configuration Options

EECLK	EEDAT	LBOOT1	LBOOT0	ASDO	CSn[7:6]	Boot Configuration
0	1	0	0	1	0 0 0 1	External boot from Sync memory space selected by DevCfg3 through the SDRAM Controller. The media type must be either SROM or SyncFLASH. The selection of the SRAM width is determined by latched **CSn[7:6]** value: 16-bit SFLASH 16-bit SROM
0	1	0	0	0	0 0 0 1	External boot from Async memory space selected by nCS0 through Synchronous Memory Controller. The selection of the SRAM width is determined by latched **CSn[7:6]** value: 8-bit SRAM 16-bit SRAM
1	1	0	1	x	01	16-bit serial boot
1	1	0	0	1	0 0 0 1	Internal boot from on-chip ROM. The selection of the ROM width is determined by latched **CSn[7:6]** value: 16-bit 16-bit
1	1	0	0	0	0 0 0 1	Internal boot from on-chip ROM. The selection of the ROM width is determined by latched **CSn[7:6]** value: 8-bit 16-bit

4.1.4 Software System Configuration Options

There are several system configuration options selectable by the DeviceCfg and SysCfg registers. These registers provide the selection of several pin multiplexing options and also provide software access to the system reset configuration options. Please refer to the descriptions of the registers, “DeviceCfg” on page 91 and “SysCfg” on page 97, for a detailed explanation.

4.1.5 Clock Control

The device uses a flexible system to generate the required clocks. The goal of the clock system is to generate as many as 20 independent clock frequencies, some with very tight accuracy requirements, all from a single external low-frequency crystal or other external clock source. The system was designed so that once it has been configured, the processor speed and bus speeds can be set to a number of different speeds without affecting the speeds of the other clocks in the system.

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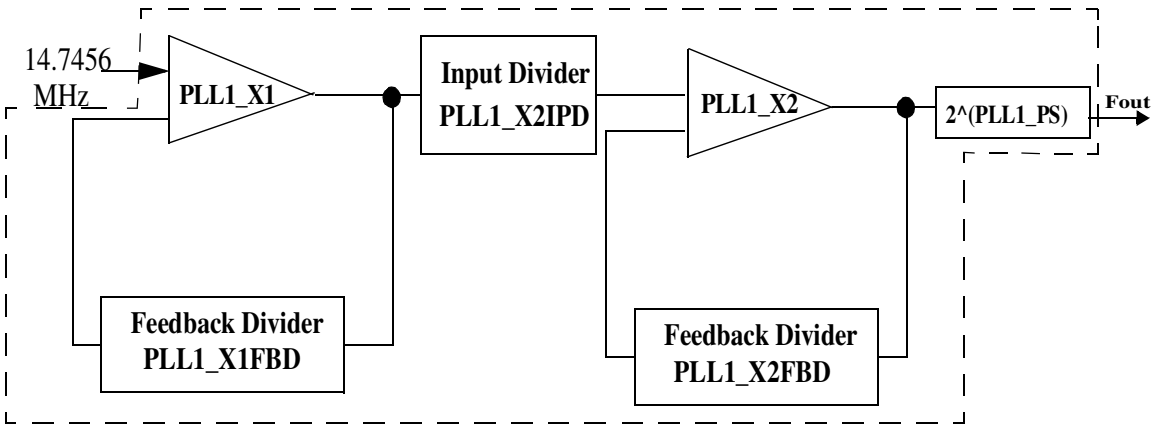
4.1.5.1 Oscillators and Programmable PLLs

The device has an interface to two external crystal oscillators with the frequency of 32 kHz and 14.7456 MHz. To generate the required high-frequency clocks, the system uses two phase-locked-loops (PLLs) to multiply the incoming 14.7456 MHz low frequency signal to much higher frequencies (up to about 400 MHz) that are then divided down by programmable dividers to produce the needed clocks. The PLLs operate independently of one another.

The system is split into two “trunks”, each of which is driven by one of the PLLs. The processor and bus clocks are derived from trunk 1 (PLL1). The USB and FIR clocks are derived from trunk 2 (PLL2). Other low-frequency clocks are divided from the original crystal frequency. The MIR and audio clocks can be independently sourced from either trunk. Figure 4-1, below, shows the PLL1 structure used in the EP9301. Since PLL2 is identical to PLL1, wherever the phrase of “PLL1” is used in the figure, it applies to PLL2 as well.

Figure 4-1. Phase Locked Loop (PLL) Structure



Both PLLs are software programmable (each value is defined in ClkSet1 and ClkSet2 registers respectively). The frequency of output clock Fout shows in the next equation:

$$\text{Fout} = 14.7456\text{MHz} \cdot \frac{(\text{PLL1_X1FBD} + 1) \times (\text{PLL1_X2FBD} + 1)}{(\text{PLL1_X2IPD} + 1) \times 2^{\text{PLL1_PS}}}$$

Here PLL1_X1FBD, PLL1_X2FBD, PLL1_X2IPD and PLL1_PS are the bit fields in ClkSet1 register. The user must be aware of the requirements of PLL operation. They are:

- PLL1_X1 desired reference clock frequency range is > 11.058 MHz and < 166 MHz
- PLL1_X1 output frequency range is > 294 MHz and < 368 MHz

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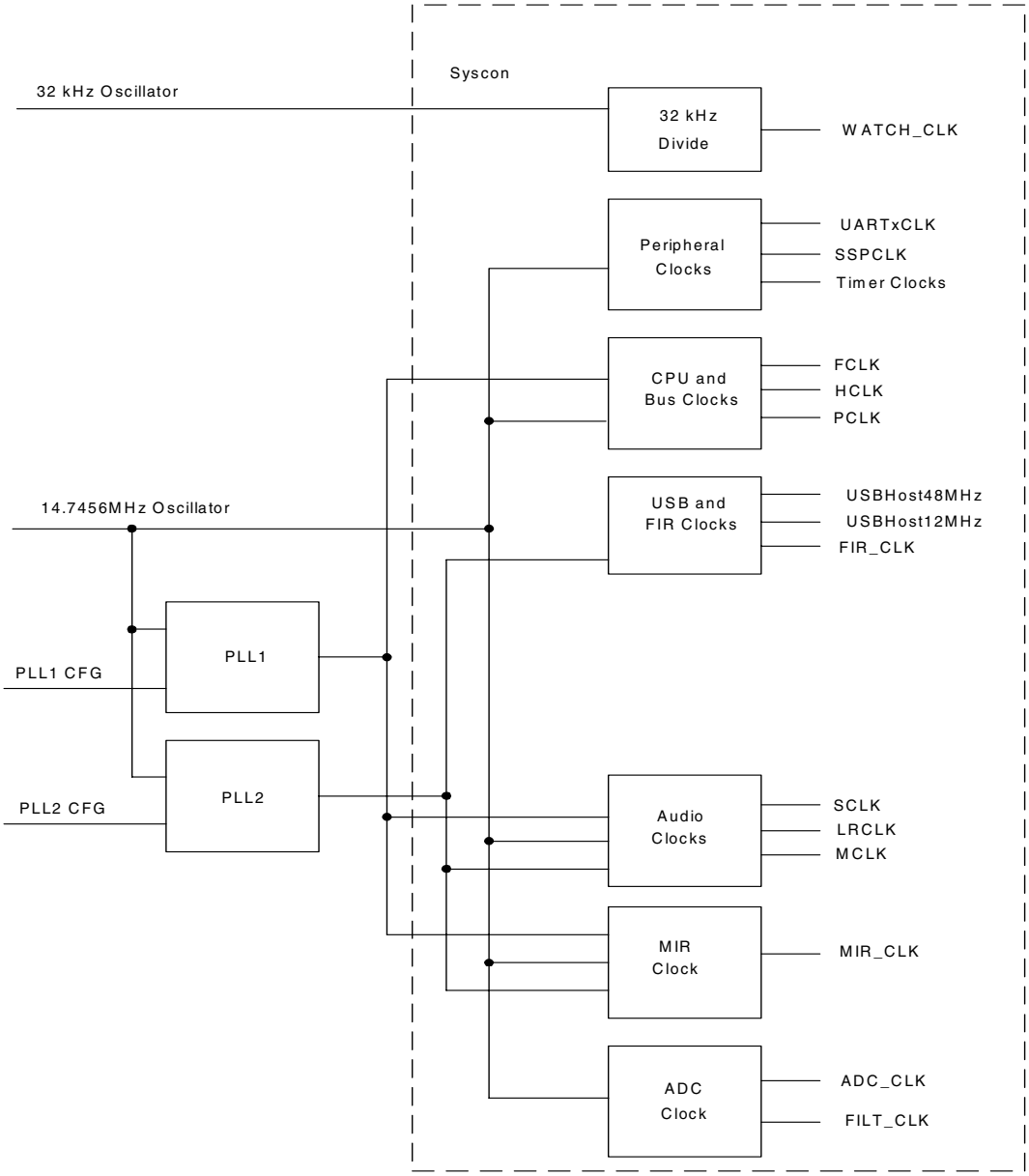
- PLL1_X2 desired reference clock frequency (after PLL1_X2IPD divider) is > 12.9 MHz and < 166 MHz.
- PLL1_X2 output, BEFORE the PS divide, must be > 290 MHz and <= 528 MHz

Again, the same conditions are applied to PLL2 as well.

4.1.5.2 Bus and Peripheral Clock Generation

Figure 4-2 illustrates the clock generation system.

Figure 4-2. EP9301 Clock Generation System



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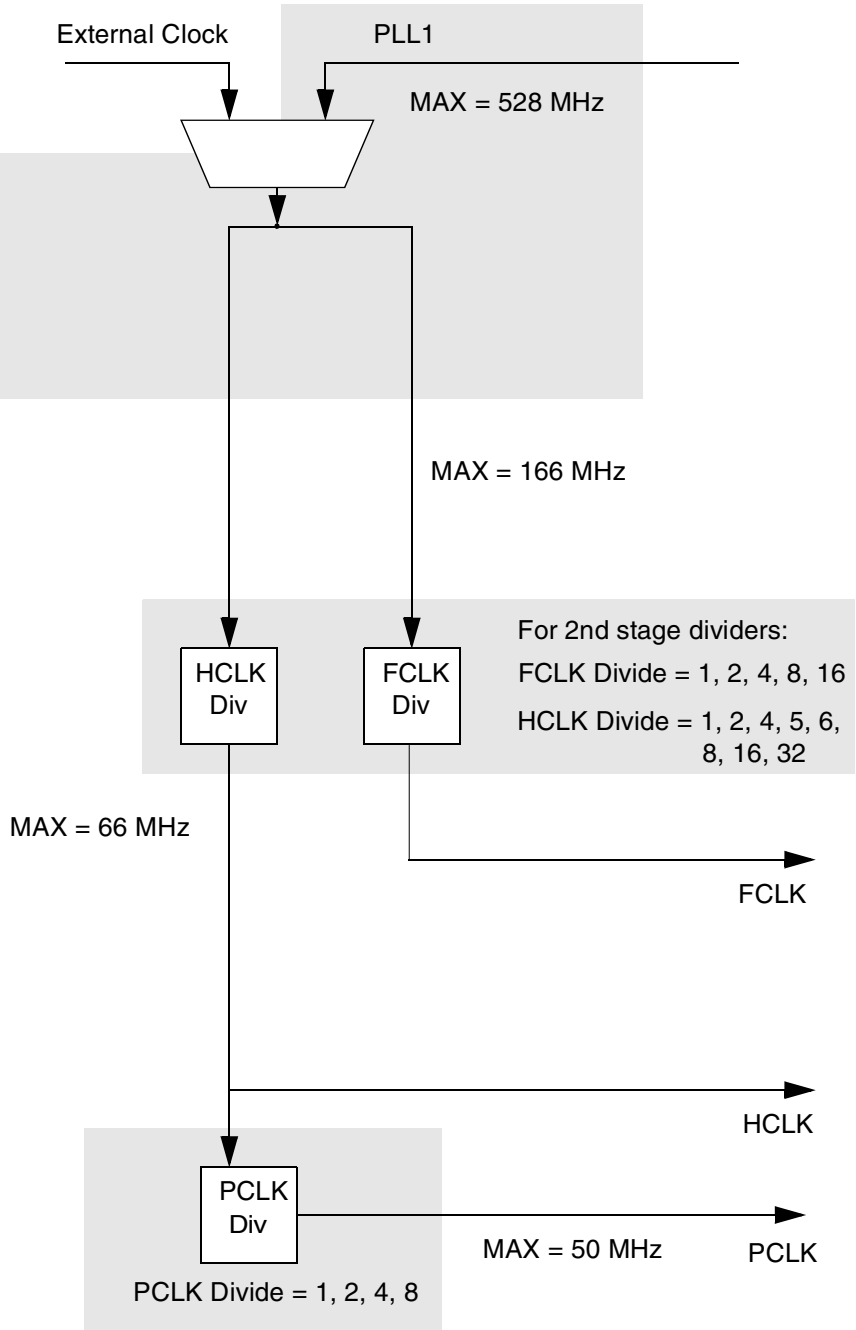
4.1.5.2.1 Bus Clock Generation

Figure 4-3 shows the flow of generated system bus clocks, including the ARM processor clock (FCLK), the AHB bus clock (HCLK), and the APB bus clock (PCLK).

Figure 4-3. Bus Clock Generation



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There are some limitations of each clock. FCLK must be <=166 MHz, HCLK<=66 MHz and PCLK<=50 MHz and FCLK >= HCLK > PCLK. Refer to register, “ClkSet1” on page 84, for the detailed configuration information regarding the divider bit fields.

It also must be pointed out that even though FCLK is the ARM processor clock, the ARM Processor has the option to run the CPU using HCLK. The ARM9 Processor supports three different clocking modes:

- Async mode
- Sync mode
- Fast Bus mode

Both Async mode and Sync mode use FCLK and potentially FCLK can be faster than HCLK which would yield higher CPU performance. Async mode and Sync mode have different clock skew requirements between FCLK and HCLK, associated with different throughput penalties due to the clock synchronization. Fast Bus mode bypasses FCLK, and the ARM runs from HCLK. In this mode, the ARM potentially has lower performance than the other two modes. **When the device starts up, it defaults to Fast Bus mode.** (The selection of ARM clocking modes is determined by the iA and nF bits in the ARM co-processor 15 register 1.)

4.1.5.2.2 Peripheral Clock Generation

The MCLK and MIR_CLK generators are identical blocks. Each block contains a pre-divider of 2, 2.5 and 3 followed by a 7-bit programmer divider. The audio clocks SCLK and LRCLK are further divided down from MCLK. The registers, “MIRClkDiv” on page 93 and “I2SClkDiv” on page 94, show the details.

USB uses a 48 MHz clock generated by PLL2. USBDIV, in register ClkSet2, is used to divide the frequency down from the PLL2 output.

Table 4-2 on page 74 describes the speeds and sources for the various clocks on the EP9301.

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Table 4-2: Clock Speeds and Sources

Block	Clocks Used	Clock Source
SSP	7.3728 MHz	Divided by 2 from 14.7456 MHz external oscillator.
UART1 UART2	14.7456 MHz 7.3728 MHz	Both are derived from 14.7456 MHz external oscillator.
AAC	2.9491 MHz	Divided-by-5 from the 14.7456MHz external oscillator.
Timers	508.4689 KHz 1.9939 KHz 983 KHz	All divided by the 14.7456 MHz external oscillator.
Watchdog	256 Hz	Tap from the 32 kHz RTC clock.

4.1.5.3 Steps for Clock Configuration

The following is a step-by-step procedure for configuring the clocks. The boot ROM contains code which performs the following steps for a 14.7456 MHz crystal. (For details, refer to Boot ROM, Chapter 3 on page 59.) The actual register values should be taken from the register descriptions for the desired clock setup.

1. After power up, the reset state of all clock control registers (all bits zero) will ensure that FCLK and HCLK are running at the crystal oscillator frequency (14.7456 MHz).
2. Configure PLL1 to multiply by the desired value, set HCLK and FCLK rates, and power it up. To do this: write the proper value (taken from the register table) to ClkSet1 immediately followed by 5 NOP instructions to flush the ARM920T instruction pipeline. The system will go into Standby while PLL1 stabilizes, then return to normal operation at the new clock rates.
3. Configure PLL2 to multiply by the desired value. To do this, write the proper value to ClkSet2.
4. Wait for PLL2 to stabilize (at least 1 ms).

   Note: The PWRSts register can be checked to confirm the PLLs are locked.

5. Program all other clock dividers to the desired values and enable them. The clocks won't actually begin running until the trunks which feed them are enabled later. Write to the following registers:
   - MIRClkDiv
   - I2SClkDiv
   - ADCClkDiv
6. All peripherals are now running from divided PLL outputs. Once the clocks have been configured, the frequency of any peripheral clock can be changed on-the-fly. To do this, perform a write to the clock register with the

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new divisor value and then set the appropriate enable bit. This ensures a problem-free change of the clock.

4.1.6 Power Management

The device follows a power-saving design plan. Power management is done by either altering the PLLs or the clock system frequency or by shutting off clocks to unused blocks. Also, there are several system power states to which the device can transition in order to save power. Care must be taken to ensure the clock system is not put into a non-operational state and that clock system dependencies are observed.

4.1.6.1 Clock Gatings

The list of peripherals with PCLK gating is shown Table 4-3. One should refer to the appropriate chapters in this User's Manual to find detailed information about clock gatings for that peripheral.

Table 4-3: Peripherals with PCLK gating

Peripheral	Peripheral/PCLK on with Enable or Register Access	PCLK on with Register Access Only	PCLK Continuous
UART1	**x**	-	-
UART2	**x**	-	-
IRDA	**x**	-	-
SEC	**x**	-	-
I2S	**x**	-	-
Watchdog	-	-	**x**
AAC	**x**	-	-
SSP	**x**	-	-
RTC	-	-	**x**
GPIO	-	**x**	-

The HCLK going to USB Host can be gated off as well to further save the power. The USH_EN bit in PwrCnt register serves the purpose.

4.1.6.2 System Power States

The device has three power states:

- Run mode: Normal operation mode.
- Halt: ARM9 Processor stops executing.
- Standby: Power is on. Only SDRAM self-refresh and RTC run.

Figure 4-4 illustrates the transitions among those states.

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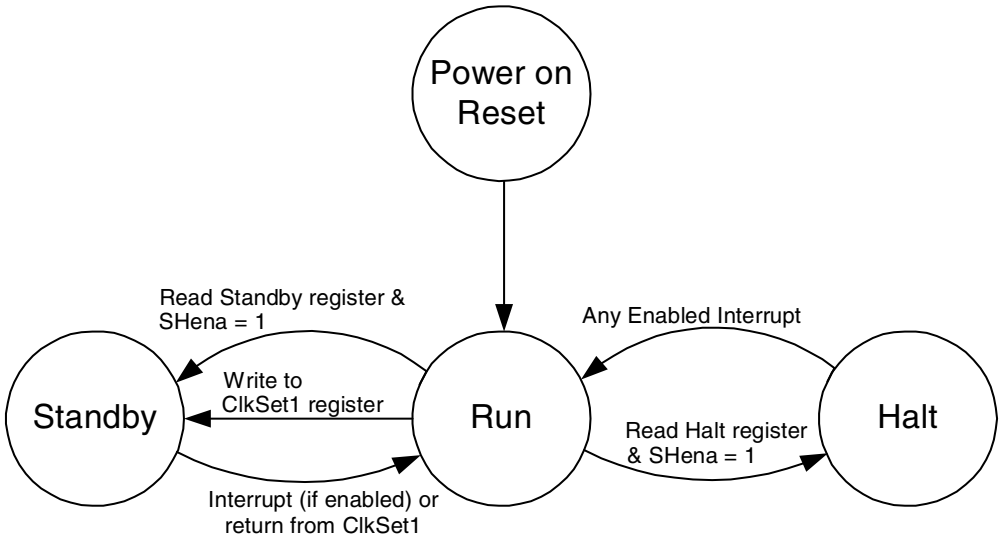
Figure 4-4. EP9301 Power States and Transitions



4.1.6.2.1 Power-on-Reset Run

During power-on-reset, the chip automatically transition into the run mode.

4.1.6.2.2 Run Standby Mode

Once in the running mode, it is possible to move to the Standby state under the following conditions:

- A read from the Standby register when SHena bit in register DeviceCfg is set to 1. This triggers the system to enter STANDBY mode.
- A write to the ClkSet1 register.

When the SHena bit is set to 1 and the user tries to read from the Standby location, the device is forced into the Standby state. After this transition the state controller will hold the Standby state before re-loading and allowing the transition to the operating state.

A write to the ClkSet1 register will also trigger the system to go into Standby mode. However, the system will automatically come back to normal operation after new clock settings take effect. The amount of time EP9301 remains in the Standby state depends on whether the PLL is enabled, or if EP9301 is using the external clock. If the PLL is enabled, EP9301 will remain in Standby until the PLL is locked. If EP9301 is in PLL bypass mode (nBYP1 = 1), then EP9301 will remain in the Standby state for 1-2 of the 16.384 kHz clock cycles. This is to ensure a minimum 'off' time. The 16.384 kHz clock, derived from the 32 kHz divide chain times how long the system, remains in the Standby state.

When the device normally enters Standby mode, the SDRAM controller puts the SDRAM into self-refresh before disabling the clocks. This condition is only

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true if the refresh enable bit (RFSHEN) in the SDRAM controller is set. One example of this is when a power-on-reset is applied and this register bit is cleared. This means that this bit will not be set on bootup and will have to be set to maintain the memory image for when the device re-enters Standby mode.

4.1.6.2.3 RUN HALT mode

A transition from Run mode to Halt mode is caused by reading the Halt location with the SHena bit set to 1. This has the effect of gating the processor clock (FCLK) bus interface, with the APB/AHB system clock, and Memory/DMA system remaining enabled.

4.1.6.2.4 STANDBY RUN mode

There are normally several conditions in which the device can move from Standby mode to Run mode.

These conditions are:

- A falling edge on **Nirq** - Global IRQ interrupt
- A falling edge on **Nfiq** - Global FIQ interrupt
- An exit from a ClkSet1 write
- **PRSTn**
- **RSTOn**

The chip comes out of Standby if an interrupt occurs or when an exit from a ClkSet1 write occurs. If a write is performed to the ClkSet1 register, the EP9301 will enter Standby and then will automatically come out of Standby and back into the Run state.

4.1.6.2.5 HALT RUN mode

The transition from the Halt state to the running state is caused by:

- a falling edge on **Nirq** - Global IRQ interrupt
- a falling edge on **Nfiq** - Global FIQ interrupt
- **RSTOn**

4.1.7 Interrupt Generation

The Syscon block generates two interrupts: TICK interrupt and Watchdog Expired interrupt.

The block generates the TICK interrupt based upon the 64 Hz clock which is derived from the 32 kHz oscillator. The interrupt becomes active on every rising edge of the internal 64 Hz clock signal. It can be cleared by writing to the TEOI location.

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Watchdog Expired interrupt becomes active on a rising edge of the 64 Hz TICK clock, if the TICK interrupt is still active. In other words, if a TICK interrupt has not been served for a complete TICK period, a watchdog expired interrupt is generated. It can be cleared by writing to the TEOI location as well.

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4.2 Registers

This section contains the detailed register descriptions for registers in the Syscon block. Table 4-4 shows the address map for the registers in this block, followed by a detailed listing for each register.

Table 4-4: Syscon Register List

Address	Name	SW Locked	Type	Size	Description
0x8093_0000	PwrSts	No	R	32	Power/state control state
0x8093_0004	PwrCnt	No	R/W	32	Clock/Debug control status
0x8093_0008	Halt	No	R	32	Reading this location enters Halt mode.
0x8093_000C	Standby	No	R	32	Reading this location enters Standby mode.
0x8093_0018	TEOI	No	W	32	Write to clear Tick interrupt
0x8093_001C	STFClr	No	W	32	Write to clear CLDFLG, RSTFLG and WDTFLG.
0x8093_0020	ClkSet1	No	R/W	32	Clock speed control 1
0x8093_0024	ClkSet2	No	R/W	32	Clock speed control 2
0x8093_0040	ScratchReg0	No	R/W	32	Scratch register 0
0x8093_0044	ScratchReg1	No	R/W	32	Scratch register 1
0x8093_0050	APBWait	No	R/W	32	APB wait
0x8093_0054	BusMstrArb	No	R/W	32	Bus Master Arbitration
0x8093_0058	BootModeClr	No	W	32	Boot Mode Clear register
0x8093_0080	DeviceCfg	Yes	R/W	32	Device configuration
0x8093_0084	-	-	-	-	Reserved
0x8093_0088	MIRClkDiv	Yes	R/W	32	MIR Clock Divider, divides MIR clock for MIR IrDA
0x8093_008C	I2SClkDiv	Yes	R/W	32	I2S Audio Clock Divider
0x8093_0090	ADCClkDiv	Yes	R/W	32	ADC Clock Divider
0x8093_0094	ChipID	Yes	R/W	32	Chip ID Register
0x8093_009C	SysCfg	Yes	R/W	32	System Configuration
0x8093_00A0	-	-	-	-	Reserved
0x8093_00C0	SysSWLock	No	R/W	1 bit	Software Lock Register

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Register Descriptions

PwrSts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CHIPMAN								CHIPID							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WDTFLG	RSVD	CLDFLG	TEST_ RESET	RSTFLG	SW_ RESET	PLL2_ LOCK_REG	PLL2_ LOCK	PLL1_ LOCK_REG	PLL1_ LOCK	RTCDIV					

Address:

0x8093_0000 - Read Only

Definition:

The PwrSts system control register is the Power/State control register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RTCDIV: The 6-bit RTCDIV shows the number of 64-seconds which have elapsed. It is the output of the divide-by-64 chain that divides the 64 Hz TICK clock down to 1 Hz though showing an incrementing count. The MSB is the 1 Hz output; the LSB is the 32 Hz output. It is reset by power-on-reset to 000000b.

PLL1_LOCK: PLL1 lock. This signal goes high when PLL1 is locked and it is at the correct frequency.

PLL1_LOCK_REG: Registered PLL1 lock. This is a one-shot registered signal of the PLL1_LOCK signal. It is only cleared on a power-on-reset, when EP9301 enters the Standby state or when PLL1 is powered down.

PLL2_LOCK: PLL2 lock. This signal goes high when PLL2 is locked, and it is at the correct frequency.

PLL2_LOCK_REG: Registered PLL2 lock. This is a one-shot registered signal of the PLL2_LOCK signal. It is only cleared on a power-on-reset, when ClkSet2 is written, EP9301 enters the Standby state, or PLL2 is powered down.

SW_RESET: Software reset flag. This bit is set if the software reset has been activated. It is cleared by writing to the STFClr location. On power-on-reset, it is reset to 0b.

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RSTFLG: Reset flag. This bit is set if the user reset button has been pressed; forcing the **RSTOn** input low. It is cleared by writing to the STFClr location. On power-on-reset, it is reset to 0b.

TEST_RESET: Test reset flag. This bit is set if the test reset has been activated; it is cleared by writing to the STFClr location. On power-on-reset, it is reset to 0b.

CLDFLG: Cold start flag. This bit is set if EP9301 has been reset with a power-on-reset; it is cleared by writing to the STFClr location. On power-on-reset, it is set to 1b.

WDTFLG: Watchdog Timer flag. This bit is set if the Watchdog timer resets the system. It is cleared by writing to the STFClr location. It is reset to 0.

CHIPID: Chip ID bits. This 8-bit register determines the Chip Identification for EP9301. For EP9301, this value is 0x20.

CHIPMAN: This 8-bit register determines the Chip Manufacturer ID for EP9301. For EP9301, this value is 0x43.

PwrCnt

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FIR_EN	RSVD	UART BAUD	USH_EN	DMA M2M CH1	DMA M2M CH0	DMA M2P CH8	DMA M2P CH9	DMA M2P CH6	DMA M2P CH7	DMA M2P CH4	DMA M2P CH5	DMA M2P CH2	DMA M2P CH3	DMA M2P CH0	DMA M2P CH1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															

Address:

0x8093_0004 - Read / Write

Definition:

The PwrCnt system control register is the Clock/Debug control status register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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DMA M2M/P CHx: These bits enable the clocks to the DMA controller channels. Note that a channels-enable bit MUST be asserted before any register within the DMA controller can be read or written. At least one ARM instruction cycle must occur between writing to this register to enable the DMA Controller channel and actually accessing it. The number of cycles will depend on the setting of HCLK and PCLK division in the ClkSetx register. To save power, ensure that all these bits are disabled (low) if the DMA controller is not being used. On a system reset, the register will be reset to zero.

USH_EN: This bit is used to gate the HCLK to the USB Host block in order to save power. It is reset to zero, thus gating off the HCLK. It can be set to one to turn on the HCLK to the USB Host. This bit must be set before any register within the USB Host can be accessed. At least one ARM instruction cycle must occur between writing to this register bit and actually accessing the USB Host. The number of cycles will depend on the setting of HCLK and PCLK division in the ClkSetx register.

This bit is also used to gate the 48 MHz and 12 MHz clocks to the USB Host block in order to save power. It is reset to zero, thus gating off the USB Host clocks. By setting this to one, the USB Host clocks are enabled. At least one ARM instruction cycle must occur between writing to this register bit and actually accessing the USB Host. The number of cycles will depend on the wake-up time for PLL2. To find out if PLL2 has locked on to its frequency, the PLL2_LOCK bit in the PwrSts register can be read.

UARTBAUD: This bit controls the clock input to the UARTs. When cleared, the UARTs are driven by the 14.7456 MHz clock divided by 2 (7.3728 MHz). This gives a maximum baud-rate of 230 Kbps. When set, the UARTs are driven by the 14.7456 MHz clock directly, giving an increased maximum baud rate of 460 Kbps. This bit is 0 on reset.

FIR_EN: This bit is used to gate the FIRCLK to the IrDA block in order to save power. It is reset to zero, thus gating off the FIRCLK. Setting this bit to one will turn on the 48 MHz clock to the IrDA.

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Standby and Halt

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															

Address:

Standby - 0x8093_000C - Read Only
Halt - 0x8093_0008 - Read Only

Definition:

The Standby and Halt registers allow entry into the power saving modes. A read to the Halt location will initiate a request for the system to enter Halt mode, if the SHena bit is set in the DeviceCfg register in Syscon. Likewise a read to Standby will request entry into Standby only when the SHena bit is set.

Note: When a read is performed to the Standby location, it must be immediately followed by 5 NOP instructions. This is needed to flush the instruction pipeline in the ARM920T core. Writes to these locations have no effect.

Bit Descriptions:

RSVD: There are no readable bits in this register.

TEOI

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															

Address:

0x8093_0018 - Write

Definition:

Writing to the TEOI location will clear the periodic Watchdog expired interrupt (WEINT) and the 64 Hz TICK interrupt (TINT). Any data written to the register triggers the clearing.

Bit Descriptions:

RSVD: There are no readable bits in this register.

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STFClr

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															

Address:

0x8093_001C - Write

Definition:

Writing to the STFClr location will clear the CLDFLG, WDTFLG and RSTFLG in the register, “PwrSts” on page 80. Any data written to the register triggers the clearing.

Bit Descriptions:

RSVD: There are no readable bits in this register.

ClkSet1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD				FCLK DIV			SMC ROM	nBYP1	HCLK DIV			PCLK DIV		PLL1_PS	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PLL1 X1FBD1				PLL1 X2FBD2								PLL1 X2IPD			

Address:

0x8093_0020 - Read/Write

Definition:

The ClkSet1 system control register is one of two register that control clock speeds.

Note: When a write is performed to the ClkSet1 location, it must be immediately followed by 5 NOP instructions. This is needed to flush the instruction pipeline in the ARM920T core. Writing to this register will cause the EP9301 to enter Standby for between 8 ms to 16 ms. Reading from this register will not cause an entry into Standby mode.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PLL1_X2IPD: These 5 register bits set the input divider for PLL1 operation. On power-on-reset the value is set to 00111b (7 decimal).

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Note: The value in the register is the actual coefficient minus one.

PLL1_X2FBD2: These 6 register bits set the first feedback divider bits for PLL1. On power-on-reset the value is set to 000111b (7 decimal).

Note: The value in the register is the actual coefficient minus one.

PLL1_X1FBD1: These 5 register bits set the second feedback divider bits for PLL1. On power-on-reset the value is set to 10011b (19 decimal).

Note: The value in the register is the actual coefficient minus one.

PLL1_PS: These two bits determine the final divide on the VCO clock signal in PLL1.
00 - Divide by 1
01 - Divide by 2
10 - Divide by 4
11 - Divide by 8

On power-on-reset these bits are reset to 11b (3 decimal).

Note: This means that PLL1 FOUT is programmed to be 36,864,000 Hz on startup.

Note: The value in the register is the actual coefficient minus one.

PCLKDIV: These two bits set the divide ratio between the HCLK AHB clock and the APB clock (PCLK)
00 - Divide by 1
01 - Divide by 2
10 - Divide by 4
11 - Divide by 8

On power-on-reset the value is set to 00b.

Note: Care must be taken to make the correct selection of PCLK divide for the HCLK frequency used, so that the required minimum ratio between PCLK and the peripheral clock is not violated

HCLKDIV: These three bits set the divide ratio between the VCO output and the bus clock (HCLK)

000 - Divide by 1	100 - Divide by 6
001 - Divide by 2	101 - Divide by 8
010 - Divide by 4	110 - Divide by 16
011 - Divide by 5	111 - Divide by 32

On power-on-reset the value is set to 000b.

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nBYP1: This bit selects the clock source for the processor clock dividers. With this bit clear, the system wakes up and boots with the PLL bypassed and uses an external clock source. With nBYP1 set, the system runs with the PLL generated clock. The default for this bit is to boot/run from external clock source.

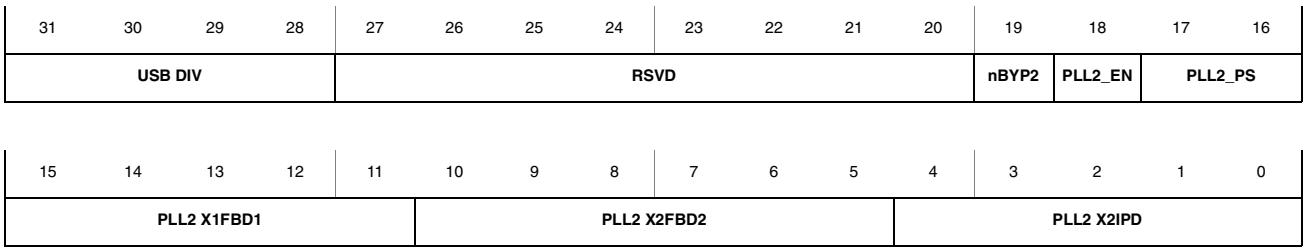
SMCROM: If set, this bit will gate off the HCLK to the Static Memory Controller when in Halt mode and therefore save power. When in Halt mode, there are no Instruction Code fetches occurring and therefore if there are no DMA operations in progress that may require the SMC, there will be no accesses to this controller. It may therefore be safely disabled when in Halt mode. This bit is 0b on reset.

FCLKDIV: These three bits set the divide ratio between the VCO output and processor clock. On power-on-reset the value is set to 000b.

000 - Divide by 1
001 - Divide by 2
010 - Divide by 4
011 - Divide by 8
100 - Divide by 16

For FCLKDIV values equal to 1xxb (except for 100b), the divide ratio will be divide by 1.

ClkSet2



Address:

0x8093_0024 - Read/Write

Definition:

The ClkSet2 register is used for setting the dividers internally to PLL2 and to the USB Host divider. The reset setting for PLL2 creates a frequency of 48 MHz. The default divider for USB_DIV is divide by 1, which will produce the USB host clock frequency and FIR clock frequency of 48 MHz.

Bit Descriptions:

PLL2_X2IPD: These 5 register bits set the input divider for PLL2 operation. On power-on-reset the value is set to 10111b (23 decimal).

Note: The value in the register is the actual coefficient minus one.

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PLL2_X2FBD2: These 6 register bits set the first feedback divider bits for PLL2. On power-on-reset the value is set to 11000b (24 decimal).

Note: The value in the register is the actual coefficient minus one.

PLL2_X1FBD1: These 5 register bits set the second feedback divider bits for PLL2. On power-on-reset the value is set to 11000b (24 decimal).

Note: The value in the register is the actual coefficient minus one.

PLL2_PS: These two bits determine the final divide function on the VCO clock signal in PLL2.
00 - Divide by 1
01 - Divide by 2
10 - Divide by 4
11 - Divide by 8

On power-on-reset these bits are reset to 11b (3 decimal).

Note: This means that PLL2 FOUT is programmed to be 48,000,000 Hz on startup.

Note: The value in the register is the actual coefficient minus one.

PLL2_EN: This bit enables PLL2. If set, PLL2 is enabled. If this bit is zero, PLL2 is disabled. On power-on-reset the value is set to 0b.

nBYP2: This bit selects the clock source for the processor clock dividers. If set, PLL2 is the clock source. If this bit is set to zero, the external clock is the clock source. On power-on-reset, this bit defaults to 0b.

USBDIV: These four bits set the divide ratio between the PLL2 output and the USB clock.

0000 - Divide by 1	1000 - Divide by 9
0001 - Divide by 2	1001 - Divide by 10
0010 - Divide by 3	1010 - Divide by 11
0011 - Divide by 4	1011 - Divide by 12
0100 - Divide by 5	1100 - Divide by 13
0101 - Divide by 6	1101 - Divide by 14
0110 - Divide by 7	1110 - Divide by 15
0111 - Divide by 8	1111 - Divide by 1

On power-on-reset these bits are reset to 0000b.

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ScratchReg0, ScratchReg1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Value															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															

Address:

ScratchReg0 - 0x8093_0040, Read/Write
ScratchReg1 - 0x8093_0044, Read/Write

Default:

0x0000_0000

Definition:

Each of these locations provide a 32-bit read/write scratch register, that can be used as a general purpose storage. These registers are reset to zero only on a power-on-reset. A System Reset will have no effect.

Bit Descriptions:

Value: This is a 32-bit read/write location.

APBWait

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															NO_WRITE_WAIT

Address:

0x8093_0050, Read/Write

Definition:

The APBWait register controls the insertion of wait states for APB peripherals.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

NO_WRITE_WAIT: Used in the AHB/APB bridge to not insert an AHB wait during writes, if set. If reset, a wait state is added by forcing HREADY = 0 during ST_WRITE. This bit resets to 0x0001.

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BusMstrArb

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				RSVD		MAC ENFIQ	MAC ENIRQ	USH ENFIQ	USH ENIRQ	DMA_ ENFIQ	DMA_ ENIRQ	PRI CORE	RSVD	PRI_ORD	

Address:

0x8093_0054 - Read/Write

Definition:

The Bus Master arbitration register (BusMstrArb) is used to configure the AHB master priority order.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PRI_ORD: Used to set the priority of the AHB arbiter. The priority order is shown below. This field resets to 00.

Priority Number	PRIOR 00 (Reset value)	PRIOR 01	PRIOR 10	PRIOR 11
1	MAC	MAC	DMA	DMA
2	USB	USB	USB	MAC
3	DMA	ARM920T	MAC	USB
4	ARM920T	DMA	ARM920T	ARM920T

PRI_CORE: When this bit is set the Core will become highest priority following a grant to one of the following: MAC, USB and DMA. If the Core then requests the bus, it is then placed in the priority order selected by PRI_ORD after it is granted, until one of the above masters is granted the bus, and is placed on top of the priority scheme.

DMA_ENIRQ: When set the arbiter will degrant DMA from the AHB bus and will ignore subsequent requests from DMA if an IRQ is active. When IRQ is cleared the DMA request is allowed again. There is no impact on other masters. Reset to 0.

DMA_ENFIQ: When set the arbiter will degrant DMA from the AHB bus and will ignore subsequent requests from DMA if an FIQ is active. When FIQ is cleared the DMA request is allowed again. There is no impact on other masters. Reset to 0.

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USH_ENIRQ: When set the arbiter will degrant USB host from the AHB bus and will ignore subsequent requests from the USB Host if an IRQ is active. When IRQ is cleared, the USB Host request is allowed again. There is no impact on other masters. Reset to 0.

USH_ENFIQ: When set the arbiter will degrant USB Host from the AHB bus and will ignore subsequent requests from USB Host if an FIQ is active. When FIQ is cleared, the USB Host request is allowed again. There is no impact on other masters. Reset to 0.

MAC_ENIRQ: When set the arbiter will degrant Ethernet MAC from the AHB bus and will ignore subsequent requests from the MAC if an IRQ is active. When IRQ is cleared, the MAC request is allowed again. There is no impact on other masters. Reset to 0.

MAC_ENFIQ: When set the arbiter will degrant the Ethernet MAC from the AHB bus and will ignore subsequent requests from the MAC if an FIQ is active. When FIQ is cleared, the MAC request is allowed again. There is no impact on other masters. Reset to 0.

BootModeClr

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															

Address:

0x8093_0058 - Write Only

Definition:

The BootModeClr register is a write-to-clear register. Reset activates the boot ROM remap function causing the internal boot ROM to map to address zero, if internal boot is selected. Writing BootModeClr removes the internal ROM address remap, restoring normal address space.

Bit Descriptions:

RSVD: There are no readable bits in this register.

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DeviceCfg

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SWRST	D1onG	D0onG	IonU2	1	0	MonG	RSVD	RSVD	0	0	U2EN	RSVD	U1EN	ADCEN	RSVD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	HC1IN	HC1EN	1	1	0	1	I2Son SSP	I2Son AC97	0	RSVD	RSVD	ADCPD	RSVD	SHena

Address:

0x8093_0080 - Read/Write, Software locked

Default:

0x0000_0000

Definition:

Device Configuration Register. This register controls the operation of major system functions.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

0: This bit must be written as “0”.

1: This bit must be written as “1”.

SHena: Standby/Halt enable. When 1, allows the system to enter Standby or Halt on a read from the Standby and Halt registers, respectively.

ADCPD: ADC Power Down.
1 - ADC and clocks are powered down.
0 - ADC and clocks are active. ADCPD must be zero for normal ADC operation.

ADCEN ADC Enable. The ADCEN bit does not affect the ADC power state. ADC power down is directly controlled by the ADCPD bit.
1 = ADC Interface enabled.
0 = ADC Interface disabled.

I2SonAC97: I2S on AC97 pins. The I2S block uses the AC97 pins. (See Table 4-5 on page 92, below.)

Note: The I2S should be enabled on only one set of pins. Therefore I2SonAc97 and I2SonSSP are mutually exclusive. Setting both I2SonAc97 and I2SonSSP will cause unexpected behavior.

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I2SonSSP: I2S on SSP pins. The I2S block uses the SSP pins. MCLK is not available in this pin option. (See Table 4-5 on page 92, below.)

Note: The I2S should be enabled on only one set of pins. Therefore I2SonAc97 and I2SonSSP are mutually exclusive. Setting both I2SonAc97 and I2SonSSP will cause unexpected behavior.

Table 4-5: Audio Interfaces Pin Assignment

Pin Name	Normal Mode Pin Description	I2S on SSP Mode Pin Description	I2S on AC'97 Mode Pin Description
SCLK1	SPI Bit Clock	I2S Serial Clock	SPI Bit Clock
SFRM1	SPI Frame Clock	I2S Frame Clock	SPI Frame Clock
SSPRX1	SPI Serial Input	I2S Serial Input	SPI Serial Input
SSPTX1	SPI Serial Output	I2S Serial Output	SPI Serial Output
		(No I2S Master Clock)	
ARSTn	AC'97 Reset	AC'97 Reset	I2S Master Clock
ABITCLK	AC'97 Bit Clock	AC'97 Bit Clock	I2S Serial Clock
ASYNC	AC'97 Frame Clock	AC'97 Frame Clock	I2S Frame Clock
ASDI	AC'97 Serial Input	AC'97 Serial Input	I2S Serial Input
ASDO	AC'97 Serial Output	AC'97 Serial Output	I2S Serial Output

HC1IN: HDLC1 clock in. This bit has no effect unless HC1EN is 1.
1 = pin EGPIO[3] is an input and drives an external HDLC clock to UART1.
0 = pin EGPIO[3] is an output driven by UART1.

HC1EN: HDLC1 clock enable.
1 = pin EGPIO[3] is used for an HDLC clock with UART1.
0 = pin EGPIO[3] is not used.

U1EN: UART1 Enable.
1 - UART1 baud rate clock is active.
0 - UART1 clock is off.

U2EN: UART2 Enable.
1 - UART2 baud rate clock is active.
0 - UART2 clock is off.

MonG: Modem on GPIO.
1 - Modem support signals use EGPIO[0] pins.
0 - Modem support signals do not use EGPIO[0] pins

IonU2: IrDA on UART2.
1 - UART2 is used as an IrDA interface,
0 - UART2 is a normal UART.

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D0onG: External DMA0 hardware handshake signals mapped to EGPIO pins.
1 - Signals mapped.
0 - Signals not supported.

D1onG: External DMA1 hardware handshake signals mapped to EGPIO pins.
1 - Signals mapped.
0 - Signals not supported.

SWRST: Software reset. A one to zero transition of this bit initiates a software reset.

MIRClkDiv

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MENA	ESEL	PSEL	RSVD			PDIV		RSVD	MDIV						

Address:

0x8093_0088 - Read/Write, Software locked

Default:

0x0000_0000

Definition:

Configures MIR clock for the MIR IrDA. Selects input to MIR clock dividers from either PLL1 or PLL2, and defines a programmable divide value.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

MENA: Enable MIR_CLK divider.

ESEL: External clock source select.
0 - Use the external **XTALI** clock input as the clock source.
1 - Use one of the internal PLLs selected by PSEL as the clock source.

PSEL: PLL source select.
1 - Select PLL2 as the clock source.
0 - Select PLL1 as the clock source.

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PDIV: Pre-divider value. Generates divide by 2, 2.5, or 3 from the clock source.
00 - Disable clock
01 - Divide-by-2
10 - Divide-by-2.5
11 - Divide-by-3

MDIV: MIR_CLK divider value. Forms a divide-by-N of the pre-divide clock output. MIR_CLK is the source clock divided by PDIV divided by N.

I2SClkDiv

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SENA	SLAVE	ORIDE	RSVD								DROP	SPOL	LRDIV		SDIV

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MENA	ESEL	PSEL	RSVD			PDIV		RSVD	MDIV						

Address:
0x8093_008C - Read/Write, Software locked

Default:
0x0000_0000

Definition:
Configures the I2S block audio clocks **MCLK, SCLK**, and **LRCLK**.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

SENA: Enable audio clock generation.

SLAVE: I2S slave. Configures the I2S clock system to operate as a slave. **SCLK** and **LRCLK** are chip inputs. The clock configuration controls in this register are ignored in slave mode.

ORIDE: Override I2S master configuration.
1 - Override the SAI_MSTR_CLK_CFG from the I2S block and use the I2SClkDiv Register settings.
0 - Use the I2S SAI_MSTR_CLK_CFG signals.

DROP: Drop SCLK clocks.
1 - When in 64x mode, drop 8 SCLKs.
0 - Do not drop SCLKs.

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SPOL: SCLK polarity. Defines the SCLK edge that aligns to LRCLK transitions.
1 - LRCLK transitions on the falling SCLK edge.
0 - LRCLK transitions on the rising SCLK edge.

LRDIV: LRCLK divide select.
00 - LRCK = SCLK / 32
01 - LRCK = SCLK / 64
10 - LRCK = SCLK / 128
11 - Reserved

SDIV: SCLK divide select.
1 - SCLK = MCLK / 4,
0 - SCLK = MCLK / 2.

MENA: Enable master clock generation.

ESEL: External clock source select.
0 - Use the external **XTALI** clock input as the clock source.
1 - Use one of the internal PLLs selected by PSEL as the clock source.

PSEL: PLL source select.
1 - Select PLL2 as the clock source.
0 - Select PLL1 as the clock source.

PDIV: Pre-divider value. Generates divide by 2, 2.5, or 3 from the clock source.
00 - Disable clock
01 - Divide-by-2
10 - Divide-by-2.5
11 - Divide-by-3

MDIV: MCLK divider value. Forms a divide-by-N of the pre-divide clock output. **MCLK** is the source clock divided by PDIV divided by N.

ADCClkDiv

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
ADCEN	RSVD														ADIV

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															

Address:

0x8093_0090 - Read/Write, Software locked

Default:

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0x0000_0000

Definition:

Configures the ADC clocks.

Bit Descriptions:

RSVD:	Reserved. Unknown During Read.
ADCEN:	ADC clock enable.
ADIV:	ADC clock divider value. 0 - ADC Clock is divide-by-16 from the external oscillator. 1 - ADC Clock is divide-by-4 from the external oscillator.

CHIP_ID

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REV				RSVD				0					RSVD	0	RSVD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ID															

Address:

0x8093_0094 - Read Only

Definition:

Chip ID register.

Bit Descriptions:

RSVD:	Reserved. Unknown During Read.
REV:	Revision: Reads chip Version number: 0000 - Rev A 0001 - Rev B 0010 - Rev C 0011 - Rev D0 0100 - Rev D1 0101 - Rev E0
0:	Reads zero.
ID[15:0]:	Chip ID Number, reads 9213.

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SysCfg

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
REV				RSVD											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD							SBOOT	LCSn7	LCSn6	LASDO	LEEDA	LEECLK	RSVD	LCSn2	LCSn1

Address:

0x8093_009C - Read/Write, Software locked

Default:

0x0000_0000

Definition:

System Configuration Register. Provides various system configuration options.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

REV: Revision: Reads chip Version number:
0000 - Rev A
0001 - Rev B
0010 - Rev C
0011 - Rev D0
0100 - Rev D1
0101 - Rev E0

SBOOT: Serial Boot Flag.
1 - hardware detected Serial Boot selection,
0 - hardware detected Normal Boot. This bit is read-only.

LCSn7, LCSn6: Latched version of **CSn7** and **CSn6** respectively. These are used to define the external bus width for the boot code.

LASDO: Latched version of **ASDO** pin. Used to select synchronous versus asynchronous boot device.

LEEDA: Latched version of **EEDAT** pin.

LEECLK: Define Internal or external boot:
1 - Internal
0 - External

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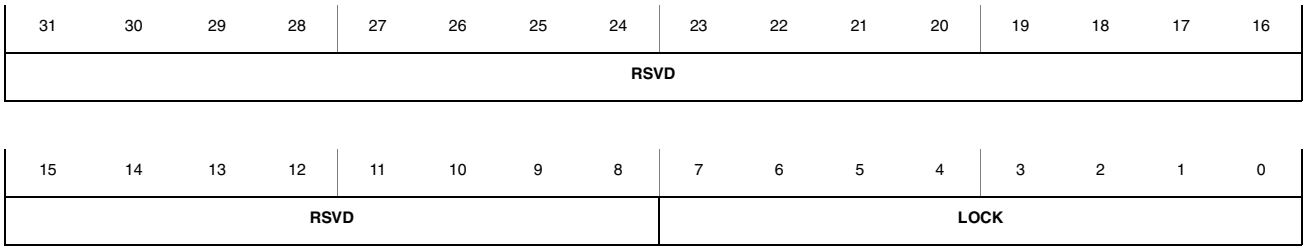
LCSn2, LCSn1: Define Watchdog startup action:
00 - Watchdog disabled, Reset duration disabled
01 - Watchdog disabled, Reset duration active
10 - Watchdog active, Reset duration disabled
11 - Watchdog active, Reset duration active

SysSWLock



Address:

0x8093_00C0 - Read/Write

Default:

0x0000_0000

Definition:

Syscon Software Lock Register. Provides software control port for all Syscon locked registers. Writing the LOCK field to 0xAA opens the lock. Reading the register will return 0x0000_0001 when the lock is open, and all zeros when the lock is closed (locked).

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

LOCK: Lock code value. This field must be written to a value of 0xAA to open the software lock. Reads 0x01 when the lock is open, 0x00 when the lock is closed.

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Chapter 5

Vectored Interrupt Controller

5.1 Introduction

The EP9301 contains two cascade Vectored Interrupt Controllers (VIC). A Vectored Interrupt has improved latency compared with a simple interrupt controller, since it provides direct information about where the interrupt's service routine is located and eliminates levels of software arbitration.

Each individual Vectored Interrupt Controller can handle up to 32 interrupts, but there are more than 32 interrupts in this design. Therefore two VICs are connected in a daisy-chain, which allows the system to handle up to 64 interrupt sources.

There are up to 16 vectored interrupts and 16 non-vectored interrupts available on each VIC. Vectored interrupts can only generate an IRQ interrupt. The vectored and nonvectored Interrupt Requests (IRQ) provide an address for an Interrupt Service Routine (ISR). Reading from the vector interrupt address register, VICxVectAddr, provides the address of the ISR, and updates the interrupt priority hardware that masks out the current and any lower priority interrupt requests. Writing to the VICxVectAddr register indicates to the interrupt priority hardware that the current interrupt is serviced, allowing lower priority interrupts to go active.

Registers in the VIC use a bit position for each different interrupt source. The bit position is fixed but the handling of each interrupt is configurable by the VIC. Software can control each request line to generate software interrupts.

The VIC provides a software interface to the interrupt system. In this system, two levels of interrupt are available:

- Fast Interrupt Request (FIQ) for fast, low latency interrupt handling.
- Interrupt Request (IRQ) for more general interrupts.

All interrupt inputs to the VIC are presented as active-high level sensitive signals. Any conditioning needed to achieve this is performed by the block generating the interrupt request. In the case of the external interrupts, the GPIO block takes care of the conditioning.

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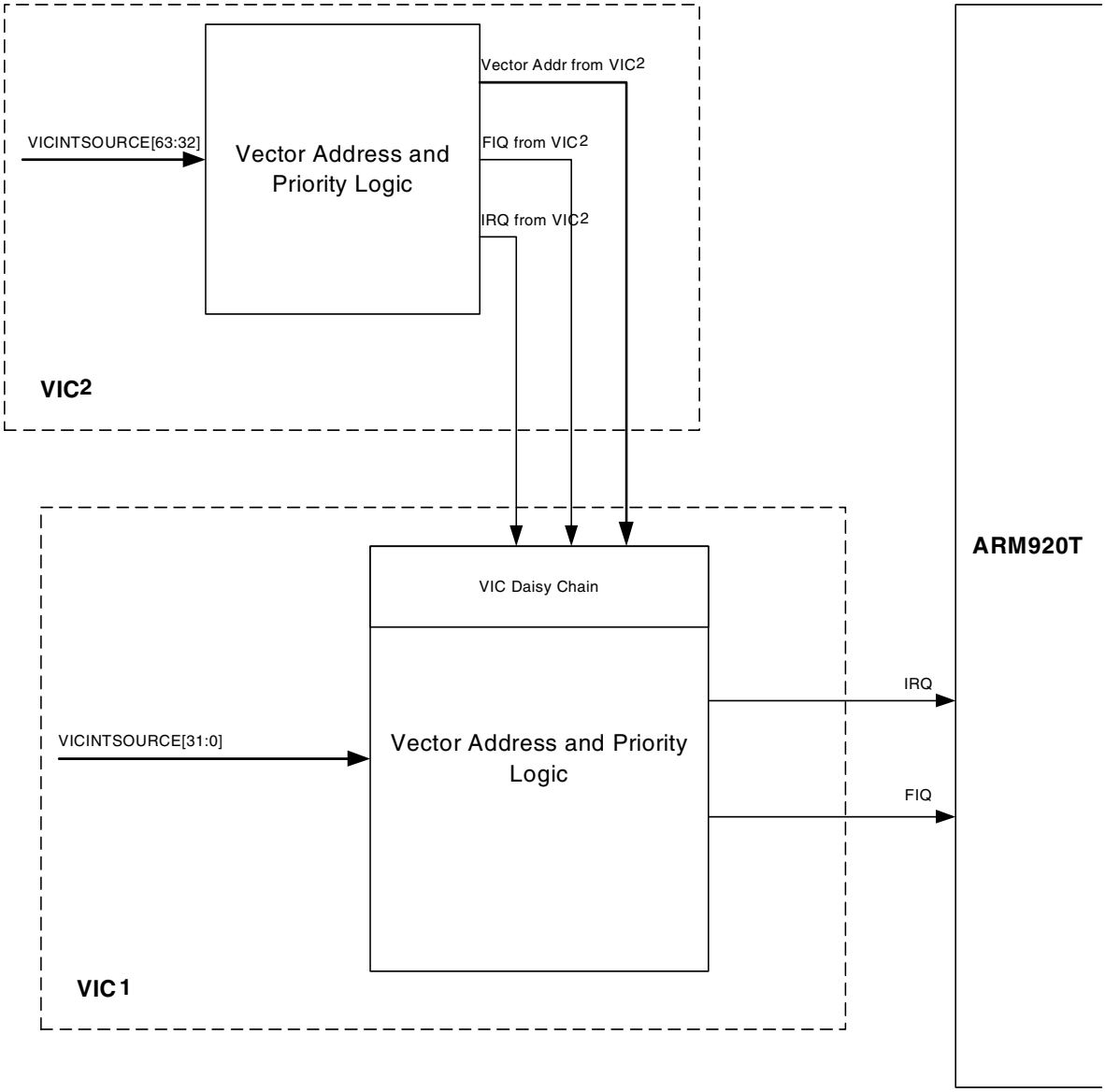
Figure 5-1. Vectored Interrupt Controller Block Diagram



5.1.1 Interrupt Priority

The FIQ interrupt has the highest priority (because the ARM9 core will always treat FIQ as higher priority), followed by vectored interrupt 0 to vectored interrupt 15. Non-vectored IRQ interrupts have the lowest priority. Any of the non-vectored Interrupts can be either FIQ or IRQ (the interrupt type is determined by programming the appropriate register, “VIC2IntSelect” on page 111). Any 16 of the 32 interrupts (per VIC) can be programmed to be vectored or not by programming the Vector address registers, “VICxVectAddr0 through VICxVectAddr15” on page 116 and the Vector Control registers, “VICxVectCntl0 through VICxVectCntl15” on page 117.

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A programmed interrupt request allows you to generate an interrupt under software control. This register is typically used to downgrade an FIQ interrupt to an IRQ interrupt.

The IRQ and FIQ request logic has an asynchronous path. This allows interrupts to be asserted when the clock is disabled.

The Interrupt Configuration is as follows:

Table 5-1: Interrupt Configuration

VIC Interrupt Source	Name	Description
0	-	Unused
1	-	Unused
2	COMMRX	ARM Communication Rx for Debug
3	COMMTX	ARM Communication Tx for Debug
4	TC1OI	TC1 under flow interrupt (Timer Counter 1)
5	TC2OI	TC2 under flow interrupt (Timer Counter 2)
6	AACINTR	Advanced Audio Codec interrupt
7	DMAM2P0	DMA Memory to Peripheral Interrupt 0
8	DMAM2P1	DMA Memory to Peripheral Interrupt 1
9	DMAM2P2	DMA Memory to Peripheral Interrupt 2
10	DMAM2P3	DMA Memory to Peripheral Interrupt 3
11	DMAM2P4	DMA Memory to Peripheral Interrupt 4
12	DMAM2P5	DMA Memory to Peripheral Interrupt 5
13	DMAM2P6	DMA Memory to Peripheral Interrupt 6
14	DMAM2P7	DMA Memory to Peripheral Interrupt 7
15	DMAM2P8	DMA Memory to Peripheral Interrupt 8
16	DMAM2P9	DMA Memory to Peripheral Interrupt 9
17	DMAM2M0	DMA Memory to Memory Interrupt 0
18	DMAM2M1	DMA Memory to Memory Interrupt 1
19	-	Reserved
20	GPIO0INTR	GPIO interrupt 0
21	GPIO1INTR	GPIO interrupt 1
22	GPIO2INTR	GPIO interrupt 2
23	UART1RXINTR1	UART 1 Receive Interrupt
24	UART1TXINTR1	UART 1 Transmit Interrupt
25	UART2RXINTR2	UART 2 Receive Interrupt
26	UART2TXINTR2	UART 2 Transmit Interrupt
27	-	Reserved
28	-	Reserved
29	-	Reserved
30	-	Reserved
31	-	Reserved
32	INT_EXT[0]	External interrupt 0
33	INT_EXT[1]	External interrupt 1
34	-	Reserved
35	TINTR	64 Hz tick Interrupt
36	WEINT	Watchdog expired Interrupt
37	INT_RTC	RTC Interrupt

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VIC Interrupt Source	Name	Description
38	INT_IrDA	IrDA Interrupt
39	INT_MAC	Ethernet MAC Interrupt
40	INT_EXT[2]	External interrupt 2
41	-	Reserved
42	-	Reserved
43	-	Reserved
44	-	Reserved
45	INT_SSP1RX	SSP Receive Interrupt
46	INT_SSP1TX	SSP Transmit Interrupt
47	-	Reserved
48	-	Reserved
49	-	Reserved
50	-	Reserved
51	TC3OI	TC3 under flow interrupt (Timer Counter 3)
52	INT_UART1	UART 1 Interrupt
53	SSPINTR	Synchronous serial port Interrupt
54	INT_UART2	UART 2 Interrupt
55	-	Reserved
56	USHINTR	USB Host Interrupt
57	-	Reserved
58	-	Reserved
59	GPIOINTR	GPIO combined interrupt
60	SAIINTR	I2S (SAI) block combined interrupt
61	-	Unused
62	-	Unused
63	-	Unused

5.1.2 Interrupt Descriptions

The interrupts described in Table 5-1 are described in detail in the descriptions that follow:

COMMRX — ARM Communication channel receive. When high, indicates the communications channel receive buffer contains data waiting to be read by the processor core. Refer to the ARM Technical Reference Manual.

COMMTX — ARM Communication channel transmit. When high indicates the communications channel transmit buffer is empty. Refer to the ARM technical reference manual.

TC1OI — Timer counter 1 under flow interrupt. This interrupt becomes active on the next falling edge of the timer counter 1 clock after the timer counter has underflowed (reached zero). It is cleared by writing to the TC1EOI location.

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TC2OI	Timer counter 2 under flow interrupt. This interrupt becomes active on the next falling edge of the timer counter 2 clock after the timer counter has underflowed (reached zero). It is cleared by writing to the TC2EOI location.
AACINTR	Advanced Audio CODEC Interrupt. Generated as described in Chapter 18, “AC’97 Controller” on page 475.
DMAM2P0	Internal Memory-to-peripheral and Peripheral-to-memory Channel 0 Interrupt. See Chapter 7, "DMA Controller".
DMAM2P1	Internal Memory-to-peripheral and Peripheral-to-memory Channel 1 Interrupt. See Chapter 7, "DMA Controller".
DMAM2P2	Internal Memory-to-peripheral and Peripheral-to-memory Channel 2 Interrupt. See Chapter 7, "DMA Controller".
DMAM2P3	Internal Memory-to-peripheral and Peripheral-to-memory Channel 3 Interrupt. See Chapter 7, "DMA Controller".
DMAM2P4	Internal Memory-to-peripheral and Peripheral-to-memory Channel 4 Interrupt. See Chapter 7, "DMA Controller".
DMAM2P5	Internal Memory-to-peripheral and Peripheral-to-memory Channel 5 Interrupt. See Chapter 7, "DMA Controller".
DMAM2P6	Internal Memory-to-peripheral and Peripheral-to-memory Channel 6 Interrupt. See Chapter 7, "DMA Controller".
DMAM2P7	Internal Memory-to-peripheral and Peripheral-to-memory Channel 7 Interrupt. See Chapter 7, "DMA Controller".
DMAM2P8	Internal Memory-to-peripheral and Peripheral-to-memory Channel 8 Interrupt. See Chapter 7, "DMA Controller".
DMAM2P9	Internal Memory-to-peripheral and Peripheral-to-memory Channel 9 Interrupt. See Chapter 7, "DMA Controller".
DMAM2M0	Memory-to-memory (incorporating external M2P/P2M) Channel 0 Interrupt. See Chapter 7, "DMA Controller".
DMAM2M1	Memory-to-memory (incorporating external M2P/P2M) Channel 1 Interrupt. See Chapter 7, "DMA Controller".
GPIO0INTR	This interrupt is generated when port F bit 0 is configured for interrupts. The interrupts can be configured to be level, rising or falling edge-sensitive. The interrupt is cleared by writing to the GPIO end of interrupt location. See Chapter 21, "GPIO Interface".

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GPIO1INTR	This interrupt is generated when port F bit 1 is configured for interrupts. The interrupts can be configured to be level, rising or falling edge sensitive. The interrupt is cleared by writing to the GPIO end of interrupt location.
GPIO2INTR	This interrupt is generated when port F bit 2 is configured for interrupts. The interrupts can be configured to be level, rising or falling edge sensitive The interrupt is cleared by writing to the GPIO end of interrupt location.
UART1RXINTR1	UART 1 receive interrupt.
UART1TXINTR1	UART 1 transmit interrupt.
UART2RXINTR2	UART 2 receive interrupt.
UART2TXINTR2	UART 2 transmit interrupt.
INT_EXT[0]	External interrupt.
INT_EXT[1]	External interrupt.
INT_EXT[2]	External interrupt.
TINTR	64 Hz TICK interrupt. This interrupt becomes active on every rising edge of the internal 64 Hz clock signal. This 64 Hz clock is derived from the 15-stage ripple counter that divides the 32.768 kHz oscillator input down to 1 Hz for the real time clock. This interrupt is cleared by writing to the TEOI location.
WEINT	Watchdog expired interrupt. This interrupt will become active on a rising edge of the periodic 64 Hz tick interrupt clock if the TICK interrupt (TINT) is still active. That is, if a tick interrupt has not been serviced for a complete tick period. Both WEINT and TINT interrupts are cleared by writing to the TEOI location. Failure to service this interrupt does not cause a system reset and the action taken on receipt of this interrupt is system dependent.
INT_RTC	Real Time Clock interrupt.
INT_IrDA	IrDA interrupt.
INT_MAC	Ethernet MAC interrupt.
CLK1HZ	1 Hz clock interrupt.
INT_SSP1RX	SSP receive interrupt.
INT_SSP1TX	SSP transmit interrupt.

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TC3OI	Timer counter 3 underflow interrupt. This interrupt becomes active on the next falling edge of the timer counter 3 clock after the timer counter has under flowed (reached zero). It is cleared by writing to the TC3EOI location.
INT_UART1	UART 1 general interrupt. This interrupt is active if any UART1 interrupt is active. Interrupt service routines will need to read the relevant status bits within the UART to determine the source of the interrupt. All these sources are individually maskable within the UART.
SSPINTR	Synchronous Serial Port (SSP) Interrupt. See Chapter 19, “Synchronous Serial Port” on page 497.
INT_UART2	UART 2 general Interrupt. This interrupt is active if any UART2 interrupt is active.
USHINTR	USB Host Interrupt.
GPIOINTR	Combined interrupt from any bit in ports A or B.
SAIINTR	Combined interrupt of all sources from the SAI block.

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5.2 Registers

The 2 VIC blocks have an identical register definition. The offset from the respective base address is the same:

- VIC1 Base address: 0x800B_0000
- VIC2 Base Address: 0x800C_0000

Using the ARM MMU, it is possible to remap the VIC base address to 0xFFFF_F000, giving an even better interrupt latency. Table 5-2 indicates the address offset from the base address.

Table 5-2: VICx Register Summary

Address	Type	Width	Reset Value	Name	Description
VIC base + 0000	Read	32	0x0000_0000	VICxIRQStatus	IRQ status register
VIC base + 0004	Read	32	0x0000_0000	VICxFIQStatus	FIQ status register
VIC base + 0008	Read	32	-	VICxRawIntr	Raw interrupt status register
VIC base + 000C	Read /Write	32	0x0000_0000	VICxIntSelect	Interrupt select register
VIC base + 0010	Read /Write	32	0x0000_0000	VICxIntEnable	Interrupt enable register
VIC base + 0014	Write	32	-	VICxIntEnClear	Interrupt enable clear register
VIC base + 0018	Read /Write	32	0x0000_0000	VICxSoftInt	Software interrupt register
VIC base + 001C	Read /Write	32	-	VICxSoftIntClear	Software interrupt clear register
VIC base + 0020	Read /Write	1	0x0	VICxProtection	Protection enable register
VIC base + 0030	Read /Write	32	0x0000_0000	VICxVectAddr	Vector address register
VIC base + 0034	Read /Write	32	0x0000_0000	VICxDefVectAddr	Default vector address register
VIC base + 0100	Read /Write	32	0x0000_0000	VICxVectAddr0	Vector address 0 register
VIC base + 0104	Read /Write	32	0x0000_0000	VICxVectAddr1	Vector address 1 register
VIC base + 0108	Read /Write	32	0x0000_0000	VICxVectAddr2	Vector address 2 register
VIC base + 010C	Read /Write	32	0x0000_0000	VICxVectAddr3	Vector address 3 register
VIC base + 0110	Read /Write	32	0x0000_0000	VICxVectAddr4	Vector address 4 register
VIC base + 0114	Read /Write	32	0x0000_0000	VICxVectAddr5	Vector address 5 register
VIC base + 0118	Read /Write	32	0x0000_0000	VICxVectAddr6	Vector address 6 register
VIC base + 011C	Read /Write	32	0x0000_0000	VICxVectAddr7	Vector address 7 register
VIC base + 0120	Read /Write	32	0x0000_0000	VICxVectAddr8	Vector address 8 register
VIC base + 0124	Read /Write	32	0x0000_0000	VICxVectAddr9	Vector address 9 register
VIC base + 0128	Read /Write	32	0x0000_0000	VICxVectAddr10	Vector address 10 register
VIC base + 012C	Read /Write	32	0x0000_0000	VICxVectAddr11	Vector address 11 register
VIC base + 0130	Read /Write	32	0x0000_0000	VICxVectAddr12	Vector address 12 register
VIC base + 0134	Read /Write	32	0x0000_0000	VICxVectAddr13	Vector address 13 register
VIC base + 0138	Read /Write	32	0x0000_0000	VICxVectAddr14	Vector address 14 register
VIC base + 013C	Read /Write	32	0x0000_0000	VICxVectAddr15	Vector address 15 register
VIC base + 0200	Read /Write	6	0x00	VICxVectCntl0	Vector control 0 register
VIC base + 0204	Read /Write	6	0x00	VICxVectCntl1	Vector control 1 register
VIC base + 0208	Read /Write	6	0x00	VICxVectCntl2	Vector control 2 register
VIC base + 020C	Read /Write	6	0x00	VICxVectCntl3	Vector control3 register
VIC base + 0210	Read /Write	6	0x00	VICxVectCntl4	Vector control 4 register
VIC base + 0214	Read /Write	6	0x00	VICxVectCntl5	Vector control 5 register
VIC base + 0218	Read /Write	6	0x00	VICxVectCntl6	Vector control 6 register
VIC base + 021C	Read /Write	6	0x00	VICxVectCntl7	Vector control 7 register

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Address	Type	Width	Reset Value	Name	Description
VIC base + 0220	Read /Write	6	0x00	VICxVectCntl8	Vector control 8 register
VIC base + 0224	Read /Write	6	0x00	VICxVectCntl9	Vector control 9 register
VIC base + 0228	Read /Write	6	0x00	VICxVectCntl10	Vector control 10 register
VIC base + 022C	Read /Write	6	0x00	VICxVectCntl11	Vector control 11 register
VIC base + 0230	Read /Write	6	0x00	VICxVectCntl12	Vector control 12 register
VIC base + 0234	Read /Write	6	0x00	VICxVectCntl13	Vector control 13 register
VIC base + 0238	Read /Write	6	0x00	VICxVectCntl14	Vector control 14 register
VIC base + 023C	Read /Write	6	0x00	VICxVectCntl15	Vector control 15 register
VIC base + 0FE0	Read	8	0x90	VICxPeriphID0	Peripheral identification register bits 7:0
VIC base + 0FE4	Read	8	0x11	VICxPeriphID1	Peripheral identification register bits 15:8
VIC base + 0FE8	Read	8	0x04	VICxPeriphID2	Peripheral identification register bits 23:16
VIC base + 0FEC	Read	8	0x00	VICxPeriphID3	Peripheral identification register bits 31:24

Register Descriptions

VIC1IRQStatus

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD				IRQStatus								RSVD	IRQStatus		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IRQStatus															

Address:

VIC1IRQStatus: 0x800B_0000 - Read Only

Definition:

IRQ Status Register. The VIC1IRQStatus register provides the status of interrupts after IRQ masking.
Interrupts 0 - 31 are in VIC1IRQStatus.
Interrupts 32 - 63 are in VIC2IRQStatus.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

IRQStatus: Shows the status of the interrupts after masking by the VIC1IntEnable and VIC1IntSelect registers. A “1” indicates that the interrupt is active, and generates an interrupt to the processor.

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VIC2IRQStatus

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IRQStatus				RSVD			IRQStatus	RSVD	IRQStatus			RSVD			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	IRQStatus		RSVD		IRQStatus	RSVD	IRQStatus					RSVD	IRQStatus		

Address:

VIC2IRQStatus: 0x800C_0000 - Read Only

Definition:

IRQ Status Register. The VIC2IRQStatus register provides the status of interrupts after IRQ masking.
Interrupts 0 - 31 are in VIC1IRQStatus.
Interrupts 32 - 63 are in VIC2IRQStatus.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

IRQStatus: Shows the status of the interrupts after masking by the VIC2IntEnable and VIC2IntSelect registers. A “1” indicates that the interrupt is active, and generates an interrupt to the processor.

VIC1FIQStatus

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD				FIQStatus								RSVD	FIQStatus		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FIQStatus															

Address:

VIC1FIQStatus: 0x800B_0004 - Read Only

Definition:

FIQ Status Register. The VIC1FIQStatus register provides the status of the interrupts after FIQ masking.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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FIQStatus: Shows the status of the interrupts after masking by the VIC1IntEnable and VIC1IntSelect registers. A “1” indicates that the interrupt is active, and generates an interrupt to the processor.

VIC2FIQStatus

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FIQStatus					RSVD		FIQStatus	RSVD		FIQStatus			RSVD		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	FIQStatus			RSVD	FIQStatus	RSVD	FIQStatus						RSVD	FIQStatus	

Address:

VIC2FIQStatus: 0x800C_0004 - Read Only

Definition:

FIQ Status Register. The VIC2FIQStatus register provides the status of the interrupts after FIQ masking.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

FIQStatus: Shows the status of the interrupts after masking by the VIC2IntEnable and VIC2IntSelect registers. A “1” indicates that the interrupt is active, and generates an interrupt to the processor.

VIC1RawIntr

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD					RawIntr							RSVD	RawIntr		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RawIntr															

Address:

VIC1RawIntr: 0x800B_0008 - Read Only

Definition:

The VIC1RawIntr register provides the status of the source interrupts (and software interrupts) to the interrupt controller.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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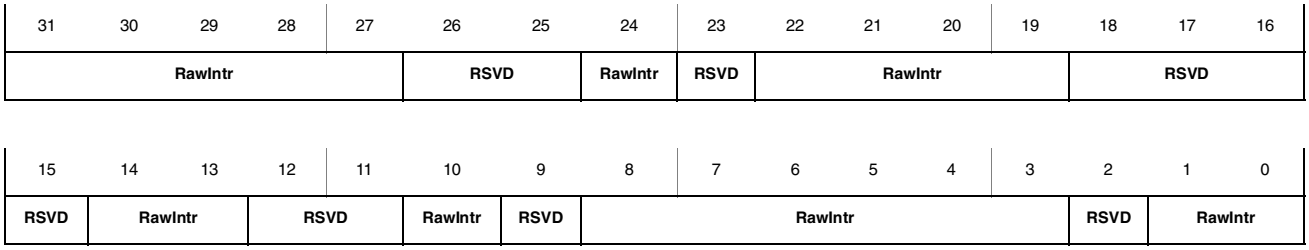
RawIntr: Shows the status of the interrupts before masking by the enable registers. A “1” indicates that the appropriate interrupt request is active before masking.

VIC2RawIntr



Address:

VIC2RawIntr: 0x800C_0008 - Read Only

Definition:

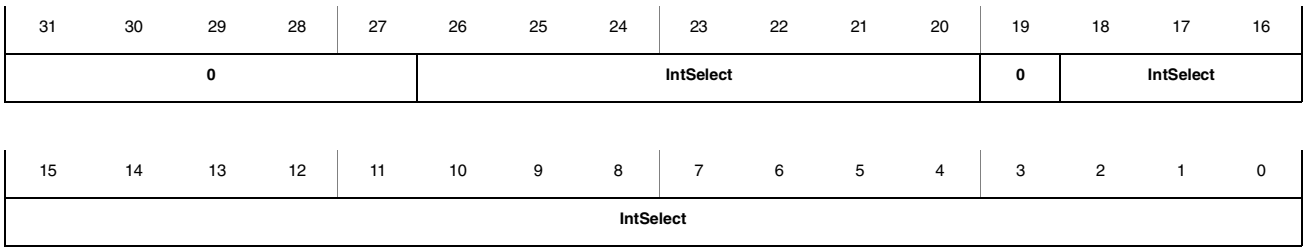
The VIC2RawIntr register provides the status of the source interrupts (and software interrupts) to the interrupt controller.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RawIntr: Shows the status of the interrupts before masking by the enable registers. A “1” indicates that the appropriate interrupt request is active before masking.

VIC1IntSelect



Address:

VIC1IntSelect: 0x800B_000C - Read/Write

Definition:

Interrupt Select Register. The VIC1IntSelect register selects whether the corresponding interrupt source generates an FIQ or an IRQ interrupt.

Bit Descriptions:

0: Must be written as “0”.

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IntSelect: Selects type of interrupt for interrupt request:
1 = FIQ interrupt
0 = IRQ interrupt.

VIC2IntSelect

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IntSelect					0		IntSelect	0	IntSelect				0		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	IntSelect		0		IntSelect	0	IntSelect						0	IntSelect	

Address:

VIC2IntSelect: 0x800C_000C - Read/Write

Definition:

Interrupt Select Register. The VIC2IntSelect register selects whether the corresponding interrupt source generates an FIQ or an IRQ interrupt.

Bit Descriptions:

0: Must be written as “0”.

IntSelect: Selects type of interrupt for interrupt request:
1 = FIQ interrupt
0 = IRQ interrupt.

VIC1IntEnable

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0					IntEnable							0	IntEnable		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IntEnable															

Address:

VIC1IntEnable: 0x800B_0010 - Read/Write

Definition:

Interrupt Enable Register. The VIC1IntEnable register enables the interrupt request lines, by masking the interrupt sources for the IRQ interrupt. On reset, all interrupts are disabled. A HIGH bit sets the corresponding bit in the VIC1IntEnable register. A LOW bit has no effect.

Bit Descriptions:

0: Must be written as “0”.

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IntEnable: Enables the interrupt request lines:
1 - Interrupt enabled. Allows interrupt request to processor.
0 - Interrupt disabled.

VIC2IntEnable

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IntEnable				0			IntEnable	0	IntEnable			0			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	IntEnable			0	IntEnable	0	IntEnable					0	IntEnable		

Address:

VIC2IntEnable: 0x800C_0010 - Read/Write

Definition:

Interrupt Enable Register. The VIC2IntEnable register enables the interrupt request lines, by masking the interrupt sources for the IRQ interrupt. On reset, all interrupts are disabled. A HIGH bit sets the corresponding bit in the VIC2IntEnable register. A LOW bit has no effect.

Bit Descriptions:

0: Must be written as “0”.

IntEnable: Enables the interrupt request lines:
1 - Interrupt enabled. Allows interrupt request to processor.
0 - Interrupt disabled.

VIC1IntEnClear

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
0				IntEnable Clear								0	IntEnable Clear		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IntEnable Clear															

Address:

VIC1IntEnClear: 0x800B_0014 - Write Only

Definition:

Interrupt Enable Clear Register. The VIC1IntEnClear register clears bits in the VIC1IntEnable register.

Bit Descriptions:

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0: Must be written as “0”.

IntEnable Clear: Clears bits in the VICxIntEnable register. Setting a bit to “1” clears the corresponding bit in the VIC1IntEnable register. Any bits set to “0” have no effect.

VIC2IntEnClear

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IntEnable Clear					0		IntEnable Clear	0	IntEnable Clear				0		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	IntEnable Clear		0		IntEnable Clear	0	IntEnable Clear						0	IntEnable Clear	

Address:

VIC2IntEnClear: 0x800C_0014 - Write Only

Definition:

Interrupt Enable Clear Register. The VIC2IntEnClear register clears bits in the VIC2IntEnable register.

Bit Descriptions:

0: Must be written as “0”.

IntEnable Clear: Clears bits in the VICxIntEnable register. Setting a bit to “1” clears the corresponding bit in the VIC2IntEnable register. Any bits set to “0” have no effect.

VICxSoftInt

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SoftInt															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SoftInt															

Address:

VIC1SoftInt: 0x800B_0018 - Read/Write
VIC2SoftInt: 0x800C_0018 - Read/Write

Definition:

Software Interrupt Register. The VICxSoftInt register is used to generate software interrupts.

Bit Descriptions:

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SoftInt: Setting a bit to “1” generates a software interrupt for the specific source interrupt before interrupt masking. Setting a bit to “0” has no effect.

VICxSoftIntClear

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SoftIntClear															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SoftIntClear															

Address:

VIC1SoftIntClear: 0x800B_001C - Write Only
VIC2SoftIntClear: 0x800C_001C - Write Only

Definition:

Software Interrupt Clear Register. The VICxSoftIntClear register clears bits in the VICxSoftInt register.

Bit Descriptions:

SoftIntClear: Clears bits in the VICxSoftInt register. Setting a bit to “1” clears the corresponding bit in the VICxSoftInt register. Setting a bit to “0” has no effect.

VICxProtection

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															Protection

Address:

VIC1Protection: 0x800B_0018 - Read/Write
VIC2Protection: 0x800C_0018 - Read/Write

Definition:

Protection Enable Register. The VICxProtection register enables or disables protected register access. If the bus master cannot generate accurate protection information, leave this register in its reset state to allow User mode access.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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Protection: Enables or disables protected register access. When enabled, only Privileged mode accesses (reads and writes) can access the interrupt controller registers. When disabled, both User mode and Privileged mode can access the registers. This register is cleared on reset, and can only be accessed in Privileged mode.

VICxVectAddr

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VectorAddr															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VectorAddr															

Address:

VIC1VectAddr: 0x800B_0030 - Read/Write
VIC2VectAddr: 0x800C_0030 - Read/Write

Definition:

Vector Address Register. The VICxVectAddr register contains the Interrupt Service Routine (ISR) address of the currently active interrupt.

Note: Reading from this register provides the address of the ISR, and indicates to the priority hardware that the interrupt is being serviced. Writing to this register indicates to the priority hardware that the interrupt has been serviced. The register should be used as follows:

- The ISR reads the VICxVectAddr register when an IRQ interrupt is generated
- At the end of the ISR, the VICxVectAddr register is written in order to update the priority hardware.

Reading or writing to the register at other times can cause incorrect operation.

Note: If you are using the VIC and a program/debugger ever reads address VIC_BASE + 0x30, a value must be written to VIC_BASE + 0x30. If not, only higher priority interrupts are enabled and there are no higher priority interrupts. Therefore, no more interrupts will occur. If you use the VIC in Vectored Interrupt mode, this is not an issue.

If you are not using the priority level in the VIC, write VIC_BASE + 0x30 with a value in order to disable the interrupt priority at the beginning of your program.

It is not always clear when the ARM debuggers read the VIC_BASE + 0x30, so it is recommended that if you are using a debugger, do not read the VIC registers via a memory window. If you must read the VIC registers, read only the VIC registers that are needed.

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Bit Descriptions:

VectorAddr: Contains the address of the currently active ISR. Any writes to this register clear the interrupt.

VICxDefVectAddr

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DefaultVectorAddr															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DefaultVectorAddr															

Address:

VIC1DefVectAddr: 0x800B_0034 - Read/Write
VIC2DefVectAddr: 0x800C_0034 - Read/Write

Definition:

Default Vector Address Register. The VICxDefVectAddr register contains the default ISR address.

Bit Descriptions:

DefaultVectorAddr: Contains the address of the default ISR handler.

VICxVectAddr0 through VICxVectAddr15

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
VectorAddr															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VectorAddr															

Address:

VIC1VectAddr0: 0x800B_0100 - Read/Write
VIC1VectAddr1: 0x800B_0104 - Read/Write
VIC1VectAddr2: 0x800B_0108 - Read/Write
VIC1VectAddr3: 0x800B_010C - Read/Write
VIC1VectAddr4: 0x800B_0110 - Read/Write
VIC1VectAddr5: 0x800B_0114 - Read/Write
VIC1VectAddr6: 0x800B_0118 - Read/Write
VIC1VectAddr7: 0x800B_011C - Read/Write
VIC1VectAddr8: 0x800B_0120 - Read/Write
VIC1VectAddr9: 0x800B_0124 - Read/Write
VIC1VectAddr10: 0x800B_0128 - Read/Write
VIC1VectAddr11: 0x800B_012C - Read/Write

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VIC1VectAddr12: 0x800B_0130 - Read/Write
VIC1VectAddr13: 0x800B_0134 - Read/Write
VIC1VectAddr14: 0x800B_0138 - Read/Write
VIC1VectAddr15: 0x800B_013C - Read/Write
VIC2VectAddr0: 0x800C_0100 - Read/Write
VIC2VectAddr1: 0x800C_0104 - Read/Write
VIC2VectAddr2: 0x800C_0108 - Read/Write
VIC2VectAddr3: 0x800C_010C - Read/Write
VIC2VectAddr4: 0x800C_0110 - Read/Write
VIC2VectAddr5: 0x800C_0114 - Read/Write
VIC2VectAddr6: 0x800C_0118 - Read/Write
VIC2VectAddr7: 0x800C_011C - Read/Write
VIC2VectAddr8: 0x800C_0120 - Read/Write
VIC2VectAddr9: 0x800C_0124 - Read/Write
VIC2VectAddr10: 0x800C_0128 - Read/Write
VIC2VectAddr11: 0x800C_012C - Read/Write
VIC2VectAddr12: 0x800C_0130 - Read/Write
VIC2VectAddr13: 0x800C_0134 - Read/Write
VIC2VectAddr14: 0x800C_0138 - Read/Write
VIC2VectAddr15: 0x800C_013C - Read/Write

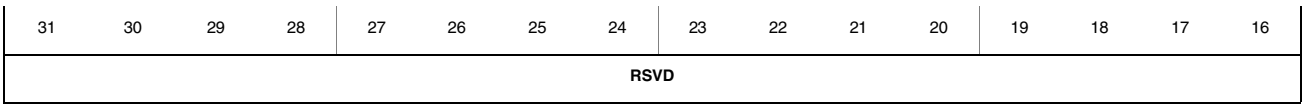
Definition:

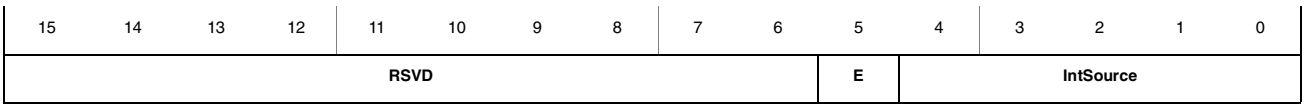
Vector Address Registers. The 32 VICxVectAdd0 through VICxVectAdd15 registers contain the ISR vector addresses, that is, the addresses of the ISRs for the particular 16 interrupts that are vectored.

Bit Descriptions:

VectorAddr: Contains ISR vector addresses.

VICxVectCntl0 through VICxVectCntl15





Address:

VIC1VectCntl0: 0x800B_0200 - Read/Write
VIC1VectCntl1: 0x800B_0204 - Read/Write
VIC1VectCntl2: 0x800B_0208 - Read/Write
VIC1VectCntl3: 0x800B_020C - Read/Write
VIC1VectCntl4: 0x800B_0210 - Read/Write
VIC1VectCntl5: 0x800B_0214 - Read/Write
VIC1VectCntl6: 0x800B_0218 - Read/Write
VIC1VectCntl7: 0x800B_021C - Read/Write

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VIC1VectCntl8: 0x800B_0220 - Read/Write
VIC1VectCntl9: 0x800B_0224 - Read/Write
VIC1VectCntl10: 0x800B_0228 - Read/Write
VIC1VectCntl11: 0x800B_022C - Read/Write
VIC1VectCntl12: 0x800B_0230 - Read/Write
VIC1VectCntl13: 0x800B_0234 - Read/Write
VIC1VectCntl14: 0x800B_0238 - Read/Write
VIC1VectCntl15: 0x800B_023C - Read/Write
VIC2VectCntl0: 0x800C_0200 - Read/Write
VIC2VectCntl1: 0x800C_0204 - Read/Write
VIC2VectCntl2: 0x800C_0208 - Read/Write
VIC2VectCntl3: 0x800C_020C - Read/Write
VIC2VectCntl4: 0x800C_0210 - Read/Write
VIC2VectCntl5: 0x800C_0214 - Read/Write
VIC2VectCntl6: 0x800C_0218 - Read/Write
VIC2VectCntl7: 0x800C_021C - Read/Write
VIC2VectCntl8: 0x800C_0220 - Read/Write
VIC2VectCntl9: 0x800C_0224 - Read/Write
VIC2VectCntl10: 0x800C_0228 - Read/Write
VIC2VectCntl11: 0x800C_022C - Read/Write
VIC2VectCntl12: 0x800C_0230 - Read/Write
VIC2VectCntl13: 0x800C_0234 - Read/Write
VIC2VectCntl14: 0x800C_0238 - Read/Write
VIC2VectCntl15: 0x800C_023C - Read/Write

Definition:

Vector Control Registers. The 32 VICxVectCntl0 through VICxVectCnt15 registers select the interrupt source for the vectored interrupt.

Note: Vectored interrupts are only generated if the interrupt is enabled. The specific interrupt is enabled in the VICxIntEnable register, and the interrupt is set to generate an IRQ interrupt in the VICxIntSelect register. This prevents multiple interrupts being generated from a single request if the controller is incorrectly programmed.

Bit Descriptions:

RSVD:	Reserved. Unknown During Read.
E:	Enables vector interrupt. This bit is cleared on reset.
IntSource:	Selects interrupt source by number. You can select any of the 32 interrupt sources.

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Chapter 6

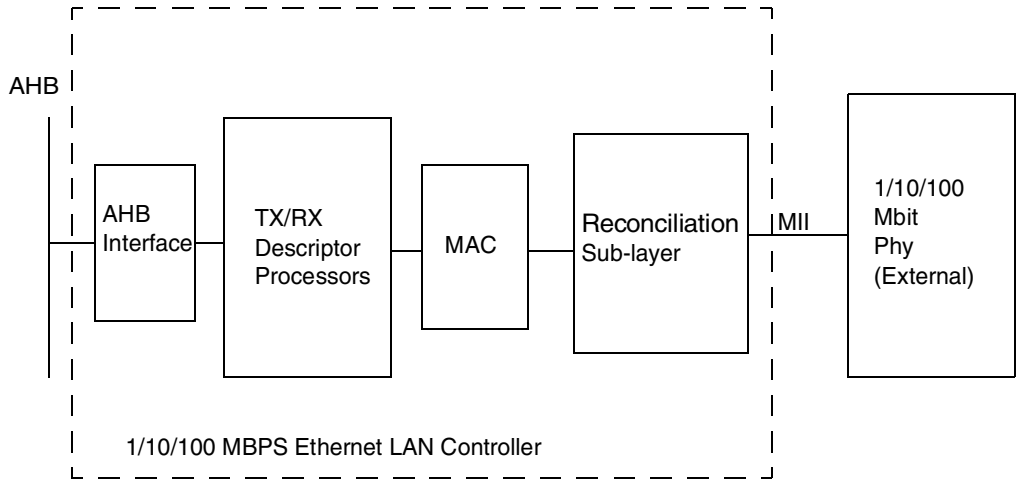
1/10/100 Mbps Ethernet LAN Controller

6.1 Introduction

The Ethernet LAN Controller incorporates all the logic needed to interface directly to the AHB and to the Media Independent Interface (MII). It includes local memory and DMA control, and supports full duplex operation with flow control support. Figure 6-1 shows a simplified block diagram.

This block was designed with a RAM of 544 words, each word containing 33 bits. These RAMs are used for packet buffering and controller data storage. One RAM is dedicated to the receiver, and one dedicated to the transmitter. These RAMs are mapped into the register space and are accessible via the AHB.

Figure 6-1. Block Diagram



6.1.1 Detailed Description

6.1.1.1 Host Interface and Descriptor Processor

The Host Interface can be functionally decomposed into the AHB Interface Controller and the Descriptor Processor. The AHB Interface Controller implements the actual connection to the AHB. The controller responds as a AHB bus slave for register programming, and acts as an AHB bus master for data transfers.

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The Descriptor Processor implements the Hardware Adapter Interface Algorithm and generates transfer requests to the AHB Interface Controller. The back-end interfaces to the MAC controllers and services MAC requests to run accesses to the FIFO and update queue status. The descriptor processor also generates internal requests for descriptor fetches. A priority arbiter arbitrates among the various requests and generates transfer requests to the AHB Interface Controller. There are 6 queues that require service in system memory:

- RxData: Write received frame data to host memory.
- RxStatus: Write received frame status to host memory.
- TxData: Read frame data from host memory.
- TxStatus: Write transmitted frame status to host memory.
- RxDescriptor: Read descriptors from host memory.
- TxDescriptor: Read descriptors from host memory.

Each queue generates a hard request (for urgent service) and a soft request (not urgent, but queue can run transfers). The priority assigned to the queues varies depending on the state of the system, but hard requests are prioritized over soft requests, and AHB write requests are prioritized over AHB read requests to allow faster back-to-back transfers.

6.1.1.2 Reset and Initialization

The Ethernet LAN Controller has three reset sources: the AHB reset, software reset from the SelfCtl register, and individual channel resets via the BMCtl register. The PHY is reset with the PHYRES function in compliance with the 802.3 specifications and has no effect on the MAC layer and up.

AHB reset initializes the entire controller, except for the receive MAC. The receive MAC is initialized by a SOFT_RESET. Upon AHB reset the AHB Interface and Descriptor Processor is put into a quiescent state.

Software Reset generates a SOFT_RESET which resets the descriptor processor, FIFO, and MAC. SOFT_RESET occurring in the middle of a frame transmission will result in the transmitted frame being truncated on the line. SOFT_RESET occurring in the middle of a received frame will result in the reset of the frame being dropped. The configuration registers remain intact during a soft reset. A SOFT_RESET should be issued following a power-on to ensure the receive MAC is fully initialized.

6.1.1.3 Powerdown Modes

The only powerdown option is to stop the TXCLK and RXCLK by disabling the PHY.

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6.1.1.4 Address Space

The Address space is mapped as:

MACBase + 0x0000 - MACBase + 0x00FF: MAC setup registers.
MACBase + 0x0100 - MACBase + 0x011F: MAC configuration registers, only first 4 words used.

The RAM blocks are interleaved in the AHB address space. AHB address bits 0 and 1 are byte selects and must be zero for direct access. AHB address bit 2 selects the left or right RAM array, which is the Transmit or Receive array. AHB address bits 3,4, and 5 perform a 1-of-8 column select. Address bit 6 selects the even or odd row address. Address bits 7, 8, 9, and 10 decode the rows. Thus from an AHB addressing perspective, the MAC FIFOs are one large RAM array.

The following table defines the FIFO RAM address map as it appears in the address space. Address are in byte units. All data transfers to the FIFO RAM are restricted to words.

Caution: Accessing the FIFO RAM while the MAC is operating will likely cause a malfunction.

There is no arbitration logic between direct AHB access and MAC descriptor processor access.

Table 6-1: FIFO RAM Address Map

FIFO RAM Address Map	Usage
0x8001_4000 to 0x8001_47FF	Rx Data
0x8001_4800 to 0x8001_4FFF	Tx Data
0x8001_5000 to 0x8001_503F	Rx Status
0x8001_5040 to 0x8001_507F	Tx Status
0x8001_5080 to 0x8001_50BF	Rx Descriptor
0x8001_50C0 to 0x8001_50FF	Tx Descriptor

The MAC configurations registers and FIFO RAMs are only word accessible

6.1.2 MAC Engine

The MAC engine is compliant with the requirements of ISO/IEC 8802-3 (1993), Sections 3 and 4.

6.1.2.1 Data Encapsulation

In transmission, the MAC automatically prepends the preamble, and computes and appends the FCS. The data after the SFD and before the FCS is supplied by the host as the transmitted data. FCS generation by the MAC may be disabled by setting InhibitCRC bit in the Transmit Frame Descriptor. Refer to Figure 6-2.

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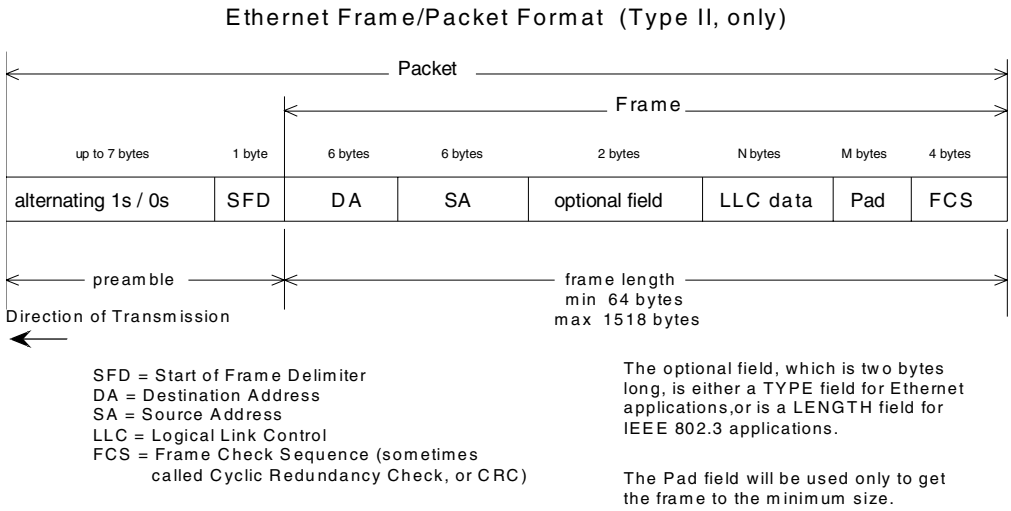
Figure 6-2. Ethernet Frame / Packet Format (Type II only)



In the receiver, the MAC detects the preamble and locks onto the embedded clock. The MAC performs destination address filtering (individual, group, broadcast, promiscuous) on the DA. The MAC engine computes the correct FCS, and reports if the received FCS is “good” or “bad”. The data after the SFD and before the FCS is supplied to the host as the received data. The received FCS may also be passed to the host by setting RXCtl.BCRC.

6.1.3 Packet Transmission Process

This section explains the complete packet transmission process as seen on the Ethernet line. This process includes: carrier deference, back-off, packet transmission, transmission of EOF, and SQE test. Refer to Figure 6-3.

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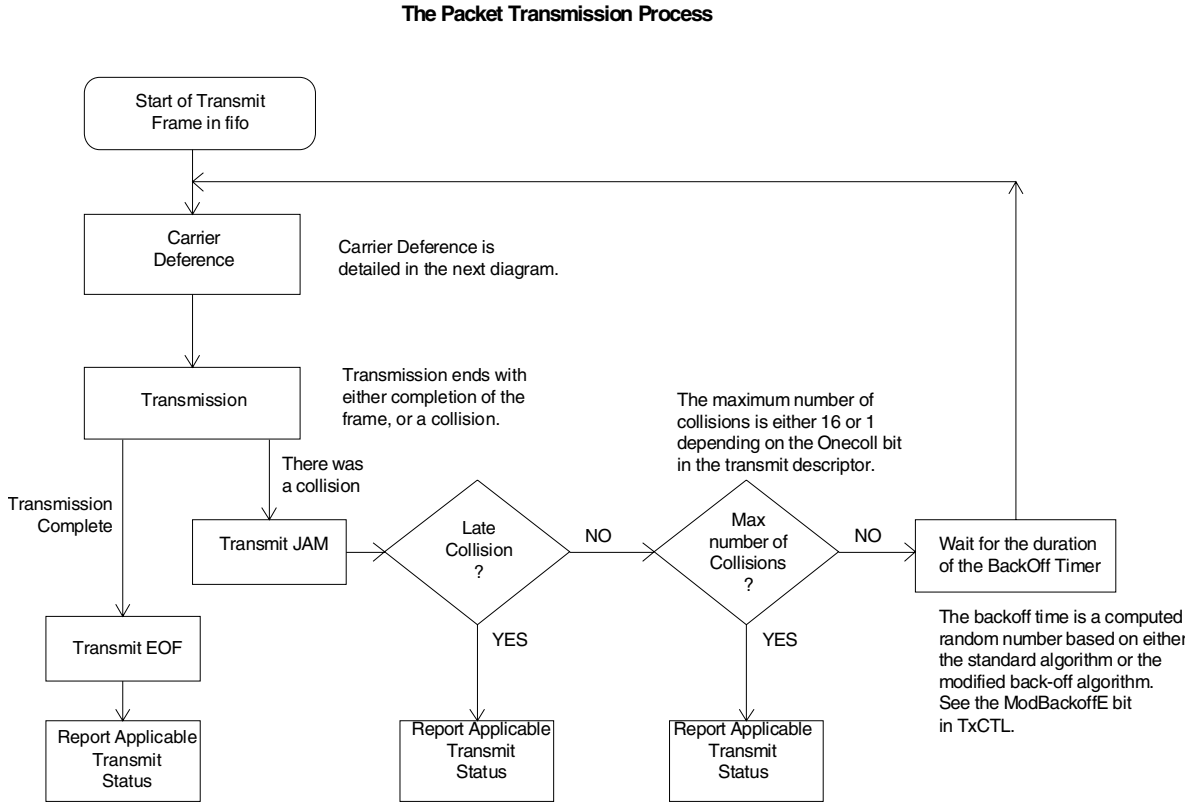
Figure 6-3. Packet Transmission Process



The Ethernet/ISO/IEC 8802-3 topology is a single shared medium with several stations. Only one station can transmit at a time. The access method is called Carrier Sense Multiple Access with Collision Detection (CSMA/CD). This method is a “listen before talk” mechanism that has an added feature to end transmissions when two, or more, stations start transmissions at nearly the same time.

The CSMA portion of this method provides collision avoidance. Each station monitors its receiver for carrier activity. When activity is detected, the medium is busy, and the MAC defers (waits) until the medium no longer has a carrier.

6.1.3.1 Carrier Deference

Refer to Figure 6-4. Once sufficient bytes have been written to the transmit FIFO, the MAC layer immediately moves to the Carrier Deference State Diagram. The Carrier Deference state is independent of entry into the state diagram. The MAC layer may enter the state diagram in any of its five states. The MAC layer exits the Carrier Deference only from the IFG Complete state. Thus, the Carrier Deference state may be entered and exited immediately, or there may be a delay depending on the state when entered.

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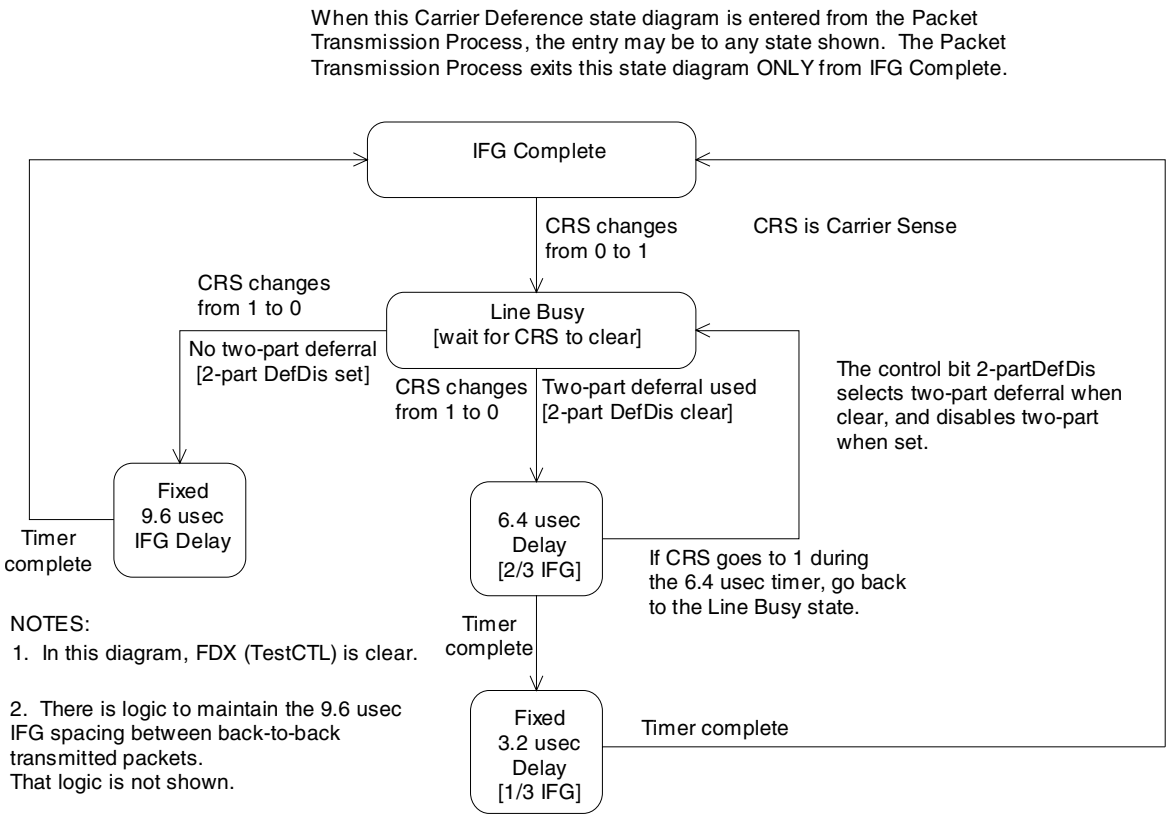
Figure 6-4. Carrier Deference State Diagram



When CRS becomes active, the Line Busy state is entered. This state is held until CRS returns to clear which starts the IFG timer. The time-out process after CRS clears is called Carrier Deference. In the MAC, Carrier Deference has two options as selected by the bit 2-part DefDis (TXCtl). If 2-part DefDis is clear, the two part deferral is used which meets the requirements of ISO/IEC 8802-3 paragraph 4.2.3.2.1. As shown in the diagram, if CRS becomes active during the first 2/3 (6.4 µsec) of the IFG, the MAC restarts the IFG timer. If CRS becomes active during the last 1/3 of the IFG, the timer is not restarted to ensure fair access to the medium.

If 2-part DefDis is set, the two part deferral is disabled. In this option, the IFG timer is allowed to complete even if CRS becomes active after the timer has started.

The 2-part deferral has an advantage for AUI connections to either 10BASE-2 or 10BASE-5. If the deferral process simply allowed the IFG timer to complete, then it is possible for a short Inter Frame Gap to be generated. The 2-part deferral prevents short IFGs. The disadvantage of the 2-part deferral is longer deferrals. In 10BASE-T systems, either deferral method should operate about the same.

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6.1.4 Transmit Back-Off

Refer to Figure 6-3. Once transmission is started, either the transmission is completed, or there is a collision. There are two kinds of collision: normal collision (one that occurs within the first 512 bits of the packet) and late collision (one that occurs after the first 512 bits). In either collision type, the MAC engine always sends a 32 bit jam sequence, and stops transmission.

After a normal collision and the jam, transmission is stopped, or "backed-off". The MAC attempts transmission again according to one of two algorithms. The ISO/IEC standard algorithm or a modified back-off algorithm may be used, and the host chooses which algorithm through the ModBackoffE control bit (TXCtl). The standard algorithm from ISO/IEC paragraph 4.2.3.2.5 is called the "truncated binary exponential backoff" and is shown below:

$$0 <= r <= 2^k$$

where r is a random integer for the number of slot times the MAC waits before attempting another transmission, and a slot time is time of 512 bits (51.2 µsec), k = minimum (n,10), and n is the nth retransmission attempt. The modified back-off algorithm uses delays longer than the ISO/IEC standard after each of the first three transmit collisions as shown below:

$$0 <= r <= 2^k$$

where k = minimum (n,10), but not less than 3, and n is the nth retransmission attempt

The advantage of the modified algorithm over the standard algorithm is that the modification reduces the possibility of multiple collisions on any transmission attempt. The disadvantage is that the modification extends the maximum time needed to acquire access to the medium.

The host may choose to disable the back-off algorithm altogether. This is done through the control bit DisableBackoff (TestCtl). When set, the MAC transmitter waits for the Inter Frame Gap time before starting transmission. There is no back-off algorithm employed. When clear, the MAC uses either the standard or the modified algorithm.

6.1.4.1 Transmission

After the transmission has passed the time for a normal collision (512 bits), then transmission is either completed, or aborted due to a late collision. For a late collision, the transmitter sends the 32 bit jam sequence, but does not back-off and try again. When a late collision occurs, Out-of-wdw collision (XStatQ) is set. A late collision is not retried, because the first 64 bytes of the FIFO are freed after the normal collision window, and will likely be refilled by a following packet. Driver intervention is needed to reconstruct the FIFO data.

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6.1.4.2 The FCS Field

If InhibitCRC (Transmit Descriptor) is clear, the MAC automatically appends the standard 32 bit FCS to the end of the frame. The MAC tests the last 32 bits received against the standard CRC computation. If received in error, CRCerror (RStatQ) is set. If CRCerroriE (Interrupt Enable) is set, there is an interrupt associated with CRCerror. The standard CRC conforms to ISO/IEC 8802-3 section 3.2.8. The polynomial for the CRC is:

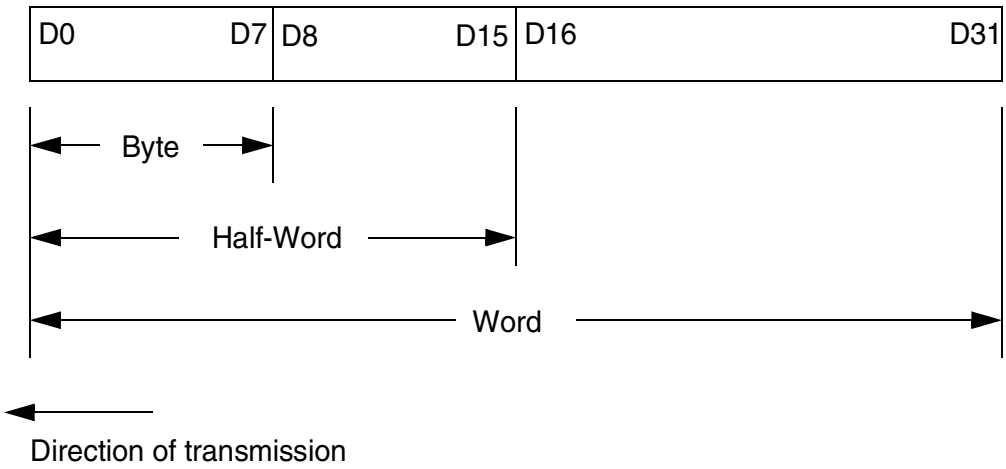
$$G(x) = x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$$

The resultant 32 bit field is transmitted on the line with bit X^{31} first through X^0 last.

6.1.4.3 Bit Order

In compliance with ISO/IEC 8802-3 section 3.3, each byte is transmitted low order bit first, except for the CRC, as noted in “The FCS Field” on page 126.

Figure 6-5. Data Bit Transmission Order



6.1.4.4 Destination Address (DA) Filter

There are two forms of destination address filtering performed by the MAC, perfect filtering, where the address is checked for an exact match, and hashing, where the address is checked for inclusion in a group. In addition there is a mode to accept all destination addresses which is enabled via the RXCtl.PA bit.

6.1.4.5 Perfect Address Filtering

The MAC includes four programmable perfect address filters, as well as the all ones filter for broadcast frames. The RXCtl register is used to control whether a particular filter is used. The filters themselves share the same address space and the value in the Address Filter Pointer register determines which filter is being accessed at any time. The filters are arranged such that the first

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is the normal MAC address for the interface, which is also used in the detection of remote wakeup frames, and may be optionally used to detect pause (flow control) frames. The primary purpose of the second filter is for the recognition of pause frames. This would normally be programmed to correspond to the multicast address used for MAC control frames. The third and fourth filters, provide extra optional address match capabilities, which can provide the capability of adding extra individual addresses or of providing two multicast address filters.

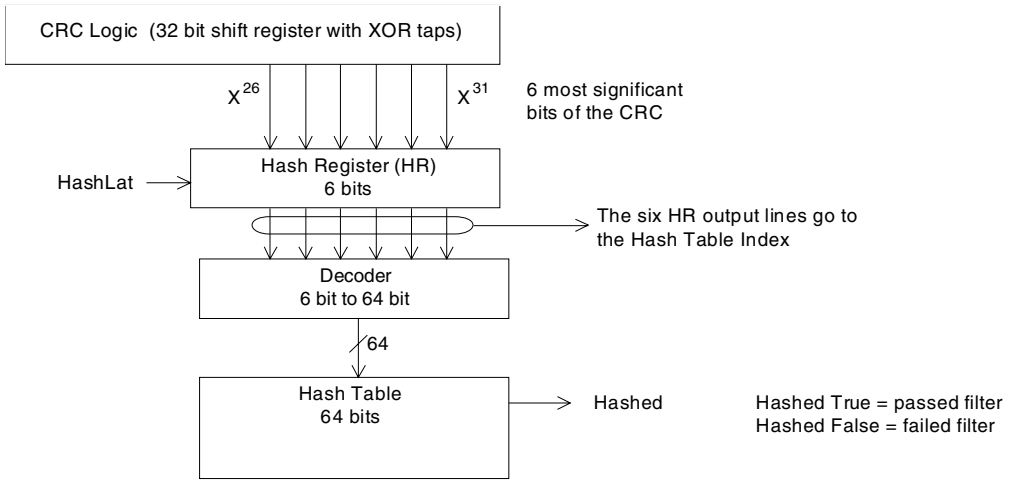
6.1.4.6 Hash Filter

The 64 bit Logical Address Filter provides DA filtering hashed by the CRC logic. The Logical Address Filter is sometimes referred to as the multicast address filter.

Referring to Figure 6-6, notice that the CRC computation starts at the first bit of the frame, which is also the first bit of the DA. (Recall that a “frame” is a “packet” without the preamble.)

The CRC Logic can be viewed as a 32 bit shift register with specific Exclusive-OR feedback taps. After the entire DA has been shifted into the CRC Logic, the signal HashLat latches the 6 most significant bits of the CRC Logic (x^{26} through x^{31}) into the 6-bit hash register (HR). The contents of HR are passed through the 6-bit to 64-bit Decoder. Only one of the 64 Decoder outputs is asserted at a time. That asserted output is compared with a corresponding bit in the Logical Address Filter. The filter output, Hashed, is used to determine if the received DA passed the hash filter. When set, the Hashed event bit shows that the received DA passed the hash filter. When clear, Hashed shows the failure of the DA to pass the hash filter.

Figure 6-6. CRC Logic



Whenever the hashed filter is passed on good frames, the output of the HR is presented on the Hash Table Index (RStatQ). A received good frame is

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determined to be one without CRC error and which is the correct length (64 ≤ length ≤ 1518).

If RXCtl.MA is set, then any received multicast frame passing the hash filter is accepted. A multicast frame is one which has RXCtl.IA[0] = 1.

If RXCtl.IAHA[0] is set, then a frame with any individual address frame AND passing the hash filter is accepted. An individual address frame is one which has RXCtl.IA[0] = 0. For a frame to pass RXCtl.IAHA[0] it must have RXCtl.IA[0] = 0 and pass the hash.

The relationship of RXCtl.MA and RXCtl.IAHA is shown below.

Table 6-2: RXCtl.MA and RXCtl.IAHA[0] Relationships

RXCtl.MA	RXCtl.IAHA[0]	Hash Filter Acceptance Results
0	0	Hash filter not used in acceptance criteria.
1	0	All multicast frames (first bit of DA = 1) passing the hash are accepted.
0	1	All individual address frames (first bit of DA = 0) passing the hash are accepted.
1	1	All frames that pass the hash are accepted.

6.1.4.7 Flow Control

The MAC provides special support for flow control by the transmission and reception of pause frames. A pause frame is a specific format of a MAC control frame that defines an amount of time for a transmitter to stop sending frames. Sending pause frames thereby reduces the amount of data sent by the remote station.

6.1.4.8 Receive Flow Control

The MAC can detect receive pause frames and automatically stop the transmitter for the appropriate period of time. To be interpreted as a pause frame the following conditions must be met:

- Destination address accepted by one of the first two individual address filters, with the appropriate RXCtl.RxFCE bit set.
- The Type field must match that programmed in the Flow Control Format register.
- The next two bytes of the frame (MAC Control Opcode) must equal 0x0001.
- The frame must be of legal length with a good CRC.

If accepted as a pause frame, the pause time field is transferred to the Flow Control Timer register. The pause frame may be optionally passed on to the Host or discarded by the MAC. Once the Flow Control Timer is set to a non-zero value, no new transmit frames are started, until the count reaches zero.

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The counter is decremented once every slot time while no frame is being transmitted.

6.1.4.9 Transmit Flow Control

When receive congestion is detected, the driver may want to transmit a pause frame to the remote station to create time for the local receiver to free resources. As there may be many frames queued in the transmitter, and there is a chance that the local transmitter is itself being paused, an alternative method is provided to allow a pause frame to be transmitted. Setting the Send Pause bit in the Transmit Control register causes a pause frame to be transmitted at the earliest opportunity. This occurs either immediately, or following the completion of the current transmit frame. If the local transmitter is paused, the pause frame will still be sent, and the pause timer will still be decremented during the frame transmission.

To comply with the standard, pause frames should only be sent on full duplex links. The MAC does not enforce this, it is left to the driver. If a pause frame is sent on a half duplex link, it is subject to the normal half duplex collisions rules and retry attempts.

The format of a transmit pause frame is:

Bytes 1-6 - Destination address - this is the last Individual address (Address Filter Pointer = 6)

Bytes 7-12 - Source address - this is the first Individual address (Address Filter Pointer = 0)

Bytes 13-14 - Type field - this is defined in the Flow Control Format register

Bytes 15-16 - Opcode - set to 0x0001

Bytes 17-18 - Pause time - this is defined in the Flow Control Format register

Once the Host sets the Send Pause bit in TXCtl, it will remain set until the pause frame starts transmission. Then the Send Pause clears and the Pause Busy bit is set and remains set until the transmission is complete. No end of frame status is generated for pause frames.

6.1.4.10 Rx Missed and Tx Collision Counters

There are three counters that help the software in recording events, transmit collisions, receive missed frames, and receive runt frames. All three counters operate in similar ways. When the appropriate events occur the counters are incremented. They are cleared following a read of the count value. If a count is incremented such that the MSB is set, the corresponding status bit in the Interrupt Status Register is set. An interrupt is generated at this time if the corresponding enable bit is set in the Interrupt Enable Register. Once the count is incremented to an all ones condition it will not be incremented further, it will remain in this state until reset by a read operation.

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6.1.4.11 Accessing the MII

This section describes the proper method to access the MII. It includes how to read/write PHY registers, how to have the PHY perform auto-negotiation, and how to startup the PHY.

The bits MDCDIV in register SelfCtl are used to control the PHY's clock divisor. The default value is 0x07, so the MDC clock frequency is HCLK divided by 8. This default value is correct for most PHYs. However, to be safe, check the PHY's data sheet to make sure that this clock frequency is correct.

The bit PSPRS in register SelfCtl is used to disable/enable Preamble Suppress for data passed from the MAC to the PHY through the MDIO. If bit PSPRS is set, the preamble is suppressed. In this case, the MAC won't prepend 32 bits of “1” to the data written to the PHY. Since the MAC automatically prepends the preamble to data when in transmission mode, bit PSPRS must be set while the MAC is transmitting frames. Otherwise, two preambles will be prepended and cause a transmission failure. The default value of “1” is appropriate for transmitting frames.

The MAC won't automatically prepend a preamble when not in transmission mode. Therefore, if the MAC wants to read/write PHY registers, bit PSPRS may be cleared since most PHYs require a preamble for access to the PHY's registers. However, to be safe, check PHY's data sheet to determine if a preamble is needed to read/write PHY registers.

6.1.4.11.1 Steps for Reading From the PHY Registers.

1. Read the value from the SelfCtl Register.
2. Since most PHYs need a Preamble for the MAC to read/write the PHY registers, you may need to clear the PreambleSuppress bit.
3. Ensure that the PHY is not busy by polling the MIIStatus_Busy Bit in MIIStatus register.
4. Issue the command to read the register within the PHY.
5. Wait until the read command is completed. Determine this by polling the MIIStatus_Busy bit in MIIStatus register.
6. Get the PHY data from the MII Data register.
7. Restore the old value to SelfCtl register.

Note: Steps 1, 2, and 7 are not required if the PHY doesn't need a preamble for access to the PHY's registers.

6.1.4.11.2 Steps for Writing To the PHY Registers.

1. Read the value from SelfCtl register.
2. Since most PHYs need a Preamble for the MAC to read/write the PHY registers, you may need to clear the PreambleSuppress bit.

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3. Ensure that the PHY is not busy by polling the MIIStatus_Busy bit in MIIStatus register.
4. Put the PHY data into the PHY Data register
5. Issue the write command to write data to the register within the PHY
6. Wait until the write command is completed. Determine this by polling the MIIStatus_Busy Bit in MIIStatus Register.
7. Restore the old value to SelfCtl register.

Note: Steps 1, 2, and 7 are not required if the PHY doesn't need a preamble for access to the PHY's registers.

6.1.4.11.3 Steps for PHY Auto-negotiation

1. Write to the Auto-Negotiation Advertisement register (0x04). Set it in accordance with IEEE_802.3 standard, and advertise 100/10M full/half duplex available.
2. Write to Basic Mode Control Register (0x00), to enable and restart Auto-Negotiation.
3. Poll bit Auto_Neg_Complete in the BMSR register in the PHY until the Auto-Negotiation is complete.

6.1.4.11.4 Steps for PHY Startup

1. Set the MDC ClockDivisor and the PreambleSuppress for the PHY in the SelfCtl register. The default value 0x0000_0F10 is appropriate for most PHYs in transmission mode.
2. Have the PHY perform auto-negotiation.
3. Read the Auto-Negotiation_Link_Partner_Ability register to check the PHY's configuration.
4. If the link is Full Duplex, then set MAC for Full Duplex.

6.2 Descriptor Processor

The MAC operates as a bus master to transfer all receive and transmit, data and status, across the AHB bus. The transfers are managed by two sets of queues for each direction, a descriptor queue and a status queue. The following section details the operation of these queues.

6.2.1 Receive Descriptor Processor Queues

The receive descriptor processor uses two circular queues in Host memory to manage the transfer of receive data frames. The receive descriptor queue is used to pass descriptors of free data buffers from the Host to the MAC. The receive status queue is used to pass information on the MAC's use of the data

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buffers back to the Host. Keeping these queues separate enables the use of burst transfers to and from the queues, reducing the overall amount of bus traffic and avoiding some potential latency problems.

6.2.2 Receive Descriptor Queue

The receive descriptors are passed from the Host to the MAC via the receive descriptor queue. The receive descriptor queue is a circular queue occupying a contiguous area of memory. The location and size of the queue are set at initialization writing to the Receive Descriptor Queue Base Address Register, the Receive descriptor current address, and the Receive Descriptor Queue Base Length. The base address must point to a word-aligned memory location. The Current Address must be set to point to the first descriptor to be used. This would normally be the first entry (same value as the base address). The Receive Descriptor Queue Base Length is set to the length (in bytes) of the queue. The number of descriptors should be an integral power-of-two (2, 4, 8, 16, etc.). Otherwise the Receive Descriptor Processor may not work properly and the MAC/Ethernet may stop receiving frames.

Each descriptor entry defines one receive data buffer, and consists of two words. The first word contains the address of the data buffer, which must be word aligned. The second word contains three fields: buffer length, buffer index and a Not Start Of Frame bit. The buffer length field specifies the maximum number of bytes to be used in the buffer and should be an integral number of words. If the buffer length is set to zero, the descriptor will be ignored, and no status will be posted for the buffer. The buffer index can be used by the Host to keep track of buffers as they are exchanged with the MAC. When the MAC reads a descriptor, it keeps a copy of the index, which it includes in any status entry associated with that buffer. The Not Start Of Frame bit may be set by the Host on any buffer in which it does not want a new frame to be started. This buffer would then only be used for chaining of frame fragments. This mode may be used to align frames on boundaries coarser than descriptors, such as when multiple physical address descriptors are used to describe one virtual address buffer.

In normal operation, the Host does not need to access the RXDQBAdd, RXDQBLen, RXDCurAdd registers following initialization. Control of the use of the descriptors is handled using the Receive Descriptor Enqueue register (RXDEnq). The term enqueue refers to the action of adding descriptors to the end of an existing queue. To enqueue receive descriptors, the Host writes the number of descriptors to the RXDEnq register. The number is automatically added to the existing value. When the MAC consumes descriptors by reading them into its on local storage (internal MAC buffer), the number read is subtracted from the total. The Host can read the total number of unread valid descriptors left in the queue from the RXDEnq. There is a restriction that no more than 255 descriptors may be added to the queue in one write operation. To add more than this number requires multiple write operations. See Figure 6-7.

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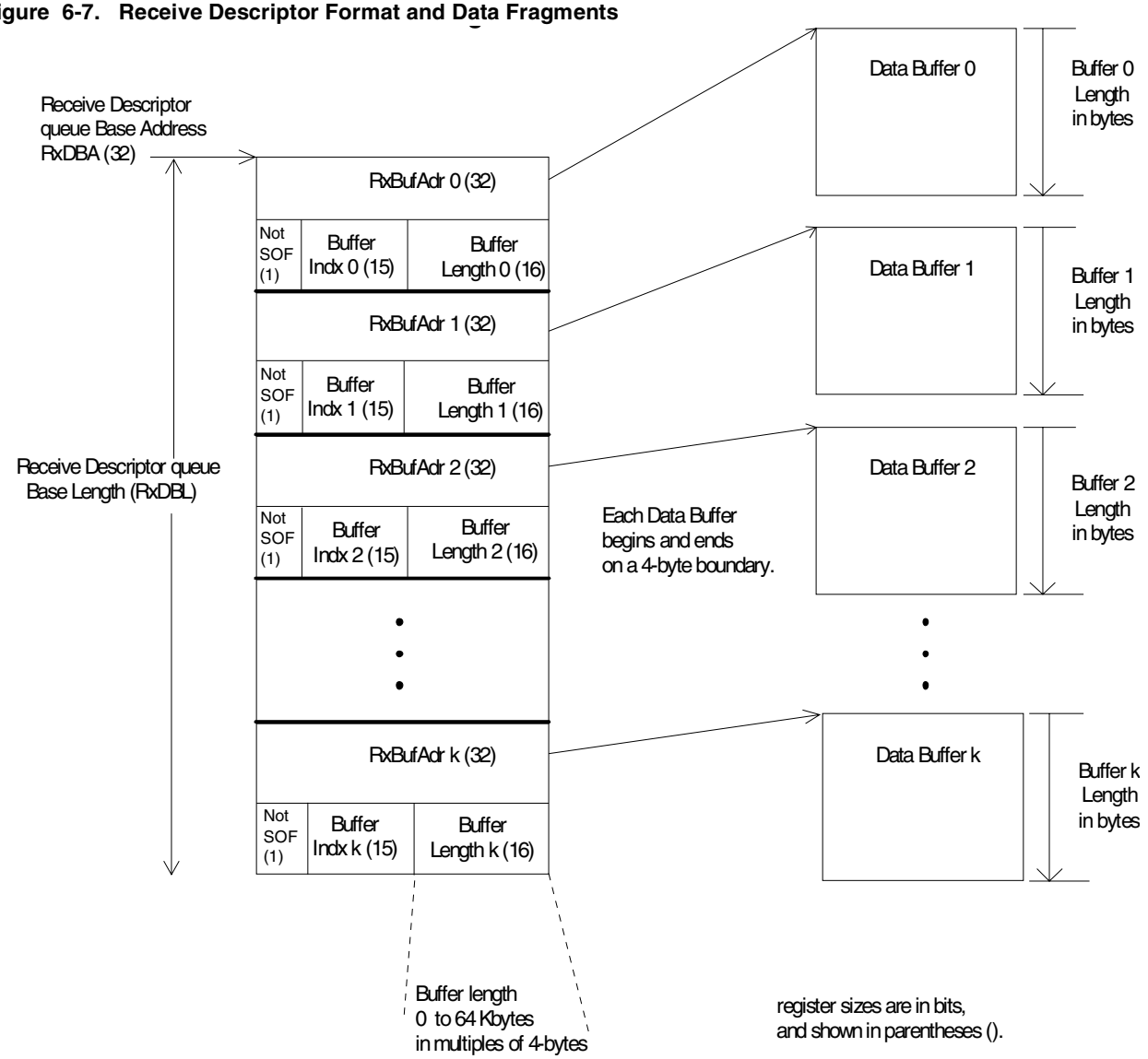
Figure 6-7. Receive Descriptor Format and Data Fragments



Receive Descriptor Format - First Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
BA															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BA															

Definition:

Receive Descriptor, first word. Contains the base address to the data buffer.

Bit Descriptions:

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BA: Buffer Address. This location holds the 32 bit address pointer to the data buffer, this must point to a word aligned location.

Receive Descriptor Format - Second Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
NSOF	BI														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BL															

Definition:

Receive Descriptor, second word. Contains control, index and length for the descriptor.

Bit Descriptions:

NSOF: Not Start of Frame. When the Not Start Of Frame bit is set in a descriptor, the associated buffer will only be used for a frame being continued from another buffer. If there is not a frame to be continued (that is, start of a new frame), the buffer will be discarded. When a buffer is discarded in this manner, there is no status posted.

BI: Buffer Index. The buffer index is provided for Host software purposes. The MAC keeps an internal copy of the index and includes it with any status writes associated with a receive buffer.

BL: Buffer Length. The Buffer Length contains the number of bytes available to be used in the receive buffer. This should be an integral number of words. If the length is set to zero, the descriptor will be ignored and no status will be posted for the buffer.

6.2.3 Receive Status Queue

The receive status queue is used to pass receive status from the MAC to the Host. In operation, the receive status queue is similar to the receive descriptor queue. It is a circular queue in contiguous memory space. The location and size of the queue are set at initialization by writing to the Receive Status Queue Base Address and the Receive Status Queue Base Length registers. The base address must point to a word aligned memory location. The length is set to the actual status queue length (in bytes) and should not exceed 64 Kbytes total. The number of status entries should be an integral power-of-two (2, 4, 8, 16, etc.), or the Receive Descriptor Processor may not work properly, and the MAC/Ethernet may stop receiving frames. The Current Address must

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be set to point to the first status entry to be used. This would normally be the first entry (same value as the base address).

When the receive status queue initialization is complete, the Receive Status Enqueue register is used by the Host to pass free status locations to the MAC. To simplify this process the Host writes the number of additional free status locations available to the enqueue register. The MAC adds the additional count to the previously available location to determine the total number of available receive status entries. When the MAC writes status to the queue, it subtracts the number written from this total. The current value of the total receive status entries is available by reading the enqueue register.

No more than 255 status entries may be added in one write. If a number greater than this needs to be written, the write should be broken up into more than one operation (that is, to add 520 status entries: write 255, then write 255, finally write 10).

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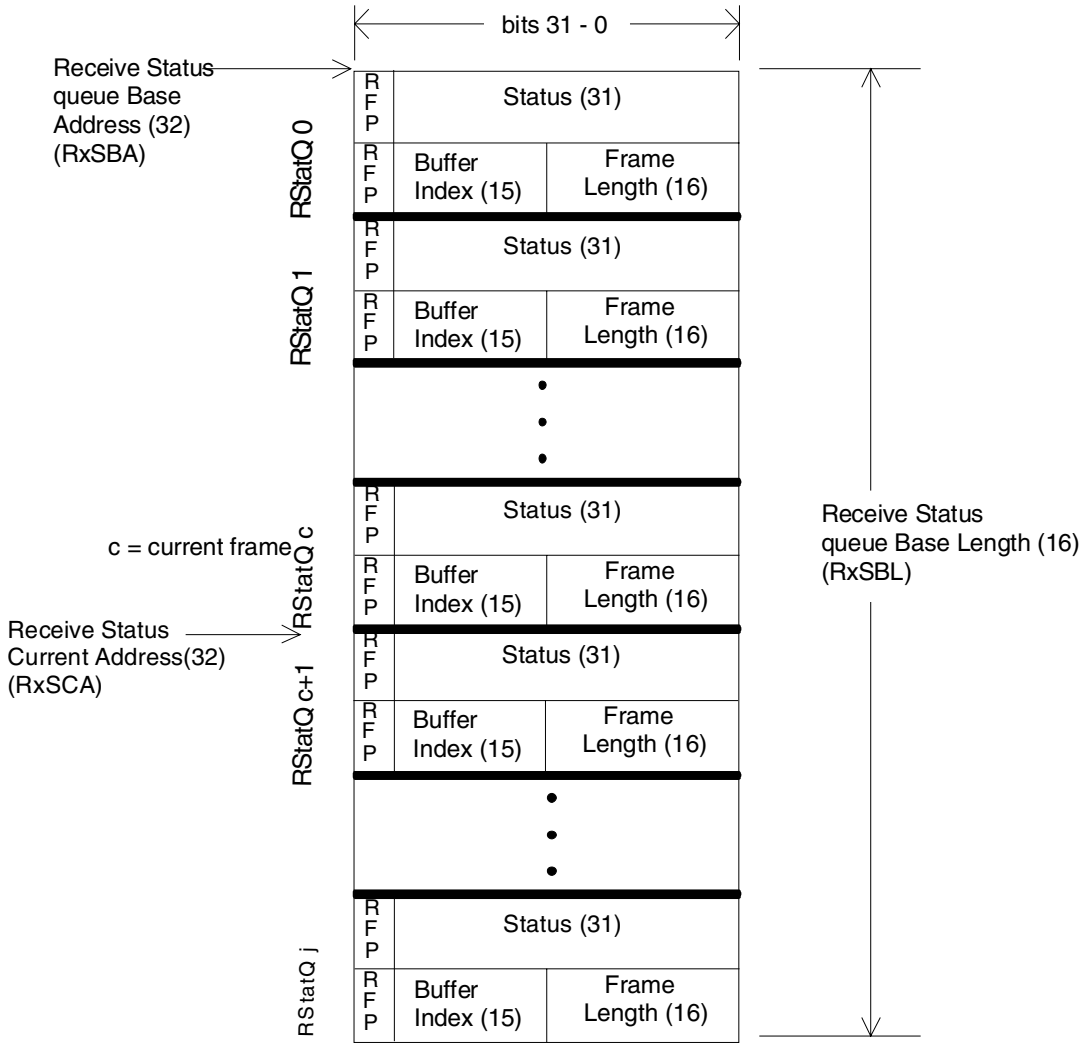
Figure 6-8. Receive Status Queue



Receive status entries are written to the status queue following one of three possible events, end of header, end of buffer, or end of frame. The status event is always written after the appropriate data transfer has been made. For example the end of frame status is written after the last byte of data has been written to the data buffer, not before. The EOF and EOB bits in the status entry can be used to determine the cause of a status entry.

If both EOF and EOB bits are zero, the entry was made for a receive header threshold. This indicates that there have been at least as many bytes transferred as specified in Receive Header Length 1 or 2. These registers may be set to any threshold to provide an early indication to the Host that a receive frame is in progress. The status will contain valid data in the address match and hash table fields, but as the status is provided before end of frame is reached, it will always indicate received without error.

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If the EOF bit is zero and the EOB bit is set, the status indicates that the end of a receive buffer has been reached before the end of the receive frame. If the receive buffers are much smaller than the frame size, there may be many such statuses per frame.

When the EOF and EOB bits are both set, the status indicates the end of frame has been transferred. The EOB is always set at this time to indicate that the MAC has finished transferring to the buffer. The buffer is not necessarily full.

When a status event causes an interrupt, the interrupt pin will be activated after the status has been transferred to the status queue.

6.2.3.1 Receive Status Format

Receive Status - First Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RFP	RWE	EOF	EOB	RSVD				AM		RX_Err	OE	FE	Runt	EData	CRCE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CRCI	RSVD	HTI						RSVD							

Definition:

Receive Status, first word. Contains status information for the receiver operation.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RFP: Receive Frame Processed. The Receive Frame Processed bit is always written as a “1” by the MAC and may be used by the Host to mark its progress through the status queue. The Host may alternatively use the RXStsQCurAdd to determine how much of the status queue to process.

RWE: Received Without Error. The Received Without Error bit indicates that the frame was received without any of the following error conditions: CRCerror, ExtraData, Runt, or Receive Overrun.

EOF: End Of Frame. When this bit is set, the associated buffer contains the last data associated with this frame. In the case of an extra data or overrun error, the buffer may not contain the actual end of frame data. For a receive header status the EOF and EOB bits will both be clear.

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EOB: End Of Buffer. When this bit is set, no more data will be transferred to the associated data buffer. This may be due to an end of frame transfer or to reaching the actual end of the buffer. For a receive header status the EOF and EOB bits will both be clear.

AM: Address Match:
00 - Individual Address match
01 - Global Address match
10 - Hashed Individual Address
11 - Hashed Multicast Address

RX_Err: RX Error. The RX_Err is set for any receive frame for which the RX_ERR (MII pin) was activated.

OE: Overrun Error. The receive overrun bit is set on any frame which could not be completely transferred to system memory. This could be as a result of insufficient buffer space, or an excessive bus arbitration time.

FE: Framing Error. This bit is set for any frame not having an integral number of bytes, and received with a bad CRC value.

Runt: Runt Frame. The Runt bit is set for any receive frame, including CRC, that is shorter than 64 bytes.

EData: Extra Data. The ExtraData bit indicates that the length of the incoming frame was equal or greater than the value programmed in the Max Frame Len register. The receive frame will be terminated at this maximum length to conserve system buffer space.

CRCE: CRC Error. This indicates the frame was received with a bad CRC.

CRCI: CRC Included. This bit is set to one when the CRC has been included in the Receive data buffer. Including or excluding the CRC is controlled by the BufferCRC bit in the RXCtl register.

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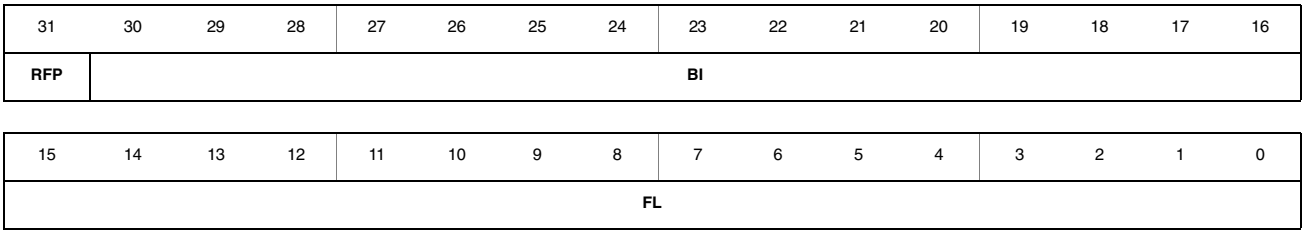
HTI: Hash Table Index. If the frame was accepted as a result of a hash table match, these bits contain the hash table index, otherwise they are written as zero. If the frame was received as a result of Promiscuous Accept, this field will be zero. If the frame was accepted as a result of an Individual Address Match then the field indicates which address was matched, as follows:

000001 - Frame matched Individual Address 0
000010 - Frame matched Individual Address 1
000100 - Frame matched Individual Address 2
001000 - Frame matched Individual Address 3

Receive Status - Second Word



Definition:

Receive Status, second word. Contains status information for the receiver operation.

Bit Descriptions:

RFP: Receive Frame Processed. The Receive Frame Processed bit is always written as a 1 by the MAC, and may be used by the Host to mark its progress through the status queue.

BI: Buffer Index. This field contains the buffer index field from the descriptor table for the data buffer associated with this status entry.

FL: Frame Length. The frame length field contains the total number of bytes transferred for this frame. For an intermediate status (not end of frame) this is the total number of bytes transferred up through the current data buffer.

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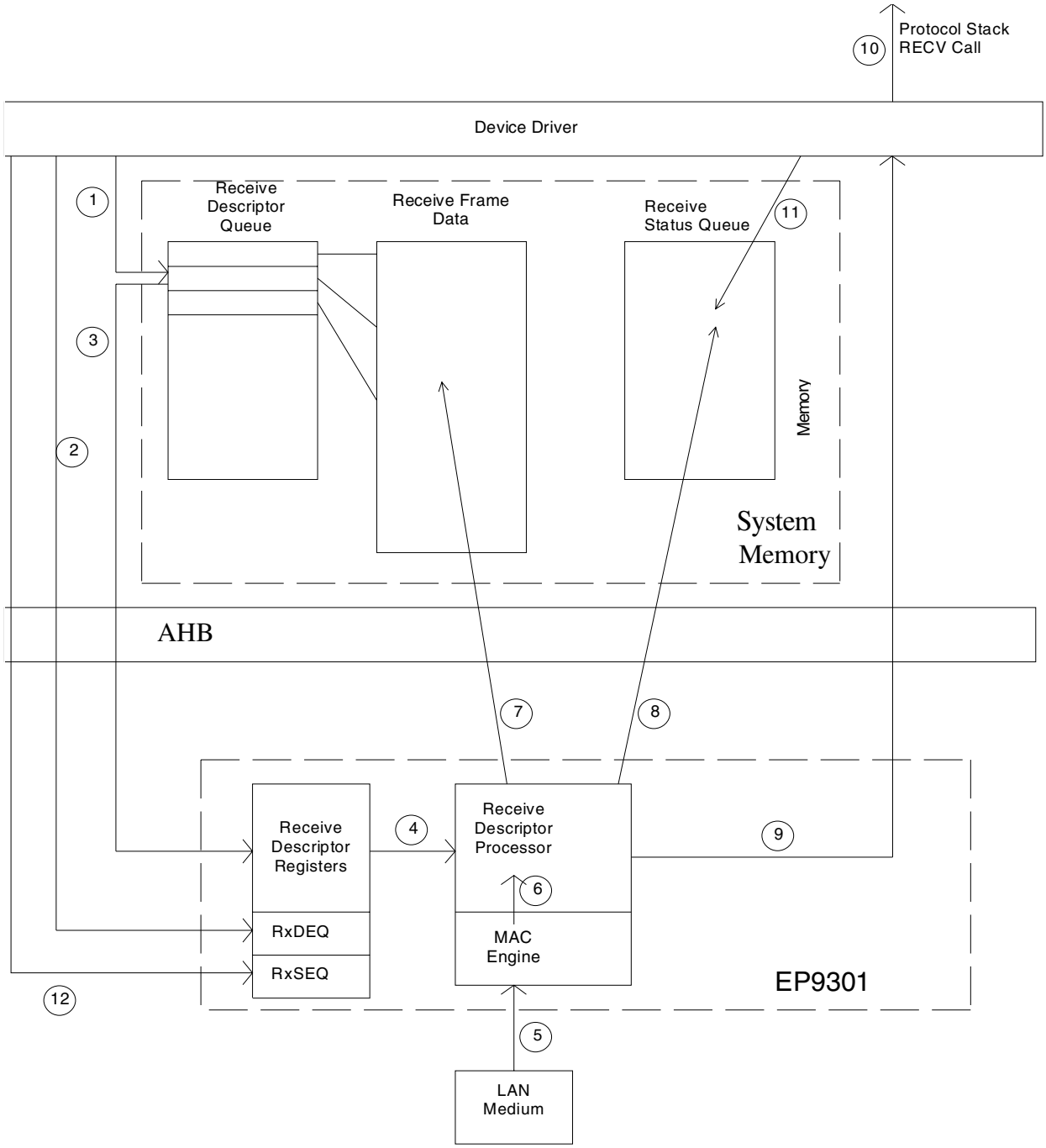
6.2.3.2 Receive Flow

Figure 6-9. Receive Flow Diagram



Refer to the circled numbers in Figure 6-9. The detailed receive flow is:

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1. Driver initializes some number of receive descriptors.
2. Driver writes RXDEnq register with the additional number of receive descriptors.
3. On-chip Descriptor Processor fetches descriptors into internal FIFO decrements RXDEnq appropriately.
4. The address of the next receive data buffer is loaded into the Receive Buffer Current Address.
5. A frame is received from the LAN medium.
6. The MAC Engine passes the frame data to the Receive Data FIFO.
7. The Receive Descriptor Processor stores the frame data into system memory.

   Steps 5, 6, and 7 can overlap.
8. End of frame status is written to the Receive Status Queue the RXStsEnq value reduced by one.
9. Driver interrupted if interrupt conditions met.
10. Received frame passed to the protocol stack.
11. Driver clears the Receive Frame Processed bit in Status Queue.
12. Driver writes number of entries processed in the status queue, freeing them for future use by the MAC.
13. After the driver gets the used receive buffers back from the stack, the driver may repeat step 2.

Steps 1, 11, and 13 are transparent to the MAC. Steps 2 through 10 and 12 directly involve the MAC.

6.2.3.3 Receive Errors

Receive error conditions are broken into two categories: hard errors and soft errors. A hard error is generally considered a reliability problem. This includes AHB bus access problems. A soft error indicates that the frame was not successfully received. The error may be expected or rare. A soft error needs a graceful recovery by the host driver. Soft errors include: CRC errors, receiver over-run, frames too long, or frames too short. Hard errors are parity errors (when enabled), system errors, and master or target aborts, these errors will stop receive DMA activity, and require host intervention for recovery. Recovery may be achieved by performing a RxChRes (Bus Master Control) and reinitializing.

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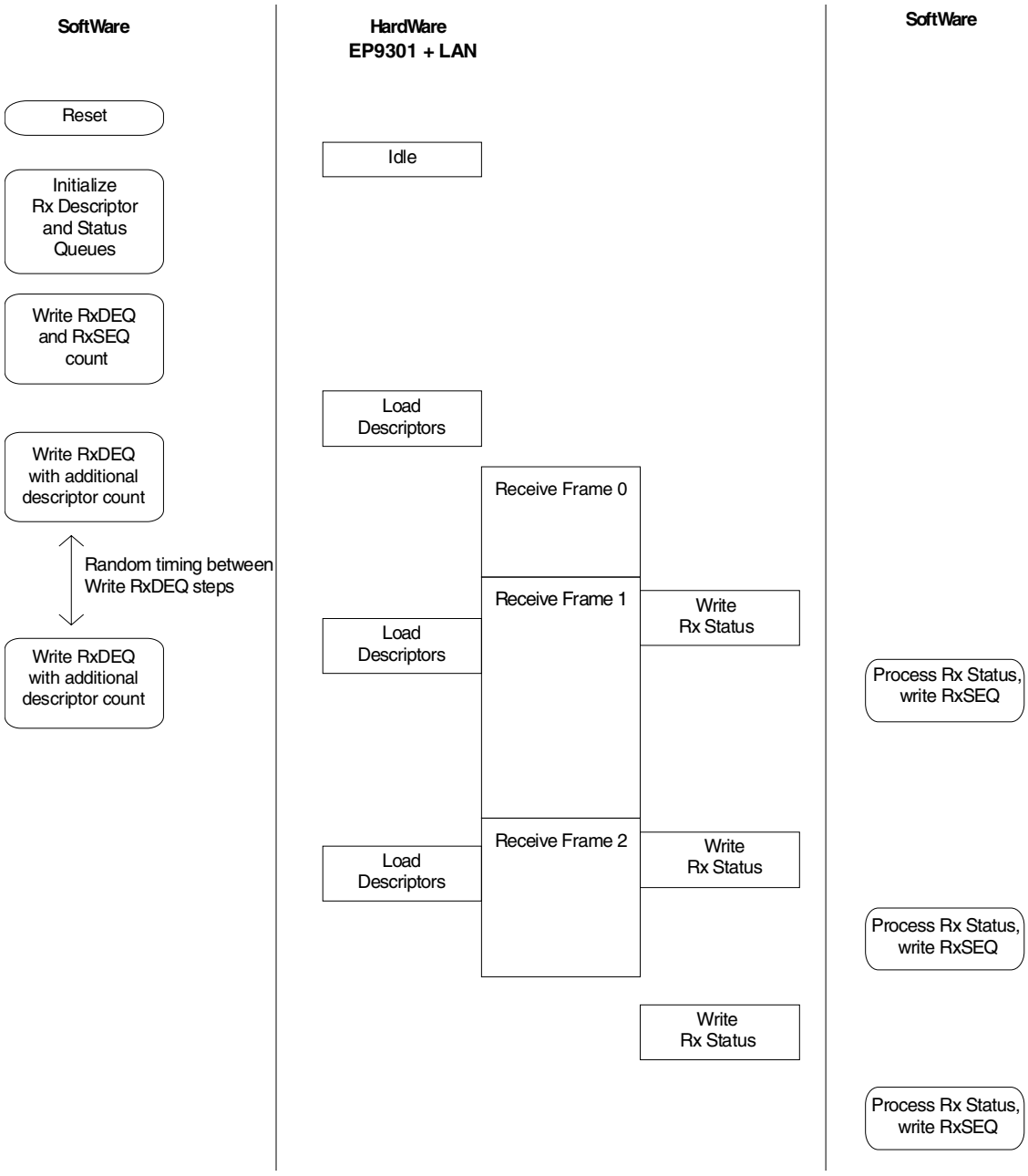
6.2.3.4 Receive Descriptor Data/Status Flow

Figure 6-10. Receive Descriptor Data/Status Flow



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6.2.3.5 Receive Descriptor Example

Figure 6-11. Receive Descriptor Example

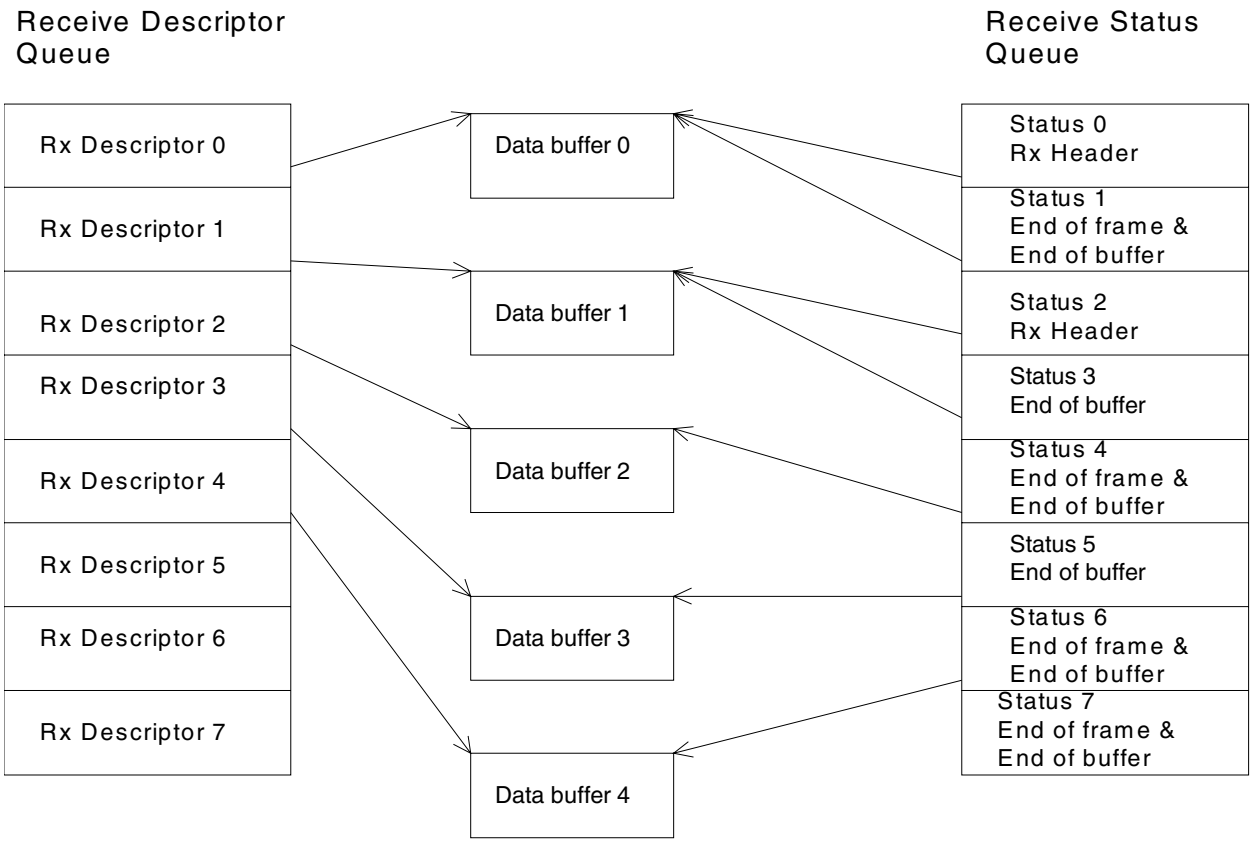

Figure 6-11 shows the state of the receive queues following the reception of four frames. The first frame uses Data buffer 0 only and there are two status entries associated with it. The first status (status 0) is for the reception of a receive header and the second (status 1) is for the end of frame/buffer, both status entries point to the beginning of data buffer 0. The second frame occupies two buffers (data buffers 1 and 2), and three status entries (2, 3, and 4). Status 2 is for the receive header, status 3 for the end of buffer 1 (frame size larger than buffer size), and status 4 for end of frame/buffer. The next two frames both occupy one data buffer each and one status each. This could be the case for short frames that do not exceed the header size or the buffer size. The result of this is that the status queue may be used at a different rate to the descriptor queue, based on the type of traffic and the options selected.

6.2.3.6 Receive Frame Pre-Processing

The MAC pre-processes all incoming receive frames. First the frame is either passed on to the next level or discarded according to the destination address filter. The next decision is whether to accept the frame. A frame is accepted

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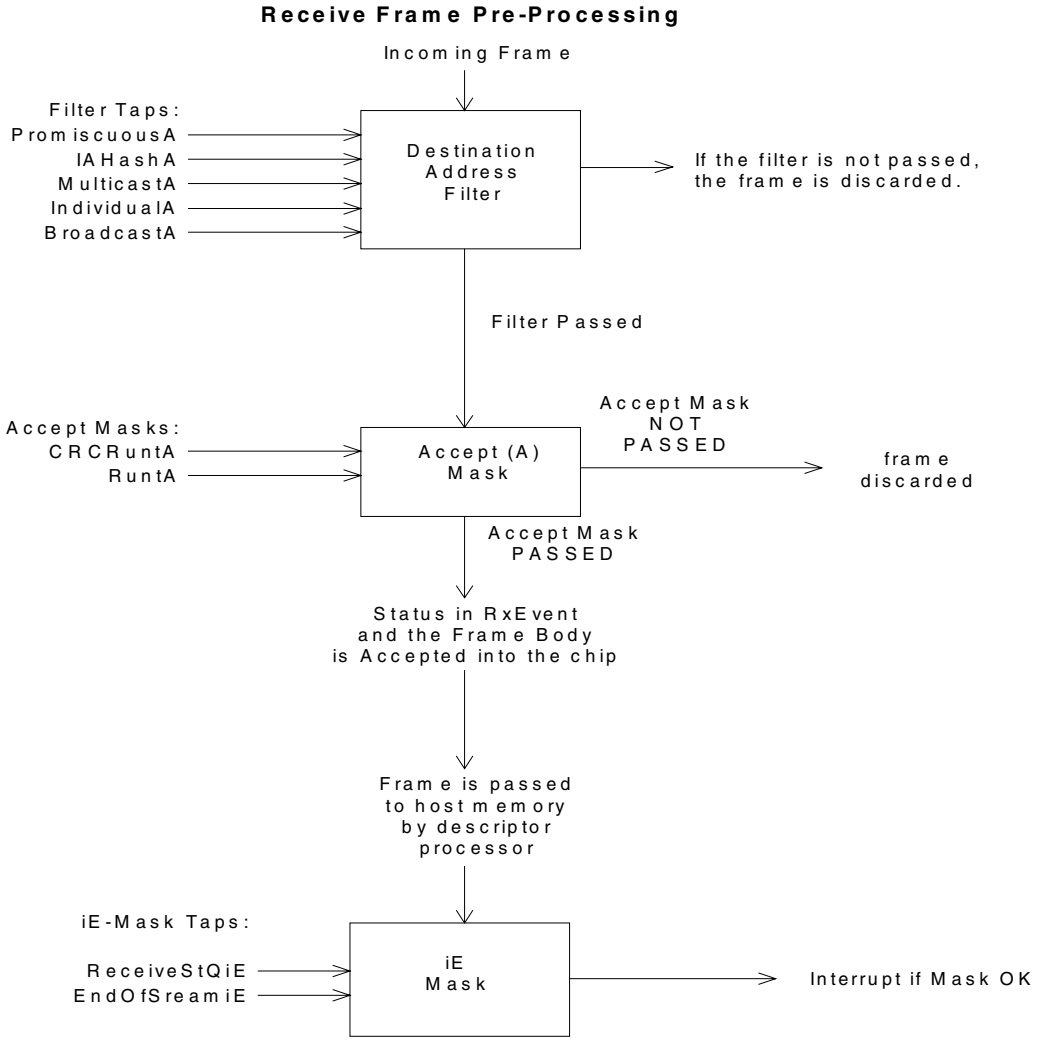
when the frame data are brought into MAC through internal memory. The final step in frame pre-processing is the decision on causing an interrupt. These pre-processing steps are detailed in the diagram on the next page.

Figure 6-12. Receive Frame Pre-processing



6.2.3.7 Transmit Descriptor Processor

6.2.3.8 Transmit Descriptor Queue

The Transmit descriptors are passed from the Host to the MAC via the Transmit descriptor queue. The Transmit descriptor queue is a circular queue occupying a contiguous area of memory. The location and size of the queue are set at initialization by the Host writing to the Transmit Descriptor Queue Base Address Register and the Transmit Descriptor Queue Base Length. The base address must point to a word aligned memory location. The Transmit Descriptor Queue Base Length is set to the length in bytes of the queue. The

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length should be an integral number of descriptors and must not exceed 64 Kbytes total. The Transmit descriptor current address must also be set at initialization to point to the first descriptor to be used. This would normally be the first entry (same value as the base address).

Following initialization, the MAC will start to use descriptors from the Current Descriptor Address, wrapping back to the base pointer whenever the end of the queue is reached. In normal operation the Host should not need to access these registers after the initialization. The management of the descriptors is handled via the Transmit Descriptor Enqueue register.

Enqueueing descriptors is the process of adding descriptors to an existing queue. This is achieved in transmit by writing the number of additional descriptors to the Transmit Descriptor Enqueue register. The written value will be added to the previous value to keep a running total, as descriptors are read by the MAC, the total is adjusted. The running total is available by reading the enqueue register. One frame may be described by more than one descriptor, but the final descriptor will contain the EOF bit. Not all the descriptors for a frame need to be supplied at once.

No more than 255 descriptors may be added in one write. If a number greater than this needs to be written. the write should be broken up into more than one operation (that is, to add 300 descriptors - first write 255, then write 45).

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Figure 6-13. Transmit Descriptor Format and Data Fragments

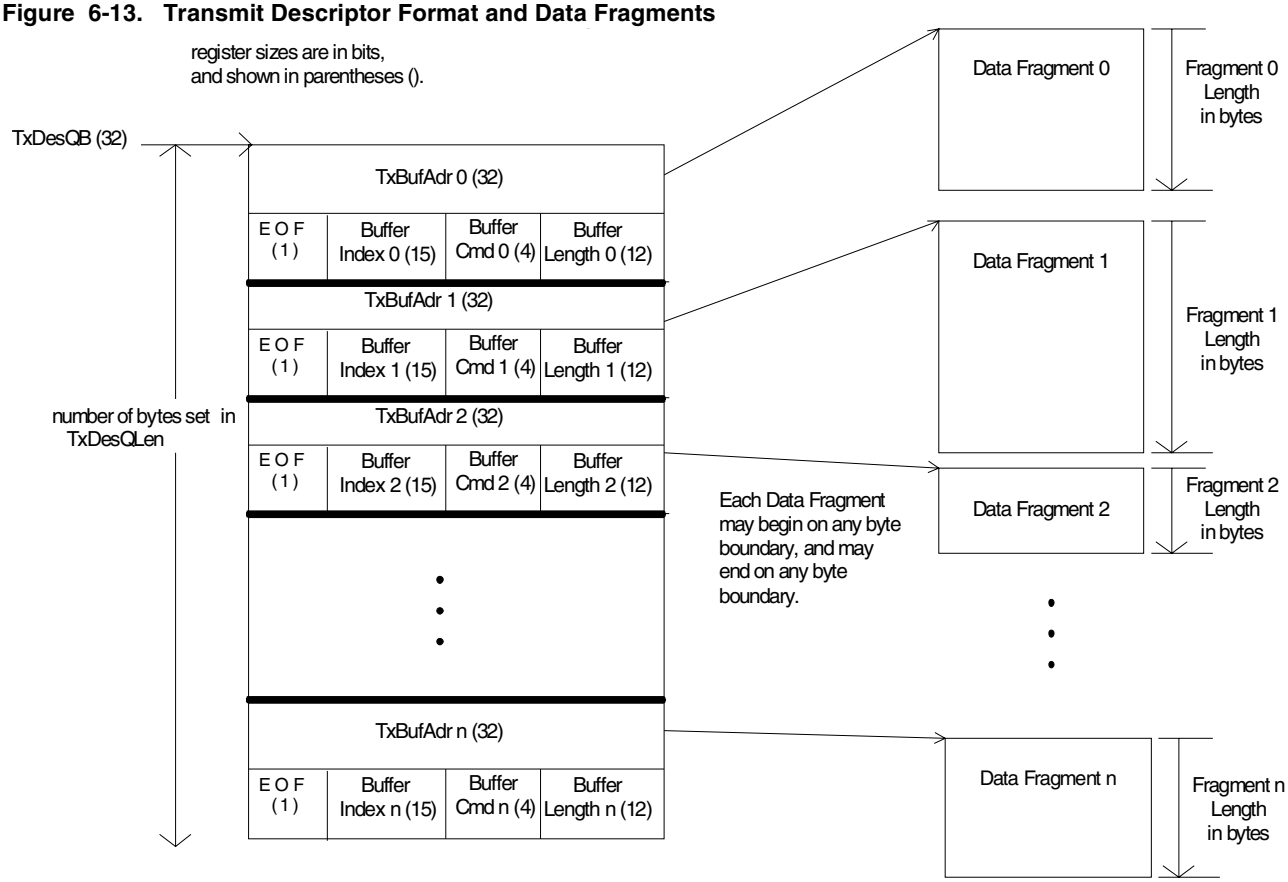
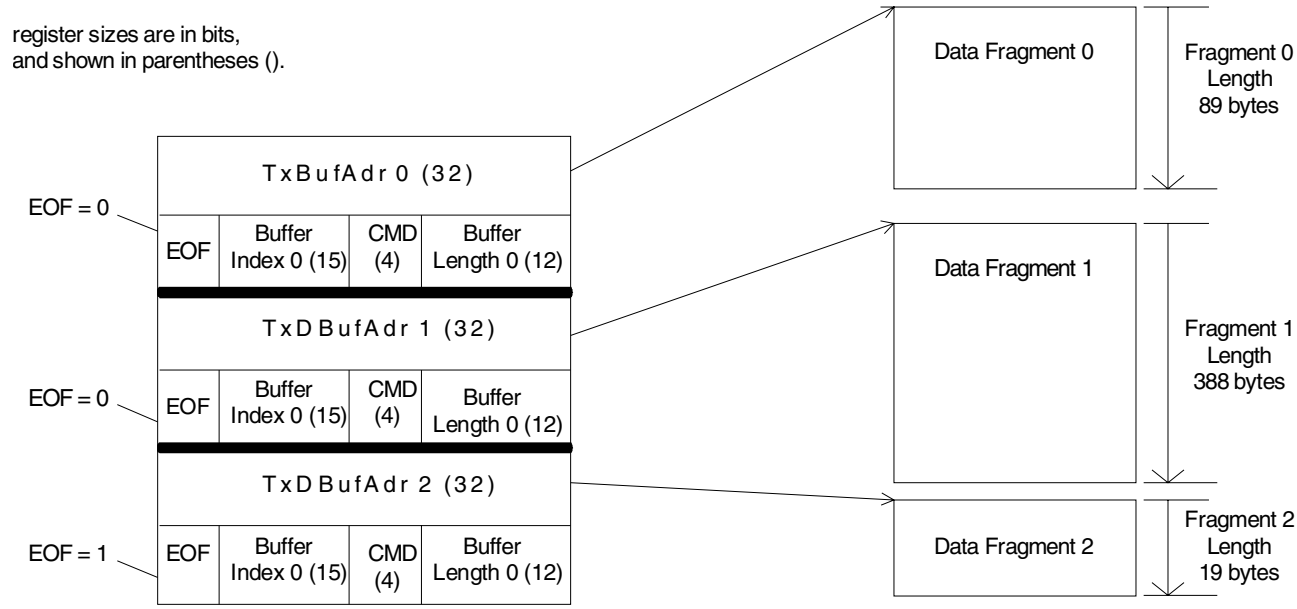


Figure 6-14. Multiple Fragments Per Transmit Frame

Example: Fragments 0, 1, 2 make-up one complete frame.



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In the example shown in Figure 6-14, one frame is transmitted from three fragments. The MAC starts the frame by acquiring the medium and transmitting the preamble. Then, the fragments 0, 1, 2 are transmitted in order for a total of 446 bytes (39 + 388 + 19). Since the CRC bit in the first frame fragment is clear, the HW appends the 4 byte CRC. Thus, 4 more bytes are added to the frame for the CRC making the total frame length 450 bytes. Finally, the MAC sends the end-of-frame.

The CMD field is 4 bits. Only the AF bit is valid. The other fields are reserved.

6.2.3.9 Transmit Descriptor Format

Transmit Descriptor Format - First Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TBA															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TBA															

Definition:

Transmit Descriptor, first word. Contains the base address of the data buffer.

Bit Descriptions:

TBA: Transmit Buffer Address. The transmit buffer address contains the 32 bit address pointer to the transmit buffer. The base address of the data buffer must be word-aligned (32-bit aligned).

Transmit Descriptor Format - Second Word

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
EOF	TBI														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AF	RSVD			TBL											

Definition:

Transmit Descriptor, second word. Contains control, index and length for the descriptor.

Bit Descriptions:

EOF: End of Frame. When this bit is set, the descriptor terminates a transmit frame. When clear, the descriptor is not the end of frame and a future descriptor will provide the EOF.

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TBI: Transmit Buffer Index. The transmit buffer index is provided to help the Host software keep track of the transmit buffers. A copy of the index for the first buffer of a frame is kept in the MAC, and is included in any status written for the particular frame.

AF: Abort Frame. When the Abort Frame and EOF bits are set in a descriptor, the transmit frame will be terminated with a bad CRC. A bad CRC is applied even when the InhibitCRC bit (TXCtl) is set. The Abort Frame bit is ignored in a descriptor which does not have the EOF bit set. The abort feature is useful in a forwarding environment, where the integrity of the incoming frame is not known before the outgoing frame is started. If the incoming frame is received with error, the outgoing frame can be then invalidated. The AF bit is the only valid bit in the CMD field.

RSVD: Reserved. Unknown During Read.

TBL: Transmit Buffer Length. This field contains the byte count of the number of bytes in the transmit buffer. There are no restrictions on the actual buffer size. If the length is set to zero, the descriptor will be ignored. A frame may not be terminated with a zero length buffer.

6.2.3.10 Transmit Status Queue

The Transmit Status queue is used to pass transmit status from the MAC to the Host. In operation the status queue is similar to the transmit descriptor queue, it is a circular queue in contiguous memory space. The location and size of the queue are set at initialization by the Host writing to the Transmit Status Queue Base Address, and the Transmit Status Queue Base Length registers. The base address must point to a word aligned memory location. The length is set to the actual status queue length in bytes. This should be an integral number of status entries and should not exceed 64 Kbytes total. The Current Address must be set to point to the first status entry to be used. This would normally be the first entry in the queue (same value as the base address).

The Host needs to ensure that in operation there is always room in the status queue for any transmit frame which is enqueued in the transmit descriptor queue.

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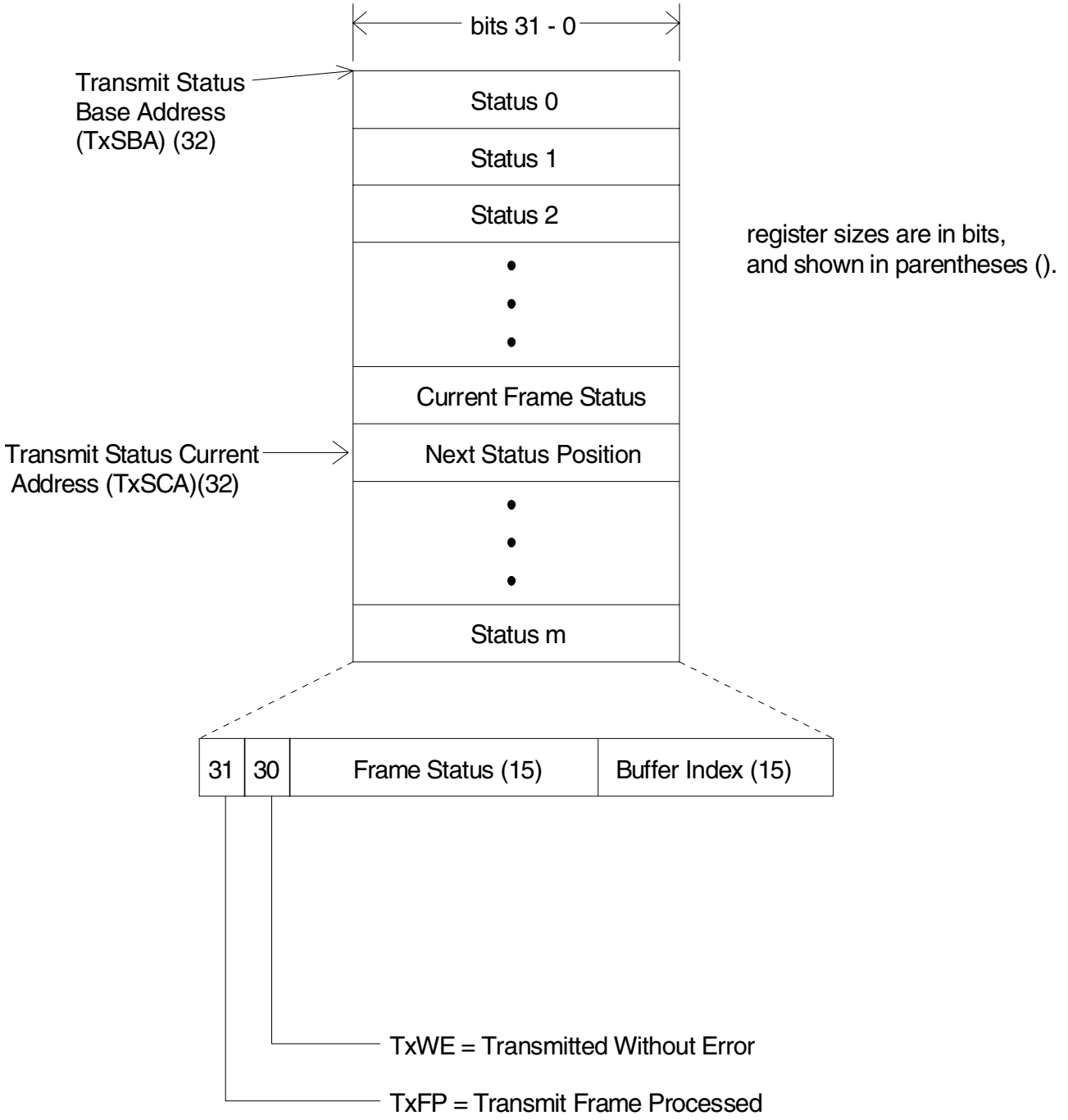
Figure 6-15. Transmit Status Queue



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6.2.3.11 Transmit Status Format

Only one Transmit Status entry is posted for each transmit frame, regardless of the number of transmit descriptors that are used to describe the frame.

Transmit Status

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TxFP	TxWE	FA	LCRS	RSVD	OW	TxU	EColl	RSVD				NColl			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	TBI														

Definition:

Transmit Status. Contains the status information for the transmitter operation.

Bit Descriptions:

TxFP: Transmit Frame Processed. The Transmit Frame Processed bit is always written as a 1 by the MAC, and may be used by the Host to mark its progress through the status queue.

TxWE: Transmitted Without Error. The transmitted Without Error bit is set when a frame is successfully transmitted without errors.

FA: Frame Abort. When a frame has been terminated by the Host with an Abort Frame command, in the transmit descriptor, the Frame Abort status bit is set.

LCRS: Loss of CRS. The Loss of CRS bit is set when a frame is transmitted and the MII CRS signal is not asserted at the end of preamble.

RSVD: Reserved. Unknown During Read.

OW: Out of Window. The Out of Window bit indicates that a collision was detected after the transmission of more than 60 bytes (from the start of preamble).

TxU: Transmit Underrun. TxUnderrun is set when a frame fails to be transmitted because of an excessive bus latency starving the transmitter.

EColl: Excess Collisions. The excessive collision bit is set when the frame failed to transmit due to excessive collisions. This may either be due to one or sixteen collisions dependent on the OneColl bit in the transmit descriptor.

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NColl: Number of Collisions. This field contains the number of collisions that were experienced in transmitting this frame.

TBI: Transmit Buffer Index. The transmit buffer index is a copy of the transmit buffer index from the first descriptor of a transmit frame. This is provided as an aid to the Host software in keeping track of the transmit buffers.

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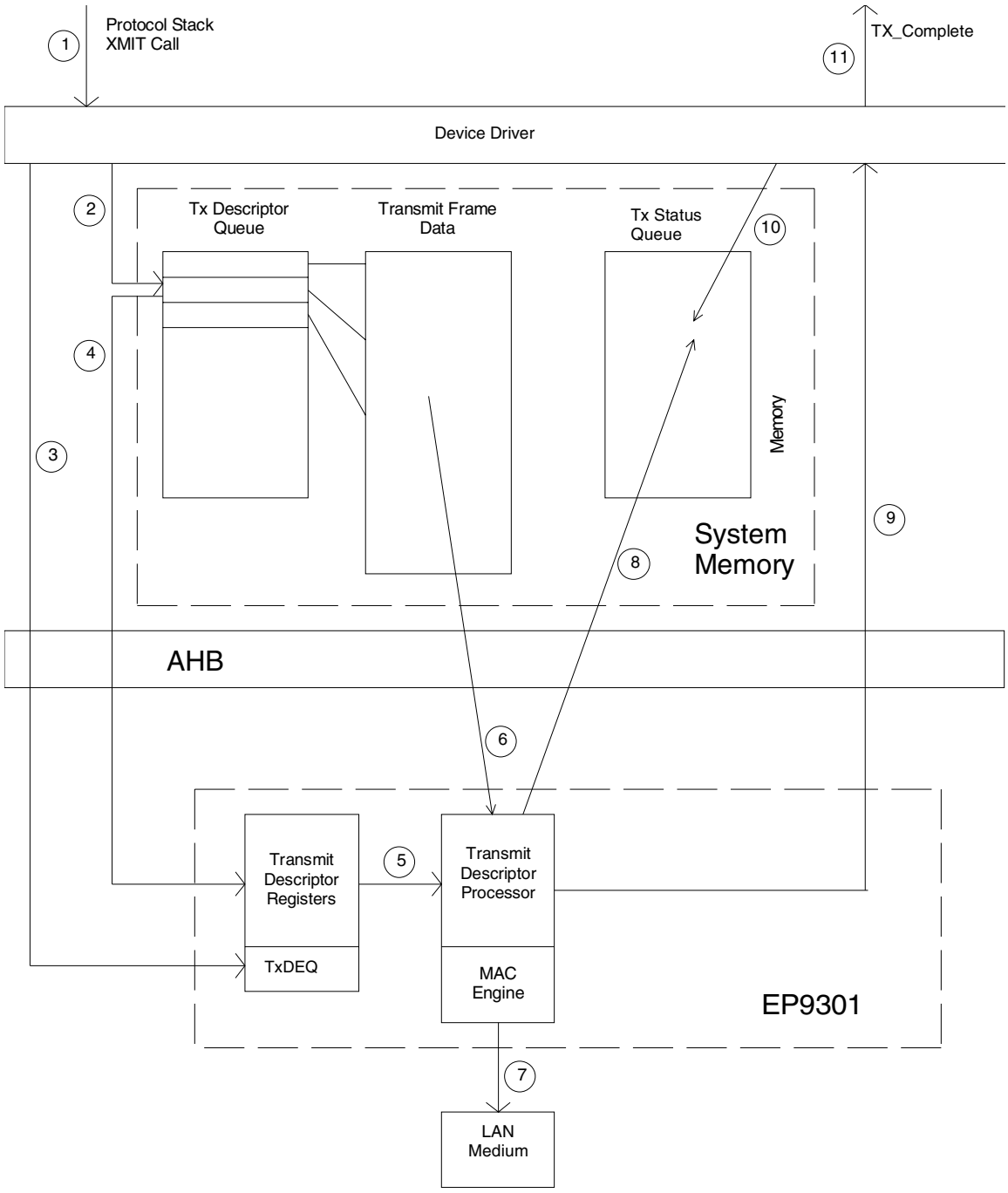
6.2.3.12 Transmit Flow

Figure 6-16. Transmit Flow Diagram



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Refer to Figure 6-16. The detailed transmit flow is:

1. Protocol stack initiates a transmit frame.
2. Driver parses protocol stack buffer into Transmit Descriptor Queue.
3. Driver writes number of additional entries to the Transmit Enqueue register.
4. On-chip Descriptor Processor fetches descriptor information.
5. On-chip Descriptor Processor initiates data move.
6. Frame data fetched from system memory into the transmit FIFO.
7. Frame transmitted onto LAN medium. Steps 6 and 7 can overlap.
8. End of frame status written to status queue
9. Driver interrupted if interrupt conditions met.
10. Driver processes the transmit status
11. Driver informs the protocol stack that transmit is complete.

Steps 1, 2, 10, and 11 are transparent to the MAC block. Steps 3 through 9, inclusive, directly involve the MAC.

6.2.3.13 Transmit Errors

Transmit error conditions are broken into two categories: hard errors and soft errors. A hard error is generally considered a reliability problem. This includes AHB bus access problems. A soft error indicates that the frame was not successfully transmitted. The error may be expected or rare. A soft error needs a graceful recovery by the host driver. Soft errors include: excessive collisions, SQE error (if connected to a MAU). Hard errors are parity errors (if enabled), system errors, master and target aborts. These will stop further transmit DMA activity and require host intervention for recovery.

Hard errors cause the descriptor processor to halt operation. This allows the Host to determine the cause of error and reinitialize and restart the bus master operations.

Most soft errors do not cause the frame processing operations to halt. The descriptor processor simply flags the error and continues on to the next frame. The exception is on a transmit underrun. By halting the transmit frame processing, the Host has the ability to reinitialize the transmit descriptor processor registers to point to the start of the failed frame and reinitialize. This will cause the MAC to reattempt the failed frame and allows the order of frame transmission to be maintained.

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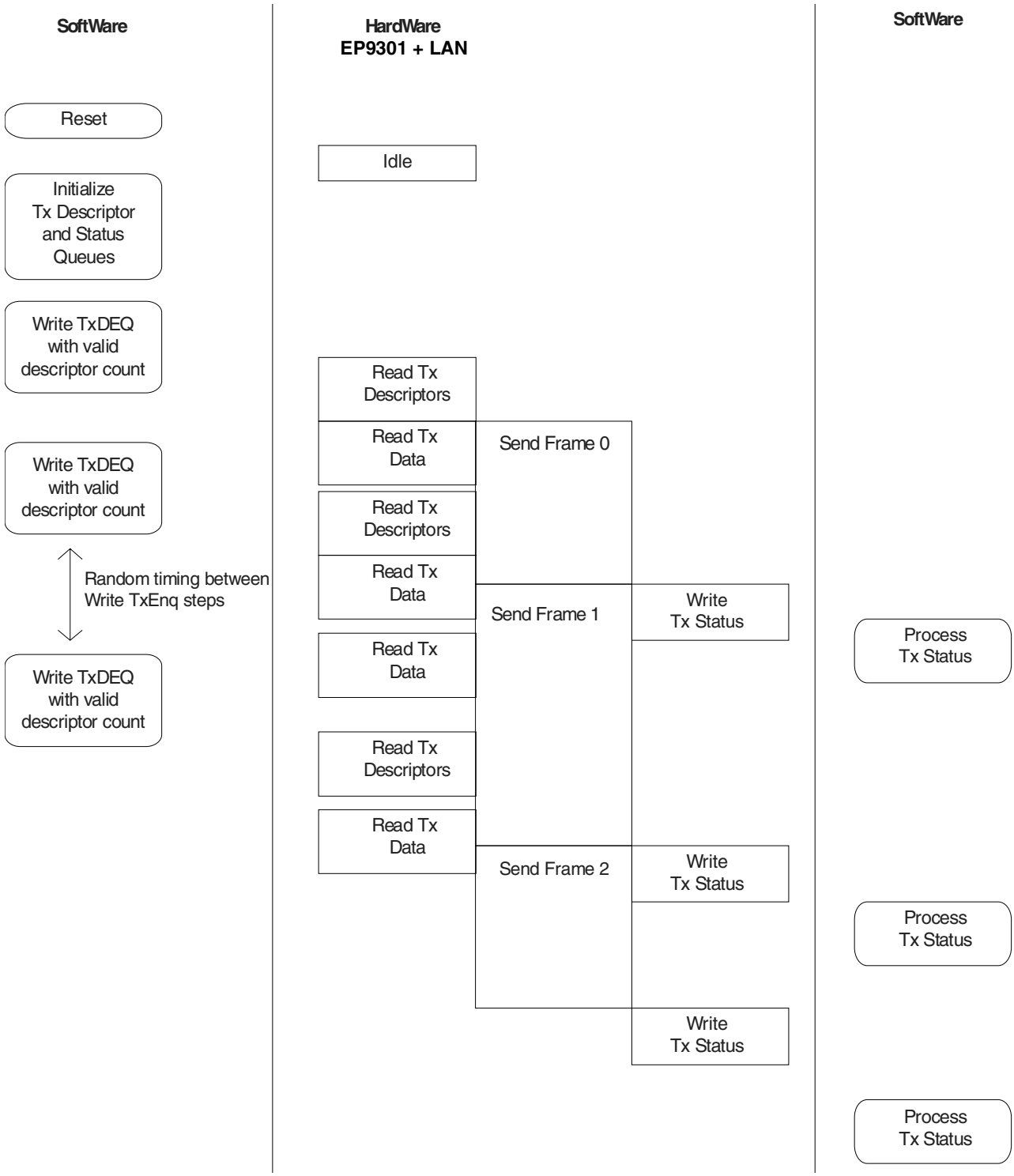
6.2.3.14 Transmit Descriptor Data/Status Flow

Figure 6-17. Transmit Descriptor Data/Status Flow



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6.2.4 Interrupts

6.2.4.1 Interrupt Processing

Interrupts can be associated with on chip status or with off-chip status. (Off-chip status is status that has been transferred to either the transmit or receive status queue.) The status for any outstanding interrupt event is available via two different register addresses: IntStsP (Interrupt Status Preserve) and IntStsC (Interrupt Status Clear).

Reading the IntStsP register has no effect on the bits set in the register. They may be explicitly cleared by writing a “1” back to any of the bit positions. This allows the Host to process interrupt events across multiple routines, only clearing the bits for which it has processed the corresponding events.

The IntStsC register will clear the status for all outstanding events when it is read. This provides a quick mechanism for the Host to accept all the outstanding events in one read and not incur the additional IO cycles required in specifically clearing the events.

6.2.5 Initialization

The following is the suggested hardware initialization sequence for a driver:

1. Determine what PHYs are available (poll PHYs via the management interface via MICmd, MIIData, and MIISts registers.
2. Enable auto negotiation to determine the mode of operation 10/100 Mbit, FDX/HDX. This may be needed to determine the amount of buffering to use.
3. Set RXDQBAdd and RXDCurAdd to point to the start of the receive descriptor queue
4. Set RXDQBLen to the length of the receive descriptor queue.
5. Set RXStsQBAdd and RXStsQCurAdd to point at the start of the receive status queue.
6. Set RXStsQBLen to the length of the status queue.
7. Set BMCtl.RxEn which clears the RXDEnq/RXStsEnq registers and initializes internal pointers to the queues. No bus master activity is triggered by the enable, because the enqueue registers are zero.
8. Set TXDQBAdd and TXDQCurAdd to point to the start of the transmit descriptor queue.
9. Set TXDQBLen to the length of the transmit descriptor queue.
10. Set TXStsQBAdd and TXStsQCurAdd to point to the start of the transmit status queue.

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11. Set TXStsQBLen to the length of the status queue.
12. Set BMCtl.TxEn which clears the TXDEnq and initializes internal pointers to the queues. No bus master activity is triggered by the enable because the enqueue register is zero.
13. Set required interrupt mask and global interrupt mask (IntEn, GlIntMsk).
14. Wait for RxAct (BMSts) to be set, and then enqueue the receive descriptors and status. This will trigger bus master activity for the descriptor reads.
15. Set the required values for Individual Address and Hash Table.
16. Set the required options in RXCtl and TXCtl, enabling SRxON, and STxON.
17. Set any required options in the PHY, and activate.
18. Enqueue transmit descriptors as required.

6.2.5.1 Interrupt Processing

This is the suggested method for processing an interrupt:

1. Interrupt received from the LAN Controller. This may be determined directly by vectoring to the interrupt service routine, or in a shared environment by polling the interrupt status register.
2. Read the Interrupt Status Clear register. Based on the result of the low byte, one or more of three processes need to run - receive queue processing, transmit queue processing, or other processing.

6.2.5.2 Receive Queue Processing

1. Read the RXStsQCurAdd. This is the point to which the Host needs to process the status queue.
2. Read status entries up to the value of RXStsQCurAdd.
3. For each status entry, process the receive data. Return the descriptor to the receive descriptor queue.
4. Write the number of statuses processed to the RXStsEnq.
5. Write the number of descriptors returned to the RXDEnq. Writing once to each enqueue register is more economical on bus cycles than writing once for every descriptor or status entry. Writing once also avoids any possible delays that may otherwise occur when the controller has to process multiple accesses to the same descriptor.

6.2.5.3 Transmit Queue Processing

1. Read TXStsQCurAdd. This is the point to which the Host needs to process the status queue.

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2. Read status entries up to the value of the TXStsQCurAdd.
3. For each status entry, free the data buffer.

6.2.5.4 Other Processing

The upper three bytes of the Interrupt Status register provide the specific information related to the “Other” bit in the LSB. There are a number of bits that relate to the descriptor queues.

1. RxMiss - This bit indicates that the receive frames have been missed which may be the result of insufficient bus bandwidth being available, or of a lack of receive descriptors, or free receive status locations.
2. RxBuffers - This bit is a warning that the last free receive descriptor has been read by the controller, and RXDEnq is now zero.In a system with a dynamic number of receive buffers, this may be use as a trigger to allocate more buffers.
3. End of Chain - This bit is set when the last transmit descriptor has been read into the controller (TXDEnq equal to zero). The controller may still be transmitting at this time due to the local descriptor and data storage. This bit may be used as a signal to add more transmit descriptors, if available.
4. TxLenErr - This signifies that the controller has processed a transmit frame that exceeds the maximum allowable length. This may be caused by an internal error in the controller, a data corruption in the transmit descriptors, or a Host programming error in the descriptor queue. The error will cause the transmit descriptor processor to halt. The Host should perform the Transmit Restart Process detailed in “Transmit Restart Process” on page 157.
5. TxUnderrun Halt - When the Halt on Underrun (BMCtl) is set and an underrun occurs, the transmit descriptor processor will halt. The underrun may be the result of insufficient bus bandwidth available, or the lack of the next transmit descriptor. The Host should perform the Transmit Restart Process detailed in “Transmit Restart Process” on page 157.

6.2.5.5 Transmit Restart Process

Following a halt of the transmit descriptor processor from a Halt on Underrun, TxLength Error, or setting the TxDis (BMCtl), processing may be restarted from the same point in the queues or from a different point. To start from the same point, the Host only needs to set BMCtl.TxEn. To start from a different point the following steps should be taken:

1. Process any transmit status entries in the transmit status queue (up to TXStsQCurAdd).
2. Set TxChRes in BMCtl and wait for the bit to clear. This ensures that the reset is complete.

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3. Set the TXDQBAdd to the start of the descriptor queue.
4. Set TXDQBLen to the length of the descriptor queue.
5. Determine the point in the transmit descriptor where the controller should start processing, and set the TXDQCurAdd to this address. This point may be from the frame which caused the initial problem.
6. Set the TXStsQBAdd to the start of the status queue.
7. Set the TXStsQBLen to the length of the status queue.
8. Determine the point at which the controller should start writing status entries, and set the TXStsQCurAdd to this address. This can be the start of the status queue, as all existing status entries have been processed.
9. Set TxEn in BMCtl. This will cause the transmit descriptor processor to reinitialize.
10. Wait for TxAct in BMSts to be set and then write the appropriate number of descriptors remaining in the queue to TXDEnq.

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6.3 Registers

Table 6-3: Ethernet Register List

Address	Name	Description
0x8001_0000	RXCtl	MAC Receiver Control Register
0x8001_0004	TXCtl	MAC Transmitter Control Register
0x8001_0008	TestCtl	MAC Test Control Register
0x8001_0010	MIICmd	MAC MII Command Register
0x8001_0014	MIIData	MAC MII Data Register
0x8001_0018	MIISts	MAC MII Status Register
0x8001_0020	SelfCtl	MAC Self Control Register
0x8001_0024	IntEn	MAC Interrupt Enable Register
0x8001_0028	IntStsP	MAC Interrupt Status Preserve Register
0x8001_002C	IntStsC	MAC Interrupt Status Clear Register
0x8001_0030 - 0x8001_0034		Reserved
0x8001_0038	DiagAd	MAC Diagnostic Address Register
0x8001_003C	DiagDa	MAC Diagnostic Data Register
0x8001_0040	GT	MAC General Timer Register
0x8001_0044	FCT	MAC Flow Control Timer Register
0x8001_0048	FCF	MAC Flow Control Format Register
0x8001_004C	AFP	MAC Address Filter Pointer Register
0x8001_0050 - 0x8001_0055	IndAd	MAC Individual Address Register, (shares address space with HashTbl)
0x8001_0050 - 0x8001_0057	HashTbl	MAC Hash Table Register, (shares address space with IndAd)
0x8001_0060	GlIntSts	MAC Global Interrupt Status Register
0x8001_0064	GlIntMsk	MAC Global Interrupt Mask Register
0x8001_0068	GlIntROSts	MAC Global Interrupt Read Only Status Register
0x8001_006C	GlIntFrc	MAC Global Interrupt Force Register
0x8001_0070	TXCollCnt	MAC Transmit Collision Count Register
0x8001_0074	RXMissCnt	MAC Receive Miss Count Register
0x8001_0078	RXRuntCnt	MAC Receive Runt Count Register
0x8001_0080	BMCtl	MAC Bus Master Control Register
0x8001_0084	BMSts	MAC Bus Master Status Register
0x8001_0088	RXBCA	MAC Receive Buffer Current Address Register
0x8001_0090	RXDQBAdd	MAC Receive Descriptor Queue Base Address Register
0x8001_0094	RXDQBLen	MAC Receive Descriptor Queue Base Length Register
0x8001_0096	RXDQCurLen	MAC Receive Descriptor Queue Current Length Register
0x8001_0098	RXDCurAdd	MAC Receive Descriptor Current Address Register
0x8001_009C	RXDEnq	MAC Receive Descriptor Enqueue Register
0x8001_00A0	RXStsQBAdd	MAC Receive Status Queue Base Address Register
0x8001_00A4	RXStsQBLen	MAC Receive Status Queue Base Length Register
0x8001_00A6	RXStsQCurLen	MAC Receive Status Queue Current Length Register
0x8001_00A8	RXStsQCurAdd	MAC Receive Status Queue Current Address Register
0x8001_00AC	RXStsEnq	MAC Receive Status Enqueue Register
0x8001_00B0	TXDQBAdd	MAC Transmit Descriptor Queue Base Address Register

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0x8001_00B4	TXDQBLen	MAC Transmit Descriptor Queue Base Length Register
0x8001_00B6	TXDQCurLen	MAC Transmit Descriptor Queue Current Length Register
0x8001_00B8	TXDQCurAdd	MAC Transmit Descriptor Current Address Register
0x8001_00BC	TXDEnq	MAC Transmit Descriptor Enqueue Register
0x8001_00C0	TXStsQBAdd	MAC Transmit Status Queue Base Address Register
0x8001_00C4	TXStsQBLen	MAC Transmit Status Queue Base Length Register
0x8001_00C6	TXStsQCurLen	MAC Transmit Status Queue Current Length Register
0x8001_00C8	TXStsQCurAdd	MAC Transmit Status Queue Current Address Register
0x8001_00D0	RXBufThrshld	MAC Receive Buffer Threshold Register
0x8001_00D4	TXBufThrshld	MAC Transmit Buffer Threshold Register
0x8001_00D8	RXStsThrshld	MAC Receive Status Threshold Register
0x8001_00DC	TXStsThrshld	MAC Transmit Status Threshold Register
0x8001_00E0	RXDThrshld	MAC Receive Descriptor Threshold Register
0x8001_00E4	TXDThrshld	MAC Transmit Descriptor Threshold Register
0x8001_00E8	MaxFrmLen	MAC Maximum Frame Length Register
0x8001_00EC	RXHdrLen	MAC Receive Header Length Register
0x8001_0100 - 0x8001_010C		Reserved
0x8001_4000 - 0x8001_FFFF	MACFIFO	MAC FIFO RAM

Control Register Description

RXCtl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD											PauseA	RxFCE1	RxFCE0	BCRC	SRxON

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		RCRCA	RA	PA	BA	MA	IAHA	RSVD				IA3	IA2	IA1	IA0

Address:

0x8001_0000 - Read/Write

Chip Reset:

0x0000_0x0x

Rx Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Receiver Control Register. The Receive Control register is reset by Rx Reset signal generated by holding the TESTSELn pin low. The same signal is also used to reset the receive MAC. The purpose of having a separate reset signal is to be able to avoid resetting the receive MAC when the AHB bus is in a

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powered down state (RESET active), and wakeup frames need to be detected.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

Table 6-4: Individual Accept, RxFlow Control Enable and Pause Accept Bits

IA[1:0] Individual Accept	RxFCE[1:0] Receive Flow Control Enable	PauseA Pause Accept	Action
0	X	X	Frame discarded (do not pass the address filter)
1	1	0	MAC Control frames are recognized, flow control action taken, and frames not passed to host. Non pause MAC Control frames are passed on to host.
1	1	1	MAC Control frames are recognized, flow control action taken, and all MAC control frames are passed on to host.
1	0	X	MAC Control frames are not distinguished from other frame types, all frames passed on to host.

Note: The IA field of the table means the same Individual Addresses as RxFCE, that is, IA0 implies RxFCE0 and IA1 implies RxFCE1

PauseA: Pause Accept. When set, Pause frames are passed on to the Host as regular frames. When clear, the frames are discarded. The handling of MAC Control frames depends on the Pause Accept bit as well as the appropriate Individual Accept and RxFlow Control Enable bits, as follows.

RxFCE1: Rx Flow Control Enable, bit 1. Setting the RxFCE1 bit causes all receive frames that pass the Individual Address [1] register to be scanned for flow control format and, if detected, the Transmit Flow Control Timer register is set appropriately.

RxFCE0: Rx Flow Control Enable, bit 0. Setting the RxFCE0 bit causes all receive frames that pass the Individual Address [0] register to be scanned for flow control format and, if detected, the Transmit Flow Control Timer register is set appropriately.

BCRC: Buffer CRC. When set, the received CRC is included in the received frame buffer, and the received frame length includes the four byte CRC. When clear, neither the receive buffer nor the receive length includes the CRC.

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SRxON: Serial Receive ON. The receiver is enabled when set. When clear, no incoming signals are passed through the receiver. When a frame is being received, and SerRxON is cleared, then that receive frame is completed. No subsequent receive frames are allowed until SerRxON is set again.

RCRCA: Runt CRCA. When set, received frames, which pass the destination address filter, but are smaller than 64 bytes, and have a CRC error are accepted. However, the MAC discards any frame of length less than 8 bytes. When clear, frames received less that 64 bytes in length with CRC errors are discarded.

RA: Runt A. When set, received frames, which pass the destination address filter, but are smaller than 64 bytes, with a good CRC, are accepted. However, the MAC discards any frame of length less than 8 bytes. When clear, frames received less that 64 bytes in length, with a good CRC are discarded.

PA: Promiscuous A. All frames are accepted when set.

BA: Broadcast A. When set, received frames are accepted with all 1s in the DA.

MA: Multicast A. When set, received frames are accepted if the DA, when hashed, matches one of the hash table bits, and the frame is a multicast frame (first bit of destination address = 1). See Descriptor Processor Transmit Registers.

IAHA: Individual Address Hash A. When set, received frame are accepted when the DA is an Individual Address (first bit of DA = 0), that is accepted by the hash table. See Descriptor Processor Transmit Registers.

IA3: Individual Accept 3. When set, received frames are accepted which the DA matches the Individual Address 3 Register.

IA2: Individual Accept 2. When set, received frames are accepted which the DA matches the Individual Address 2 Register.

IA1: Individual Accept 1. When set, received frames are accepted which the DA matches the Individual Address 1 Register.

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IA0: Individual Accept 0. When set, received frames are accepted which the DA matches the Individual Address 0 Register.

NOTE: It may become necessary for the host to change the destination address filter criteria and NOT go through a controller reset. This can be done. The host should:

1. Clear SerRxON (RXCtl) to prevent an additional received frame while the filters are being changed.
2. Modify the destination filter bits in this register.
   Modify the Logical Address Filter, if necessary.
   Modify the Individual Address Filter, if necessary.
3. Set SerRxON to re-enable the receiver.

When the host changes the destination filter, it is possible that a frame will be missed while SerRxON is clear.

TXCtl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								DefDis	MBE	ICRC	TxPD	OColl	SP	PB	STxON

Address:
0x8001_0004 - Read/Write

Chip Reset:
0x0000_0000

Soft Reset:
0x0000_0000

Definition:
Transmit Control Register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

DefDis: 2-part DefDis. Before a transmission can begin, the MAC follows a deferral procedure. With the 2-part DefDis bit clear, the deferral is the standard two-part deferral as defined in ISO/IEC 8802-3 paragraph 4.2.3.2.1. With the 2-part DefDis bit set, the two-part deferral is disabled. See Transmit Back-Off paragraph.

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MBE: ModBackoff Enable. When clear, the ISO/IEC standard backoff algorithm is used. When set, the Modified Backoff algorithm is used, which delays longer after each of the first three Tx collisions.

ICRC: Inhibit CRC. When this bit is set, there will be no CRC appended to transmit frames. If the Abort Frame bit is set in the transmit descriptor for a frame, the frame will be terminated with a bad CRC.

TxPD: Tx Pad Disable. When this bit is set, the MAC will not pad the frame to the legal minimum size (64 bytes). If clear, the MAC will pad the frame to the minimum legal frame size if the supplied length is less than 64 bytes. The padded characters will be the last supplied character in the frame, repeated.

OColl: One Collision. When this bit is set, no attempt is made to resend frames in the event of a collision.

SP: Send Pause. When set by the host, this bit causes a pause frame to be transmitted at the earliest opportunity. This is at the end of the current frame, if one is already in progress. This bit will remain set until the transmission of the frame has started. The pause frame is comprised of the following elements:

Destination Address	Individual Address number 6
Source Address	Individual Address number 1
Type Field	Type Field defined in the Flow Control Format register0
Opcode	0x0001
Pause Time	Pause Field defined in the Flow Control Format register
Pad fill	

PB: Pause Busy: This bit remains set as long as a pause frame is being transmitted. Only one pause frame may be sent at any time, therefore the Send Pause and Pause Busy bits should be zero before a new pause frame is defined.

STxON: Serial TC On. Serial Transmit ON. The transmitter is enabled when set. When clear, no transmissions are allowed. When a frame is being transmitted, and STxON is cleared, then that transmit frame is completed. No subsequent frames are transmitted until STxON is set again.

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SelfCtl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	MDCDIV						PSPRS	RWP	RSVD	GPO0	PUWE	PDWE	MIIL	RSVD	RESET

Address:

0x8001_0020 - Read/Write

Chip Reset:

0x0000_0F10

Soft Reset:

0x0000_0000

Definition:

Self Control Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

MDCDIV: MDC clock divisor. HCLK is divided by MDCDIV + 1 to create the MDC clock frequency. Default value is 0x07, which is divide by 8.

PSPRS: Preamble Suppress. Default is 1.
1 = The first MDC qualifies an SFD on MDIO.
0 = Get 32 ones before SFD.

Note: The user must check the datasheet of the PHY being used in the design. If the PHY needs a preamble for reading/writing to/from PHY registers, the PSPRS must be cleared (set to 0). The following procedure will correctly set the SelfCtl register value:
Read the value of SelfCtl (should be 0x0F00).
Clear PSPRS bit in SelfCtl Register.
Read/write PHY registers.
Restore the old value to SelfCtl.

RWP: Remote Wake Pin. This bit reflects the current state of the **REMWAKE** pin. Following a system power up, caused by a Remote Wakeup frame being detected by the MAC, this bit is set.

GPO0: General Purpose Output 0. This bit directly controls the GPO[0] pin. A “1” corresponds to a logic high on the pin.

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PUWE: Power Up Wakeup Enable. Setting the Power Up Wakeup enable bit causes the MAC to enter the remote wakeup mode, during normal operation (AHB bus powered up). In this mode all receive frames that pass the destination address filter are scanned for the remote wakeup pattern (six bytes of 0xFF followed directly by sixteen consecutive copies of the Individual address). When this pattern is detected, the **REMWAKE** pin is driven high and Remote Wakeup (Interrupt Status is set).

PDWE: Power Down Wakeup Enable. Setting the Power Down Wakeup Enable bit causes the MAC to enter the remote wakeup mode when the AHB bus is powered down. In this mode all receive frames that pass the destination address filter are scanned for the remote wakeup pattern (six bytes of FFh followed directly by sixteen consecutive copies of the Individual address). When this pattern is detected, the **REMWAKE** pin is driven high, and can be used to initiate a system power up, the state of the **REMWAKE** pin is visible via the Remote Wake Pin bit of this register.

MIIL: MII Loopback. Setting the MII Loopback bit causes transmit data to be diverted back into the receive data path prior to the MII interface pins, the transmit data does not appear on the MII bus and the receive data on the MII bus is ignored. The clock for the transmit and receive data is derived from the AHB CLK in the loopback mode. It is strongly recommended that TXCLK and RXCLK come from a single clock source with minimum skew in order to ensure the proper operation of the loopback test. For reliable operation a software reset should be issued when the MII loopback bit is changed.

RESET: Soft Reset. This is an act-once bit. When set, a Soft Reset is initiated immediately, this will reset the FIFO, mac and descriptor processor. This bit is cleared as a result of the reset. Driver software should wait until the bit is cleared before proceeding with MAC initialization.

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DiagAd

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								ADDR							

Address:

0x8001_0038 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Diagnostic Address Register. The Diagnostic Address Register provides an indirect addressing method to point to internal diagnostic locations, which provide access to features not required for normal driver operation. To access the internal registers, the address of the register is written to the Diagnostic Address register, and the Diagnostic Data register is used to access the actual data.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

ADDR: Diagnostic Address. The following table identifies the address map.

Address	Register Name
0x00	Debug Control
0x04	Debug FIFO Control
0x08	Debug FIFO Data
0x98	Receive Data FIFO Pointers
0x9C	Transmit Data FIFO Pointers
0xA0	Receive Status FIFO Pointers
0xA4	Transmit Status FIFO Pointers
0xA8	Receive Descriptor FIFO Pointers
0xAC	Transmit Descriptor FIFO Pointers

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DiagDa

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															

Address:

0x8001_003C - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Diagnostic Data Register. The Diagnostic Data Register provides access to the internal register pointed to by the value in the Diagnostic Address register. For debug only.

Bit Descriptions:

DATA: Internal register data value.

GT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
GTC															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
GTP															

Address:

0x8001_0040 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

General Timer Register

Bit Descriptions:

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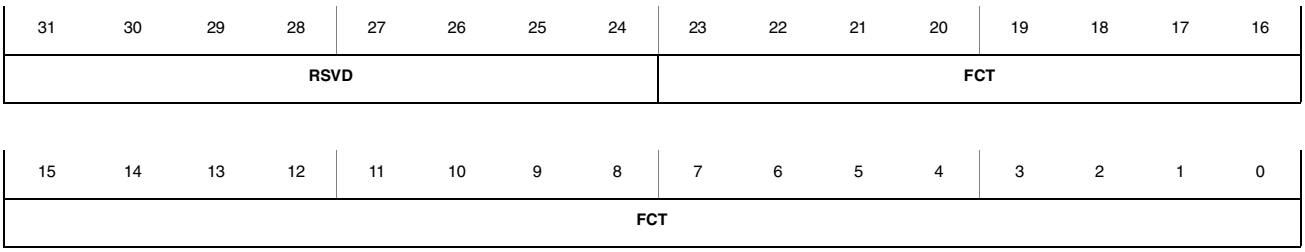
GTC: General Timer Count, read only. The timer count contains the running value of the timer function, it cannot be written to directly. When the General Timer Period is written and the same value is loaded into the General Timer Count, or when the count value reaches 0, it is reloaded from the General Timer Period. Additionally when the count reaches zero, the Timeout Status (Interrupt Status register) is set. The timer value is decremented at 1/8th of the transmit bit rate.

GTP: General Timer Period, read write. The Timer Period holds the periodic time for the timer. When the period is written, the count is preloaded with the same value. Setting a value of zero in the Period disables the generation of Timeout Status.

FCT



Address:

0x8001_0044 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Flow Control Timer

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

FCT: Flow Control Timer value. The Flow Control Timer is loaded as a result of receiving a flow control frame, with the pause value from the received frame. The value in the timer is then decremented every 512 bit times, as soon as the transmit line is idle. While the timer is non zero, no new transmit frames are started. The decrement time depends on the speed, but always corresponds to the duration of a 64 byte minimum packet.

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FCF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MACCT															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TPT															

Address:

0x8001_0048 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Flow Control Format Register

Bit Descriptions:

MACCT: MAC Control Type. The MAC Control Type field defines the Ethernet type field for receive and transmit MAC control frames. This is used in the processing of transmit and receive pause frames, which are a special form of MAC control frames. For a receive frame to be identified as a pause frame, the following conditions must be met:

1. The destination address must match one of first two individual addresses, with the appropriate RxFlowControlEn bit set.
2. The Ethernet type field must match MAC Control Type.
3. The first two data bytes of the frame must equal 0x0001.

When a transmit pause command is processed, the MAC Control Type is inserted in the transmit frame as the ethernet type field.

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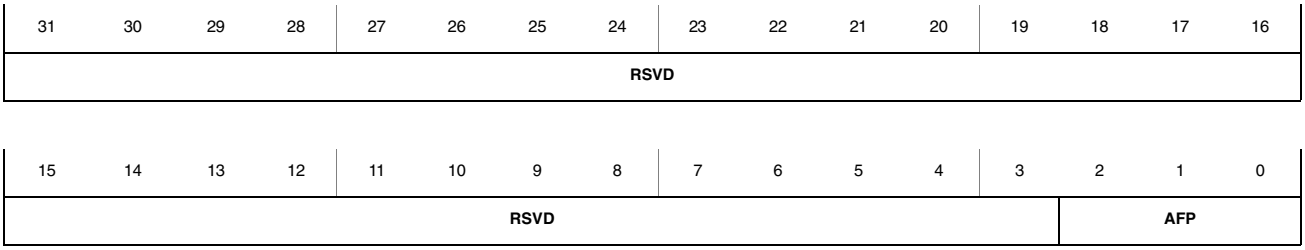
TPT: Transmit Pause Time. When a transmit pause command is processed, the Transmit Pause Time is inserted as the actual time to pause. The format of a transmit pause frame is:

1. Destination address = Individual address[6] (6 bytes)
2. Source address = Individual address[0] (6 bytes)
3. Type field = MAC Control Type (2bytes)
4. Opcode = 0x0001 (2bytes)
5. Pause time = Transmit Pause Time (FCF) (2bytes)
6. Padding to complete minimum size packet.
7. CRC

AFP



Address:
0x8001_004C - Read/Write

Chip Reset:
0x0000_0000

Soft Reset:
0x0000_0000

Definition:
Address Filter Pointer Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

AFP: Address Filter Pointer. The Address Filter Pointer controls access to a block of storage which is used to hold MAC addresses, and the destination address hash table. The pointer defines which set of address match functions are visible to the Host at offset 0x0050 through 0x005F.

Table 6-5: Address Filter Pointer

AFP	Data Accessed at Offset 0050 through 005F
000	This is the primary Individual Address, used in the recognition of Wakeup frames, as the source address for transmit pause frames, and may be optionally used to qualify receive pause frames.
001	This is a secondary MAC address that may be optionally used to qualify receive pause frames

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010 011	These secondary addresses are only used for qualifying the destination addresses of receive frames.
100 101	These locations are not implemented
110	This address is used as the destination address of transmit pause frames
111	This block comprises the hash table used for qualifying the destination of receive frames.

IndAd

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
IAD															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
IAD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IAD															

Address:

0x8001_0050 through 0x8001_0055 - 6 Bytes - Read/Write,
when AFP = 000b, 010b or 001b

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Individual Address Register. There are five different Individual Addresses accessible at offset 0x050, the Address Filter Pointer determines which one is accessed at any one time. The first four addresses (pointer offset 0x000 through 0x011), may be used to implement destination address filters for receive frames. The first two may also be used to qualify receive frames for flow control processing, and the first address is used for wakeup frame processing. The fifth address (pointer offset 0x110), is only used as the destination address for transmit pause frames.

The least significant byte of the Individual Address corresponds to the first byte of the address on the serial interface, with the least significant bit of the byte corresponding to the first bit on the serial interface.

Bit Descriptions:

IAD: Individual Address.

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HashTbl

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
HTb															

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
HTb															

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
HTb															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HTb															

Address:

0x8001_0050 through 0x8001_0057 - 8 Bytes - Read/Write, when AFP = 111b

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Hash Table Register. The hash table is used as a way of filtering groups of addresses in the receiver. Following the reception of the destination address (first 6 bytes of a receive frame), the upper 6 bits of the computed CRC are used as an address into the hash table. If the bit accessed by this address is a “1”, the frame passes the hash table test, if the bit is a “0”, the frame fails the hash table test.

The hash table may be used for either or both of individual addressed frames and group address frames, depending on the IAHA and MA bits in RXCtl. A frame has a group address if the first bit of the frame is a one.

If an individual address frame passes the hash test and the IAHA bit is set, the frame passes the destination filter.

If a group address frame passes the hash test and the MA bit set, the frame passes the destination filter.

Bit Descriptions:

HTb: Hash Table entries.

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TXCollCnt

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TXC															

Address:

0x8001_0070 - Read Only

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Transmit Collision Count Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TXC: Transmit Collision Count. The transmit collision count records the total number of collisions experienced on the transmit interface, including late collisions. When the most significant bit of the count is set, an optional interrupt may be generated. The register is cleared automatically following a read and writing to the register will have no effect.

RXMissCnt

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RMC															

Address:

0x8001_0074 - Read Only

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

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Definition:

Receive Miss Count Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RMC: The receive miss count records the number of frames that pass the destination address filter, but fail to be received due to lack of bus availability or lack of receive storage. Frames that are partially stored and marked as overruns are included in the count. When the most significant bit of the count is set, an optional interrupt may be generated. The register is cleared automatically following a read, writing to the register will have no effect.

RXRuntCnt

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RRC															

Address:

0x8001_0078 - Read Only

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Receive Runt Count Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RRC: Receive Runt Count. The receive runt count records the total number of runt frames received, including those with bad CRC. When the most significant bit of the count is set, an optional interrupt may be generated. The register is cleared automatically following a read, writing to the register will have no effect.

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TestCtl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								MACF	MFDX	DB	RSVD				

Address:

0x8001_0008 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Test Control Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

MACF: MAC Fast. When set, internal MAC timers for link pulses and collision backoff are scaled in order to speed-up controller testing. When clear, normal timing is used.

MFDX: MAC Full Duplex. This bit is used to enable full duplex operation, when set, the transmitter ignores carrier sense for transmit deferral. For normal loopback testing this bit should be set. This bit is valid for 10-BaseT operation only.

DB: Disable Backoff. When set, the backoff algorithm is disabled. The MAC transmitter looks only for completion of the Inter Frame Gap before starting transmission. When clear, the backoff algorithm is used as described in “Transmit Back-Off” on page 125.

IntEn

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD		RxMIE	RxBIE	RxSQIE	TxLEIE	ECIE	TxUHIE	RSVD					MOIE	TxCOIE	RxROIE

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		RSVD	MIIIE	PHYSIE	TIE	RSVD	SWIE	RSVD				TSQIE	REOFIE	REOBIE	RHDRIE

Address:

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0x8001_0024 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Interrupt Enable Register

Bit Descriptions:

RSVD:	Reserved. Unknown During Read.
RWIE:	Remote Wakeup Interrupt Enable. Setting this bit causes an interrupt to be generated when a remote wakeup frame is detected and the MAC is in the Remote Wakeup mode (RXCtl).
RxMIE:	Receiver Miss Interrupt Enable. When set, this bit will cause an interrupt whenever a complete receive frame is discarded due to lack of storage. This may be as a result of long bus latency or insufficient receive descriptors. The total number of missed frames is also counted in the RxMiss Counter.
RxBIE:	Receive Buffer Interrupt Enable. When set, this bit will cause an interrupt to be generated when the last available receive descriptor has been read into the MAC.
RxSQIE:	Receive Status Queue Interrupt Enable. When this bit is set, an interrupt will be generated when the last available status queue entry has been written (RXStsEnq = 0).
TxLEIE:	Transmit Length Error Interrupt Enable. Setting this bit causes an interrupt to be generated when a transmit frame equals or exceeds the length specified in the Max Frame Length register.
ECIE:	End of Chain Interrupt Enable. The end of chain interrupt is generated when the last transmit descriptor has been loaded into the MAC. There may still be transmit descriptors and or transmit data remaining in the MAC at this time.
TxUHIE:	Transmit Underrun Halt Interrupt Enable. If there is a transmission, and the MAC runs out of data before the full transmitted length, then there is a transmit underrun. If the MAC is programmed to halt in this condition (Bus Master Control), setting TxUnderrunHaltiE will cause an interrupt to be generated.

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MOIE: Receive Miss Overflow Interrupt Enable. If received frames are lost due to slow movement of receive data out of the receive buffers, then a receive miss is said to have occurred. When this happens, the RxMISS counter is incremented. When the MSB of the count is set, the MissCnt bit in the Interrupt Status Register is set. If the MissCntiE bit is set at this time, an interrupt is generated.

TxCOIE: Transmit Collision Overflow Interrupt Enable. When a transmit collision occurs, the transmit collision count is incremented. When the MSB of the count is set, the TXCollCnt bit in the Interrupt Status Register is set. If the TxCollCntiE is set at this time, an interrupt is generated.

RxROIE: Receive Runt Overflow Interrupt Enable. When a runt frame is received with a CRC error, the RxRuntCnt register is incremented. When the MSB of the count is set the RuntOv bit is set in the Interrupt Status Register. If the RuntOviE bit is set at this time, an interrupt is generated.

MIIIE: MII Management Interrupt Enable. When set, the MII Interrupt enable causes an interrupt to be generated whenever a management read or write cycle is completed on the MII bus.

PHYSIE: The PHY Status Interrupt Enable bit provides a mechanism to generate an interrupt whenever a change of status is detected in the PHY.

TIE: Setting the Timer Interrupt Enable bit will cause an interrupt to be generated whenever the general timer (GT) counter reaches zero.

SWIE: Writing a “1” to this bit causes a software generated interrupt to be generated. The SWint bit in the Interrupt Status register is set to indicate the cause of the interrupt. This bit will always read zero.

TSQIE: Transmit Status Queue Interrupt Enable. Setting this bit causes an interrupt to be generated whenever a transmit status is posted to the transmit status queue.

REOFIE, REOBIE, RHDRIE: Setting all three bits causes interrupts to be generated whenever a receive-end-of-frame status, or a receive-end-of-buffer status, or a receive-header status is written to the receive status queue.

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IntStsP/IntStsC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	RWI	RxMI	RxBI	RxSQI	TxLEI	ECI	TxUHI	RSVD					MOI	TxCOI	RxROI

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			MIII	PHYSI	TI	AHBE	SWI	RSVD			OTHER	TxSQ	RxSQ	RSVD	

Address:

0x8001_0028, for IntStsP - Read/Write
0x8001_002C, for IntStsC - Read Only

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Interrupt Status Preserve and Clear Registers. The interrupt status bits are set when the corresponding events occur in the MAC. If the corresponding interrupt enable bit is set in the interrupt enable register, an interrupt signal will be generated.

Interrupt status is available at two different offsets: Interrupt Status Preserve and Interrupt Status Clear. Both offsets are a read of the same storage. Reading the Interrupt Status register Preserve has no effect on the status in the register, but writing a 1 to a location in this register clears the status bit, writing a zero has no effect. Reading the Interrupt Status Clear register clears all the bits in the register that are accessed as defined by the AHB **HSIZE** signal. Therefore a routine which will handle all reported status may read via the Interrupt Status Clear thereby saving a write operation.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RWI: Remote Wakeup Interrupt. The remote wake status is set when a remote wakeup frame is received, and the RemoteWakeEn (RXCtl) is set. A remote wakeup frame must pass the receive destination address filter and have a contiguous sequence of 6 bytes of FFh followed by 8 repetitions of the Individual Address and be a legal frame (legal length and good CRC).

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RxMI: RxMI is set when a receive frame was discarded due to the internal FIFO being full. This may be as a result of a long latency in acquiring the bus or a lack of receive descriptors. RxMiss is not set in response to a frame that was partially stored in the FIFO and then discarded due to lack of FIFO space. This is marked as an Overrun Error in the Status Queue.

RxBI: RxBuffers is set when the last available receive descriptor has been read into the MAC (RxDesEnq = 0). Free descriptors may still be available in the MAC to accommodate receive frames.

RxSQI: The Receive Status Queue bit is set when the last free status queue location has been written (RXStsEnq = 0).

TxLEI: The Transmit Length Error status is set when any excessively long frame is transferred into the transmit data FIFO. When this occurs, the MAC assumes an error has occurred in the transmit descriptor queue, and therefore stops further transmit DMA transfers. An excessively long frame is defined as one equal or longer than the value programmed in the Max Frame Length register. The frame itself will be terminated with a bad CRC.

ECIE: When set to 1, this bit indicates that the MAC has exhausted the transmit descriptor chain.

TxUHI: This bit is set if the MAC runs out of data during a frame transmission, and the Underrun Halt bit (BMCtl) is set, at this time the transmit descriptor processor will have been halted. If the Underrun Halt bit is clear, the MAC will write an Underrun Status for the frame and continue to the next transmit frame.

MOI: If received frames are lost due to slow movement of receive data out of the receive buffers, then a receive miss is said to have occurred. When this happens, the RxMISS counter is incremented. When the MSB of the count is set, the MissCnt bit in the Interrupt Status Register is set. If the MissCntiE bit is set, an interrupt will be generated.

TxCOI: When a transmit collision occurs, the transmit collision count is incremented. When the MSB of the count is set the TxCOI bit in the Interrupt Status Register is set. If the TxCOIE bit is set, an interrupt will be generated.

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RxROI: When a runt frame is received with a CRC error, the RxRuntCnt register is incremented, when the MSB of the count is set, the RuntOv bit is set in the Interrupt Status Register. If the RxROIE bit is set, an interrupt will be generated.

MIIII: The MII Status bit is set whenever a management operation on the MII bus is completed.

PHYI: The PHY Status bit is set when the MAC detects a change of status event in the PHY.

TI: The Timeout bit is set when the general timer (GT) count register reaches zero.

AHBE: This bit is set if a MAC generated AHB cycle terminated abnormally. The Queue ID bits (Bus Master Status) will indicate the DMA Queue which was active when the abort occurred. DMA operation is halted on all queues until this bit is cleared, and the queues are restarted via the Bus Master Control register.

OTHER: This bit is set when a status other than that covered by bits 10, 3 and 2 is present.

TxSQ: This bit is set when a status affecting the transmit status queue has been posted.

RxSQ: This bit is set when a status affecting the receive status queue has been posted. This bit can only be set if bit 2 (REOFIE), bit 1 (REOBIE) and bit 0 (RHDRIE) of the Interrupt Enable (IntEn) register are set (enabled).

GIIntSts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT	RSVD														

Address:

0x8001_0060 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

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Definition:

Global Interrupt Status Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

INT: Global interrupt bit. This bit is set whenever the MACint signal to the interrupt controller is active. Writing a one to this bit location will clear this bit until a new interrupt condition occurs.

GlIntMsk

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT	RSVD														

Address:

0x8001_0064 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Global Interrupt Mask Register. This register is used to mask the GlIntSts bit, to allow of block interrupts to the processor.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

INT: Global interrupt mask bit. When set, any interrupt enabled by the Interrupt Enable Register will set the Global Interrupt Status interrupt bit. When clear, no interrupts will reach the processor.

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GlIntROSts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT	RSVD														

Address:

0x8001_0068 - Read Only

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

General Interrupt Read-Only Status register. This is a read-only version of the Global Interrupt Status Register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

INT: Global interrupt read-only status bit. This bit is set whenever the MACint signal to the interrupt controller is active.

GlIntFrc

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT	RSVD														

Address:

0x8001_006C - Write Only

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Global Interrupt Force Register. This register allows software to generate an interrupt.

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Bit Descriptions:

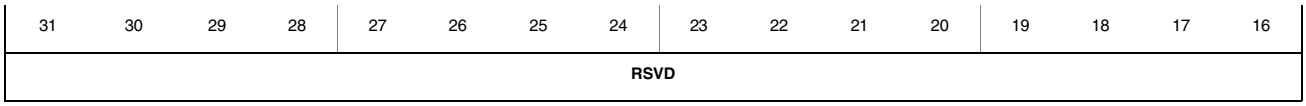
RSVD: Reserved. Unknown During Read.

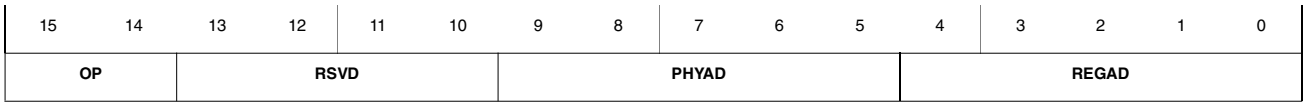
INT: Global interrupt force bit, write only, always reads zero. Writing a one to this bit will set the Global Interrupt Status bit, if it is enabled. Writing a zero has no effect.

MII/PHY Access Register Descriptions

All PHY registers are accessed through the MII Command, Data and Status Registers. Write operations are accomplished by writing the required data to the MII Data Register and then writing the required Command to the MII Command Register (Opcode = 01, PhyAd = target phy, RegAd = target register), which causes the Busy bit (MII Status) to be set. When the Busy bit is clear, the write operation has been performed. Read operations are performed by writing a read command to the MII Command register (Opcode = 10b, PhyAd = target phy, RegAd = source register), which will also cause the Busy bit (MII Status) to be set. When the read operation has been completed, the Busy bit is cleared and the read data is available in the MII Data register.

MIICmd





Address:

0x8001_0010 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

MII Command Register. Provides read-write access to the external PHY registers using the MII command data port.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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OP:	OPcode. This Opcode field defines the type of operation to be performed to the appropriate PHY register. 10 - Read register 01 - Write register
PHYAD:	PHY Address. This field defines which external PHY is to be accessed.
REGAD:	Register Address. This field defines the particular register in the PHY to be accessed.

MIIData

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MIIData															

Address:

0x8001_0014 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

MII Data Transfer Register

Bit Descriptions:

RSVD:	Reserved. Unknown During Read.
MIIData:	MII Data Register. This register contains the 16 bit data word that is either written to or read from the appropriate PHY register.

MIISts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															BUSY

Address:

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0x8001_0018 - Read Only

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

MII Status Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

Busy: MII Busy. The Busy bit is set whenever a command is written to the MII Command Register. It is cleared when the operation has been completed.

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Descriptor Processor Registers

The Descriptor Processor Registers are in three parts: the bus master control, receive registers, and transmit registers.

BMCtl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		MT	TT	UnH	TxChR	TxDis	TxEn	RSVD	EH2	EH1	EEOB	RSVD	RxChR	RxDis	RxEn

Address:

0x8001_0080 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

0x0000_0000

Definition:

Bus Master Control Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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MT: Manual Transfer. Writing a one to this bit causes all internal FIFOs to be marked pending for transfer, as if they had crossed their threshold. This provides a mechanism for flushing stale status from the internal FIFOs, when the Timed Transfer is not used and non zero thresholds have been set. When the Manual Transfer is set, the Transfer Pending (BMCtl), is set until all FIFOs have been either active for a DMA transfer, or have been determined inactive (that is, an empty receive data FIFO). When reading the BMCtl register, the Manual Transfer bit will always return a zero.

TT: Timed Transfer. Setting the Timed Transfer bit causes the internal FIFOs to be marked as pending for transfer whenever the timer reaches zero. This provides a mechanism for flushing stale status from the internal FIFOs when a non zero threshold has been set.

UnH: Underrun Halt. When set, this bit causes the transmit descriptor to perform the following operations when a transmit underrun is encountered:

1. Halt all transmit DMA operations.
2. Flush the transmit descriptor queue.
3. Set transmit enqueue to zero.

This allows the host to reinitialize the transmit descriptor processor, to start at the desired point. When clear, the MAC will proceed to the next transmit frame in the queue.

TxChR: Transmit Channel Reset. Writing a “1” to Transmit Channel Reset causes the Transmit Descriptor Processor and the transmit FIFO to be reset. This bit is an act-once-bit and will clear automatically when the reset is complete.

TxDis: Transmit Disable. Writing a “1” to Transmit Disable causes the transmit DMA transfers to be halted. If a transmit frame is currently in progress, transfers are halted when the transmit status is written to the status buffer. When transfers have been halted, the TxAct bit (Bus Master Status) is clear. TxDis is an act-once-bit and will clear immediately.

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TxEn: Transmit Enable. Writing a one to Transmit Enable causes transmit DMA transfers to be enabled. This is reflected in TxAct (Bus Master Status) being set. TxEn is an act-once-bit and will clear automatically when the enable is complete. The first time the TxEn bit is set following an AHB reset, or a TxChRes, the MAC performs a transmit channel initialization. During this initialization the TXDEnq is cleared, and the Transmit Descriptor and Status Queues are calculated. When the initialization is complete, the TxAct (BMSts) is set.

EH2: Enable Header 2. When Enable Header2 is set, a status is written to the receive status queue when the number of bytes specified in Receive Header Length2 have been transferred to the receive data buffer. If the transfer either fills a receive buffer or ends a receive frame, only an end of buffer or end of frame status is generated. The value in Receive Header Length 2 should be greater than the value in Receive Header Length 1 in order to generate a status event.

EH1: Enable Header 1. When Enable Header1 is set, a status is written to the receive status queue when the number of bytes specified in Receive Header Length1 have been transferred to the receive data buffer. If the transfer either fills a receive buffer or ends a receive frame, only an end of buffer or end of frame status is generated.

EEOB: Enable EOB. When Enable End Of Buffer bit is set, a status is written to the receive status queue whenever an end of receive buffer is reached. If reaching the end of the receive buffer coincides with the end of frame, only one status is written to the queue.

RxChR: Receive Channel Reset. Writing a “1” to Receive Channel Reset causes the Receive Descriptor Processor and the receive FIFO to be reset. This bit is an act-once-bit and will clear automatically when the reset is complete.

RxDis: Receive Disable. Writing a “1” to Receive Disable causes receive DMA transfers to be halted. If a receive frame is currently in progress, transfers will be halted when the receive frame status has been transferred to the status buffer. When the transfers are halted, the RxAct bit (Bus Master Status) is cleared. This bit is an act-once-bit and will clear immediately.

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RxEn: Receive Enable. Writing a one to Receive Enable causes receive DMA transfers to be enabled. This is reflected in RxAct (Bus Master Status) being set. This bit is an act-once-bit and will clear automatically when the enable is complete. The first time the RxEn bit is set following a AHB reset, or a RxChRes, the MAC performs a receive channel initialization. During this initialization the RXDEnq, and RXStsEnq registers are cleared and the endpoints of the Receive Descriptor and Status Queues are calculated. When the initialization is complete, the RxAct (BMSts) is set.

BMSts

Address:
0x8001_0084 - Read Only

Chip Reset:
0x0000_0000

Soft Reset:
0x0000_0000

Definition:
Bus Master Status Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TxAct: Transmit Active. When this bit is set, the channel is active and may be in the process of transferring transmit data. Following a TxDisable Command (Bus Master Control), when transfers have been halted, this bit is cleared.

TP: Transfer Pending. When the Manual Transfer bit (BMCtl) is set, the Transfer Pending bit is set, until all internal FIFOs have either been active for a DMA transfer, or have been determined to be inactive (that is, empty transmit status FIFO).

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RxAct: Receive Active. When this bit is set, the channel is active and may be in the process of transferring receive data. Following a RxDisable Command (Bus Master Control), when transfers have been halted, this bit is cleared.

QID: Queue ID. The queue ID reflects the current or last DMA queue active on the AHB bus. When an AHB error halts DMA operation, this field may be used to determine the queue that caused the error.

ID Type of transfer
000 - Receive data
001 - Transmit data
010 - Receive status
011 - Transmit status
100 - Receive descriptor
101 - Transmit descriptor

Descriptor Processor Receive Registers

RXDQBAdd

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDBA															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDBA															

Address:

0x8001_0090 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Descriptor Queue Base Address register. The Receive Descriptor Queue Base Address defines the system memory address of the receive descriptor queue, this address is used by the MAC to reload the Receive Current Descriptor Address whenever the end of the descriptor queue is reached. The base address should be set at initialization time and must be set to a word aligned memory address.

Bit Descriptions:

RDBA: Receive Descriptor Base Address.

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RXDQBLen

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDBL															

Address:

0x8001_0094 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Descriptor Queue Base Length register. The Receive Descriptor Queue Base Length defines the actual number of bytes in the receive descriptor queue, which thereby sets the number of receive descriptors that can be supplied to the MAC. The length should be set at initialization time and must define an integral number of receive descriptors.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RDBL: Receive Descriptor Base Length.

RXDQCurLen

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RDCL															

Address:

0x8001_0096 - Read/Write. Note half word alignment.

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

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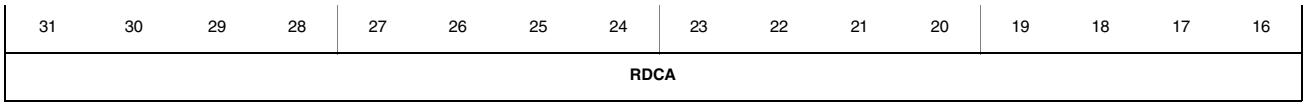
Receive Descriptor Queue Current Length register. The Receive Descriptor Queue Current Length defines the number of bytes between the Receive Descriptor Current Address and the end of the receive descriptor queue. This value is used internally to wrap the pointer back to the start of the queue. The register should not normally be written.

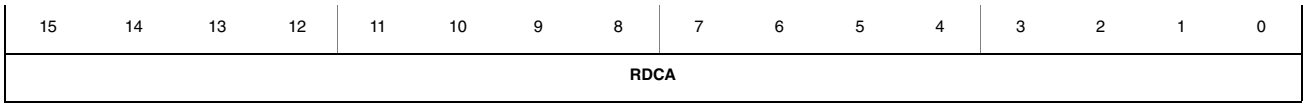
Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RDCL: Receive Descriptor Base Length.

RXDCurAdd





Address:

0x8001_0098 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Descriptor Current Address register. The Receive Current Descriptor Address contains the pointer to the next entry to be read from the receive descriptor queue. This should be set at initialization time to the required starting point in the descriptor queue. During operation the MAC will update this address following successful descriptor reads. Intermediate values in this register will not necessarily align to descriptor boundaries, nor directly effect the current descriptor in use because several descriptors may be buffered inside the MAC.

Bit Descriptions:

RDCA: Receive Descriptor Current Address.

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RXDEnq

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RDV															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								RDI							

Address:

0x8001_009C - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Descriptor Enqueue register. The Receive Descriptor Enqueue register is used to define the number of valid entries in the descriptor queue. The register operates as follows: only the Receive descriptor Increment field is writable and any value written to this field is added to the existing Receive Descriptor Value. Whenever complete descriptors are read by the MAC, the Receive Descriptor Value is decremented by the number read. For example, if the Receive Descriptor Value is 0x07 and the Host writes 03 to the Receive Descriptor Increment, the new Value will be 0x0A. If the controller then reads two descriptors, the Value will be 0x08.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RDV: Receive Descriptor Value.

RDI: Receive Descriptor Increment.

RXBCA

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RBCA															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RBCA															

Address:

0x8001_0088 - Read/Write

Chip Reset:

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0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Buffer Current Address register. The Receive buffer current address contains the current address being used to transfer receive data. This value may be useful in debugging.

Bit Descriptions:

RBCA: Receive Buffer Current Address.

RXStsQBAdd

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSQBA															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSQBA															

Address:

0x8001_00A0 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Status Queue Base Address. The Receive Status Queue Base Address defines the system memory address of the receive status queue. This address is used by the MAC to reload the Receive Current Status Address whenever the end of the status queue is reached. The base address should be set at initialization time and must be set to a word aligned memory address.

Bit Descriptions:

RSQBA: Receive Status Queue Base Address.

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RXStsQBLen

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSQBL															

Address:

0x8001_00A4 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Status Queue Base Length. The Receive Status Queue Base Length defines the actual number of bytes in the receive status queue. The length should be set at initialization time and must define an integral number of receive statuses.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RSQBL: Receive Status Queue Base Length.

RXStsQCurLen

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSQCL															

Address:

0x8001_00A6 - Read/Write. Note half word alignment.

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Status Queue Current Length. The Receive Status Queue Current Length defines the number of bytes between the Receive Status Current

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Address and the end of the receive status queue. This value is used internally to wrap the pointer back to the start of the queue. The register should not normally be written to.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RSQCL: Receive Status Queue Current Length.

RXStsQCurAdd

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSQCA															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSQCA															

Address:

0x8001_00A8 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Status Queue Current Address. The Receive Status Queue Base Address defines the system memory address of the receive status queue. This address is used by the MAC to reload the Receive Status Queue Current Status Address whenever the end of the status queue is reached. The base address should be set at initialization time and must be set to a word aligned memory address.

Bit Descriptions:

RSQCA: Receive Status Queue Current Address.

RXStsEnq

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSV															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								RSI							

Address:

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0x8001_00AC - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Status Enqueue register. The Receive Status Enqueue register is used to define the number of free entries available in the status queue. Only the Receive Status Increment field is writable and any value written to this field will be added to the existing Receive Status Value. Whenever complete statuses are written by the MAC, the Receive Status Value is decremented by the number read. For example, if the Receive Status Value is 0x07, and the Host writes 0x03 to the Receive Status Increment, the new Receive Status Value will be 0x0A. If the controller then reads two descriptors, the Value will be 0x08.

Bit Descriptions:

RSVD:	Reserved. Unknown During Read.
RSV:	Receive Status Value.
RSI:	Receive Status Increment.

RXHdrLen

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD								RHL2							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								RHL1							

Address:

0x8001_00EC - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Header Length register. The Receive Header Length registers are used to generate status after receiving a specific portion of a receive frame. When the number of bytes specified in either register has been transferred to the external data buffer, an appropriate status is generated. The status for a receive header will reflect the number of bytes transferred for the current frame, the address match field will be valid, and the other status bits will be set

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to zero. A status will only be generated for header length 2 if the length is greater than that specified for header length 1.

Bit Descriptions:

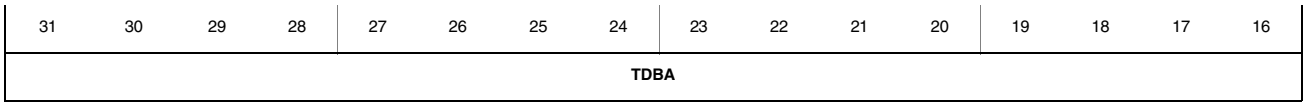
RSVD: Reserved. Unknown During Read.

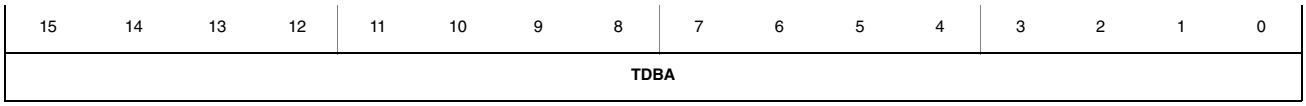
RHL2: Receive Header Length 2.

RHL1: Receive Header Length 1.

Descriptor Processor Transmit Registers

TXDQBAdd





Address:

0x8001_00B0 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Transmit Descriptor Base Address register. The Transmit Descriptor Queue Base Address defines the system memory address of the transmit descriptor queue. This address is used by the MAC to reload the Transmit Current Descriptor Address whenever the end of the descriptor queue is reached. The base address should be set at initialization time and must be set to a word aligned memory address.

Bit Descriptions:

TDBA: Transmit Descriptor Base Address.

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TXDQBLen

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDBL															

Address:

0x8001_00B4 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Transmit Descriptor Queue Base Length register. The Transmit Descriptor Queue Base Length defines the actual number of bytes in the transmit descriptor queue, which thereby sets the maximum number of transmit descriptors that can be supplied to the MAC at any one time. The length should be set at initialization time and must define an integral number of transmit descriptors.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TDBL: Transmit Descriptor Base Length.

TXDQCurLen

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TDCL															

Address:

0x8001_00B6 - Read/Write. Note half word alignment.

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

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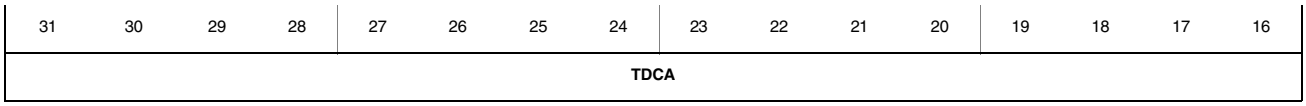
Transmit Descriptor Queue Current Length register. The Transmit Descriptor Queue Current Length defines the number of bytes between the Transmit Descriptor Current Address and the end of the transmit descriptor queue. This value is used internally to wrap the pointer back to the start of the queue. The register should not normally be written.

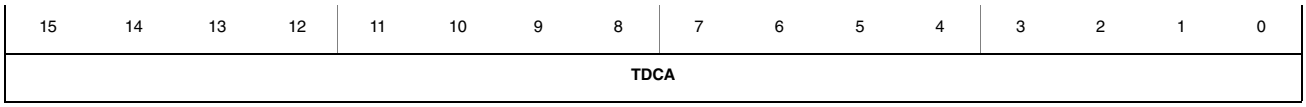
Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TDCL: Transmit Descriptor Base Length.

TXDQCurAdd





Address:

0x8001_00B8 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Transmit Descriptor Queue Current Address register. The Transmit Descriptor Queue Current Address contains the pointer to the next memory location to be read from the transmit descriptor queue. This should be set at initialization time to the required starting point in the descriptor queue. During operation, the MAC will update this address following successful descriptor reads. Intermediate values in this register will not necessarily align to descriptor boundaries, nor directly effect the current descriptor in use because several descriptors may be buffered inside the MAC.

Bit Descriptions:

TDCA: Transmit Descriptor Current Address.

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TXDEnq

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TDV															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								TDI							

Address:

0x8001_00BC - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Transmit Descriptor Enqueue register. The Transmit Descriptor Enqueue register is used to define the number of valid descriptors available in the transmit descriptor queue. Only the Transmit descriptor Increment field is writable and any value written to this field will be added to the existing Transmit Descriptor Value. When complete descriptors are read by the MAC, the Transmit Descriptor Value is decremented by the number read. For example if the Transmit Descriptor Value is 0x07, and the Host writes 0x03 to the Transmit Descriptor Increment, the new Value will be 0x0A. If the controller then reads two descriptors, the Value will be 0x08.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TDV: Transmit Descriptor Value.

TDI: Transmit Descriptor Increment.

TXStsQBAdd

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
TSQBA															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSQBA															

Address:

0x8001_00C0 - Read/Write

Chip Reset:

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0x0000_0000

Soft Reset:

Unchanged

Definition:

Transmit Status Queue Base Address. The Transmit Status Queue Base Address defines the system memory address of the transmit status queue. This address is used by the MAC to reload the Transmit Current Status Address whenever the end of the status queue is reached. The base address should be set at initialization time and must be set to a word aligned memory address.

Bit Descriptions:

TSQBA: Transmit Status Queue Base Address.

6

TXStsQBLen

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSQBL															

Address:

0x8001_00C4 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Transmit Status Queue Base Length. The Transmit Status Queue Base Length defines the actual number of bytes in the transmit status queue. The length should be set at initialization time and must define an integral number of transmit statuses.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TSQBL: Transmit Status Queue Base Length.

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TXStsQCurLen

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TSQCL															

Address:

0x8001_00C6 - Read/Write. Note half word alignment.

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Transmit Status Queue Current Length. The Transmit Status Queue Current Length defines the number of bytes between the Transmit Status Current Address and the end of the transmit status queue. This value is used internally to wrap the pointer back to the start of the queue. The register should not normally be written.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TSQCL: Transmit Status Queue Current Length.

TXStsQCurAdd

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSQCA															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSQCA															

Address:

0x8001_00C8 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

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Transmit Status Queue Current Address. The Transmit Status Queue Current Address contains the address being used to transfer transmit status to the queue. This register is available for debugging.

Bit Descriptions:

TSQCA: Transmit Status Queue Current Address.

RXBufThrshld

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD						RDHT								0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						RDST								0	0

Address:

0x8001_00D0 - Read/Write

Suggested Value:

0x0080_0040

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Buffer Threshold register. The receive buffer thresholds are used to set a limit on the amount of receive data which is held in the receive data FIFO before a bus request will be scheduled. When the number of words in the FIFO exceeds the threshold value, the descriptor processor will schedule a bus request to transfer data. The actual posting of the bus request may be delayed due to lack of resources in the MAC, such as no active receive descriptor.

Note: There are other reasons to schedule bus transfers other than reaching the threshold. One of these is when an end of frame is received. The lower 2 bits of each threshold are always zero.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

0: Must be written as “0”.

RDHT: Receive Data Hard Threshold.

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RDST: Receive Data Soft Threshold. The hard and soft threshold work in exactly the same manner except one. The soft threshold will not cause a bus request to be made if the bus is currently in use, but only when it is deemed to be idle (no transfers for four AHB clocks). The hard threshold takes effect immediately, regardless of the state of the bus. This operation allows for more efficient use of the AHB bus by allowing smaller transfers to take place when the bus is lightly loaded and requesting larger transfers only when the bus is more heavily loaded.

TXBufThrshld

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD								TDHT						0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								TDST						0	0

Address:

0x8001_00D4 - Read/Write

Suggested Value:

0020_0010

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Transmit Buffer Threshold register. The transmit buffer thresholds are used to set a limit on the amount of empty space allowed in the transmit FIFO before a bus request will be scheduled. When the number of empty words in the FIFO exceeds the threshold value, the descriptor processor will schedule a bus request to transfer data. The actual posting of the bus request may be delayed due to lack of resources in the MAC, such as no active transmit descriptor. The lower two bits of the thresholds are always zero.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TDHT: Transmit Data Hard Threshold.

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TDST: Transmit Data Soft Threshold. The hard and soft threshold work in exactly the same manner except one. The soft threshold will not cause a bus request to be made if the bus is currently in use, but only when it is deemed to be idle (no transfers for four AHB clocks). The hard threshold takes effect immediately regardless of the state of the bus. This operation allows for more efficient use of the AHB bus by allowing smaller transfers to take place when the bus is lightly loaded and requesting larger transfers only when the bus is more heavily loaded.

RXStsThrshld

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD										RSHT				0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										RSST				0	0

Address:

0x8001_00D8 - Read/Write

Suggested Value:

0x0004_0002

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Status Threshold register. The receive status threshold are used to set a limit on the amount of receive status which is held in the receive status FIFO before a bus request will be scheduled. When the number of words in the FIFO exceeds the threshold value, the descriptor processor will schedule a bus request to transfer status. The actual posting of the bus request may be delayed due to lack of resources in the MAC, such as the RXStsEnq register being equal to zero. The lower two bits of the thresholds are always zero.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RSHT: Receive Status Hard Threshold.

RSST: Receive Status Soft Threshold.

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The hard and soft threshold work in exactly the same manner except one. The soft threshold will not cause a bus request to be made if the bus is currently in use, but only when it is deemed to be idle (no transfers for four AHB clocks). The hard threshold takes effect immediately regardless of the state of the bus. This operation allows for more efficient use of the AHB bus by allowing smaller transfers to take place when the bus is lightly loaded and requesting larger transfers only when the bus is more heavily loaded.

TXStsThrshld

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD										TSHT				0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										TSST				0	0

Address:

0x8001_00DC - Read/Write

Suggested Value:

0x0004_0002

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Transmit Status Threshold register. The transmit status thresholds are used to set a limit on the amount of transmit status which is held in the transmit status FIFO before a bus request will be scheduled. When the number of words in the FIFO exceeds the threshold value, the descriptor processor will schedule a bus request to transfer status. The lower two bits of the thresholds are always zero.

Bit Descriptions:

RSVD:	Reserved. Unknown During Read.
0:	Must be written as “0”.
TSHT:	Transmit Status Hard Threshold.
TSST:	Transmit Status Soft Threshold.

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The hard and soft threshold work in exactly the same manner except one. The soft threshold will not cause a bus request to be made if the bus is currently in use, but only when it is deemed to be idle (no transfers for four AHB clocks). The hard threshold takes effect immediately regardless of the state of the bus. This operation allows for more efficient use of the AHB bus by allowing smaller transfers to take place when the bus is lightly loaded and requesting larger transfers only when the bus is more heavily loaded.

RXDThrshld

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD										RDHT				0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										RDST				0	0

Address:

0x8001_00E0 - Read/Write

Suggested Value:

0x0004_0002

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Receive Descriptor Threshold register. The receive descriptor thresholds are used to set a limit on the amount of empty space allowed in the MAC's receive descriptor FIFO before a bus request will be scheduled. When the number of empty words in the FIFO exceeds the threshold value, the descriptor processor will schedule a bus request to transfer descriptors. The actual posting of the bus request may be delayed due to lack of resources in the MAC, such as a RXDEnq equal to zero. The lower two bits of the thresholds are always zero.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

0: Must be written as "0".

RDHT: Receive Status Hard Threshold.

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RDST: Receive Descriptor Soft Threshold.

The hard and soft threshold work in exactly the same manner except one. The soft threshold will not cause a bus request to be made if the bus is currently in use, but only when it is deemed to be idle (no transfers for four AHB clocks). The hard threshold takes effect immediately regardless of the state of the bus. This operation allows for more efficient use of the AHB bus by allowing smaller transfers to take place when the bus is lightly loaded and requesting larger transfers only when the bus is more heavily loaded.

TXDThrshld

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD										TDHT				0	0

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD										TDST				0	0

Address:

0x8001_00E4 - Read/Write

Suggested Value:

0x0004_0002

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Transmit Descriptor Threshold register. The transmit descriptor thresholds are used to set a limit on the amount of empty space allowed in the MAC's transmit descriptor FIFO before a bus request will be scheduled. When the number of empty words in the FIFO exceeds the threshold value, the descriptor processor will schedule a bus request to transfer descriptors. The actual posting of the bus request may be delayed due to lack of resources in the MAC, such as a TXDEnq equal to zero. The lower two bits of the thresholds are always zero.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

0: Must be written as "0".

TDHT: Transmit Descriptor Hard Threshold.

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TDST: Transmit Descriptor Soft Threshold.

The hard and soft threshold work in exactly the same manner except one. The soft threshold will not cause a bus request to be made if the bus is currently in use, but only when it is deemed to be idle (no transfers for four AHB clocks). The hard threshold takes effect immediately regardless of the state of the bus. This operation allows for more efficient use of the AHB bus by allowing smaller transfers to take place when the bus is lightly loaded and requesting larger transfers only when the bus is more heavily loaded.

6 MaxFrmLen

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD								MFL							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								TST							

Address:

0x8001_00E8 - Read/Write

Chip Reset:

0x0000_0000

Soft Reset:

Unchanged

Definition:

Maximum Frame Length and Transmit Start Threshold register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

MFL: Maximum Frame Length. The maximum frame length is a limit for the amount of data permitted to be transferred across the AHB bus for a transmit frame, or on the wire for a receive frame. When this limit is reached for a transmit frame, the transmit descriptor processor is halted and a transmit length error is set in the Interrupt Status register. When the limit is reached for a receive frame, no further data will be transferred to memory for the current frame. The status written for the frame will indicate the length error, and further frames will continue as normal, (the receive descriptor processor will not halt).

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TST: Transmit Start Threshold. The transmit start threshold defines the number of bytes that must be written to the transmit data FIFO before a frame will start transmission on the serial interface. This value is primarily of concern when the transmit frame is spread across multiple descriptors and the first descriptors define small amounts of data.

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Chapter 7

DMA Controller

7.1 Introduction

The DMA Controller can be used to interface streams from 20 internal peripherals to the system memory using 10 fully-independent programmable channels that consist of 5 Memory to Internal Peripheral (M2P) transmit channels and 5 Peripheral to Memory (P2M) receive channels.

The DMA Controller can also be used to interface streams from Memory to Memory (M2M), from Memory to Internal Peripheral (M2P), or from Memory to External Peripheral (M2P), using 2 dedicated M2M channels. External handshake signals are optionally available to support Memory to/from External Peripheral transfers (M2P/P2M). A software trigger is available for Memory to Memory transfers, and a hardware trigger is available for Memory to Internal Peripheral.

On the EP9301 chip the following peripherals may be allocated to the 10 channels.

- I2S (which contains 3 Tx and 3 Rx DMA Channels)
- AAC (which contains 3 Tx and 3 Rx DMA Channels)
- UART1 (which contains 1 Tx and 1 Rx DMA Channels)
- UART2 (which contains 1 Tx and 1 Rx DMA Channels)
- IrDA (which contains 1 Tx and 1 Rx DMA Channels)

Each peripheral has it's own bi-directional DMA bus capable of transferring data in both directions simultaneously. All memory transfers take place via the main system AHB bus.

SSP can also use the M2M channels to send or receive data using memory mapping to perform transfers.

SSPRx and SSPTx have access to DMA M2M hardware transfer requests.

7.1.1 DMA Features List

DMA specific features are:

- Ten fully independent, programmable DMA controller internal M2P/P2M channels (5 Tx and 5 Rx).
- Two dedicated channels for Memory-to-Memory (M2M) and Memory-to-

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External Peripheral Transfers (external M2P/P2M).

- Five hardware requests for M2M transfers; 2 for external peripherals that follow the handshake protocol, and 3 simple requests from SSPRx and SSPTx.
- Independent source and destination address registers. Source and destination can be programmed to auto-increment or not for Memory-to-Memory channels.
- Two buffer descriptors per M2P/P2M and M2M channel to avoid potential data underflow/overflow due to software introduced latency.
- For the internal M2P/P2M channels, buffer size is independent of the peripheral's packet size. Transfers can automatically switch between buffers.
- Per channel maskable interrupt generation.
- For DMA Data transfer sizes, byte, word and quad-word data transfers are supported using a 16-byte data bay. Programmable max data transfer size per M2M channel.
- Per-channel clock gating reduces power in channels which have not been enabled by software.

7.1.2 Managing Data Transfers Using a DMA Channel

A set of control and status registers are available to the system processor for setting up DMA operations and monitoring their status, and monitoring system interrupts generated when any of the DMA channels wish to inform the processor to update the buffer descriptor. The DMA controller can service 10 out of 20 possible peripherals using the 10 internal M2P/P2M DMA channels, each with its own peripheral DMA bus capable of transferring data in both directions simultaneously.

The UART1/2/3 and IrDA can each use two DMA channels, one for transmit and one for receive. The AC'97 interface can use six DMA channels (three transmit and three receive) to allow different sample frequency data queues to be handled with low software overhead. The I^2S interface can also use up to six DMA channels (three transmit and three receive) to allow up to six channels of audio out and six channels of audio in.

To perform block moves of data from one memory address space to another with minimum of program effort and time the DMA controller includes a memory-to-memory transfer feature. An M2M software trigger capability is provided. It can also fill a block of memory with data from a single location.

A hardware trigger is also provided for internal peripherals (SSP) or for external peripherals which don't use a handshaking protocol, to allow data

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streams between their internal memory location (or the SMC) and the system memory.

For byte or word wide peripherals, the DMA can be programmed to request byte- or word-wide AHB transfers respectively.

The transfer is completed when the Byte Count Register of the active buffer descriptor reaches zero. Status bits will indicate if the actual byte count is equal to the programmed limit. Completion of transfer will cause a DMA interrupt on that channel and rollover to the “other” buffer descriptor, if configured.

The DMA controller memory-to-memory channels can also be used in “Memory to External Peripheral” mode with handshaking protocol. A set of external handshake signals **DREQ**, **DACK** and **TC/DEOT** are provided for each of 2 M2M channels.

- **DREQ** (input) can be programmed edge or level active, and active high or low. The peripheral may hold **DREQ** active for the duration of the block transfers or may assert/deassert on each transfer.
- **DACK** (output) can be programmed active high or low. **DACK** will cycle with each read or write, the timing is to coincide with the **nOE** or **nWE** of the EBI.
- **TC/DEOT** is a bidirectional signal, the direction and the active sense is programmable. When configured as an output, the DMA will assert **TC** (Terminal Count) on the final transfer to coincide with the **DACK**, typically when the byte count has expired. When configured as an input, the peripheral must assert **DEOT** concurrent with **DREQ** for the final transfer in the block.

Transfer is completed either on **DEOT** being asserted by the external peripheral or the byte count expiring. Status bits will indicate if the actual byte count is equal to the programmed limit, and also if the count was terminated by peripheral asserting **DEOT**. Completion of transfer will cause a DMA interrupt on that channel and rollover to the “other” buffer descriptor if configured.

For byte or word wide peripherals, the DMA will be programmed to request byte or word wide AHB transfers respectively. The DMA will not issue an AHB **HREQ** for a transfer until it has sampled **DREQ** asserted after **DACK** of the previous transfer has been asserted for the duration of the programmed wait states in the SMC (and possibly **DREQ** is sampled in the cycle **DACK** is deasserted).

7.1.3 DMA Operations

The operation of the DMA controller can be defined in terms of channel functionality. Two types of channels exist:

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- Memory-to-Memory (M2M) channel
- Memory-to/from-Internal-Peripheral (M2P/P2M) channel.

7.1.3.1 Memory-to-Memory Channels

The two M2M channels support data transfers between:

- Memory locations which may be located in any accessible system memory banks.

  These memory to memory moves can be initiated by software, in which case the transfer will begin as soon as the channel is configured and enabled for memory to memory move. For this transfer type, the DMA first fills the internal 16-byte data bay by initiating read accesses on the source bus. It then empties the data from the data bay to the destination bus by initiating write accesses.

- Memory locations related to an internal peripheral (SSPRx, SSPTx).

  The transaction is initiated by a peripheral request (**SSPRxREQ** or **SSPTxREQ**). This peripheral request is masked after each peripheral width transfer, in order to allow latency for the peripheral to deassert its request line.The transfer terminates when the Byte Count Register equals zero.

- Memory and External peripherals.

  These can be memory- or FIFO-based and memory-mapped through the SMC. Working with peripheral devices may optionally use the external signals **DREQ, DACK** and **DEOT/TC** to control the data transfer using the following rules:

  - The peripheral sets a request for data to be read-from/written-to by asserting **DREQ**.
  - The peripheral transfers/samples the data when **DACK** is asserted.
  - To terminate the current transfer, depending on the programmed direction of **DEOT/TC**, the peripheral asserts **DEOT** coincident with **DREQ** or the DMA asserts TC coincident with **DACK**.

These data transfer handshaking signals are optional: if the peripheral doesn't use them, then the transfer will operate like an internal peripheral transfer. To support an external DMA peripheral, each request generates one peripheral-width DMA transfer. The M2M Channel 0 is dedicated to servicing External Peripheral 0 and the M2M Channel 1 is dedicated to servicing External Peripheral 1.

7.1.3.2 Memory-to-Peripheral Channels

The 5 M2P and 5 P2M channels support data transfers between Memory and Internal Peripherals (which are byte-wide). Five dedicated channels are

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available to transfer data between internal peripheral and memory (receive direction), and five channels are available to transfer data between memory and peripheral (transmit direction). Transfers are controlled using a REQ/ACK handshake protocol supported by each peripheral.

7.1.4 Internal M2P or P2M AHB Master Interface Functional Description

The AHB Master interface is used to transfer data between the system memory and the DMA Controller internal M2P/P2M channels in both receive and transmit directions as follows:

- In the receive direction, data is transferred to system memory from a packer unit.
- In the transmit direction, data is transferred from the system memory into the unpacker unit.

The AHB bus burst transfer size is a quad-word, that is, if the base memory address programmed into the BASEx register is quad-word aligned then a quad-word transfer either to memory from the 16-byte receive packer, or from memory to the 16-byte transmit packer is carried out.

The internal M2P **RxEnd** signals are asserted by the peripheral to indicate the end of received data or a receiver error. This causes the AHB master interface to write any valid data in the receive packer to main memory. If **RxEnd** signals an error in receive data, and if the ICE bit (Ignore Channel Error) is set, then the DMA continues transfers as normal. The **RxEnd** is asserted by the peripheral coincident with the last good data before the overrun occurred. If the ICE bit is not set, then the DMA flushes the last good data out to memory and terminates the transfer for the current buffer. Where whole words are present in the packer, word transfers are used. For the remaining bytes (up to a maximum of 3), byte transfers are used. Thus the maximum number of bus transfers performed to empty the packer is 6, that is, 3 word transfers and 3 byte transfers.

If the number of bytes transferred from a receive peripheral reaches the MaxTransfer count then this has the same effect as the **RxEnd** signals being asserted by the peripheral. The DMA controller asserts **RxTC** to the peripheral to indicate this condition.

The end of the transfer is signalled by the transfer count being reached, or by the peripheral. In the latter case, any data remaining in a packer unit is written to memory. Any data in an un-packer unit is considered invalid, and therefore discarded, as is data remaining in the transmit FIFO.

When a peripheral receive transfer is complete any data in the packer unit is written to memory. The data may not form a complete quad-word. If an incomplete quad-word is present, data is transferred to memory in either word or byte accesses. The number of valid bytes remaining to be transferred is used to control the type of access. If the number of bytes is 16, then a normal

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quad word write is performed. If the number of bytes is more than 4, then word accesses are performed until the number of bytes is less than 4. If the number of bytes is less than 4, then byte accesses are performed until the remainder of the data has been transferred.

If the peripheral ended the transfer with an error code, an interrupt is generated, and operation continues as normal using the next buffer descriptor (if it has been set up) to ensure that a minimal amount of data is lost. The point at which the transfer failed can be determined by reading the channel current address register for the last buffer. An example of an internal peripheral error code is the Transmit FIFO underflow error in the AAC.

7.1.5 M2M AHB Master Interface Functional Description

The AHB Master interface is also used to transfer data between either the system memory or external peripheral and the DMA Controller M2M channels in both receive and transmit directions.

7.1.5.1 Software Trigger Mode

When a M2M channel receives a software trigger and the buffer descriptor has been programmed, the AHB master interface begins to read data from memory into the data bay. When the DMA_MEM_RD state is exited (that is, data transfer to the data bay has finished) this causes the AHB master interface to write the data contained in the data bay to main memory. The data may not form a complete quad-word. If an incomplete quad-word is present, data is transferred to memory in either word or byte accesses. The number of valid bytes remaining to be transferred is used to control the type of access. If the number of bytes is 16, then a normal quad word write is performed. If the number of bytes is more than 4, then word accesses are performed until the number of bytes is less than 4. If the number of bytes is less than 4, then byte accesses are performed until the remainder of the data has been transferred.

7.1.5.2 Hardware Trigger Mode for Internal Peripherals (SSP) and for External Peripherals without Handshaking Signals

When a M2M channel is set up to transfer to/from SSP or an external peripheral, the transfer width used (that is, the AMBA **HSIZE** signal) is determined by the peripheral width - programmed via the CONTROL.PW bits of the channel. This means that the transfers occur one at a time, as opposed to burst transfer operation for software triggered M2M. Thus the 16-byte data bay which is available for software triggered transfers is never fully utilized - at most 1 word of it is used (depending on PW bits).

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7.1.5.3 Hardware Trigger Mode for External Peripherals with Handshaking Signals

When a M2M channel is set up to transfer to/from an external peripheral, the transfer width used (that is, the AMBA **HSIZE** signal) is determined by the peripheral width - programmed via the CONTROL.PW bits of the channel. This means that the transfers occur one at a time, as opposed to burst transfer operation for software triggered M2M. Thus the 16-byte data bay which is available for software triggered transfers is never fully utilized - at most 1 word of it is used (depending on PW bits).

7.1.6 AHB Slave Interface Limitations

The AHB slave interface is used to access all control and status registers.

The behavior of the AMBA AHB signals complies with the standard described in AMBA Specification (Rev 2.0) from ARM Limited. The DMA does not utilize the AHB slave split capabilities, so does not receive **HMASTER** or **HMASTERLOCK** and does not drive **HSPLIT**. It does not receive **HPROT** or **HRESP** and does not drive **HLOCK**.

7.1.7 Interrupt Interface

Each of the 12 DMA channels (10 M2P/P2M and 2 M2M) generates a single interrupt signal which is a combination of the interrupt sources for that channel. There are 3 interrupt sources, which are enabled in the channel control register (for both M2P/P2M and M2M): **DONE**, **STALL** and **NFB.**The interrupt signals are ORed before being transmitted to the **DMA_INT** output bus. Status of the interrupt bus is reflected in the DMA Global Interrupt Register (DMAGIInt). The status of each interrupt source per channel is found in the channel's interrupt register.

7.1.8 Internal M2P/P2M Data Unpacker/Packer Functional Description

The DMA controller transfers data to and from the system memory in four word bursts. The peripheral DMA bus protocol is used to transfer data to and from the peripherals as single bytes. In order to build the quad word bursts from the single bytes received from the peripheral, the DMA controller uses the Rx Burst Packers. To decompose the quad word bursts into byte transfers to the peripherals the Tx Burst Un-Packers are used.

The data received on each of the five peripheral receive DMA Rx Data buses is transferred into an internal receive packer unit. The packer unit is used to convert the byte-wide data received from the peripheral into words to be transferred over the system bus to the memory. The packer unit stores 4 words (one quad-word) of data, which is the size of the burst transfers to and from memory over the system bus. Provision for the memory access latency is

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provided by FIFOs within the peripheral. The size of the FIFOs can be selected as appropriate for the data rate generated by the peripheral.

Transmit data is fetched from system memory by the AHB master interface and placed into the transmit un-packer. The transmit un-packer converts the quad-word burst of DMA data into byte data for transmission over the transmit peripheral DMA bus. The transmit un-packer contains 4 words (one quad-word) of storage. Additional latency is provided by FIFOs within the peripheral, the size of which can be selected as appropriate for the peripheral.

The number of data transfers over the peripheral DMA bus (that is, the number of bytes) are counted by packer/un-packer unit. If the number of bytes transferred reaches the MaxTransfer count, the appropriate **RxTC/TxTC** signal is asserted causing the flush to memory of data from a packer unit, and the invalidation of any data remaining in an un-packer unit.

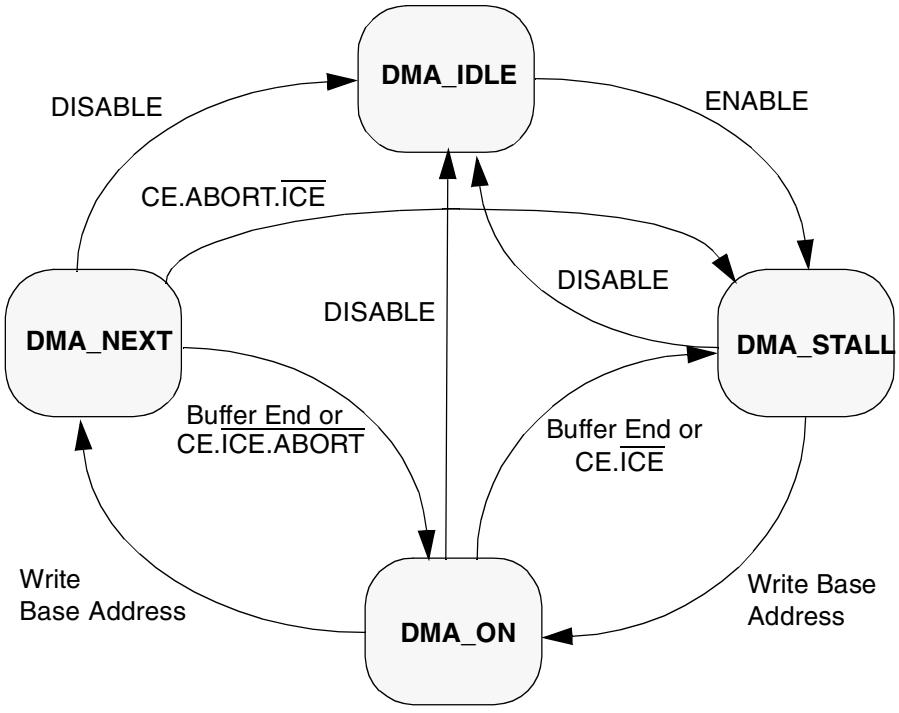
7

7.1.9 Internal M2P/P2M DMA Functional Description

7.1.9.1 Internal M2P/P2M DMA Buffer Control Finite State Machine

Each DMA internal M2P/P2M channel is controlled by a finite state machine (FSM) which determines whether the channel is transferring data, and whether it is currently generating an interrupt.

Figure 7-1. DMA M2P/P2M Finite State Machine



CE: Channel (Peripheral) Error

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ICE: CONTROL[6] - Ignore Channel Error. This bit may be set for data streams whereby the end user can tolerate occasional bit errors. If it is not set then the DMA will abort its transfer in receipt of a peripheral error.

ABORT: CONTROL[5]

7.1.9.1.1 DMA_IDLE

The DMA Channel FSM always resets to the DMA_IDLE state.

The DMA Channel FSM always enters the DMA_IDLE state when the channel is disabled (CONTROL[4]).

7.1.9.1.2 DMA_STALL

The DMA Channel FSM enters the DMA_STALL state when the channel enabled, no STALL interrupt is generated for this condition.

The DMA Channel FSM enters the DMA_STALL state if a memory buffer completes in the ON state. A DMA_STALL interrupt is generated for this condition.

The DMA Channel FSM enters the DMA_STALL state and terminates the current memory buffer if there is a peripheral error (**TxEnd/RxEnd** indication) while in the DMA_ON state, and ICE is not active.

The DMA Channel FSM enters the DMA_STALL state and terminates the current memory buffer if there is a peripheral error (**TxEnd/RxEnd** indication) while in the DMA_NEXT state, and ABORT is active, and ICE inactive. No STALL interrupt is generated for this condition.

No data transfers occur in this state.

7.1.9.1.3 DMA_ON

The DMA Channel FSM enters this state when a base address is written in the stall state.

Data transfers occur in this state.

The DMA Channel FSM enters this state when the current memory buffer expires, or when a peripheral error occurs that does not cause an abort, while in the DMA_NEXT state. The transition from DMA_NEXT to DMA_ON state results in a NFB interrupt being generated.

7.1.9.1.4 DMA_NEXT

The DMA Channel FSM enters this state when a base address register is written in the DMA_ON state (that is, for buffer Y). The DMA will continue to transfer using the buffer (that is, buffer X) that it began with in the DMA_ON state. When buffer X expires or when a peripheral error occurs, then the DMA will automatically switch over to using the next buffer (buffer Y). It will generate

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an interrupt (NFBint) to signal to the processor that it is switching over to a new buffer and that the old buffer descriptor (buffer X) is available to be updated.

Data transfers occur in this state.

7.1.9.2 Data Transfer Initiation and Termination

The DMA Controller initiates data transfer in the receive direction when:

- A packer unit becomes full
- A packer unit, dependent on the next address access, contains enough data for an unaligned byte/word access.

The DMA Controller stops data transfers in the receive direction and moves onto the next buffer when:

- **RxEnd** signal is asserted to indicate end of received data or received error.

  No matter what the alignment up to now, this causes the AHB Master interface to write any valid data in the receive packer to main memory. If RxEnd signals the end of received data then all data which is present in the receive packer gets flushed to memory. If RxEnd signals an error in receive data, and if the ICE bit (Ignore Channel Error) is not set, then the erroneous byte is not written to memory. Only valid bytes are written. If ICE bit is set then the erroneous byte is written to memory. The DMA will update the Channel Status Register, generating a system interrupt which informs the processor that a new buffer needs to be allocated, and DMA will also indicate (NEXTBUFFER field) which pair of buffer descriptor registers (MAXCNTx, BASEx) should be used for the next buffer.

- The number of bytes transferred from a receive peripheral reaches MAXCNTx.

  Note: This refers to bytes entering the data packer and not just data transmitted over the AHB bus (that is, has same effect as RxEnd signal generated by the peripheral). The DMA Controller asserts RxTC to the peripheral to indicate this condition. The DMA will update the Channel Status Register, generating a system interrupt, which informs the processor that a new buffer needs to be allocated and DMA will also indicate (NEXTBUFFER field) which pair of buffer descriptor registers (MAXCNTx, BASEx) should be used for the next buffer.

The DMA Controller initiates data transfers in the transmit direction when an Un-packer unit becomes empty.

The DMA Controller stops data transfer in the transmit direction when:

- **TxEnd** signal is asserted to indicate that the transfer is the last in the transmit data stream. Any data remaining in the Un-packer unit is considered invalid and flushed. At this point, the Channel Status Register

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will be updated and next buffer defined.

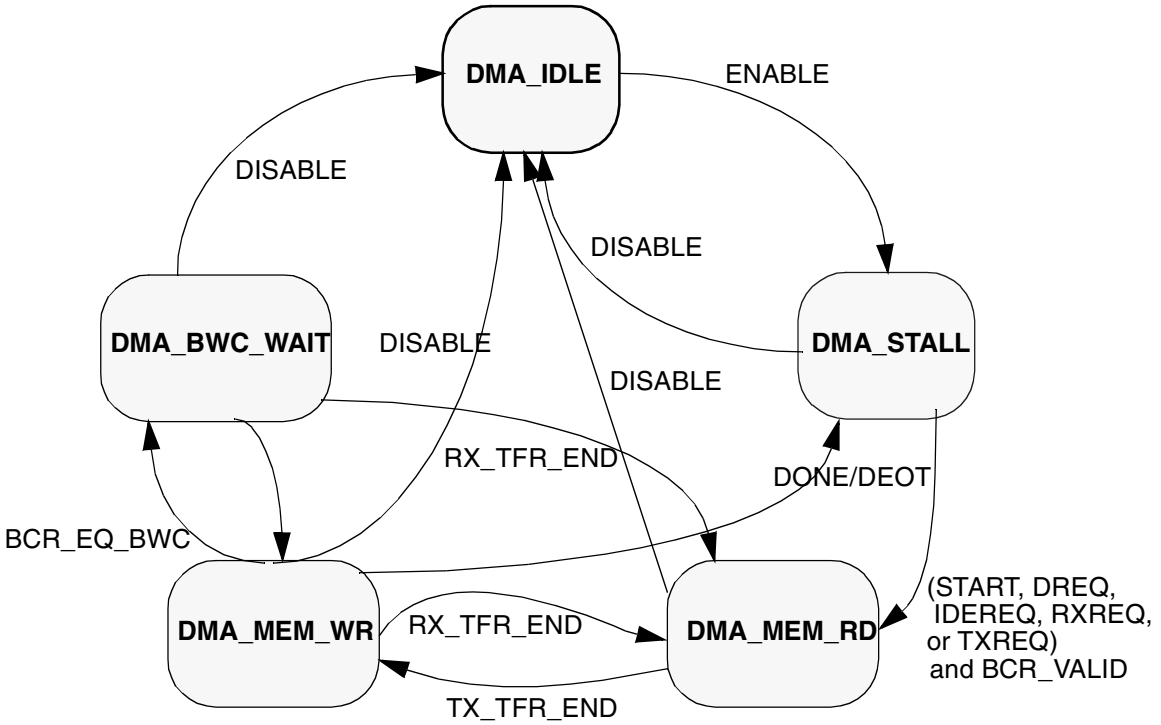
- **TxTC** signal asserted by DMA Controller to indicate to the peripheral that the transfer is the last as the byte count limit has been reached. At this point, the Channel Status Register will be updated and next buffer defined.
- Bursting across buffers cannot be carried out in either transmit or receive directions. The reason is that buffer pairs may not be contiguous, as required by HTRANS SEQ transfer type (where address = address of previous transfer + size in bytes).

7.1.10 M2M DMA Functional Description

7.1.10.1 M2M DMA Control Finite State Machine

Each DMA M2M channel is controlled by 2 finite state machines (FSM) which determine whether the channel is transferring data to or from memory, which buffer from the double-buffer descriptor set it is using, and whether it is currently generating an interrupt.

Figure 7-2. M2M DMA Control Finite State Machine



7.1.10.1.1 DMA_IDLE

The DMA M2M Control FSM always resets to the DMA_IDLE state.

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The DMA Control M2M FSM always enters the DMA_IDLE state when a channel is disabled (CONTROL[3]).

The DMA Control M2M FSM exits the DMA_IDLE state and moves to the DMA_STALL state when the ENABLE bit of the CONTROL register is set.

7.1.10.1.2 DMA_STALL

The DMA M2M Control FSM enters the DMA_STALL state when an M2M channel is enabled. No STALL interrupt is generated for this condition.

The DMA M2M Control FSM enters the DMA_STALL state when a memory-to-memory transfer has completed successfully. The DONE and STALL interrupts are generated for this condition, if enabled.

No data transfers occur in this state.

7.1.10.1.3 DMA_MEM_RD

The DMA M2M Control FSM enters the DMA_MEM_RD state when a M2M channel has received a software trigger to begin a transfer, that is, the START bit is set (CONTROL[4]) and CONTROL.TM = “00”; or when an internal peripheral (SSP) asserts its request line and CONTROL.TM = “01” or “10”; or when an external peripheral asserts its **DREQ** o/p to the DMA and CONTROL.TM = “01” or “10”. At least one of the BCRx registers must contain a valid value, otherwise the DMA stays in the DMA_STALL state. For software triggered mode a valid BCR value is any non-zero value. For external peripheral mode a valid BCR value depends on the peripheral width (programmed via the PW bits of the CONTROL register). For word/halfword/byte-wide peripherals the BCR value must be greater than or equal to four/two/one respectively.

The DMA M2M Control FSM enters the DMA_MEM_RD state when a memory write transfer has finished and the BCR register is still not equal to zero, that is, more data needs to be transferred from memory-to-memory. For external peripheral and SSP transfers, BCR not-equal-to 0 must be qualified with a **DREQ** before the DMA_MEM_RD state is entered again.

The DMA M2M Control FSM enters the DMA_MEM_RD state on exit from the DMA_BWC_WAIT state, if all the data present in the data bay had been transferred to memory when DMA_BWC_WAIT state was entered.

The DMA M2M Control FSM stays in this state until the data transfer from memory has completed for software trigger mode, that is, the data bay is filled with 16 bytes (or less depending on transfer size and BCR value etc.).

The DMA M2M Control FSM enters the DMA_MEM_RD state when the BCR register is equal to zero for the current buffer, and the other buffer descriptors BCR register has been programmed non-zero. DMA will proceed to do a memory read using the new buffer and the NFB interrupt is generated, if enabled.

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Data transfers from memory or external peripherals (depending on the CONTROL.TM bits), occur in this state.

7.1.10.1.4 DMA_MEM_WR

The DMA M2M Control FSM enters the DMA_MEM_WR state when a memory read transfer has completed.

The DMA M2M Control FSM enters the DMA_MEM_WR state on exit from the DMA_BWC_WAIT state, if all the data present in the data bay had not been transferred to memory when DMA_BWC_WAIT state was entered.

The DMA M2M Control FSM stays in this state until the data transfer to memory has completed, that is, the data bay is emptied.

Data transfers, to memory or external peripheral (depending on the CONTROL.TM bits), occur in this state.

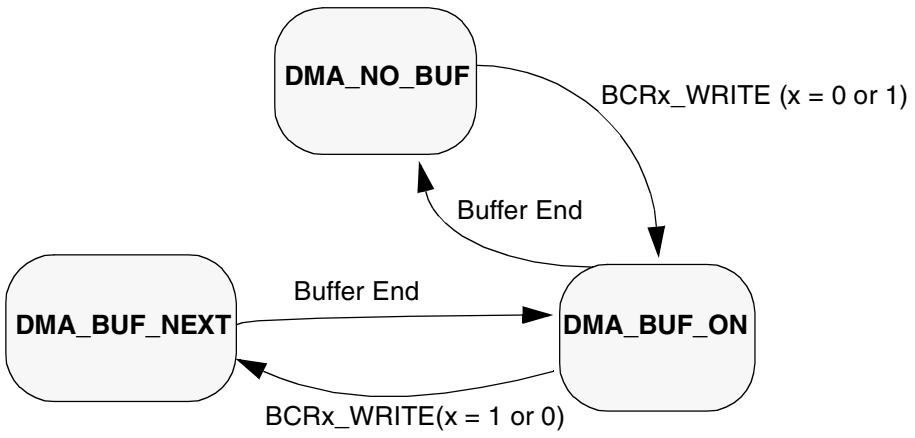
7.1.10.1.5 DMA_BWC_WAIT

The DMA M2M Control FSM enters the DMA_BWC_WAIT state when the byte count is within 15 bytes of a multiple of the BWC value.

The DMA M2M Control FSM stays in this state for one cycle only.

7.1.10.2 M2M Buffer Control Finite State Machine

Figure 7-3. M2M DMA Buffer Finite State Machine



7.1.10.2.1 DMA_NO_BUF

The DMA M2M Buffer FSM resets to the DMA_NO_BUF state. This state reflects that no buffer descriptor has as yet been programmed in the DMA controller.

The DMA M2M Buffer FSM exits this state when one of the BCRx (x = 0 or 1) registers is programmed. If BCR0 is written to, then the FSM moves to the DMA_BUF_ON state and buffer0 becomes the active buffer available for a

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transfer. If BCR1 is written to then the FSM moves to the DMA_BUF_ON state and buffer1 becomes the active buffer available for a transfer.

7.1.10.2.2 DMA_BUF_ON

The DMA Buffer FSM enters the DMA_BUF_ON state from the DMA_NO_BUF state when one of the BCRx registers is written to.

The DMA Buffer FSM enters the DMA_BUF_ON state from the DMA_BUF_NEXT state when the transfer from the active buffer has ended. This end-of-buffer can be due to the BCRx register value reaching zero, or receipt of a **DEOT** input from the external peripheral (when in external peripheral transfer mode and **DEOT** is configured as an input signal to the DMA).

Data transfers to or from memory or external peripherals can occur in the DMA_BUF_ON state. When the DMA Buffer FSM transitions from DMA_BUF_NEXT to DMA_BUF_ON state, the NFB (Next Frame Buffer) interrupt is generated. This signals to software that rollover is occurring to the other buffer and also that one of the BCRx registers is now free for update (which BCRx is free can be determined using the STATUS.Nextbuffer status bit - see “STATUS” on page 251).

When the DMA Buffer FSM transitions from DMA_BUF_ON to DMA_NO_BUF state due to end of buffer, the DONE status bit is asserted and the DONE interrupt is set if enabled. The **TC** (Terminal Count) output is asserted by the DMA to the external peripheral if the BCR register has expired for the current buffer (when in external peripheral transfer mode and **TC** is programmed as an output signal from the DMA). The end of buffer can also be due to receipt of a **DEOT** input from the external peripheral (when in external peripheral transfer mode and **DEOT** is configured as an input signal to the DMA). The TCS and EOTS status bits of the STATUS register indicate what caused the end of buffer.

7.1.10.2.3 DMA_BUF_NEXT

The DMA Buffer FSM enters the DMA_BUF_NEXT state from the DMA_BUF_ON state when a write occurs to the second of the BCRx registers (that is, the BCRx register that was not written to when in the DMA_NO_BUF state).

The DMA Buffer FSM stays in this state until the transfer using the active buffer has ended, either as a result of BCRx reaching zero or due to receipt of a **DEOT** input from the external peripheral (when in external peripheral transfer mode and **DEOT** is configured as an input signal to the DMA). The TCS and EOTS status bits of the STATUS register indicate what caused the end of buffer.

Data transfers to/from memory or external peripheral can occur in the DMA_BUF_NEXT state.

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When the DMA Buffer FSM transitions from DMA_BUF_NEXT to DMA_BUF_ON state as a result of the BCR count expiring, the **TC** (Terminal Count) output is asserted by the DMA to the external peripheral to indicate that the BCR register has expired for the current buffer (when in external peripheral transfer mode and **TC** is programmed as an output signal from the DMA).

When the DMA Buffer FSM transitions from DMA_BUF_NEXT to DMA_BUF_ON state, the NFB (Next Frame Buffer) interrupt is generated (if enabled). This signals that one of the buffer descriptors is now free for update. For example the following sequence of events could occur:

- BCR0 is programmed => move to DMA_BUF_ON state.
- BCR1 is programmed => move to DMA_BUF_NEXT state.
- Channel is enabled => transfers begin using Buffer0.
- Buffer0 transfer ends => move to DMA_BUF_ON state and begin transfers with Buffer1.
- NFB interrupt is generated when FSM moves to DMA_BUF_ON state, signalling that
- Buffer0 is now free for update.

7.1.10.3 Data Transfer Initiation

Memory-to-memory transfers require a read-from and a write-to memory to complete each transfer.

The DMA Controller initiates memory-to-memory transfers in the receive direction (that is, from memory/peripheral to DMA) under the following circumstances:

- A channel has been triggered by software, that is, setting the START bit to “1”. Setting the START bit causes the channel to begin requesting the bus, and when granted ownership it will start transferring data immediately. The DMA controller drives the SAR_BASEx value onto the internal AHB address bus. If CONTROL.SCT is not set, the SAR_BASEx increments by the appropriate number of bytes upon a successful read cycle. The DMA initiates the write portion of the transfer when the appropriate number of read cycles is completed, that is, either when the 16-byte data bay has been filled, or when it contains the number of bytes (less than 16) that remain to be transferred, or when it contains sufficient data for an unaligned byte/word access (dependant on the next address access).
- A channel receives a transfer request from an internal peripheral (SSP) or from an external peripheral without handshaking signals (that is, CONTROL.NO_HDSK = “1”), and the transfer mode is set to be either memory-to-external peripheral mode or external peripheral-to-memory

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mode (that is, CONTROL.TM = “01”/“10” respectively). The DMA drives the SAR_BASEx value onto the address bus and requests a transfer size equal to the programmed peripheral width. In the case of CONTROL.TM = “10” where the external peripheral (which is the source for the data) is FIFO-based, it is up to software to program the SAH bit correctly (Source Address Hold), so that on successive transfers from the peripheral, the SAR_CURRENTx value will not increment, thus reflecting the FIFO-nature of the peripheral.

- A channel receives a request from an external peripheral and the transfer mode is set to be either memory-to-external peripheral mode or external peripheral-to-memory mode (that is, CONTROL.TM = “01” or “10” respectively). The DMA drives the SAR_BASEx value onto the address bus and requests a transfer size equal to the programmed peripheral width. In the case of CONTROL.TM = “10” where the external peripheral (which is the source for the data) is FIFO-based, it is up to software to program the SAH bit correctly (Source Address Hold), so that on successive transfers from the peripheral, the SAR_CURRENTx value will not increment, thus reflecting the FIFO-nature of the peripheral.

- When the current transfer terminates the DMA will check if the BCR register for the “other” buffer (of the double-buffer set) has been programmed. If BCR is non-zero and CONTROL.TM = “00”, that is, software trigger mode, then the DMA will proceed immediately to request the AHB bus and begin a transfer from memory to DMA using the other buffer descriptor. Software does not need to reprogram the START bit, it is enough to have the second buffer descriptor set up while the first buffer transfer is in progress. In the case where TM is such that external-peripheral mode is set up, then rollover to the other buffer will also occur if the current transfer terminates, but the DMA will wait until it receives a **DREQ** from the external peripheral before initiating a transfer.

The DMA Controller initiates memory-to-memory transfers in the transmit direction (that is, from DMA to memory/peripheral) under the following circumstances:

- For a software triggered M2M transfer and transfers involving internal peripherals a memory-write is initiated when the 16-byte data bay has been filled (in the case where 16 or more bytes remain to be transferred) or when it contains the appropriate number of bytes (equal to BCR register value if BCR is less than 16). The DMA controller drives the DAR_BASEx onto the address bus. This address can be any aligned byte address. The BCR register decrements by the appropriate number of bytes. When BCR = 0 then the transfer is complete. If BCR is greater than zero, another read/write transfer is initiated.
- For transfers involving external peripherals or SSP, the DMA memory-write phase is initiated when the data bay contains the byte/halfword/word data, depending on PW value, that is, peripheral width. The DMA will then

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drive the DAR_BASEx onto the address bus and will set the AMBA **HSIZE** signal in accordance with the PW value. Once the DMA has received confirmation that the write is done (from **HREADY** in case of an internal memory write, or from the SMC acknowledge signal in case of an external peripheral write), a wait state counter is started. During the count, the hardware request line is masked, in order to allow the related peripheral to de-assert its request.In the case of CONTROL.TM = “01” and the external peripheral (which is the destination for the data) is FIFO-based, it is up to software to program the DAH bit correctly (Destination Address Hold), so that on successive transfers to the peripheral, the DAR_CURRENTx value will not increment, thus reflecting the FIFO-nature of the peripheral.

7.1.10.4 Data Transfer Termination

The DMA Controller terminates a memory-to-memory channel transfer under the following conditions:

- For software-triggered transfers which use a single buffer, the transfer is terminated when the BCR register of the active buffer has reached zero. The DONE status bit and corresponding interrupt (if enabled) are set. In the case of double/multiple buffer transfers, termination occurs when the BCR registers of both buffer descriptors has reached zero. The DONE status bit and corresponding interrupt (if enabled) are set. When the DONE interrupt is set the processor can then write a one to clear the interrupt before reprogramming the DMA to carry out another M2M transfer.
- For hardware triggered transfers involving internal peripherals (SSP) or external peripherals without handshaking signals, the transfer is also terminated when the BCR register of the active buffer has reached zero. The DONE status bit and corresponding interrupt (if enabled) are set. When the DONE interrupt is set, the processor can then write a one to clear the interrupt before reprogramming the DMA to carry out another external M2P/P2M transfer.
- For operations involving external peripherals using a single buffer, the transfer is terminated on the first occurrence of **DEOT** being asserted by the peripheral or the byte count expiring for the active buffer. In the case of the DMA receiving a **DEOT** from the peripheral (which is aligned to **DREQ**) the DMA knows that this is the final transfer to be performed. The DONE status bit and corresponding interrupt (if enabled) are set. In the case of double/multiple buffer transfers, termination occurs on either the occurrence of the DMA receiving a **DEOT** from the peripheral while it is transferring to/from the last buffer (that is, no other buffer has been set up), or when the BCR registers of both buffer descriptors has reached zero.

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When the DONE interrupt is set, the processor can then write a one to clear the interrupt before reprogramming the DMA to carry out another external M2P/P2M transfer. If the **DEOT_TC** pin is configured as an output pin (**TC**), the DMA asserts **TC** when each buffers byte count expires. It then rolls over to the other buffer. If the **DEOT_TC** pin is configured as an input pin (**DEOT**), the DMA terminates transfers from the active buffer when **DEOT** is asserted and rolls over to the other buffer. The DONE interrupt is not asserted when the DMA has another buffer available to which it can roll over. However the NFB interrupt is generated when the rollover occurs.

7.1.10.5 Memory Block Transfer

The DMA Controller M2M channels provide a feature whereby block moves of data from one memory location can occur. If the CONTROL.SCT register bit is set for a channel, then its source address will not increment. In order to use this feature, both the source and destination addresses must be word-aligned, thus facilitating the transfer of a word of data from 1 location to a block of memory with the number of destination memory addresses written to is determined by the byte count register. For example, to copy a word to 10 consecutive destination addresses, then BCR must be set to 40.

7.1.10.6 Bandwidth Control

The Bandwidth Control feature makes it possible to force the DMA off the AHB bus during M2M transfers, to allow access to another device/peripheral. CONTROL.BWC register bits provide 12 levels of block transfer sizes. If the BCR decrements to within 15 bytes of a multiple of the decode of BWC, then the DMA bus request is negated until the bus cycle terminates, to allow the AHB bus arbiter to switch masters.

If BWC is equal to zero, then the bus request stays asserted until BCR = zero, that is, the transfer is finished. If the initial value of BCR is equal to the BWC decode, the bus request will not be negated straight away. Some data must first be transferred.

7.1.10.7 External Peripheral DMA Request (DREQ) Mode

When the external peripheral requires DMA service, it asserts **DREQ**, which may be configured as either edge or level sensitive using bit DREQP[1] of the CONTROL register.

External peripheral DMA requests are processed as follows:

- In level-sensitive mode, the external peripheral requests service by asserting **DREQ** and leaving it asserted as long as it needs service. The DMA synchronizes the **DREQ** input using 2 HCLK flip-flops for metastability protection. To prevent another transfer from taking place, the external peripheral must deassert the **DREQ** pin during the **DACK** (DMA Acknowledge) cycle. The number of cycles that **DACK** is asserted is governed by the number of wait states in the Static Memory Controller.

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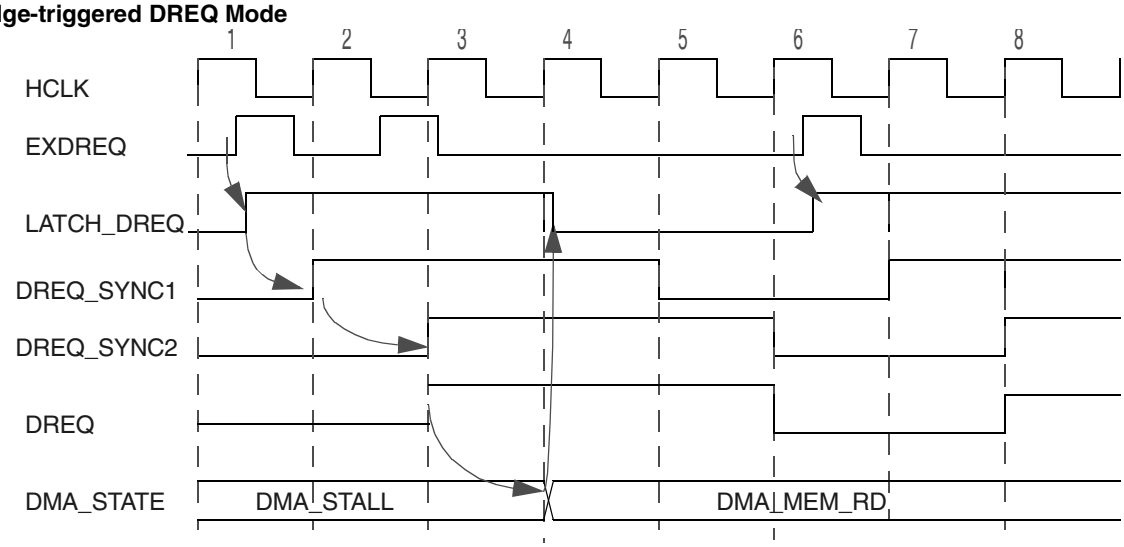
- For external peripherals that generate a pulsed signal for each transfer, edge-sensitive mode should be used. When the DMA detects a rising/falling edge on **DREQ** (as configured by bit DREQP[0] of the CONTROL register), a request becomes pending. The DMA synchronizes the latched **DREQ** input using 2 HCLK flip-flops for metastability protection. The DREQS status bit is set to indicate that a request is pending. Subsequent changes on **DREQ** are ignored until the pending request begins to be serviced. When the pending request has begun to be serviced, the DREQS status bit is cleared and subsequent edge-triggered requests are again recognized (latched) by the DMA. The DREQS status bit can be cleared by a software write to the channel STATUS register, thus causing the DMA to ignore the request.

Figure 7-4. Edge-triggered DREQ Mode



1. A **DREQ** rising edge (**DREQ** is active high) is latched onto **LATCH_DREQ** during cycle 1.
2. This signal is synchronized using 2 HCLK flip-flops. The DREQS status bit indicates a request is pending at start of cycle 3.
3. The DMA state machine moves into the DMA_MEM_RD state to begin servicing the first request in cycle 4.
4. The **DREQ** latch is reset as a result of this state change and 2 cycles later the DREQS status bit is cleared.
5. A second request cannot be recognized until DREQS is cleared. Hence the request received during cycle 2 is ignored by the DMA.
6. A rising edge on **DREQ** during cycle 6 is latched and causes the DREQS status bit to be set again, thus indicating that another external peripheral request is pending.

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7.1.11 DMA Data Transfer Size Determination

7.1.11.1 Software Initiated M2M and M2P/P2M Transfers

Data transfer size flexibility is guaranteed by allowing the start address of a DMA transfer to be aligned to any arbitrary byte boundary since this is the case for the 10 internal byte-wide M2P/P2M channels and for the 2 M2M channels when used in software initiated mode.

At the start of a receive or transmit data transfer, the AHB Master Interface uses the low order 4 bits of the current DMA address to decide on the data transfer size to use. If the low-order 4 bits are zero, the first transfer is a quad word access. If they are not all zero, then if the low-order two bits are zero, then the first transfer is a word transfer. Word transfers will continue, and the current address incremented each time by one word, until the low-order address bits indicate that the address is quad-word aligned. If the start address is not word aligned, then the first transfer is a byte transfer, and the current address is incremented by one byte each time until the current address is word aligned. Transfers will then be performed as word transfers until the address is quad-word aligned. (Unless the address becomes quad-word aligned immediately, in which case quad word transfers are used). Note that in the case of the M2M channels, source address alignment takes precedence over destination address alignment. This means that if the source is aligned on a quad-word boundary and the destination address is aligned on a byte boundary, the channel will burst data into the data bay and then perform byte transfers to the destination.

The maximum transfer count can be any arbitrary number of bytes.

Table 7-1: Data Transfer Size

Current DMA Addr Bits [3:0]	Transfer Type
0000	Quad-Word access (unless there are less than 4 word addresses remaining)
0100,1000,1100	Word access
xx01, xx10, xx11	Byte access

The DMA Controller transfers data when it owns the AHB bus. Note that with byte/ word/quad-word scheme that the DMA Controller employs, it can never burst across a 1KB boundary. The reason is that the DMA Controller only bursts when the 4 LSB Address bits are 0000b. A 1 KB boundary has the LSB 10 Address bits being zero. (ref: ARM AMBA Specification).

7.1.11.2 Hardware Initiated M2M Transfers

The data transfer size for DMA transfers to/from external peripherals or SSP is dictated by the peripheral width. For byte, half-word or word wide peripherals, the DMA is programmed, using the PW bits of a channels control register, to

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request byte, half-word or word wide transfers respectively. Each external peripheral request generates one peripheral width DMA transfer. If the memory involved is narrower than the peripheral then multiple memory accesses may be needed, for example, a word wide peripheral transferring to byte wide memory requires 4 memory transfers. The memory controller handles the generation of multiple memory accesses if necessary (and not the DMA).

7.1.12 Buffer Descriptors

A “buffer” refers to the area in system memory that is characterized by a buffer descriptor, that is, a start address and the length of the buffer in bytes.

7.1.12.1 Internal M2P/P2M Channel Rx Buffer Descriptors

Only one Rx buffer descriptor is allocated per transaction. There are five Rx buffer descriptors, one for each of the five receive channels. Each buffer descriptor allows a channel double buffering scheme by containing programming for two buffers, that is, two system buffer base addresses and two buffer byte counts. This ensures that there is always one free buffer available for transfers to avoid potential data over/under-flow due to software-introduced latency.

7.1.12.2 Internal M2P/P2M Channel Tx Buffer Descriptors

Only one Tx buffer descriptor is allocated per transaction. There are five Tx buffer descriptors, one for each of the five transmit channels Each buffer descriptor allows a channel double buffering scheme by containing programming for two buffers, that is, two system buffer base addresses and two buffer byte counts. This ensures that there is always one free buffer available for transfers to avoid potential data over/under-flow due to software introduced latency.

7.1.12.3 M2M Channel Buffer Descriptors

Only one M2M channel buffer descriptor is allocated per transaction. There are two M2M buffer descriptors, one for each of the 2 M2M channels. Each buffer descriptor allows a channel double buffering scheme by containing programming for two buffers, that is, two source base addresses, two destination base addresses and two buffer byte counts. The buffers are limited to 64 kBytes (0xFFF). This ensures that there is always one free buffer available for transfers which avoids potential data overflow/underflow due to software introduced latency.

7.1.13 Bus Arbitration

When ready to do a transfer, the DMA Controller arbitrates internally between DMA Channels, then requests AHB bus access to the external AHB bus

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arbiter. Then a default setting of M2P having a higher priority than M2M is implemented. The default setting is programmable and can be changed if required (DMA Arbitration register bit[0] = CHARB).

The channel arbitration scheme is based on rotating priority, the order is as shown below in Table 7-2:

Table 7-2: M2P DMA Bus Arbitration

Internal Arbitration Priority		
	CHARB = 0	**CHARB = 1**
Highest	M2P Ch 0	M2M Ch 0
	M2P Ch 1	M2M Ch 1
	M2P Ch 2	M2P Ch 0
	M2P Ch 3	M2P Ch 1
	M2P Ch 4	M2P Ch 2
	M2P Ch 5	M2P Ch 3
	M2P Ch 6	M2P Ch 4
	M2P Ch 7	M2P Ch 5
	M2P Ch 8	M2P Ch 6
	M2P Ch 9	M2P Ch 7
	M2M Ch 0	M2P Ch 8
Lowest	M2M Ch 1	M2P Ch 9

During normal operation, using the “fair” rotating priority scheme shown in Table 7-2, the last channel to be serviced becomes the lowest priority channel with the others rotating accordingly. In addition, any device requesting service is guaranteed to be recognized after no more than eleven higher priority services has occurred. This prevents any one channel from monopolizing the system. When the bus is idle, the scheme reverts to a fixed priority whereby the highest priority request gets in first (as shown in Table 7-2) when the bus resumes to normal operation.

In the case where the two M2M channels are requesting a service, the read and write transfers for the first channel are completed before the read transfer for the second channel begins.

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7.2 Registers

7.2.1 DMA Controller Memory Map

The following table defines the DMA Controller mapping for each of 10 M2P (memory-to-peripheral) channels (5 Tx and 5 Rx), plus the 2 M2M (memory-to-memory) channels.

Before programming a channel, the clock for that channel must be turned on by setting the appropriate bit in the PwrCnt register of the Clock and State Controller block.

Table 7-3: DMA Memory Map

ARM920T Address	Description	Channel Base Address
0x8000_0000 -> 0x8000_003C	M2P Channel 0 Registers (Tx)	0x8000_0000
0x8000_0040 -> 0x8000_007C	M2P Channel 1 Registers (Rx)	0x8000_0040
0x8000_0080 -> 0x8000_00BC	M2P Channel 2 Registers (Tx)	0x8000_0080
0x8000_00C0 -> 0x8000_00FC	M2P Channel 3 Registers (Rx)	0x8000_00C0
0x8000_0100 -> 0x8000_013C	M2M Channel 0 Registers	0x8000_0100
0x8000_0140 -> 0x8000_017C	M2M Channel 1 Registers	0x8000_0140
0x8000_0180 -> 0x8000_01BC	Not Used	
0x8000_01C0 -> 0x8000_01FC	Not Used	
0x8000_0200 -> 0x8000_023C	M2P Channel 5 Registers (Rx)	0x8000_0200
0x8000_0240 -> 0x8000_027C	M2P Channel 4 Registers (Tx)	0x8000_0240
0x8000_0280 -> 0x8000_02BC	M2P Channel 7 Registers (Rx)	0x8000_0280
0x8000_02C0 -> 0x8000_02FC	M2P Channel 6 Registers (Tx)	0x8000_02C0
0x8000_0300 -> 0x8000_033C	M2P Channel 9 Registers (Rx)	0x8000_0300
0x8000_0340 -> 0x8000_037C	M2P Channel 8 Registers (Tx)	0x8000_0340
0x8000_0380	DMA Channel Arbitration register	
0x8000_03C0	DMA Global Interrupt register	
0x8000_03C4 -> 0x8000_FFFC	Not Used	0x8000_03C4

7.2.2 Internal M2P/P2M Channel Register Map

The DMA Memory Map above includes the base address mapping for the channel registers for each of the 10 M2P/P2M channels that are shown in the following table, the Internal M2P/P2M Channel Register Map. This mapping is common for each channel thus offset addresses from the bases in table DMA Memory Map are shown.

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Table 7-4: Internal M2P/P2M Channel Register Map

Offset	Name	Access	Bits	Reset Value
Channel Base Address + 0x0000	CONTROL	R/W	6	0
Channel Base Address + 0x0004	INTERRUPT	R/W TC *	3	0
Channel Base Address + 0x0008	PPALLOC	R/W	4	Channel dependant (see register description)
Channel Base Address + 0x000C	STATUS	RO	8	0
Channel Base Address + 0x0010	Reserved			
Channel Base Address + 0x0014	REMAIN	RO	16	0
Channel Base Address + 0x0018	Reserved			
Channel Base Address + 0x001C	Reserved			
Channel Base Address + 0x0020	MAXCNT0	R/W	16	0
Channel Base Address + 0x0024	BASE0	R/W	32	0
Channel Base Address + 0x0028	CURRENT0	RO	32	0
Channel Base Address + 0x002C	Reserved			
Channel Base Address + 0x0030	MAXCNT1	R/W	16	0
Channel Base Address + 0x0034	BASE1	R/W	32	0
Channel Base Address + 0x0038	CURRENT1	RO	32	0
Channel Base Address + 0x003C	Reserved			

Note: See Table 7-3 for Channel Base Addresses

*Note: * - write this location once to clear the interrupt (see Interrupt register description for which bits this rule applies to).*

Register Descriptions

CONTROL

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									ICE	ABORT	ENABLE	ChErrorIntEn	RSVD	NFBIntEn	STALLIntEn

Address:

Channel Base Address + 0x0000 - Read/Write

Definition:

This is the Channel Control Register, used to configure the DMA Channel.

Important Programming Note: The control register should be read immediately after being written. This action will allow hardware state machines to transition and prevent a potential problem when the registers are being written in back to back clock cycles.

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Bit Descriptions:

RSVD: Reserved. Unknown During Read.

STALLIntEn: Setting this bit to 1 enables the generation of the STALL interrupt in the STALL State of the DMA Channel State machine. Setting this bit to zero disables generation of the STALL Interrupt.

NFBIntEn: Setting this bit to 1 enables the generation of the NFB (next frame buffer) interrupt in the ON State of the DMA Channel State machine. Setting this bit to zero disables generation of the NFB Interrupt. Normally when the channel is enabled, this bit should be 1. However in the case where the current buffer is the last, then this bit can be cleared to prevent the generation of an interrupt while the DMA State machine is in the ON State.

ChErrorIntEn: Setting this bit to 1 enables the ChError Interrupt which indicates if the buffer transfer occurred with an error.

ENABLE: Setting this bit to 1 enables the channel, clearing this bit disables channel, and causes the remaining unpacker/packer data to be discarded. The channel must always be enabled before writing the Base address register.

ABORT: This bit determines how the DMA Channel State machine behaves while in the NEXT state and in receipt of a peripheral error, indicated on **RxEnd/TxEnd**. This bit is ignored when ICE is set.
0 - NEXT -> ON state, effectively ignoring the error.
1 - NEXT -> STALL state, effectively disabling the channel. No STALLInt interrupt is set for this condition.

ICE: Ignore Channel Error bit. Setting this bit results in suppression of the generation of the ChErrorInt interrupt and does not result in buffer termination. This bit may be set for data streams whereby the end user is tolerant to occasional bit errors.

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PPALLOC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												PPALLOC			

Address:

Channel Base Address + 0x0008 - Read/Write

Definition:

This is the Peripheral Port Allocation register used to configure the internal M2P channel programmability. It is possible to program a channels use on one of a number of different peripherals.

There can be 20 external peripherals - 10 Tx and 10 Rx - connected to the 20 “ports” of the DMA. The 10 internal M2P DMA channels can serve 10 of these ports at one time.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PPALLOC: The following tables give the PPALLOC decode for the port allocation for both a transmit channel and a receive channel.

Two channels cannot be programmed to serve the same port since, in the case of an erroneous software write operation, the lower channel number is given priority. For example, if software writes the value 0x01 to Channel 0 Tx PPALLOC[3:0], and also writes this same value to Channel 2 Tx PPALLOC[3:0], then the Channel 0 Tx will be configured for Port 0 and Channel 2 will not function correctly.

The PPALLOC register must be written to before a channel is enabled. If this is not done, then the default allocation of the ports will be used.

NOTE: The naming convention used for channels and ports is as follows - even numbers correspond to transmit channels/ports and odd numbers correspond to receive channels/ports.

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Table 7-5: PPALLOC Register Bits Decode for a Transmit Channel

Ch 0, 2, 4, 6, 8 PPALLOC[3:0]	Port allocated	Peripheral Allocated
0000	PORT 0	I2S1 Tx
0001	PORT 2	I2S2 Tx
0010	PORT 4	AAC1 Tx
0011	PORT 6	AAC2 Tx
0100	PORT 8	AAC3 Tx
0101	PORT 10	I2S3 Tx
0110	PORT 12	UART1 Tx
0111	PORT 14	UART2 Tx
1000	PORT 16	Reserved
1001	PORT 18	IrDA Tx
other values	not used	

Table 7-6: PPALLOC Register Bits Decode for a Receive Channel

Ch 1, 3, 5, 7, 9 PPALLOC[3:0]	Port allocated	Peripheral Allocated
0000	PORT 1	I2S1 Rx
0001	PORT 3	I2S2 Rx
0010	PORT 5	AAC1 Rx
0011	PORT 7	AAC2 Rx
0100	PORT 9	AAC3 Rx
0101	PORT 11	I2S3 Rx
0110	PORT 13	UART1 Rx
0111	PORT 15	UART2 Rx
1000	PORT 17	Reserved
1001	PORT 19	IrDA Rx
other values	not used	

Table 7-7: PPALLOC Register Reset Values

M2P Channel	PPALLOC[3:0]	Port allocated on reset
0	0000	PORT 0
1	0000	PORT 1
2	0001	PORT 2
3	0001	PORT 3
4	0010	PORT 4
5	0010	PORT 5
6	0011	PORT 6
7	0011	PORT 7
8	0100	PORT 8
9	0100	PORT 9

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INTERRUPT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												ChErrorInt	0	NFBInt	STALLInt

Address:

Channel Base Address + 0x0004 - Read/Write

Definition:

This is the interrupt status register. The register is read to obtain interrupt status for enabled interrupts. An interrupt is enabled by writing the corresponding bits in the CONTROL register.

Write this location once to clear the interrupt. (See Interrupt Register Bit Descriptions for the bits where this rule applies.)

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

STALLInt: Indicates channel has stalled. This interrupt is generated on a Channel State machine transition from ON to STALL state, if STALLIntEn set. This is a critical interrupt as it indicates that an over/underflow condition will occur as soon as the peripheral's FIFO is full/empty. The interrupt is cleared by either disabling the channel or writing a new base address which will move the state machine onto the ON state.

NFBInt: Indicates channel requires a new buffer. This interrupt generated on a Channel State machine transition from NEXT to ON state if NFBIntEn set. The interrupt is cleared by either disabling the channel or writing a new base address, which will move the state machine onto the next state.

ChErrorInt: This interrupt is activated when the peripheral attached to the DMA Channel detects an error in the data stream. The peripherals signal this error by ending the current transfer with a **TxEnd/RxEnd** error response. The interrupt is cleared by writing either a "1" or a "0" to this bit.

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STATUS

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				BYTES					NextBuffer	Current State		ChError	RSVD	NFB	STALL

Address:

Channel Base Address + 0x000C - Read Only

Definition:

This is the channel status register, which is a read-only register, used to provide status information with respect to the DMA channel.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

Stall: A “1” indicates channel is stalled and cannot currently transfer data because a base address has not been programmed. When the channel is first enabled, the Stall bit is suppressed until the first buffer has been transferred, that is, no stall interrupt generated when STALL state entered from IDLE state, only when entered from ON State. The STALL state can be cleared by writing a base address or disabling the DMA channel. The reason for channel completion can be ascertained by reading the BYTES_REMAINING register, if it is zero, the channel was stopped by the DMA Channel; if it is non-zero, the peripheral ended transfer with **TxEnd/RxEnd**. If the transfer ended with error, ChError bit/interrupt is set.

NFB: A “1” indicates the Channel FSM has moved from NEXT State to ON State. This means that the channel is currently transferring data from a DMA buffer but the next base address for the next buffer in the transfer has not been programmed, and may now be.
0 - Not in ON State, not ready for next buffer update.
1 - In ON State, ready for next buffer BASE/MAXCOUNT updates. NFB interrupt generated if not masked.

ChError: Indicates error status of buffer transfer:
0 - The last buffer transfer completed without error.
1 - The last buffer transfer terminated with an error.

BYTES: This is the number of valid DMA data currently stored by the channel in the DMA Controller in packer or unpacker. Usually used for test/debug.

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Current State: Indicates the state that the Channel FSM is currently in:
00 - IDLE
01 - STALL
10 - ON
11 - NEXT

NextBuffer: Informs the NFB service routine, after a NFB interrupt, which pair of BASEx/MAXCOUNTx registers is free for update.
0 - Update MAXCNT0/BASE0
1 - Update MAXCNT1/BASE1

The NextBuffer bit gets set to “1” when a write occurs to BASE0 and it gets set to “0” when a write occurs to BASE1. This bit alone cannot be used to determine which of the two buffers is currently being transferred to. For example, if BASE0 is written to, then NextBuffer gets set to “1” and transfers will occur using buffer0. If, during this transfer BASE1 gets written to, then NextBuffer gets set to “0”, but the current transfer will continue using buffer0 until it terminates. Then the DMA switches over to using buffer1, at which time the NFB interrupt is generated and software reads the NextBuffer status bit to determine what buffer descriptor is now free for update. In this case it is buffer0.

The NextBuffer status bit can be used in conjunction with the CurrentState status bits to determine the active buffer.

If CurrentState = DMA_ON and NextBuffer = 1 then Buffer0 is the active buffer.

If CurrentState = DMA_ON and NextBuffer = 0 then Buffer1 is the active buffer.

If CurrentState = DMA_NEXT and NextBuffer = 0 then Buffer0 is the active buffer.

If CurrentState = DMA_NEXT and NextBuffer =1 then Buffer1 is the active buffer.

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REMAIN

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
REMAIN															

Address:

Channel Base Address + 0x0014 - Read Only

Definition:

The Channel Bytes Remaining Register contains the number of bytes remaining in the current DMA transfer. Only the lower 16 bits are valid

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

REMAIN: Loaded from the Channel MAXCNT register when the DMA Channel State Machine enters the ON State. Although there are 2 Data transfer states, ON and NEXT, this register need only be assigned in the ON state, because in this state the next buffer to be used is determined (there is only one) and this MAXCNT value is assigned to REMAIN. The DMA State Machine counts down by one byte every time a byte is transferred between the DMA Controller and the Peripheral. When this register reaches zero, the current buffer transfer is complete and the **TxTC/RxTC** are generated and used to indicate this to the peripheral. DMA transfers may also be stopped with the **TxEnd/RxEnd** signals from the peripheral, where the REMAIN register is non-zero at the end of transfer, allowing software to determine the last valid data in a buffer.

MAXCNTx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAXCNTx															

Address:

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MAXCNT0: Channel Base Address + 0x0020 - Read/Write
MAXCNT1: Channel Base Address + 0x0030 - Read/Write

Definition:

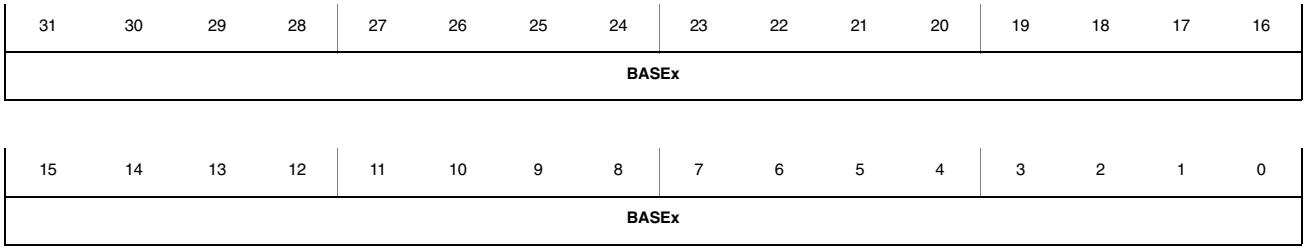
x = “0” or “1”. Maximum byte count for the buffer. Represents the double buffer per channel. Only the low order 16 bits are used. Each MAXCNTx register must be programmed before it’s corresponding BASEx register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

MAXCNTx: Maximum byte count for the buffer.

BASEx



Address:

BASE0: Channel Base Address + 0x0024 - Read/Write
BASE1: Channel Base Address + 0x0034 - Read/Write

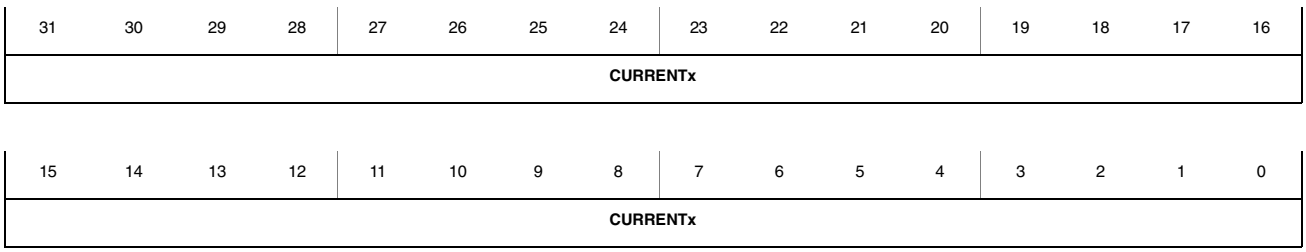
Definition:

Base address for the current and next DMA transfer.

Bit Descriptions:

BASEx: x = “0” or “1”. Base address for the current and next DMA transfer. Loaded with start address after enabling the DMA Channel, the latter event required to take the Channel State machine into the STALL state, the former event required to enter the ON State.

CURRENTx



Address:

CURRENT0: Channel Base Address + 0x0028 - Read Only
CURRENT1: Channel Base Address + 0x0038 - Read Only

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Definition:

This is the Channel Current Address Register.

Bit Descriptions:

CURRENTx: Returns the current value of the channel address pointer. Upon enabling the DMA Channel and writing the BASE Address Register the contents of this register is loaded into the CURRENTx register and the x buffer becomes active. Following completion of a transfer from a buffer, the post-incremented address is stored in this register so that a software service routine can detect the point in the buffer at which transfer was terminated.

M2M Channel Register Map

The DMA Memory Map defines the mapping for the channel registers for each of the 2 M2M channels that are shown in Table 7-8, the M2M Channel Register Map. This mapping is common for each channel thus offset addresses are shown.

Note that M2M Channel 0 is dedicated to servicing External Peripheral 0, and M2M Channel 1 is dedicated to servicing External Peripheral 1 (when in external peripheral transfer mode).

Table 7-8: M2M Channel Register Map

Offset	Name	Access	Bits	Reset Value
Channel Base Address + 0x0000	CONTROL	R/W	32	0
Channel Base Address + 0x0004	INTERRUPT	R/W TC*	3	0
Channel Base Address + 0x0008	Reserved			
Channel Base Address + 0x000C	STATUS	R/W TC*	14	0
Channel Base Address + 0x0010	BCR0	R/W	16	0
Channel Base Address + 0x0014	BCR1	R/W	16	0
Channel Base Address + 0x0018	SAR_BASE0	R/W	32	0
Channel Base Address + 0x001C	SAR_BASE1	R/W	32	0
Channel Base Address + 0x0020	Reserved			
Channel Base Address + 0x0024	SAR_CURRENT0	RO	32	0
Channel Base Address + 0x0028	SAR_CURRENT1	RO	32	0
Channel Base Address + 0x002C	DAR_BASE0	R/W	32	0
Channel Base Address + 0x0030	DAR_BASE1	R/W	32	0
Channel Base Address + 0x0034	DAR_CURRENT0	RO	32	0
Channel Base Address + 0x0038	Reserved			
Channel Base Address + 0x003C	DAR_CURRENT1	RO	32	0

Note: See Table 7-3 for Channel Base Addresses

*Note: * Write this location once to clear the bit (see Interrupt/Status register description for which bits this rule applies to).*

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CONTROL

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
PWSC							NO_HDSK	RSS		NFBintEn	DREQP		RSVD	DACKP	ETDP

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ETDP	TM		SAH	DAH	PW		BWC				START	ENABLE	DONEIntEn	SCT	STALLIntEn

Address:

Channel Base Address + 0x0000 - Read/Write

Definition:

This is the Channel Control Register. Used to configure the DMA M2M Channel. All control bits should be programmed before the ENABLE bit is set.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

STALLIntEn: Setting this bit to “1” enables the generation of the STALL interrupt in the STALL State of the DMA Channel State machine. Setting this bit to “0” disables generation of the STALL Interrupt.

SCT: Source Copy Transfer. This bit is used to set up a block transfer from 1 memory source location. If SCT = 1, then one word is read from the source memory location and copied to a block of memory (the number of destination locations written to is determined by BCR). If SCT = 0 then the source address increments as normal after each successful transfer as determined by the transfer size (this is the default setting). In order to use this feature the SAR_BASEx and DAR_BASEx registers must contain word-aligned addresses - the DMA will ignore the 2 LSB’s of the source and destination addresses to avoid any problems in the case where software erroneously programs a byte-aligned address. The SCT bit is used only when in M2M software-triggered transfer mode.

DoneIntEn: Setting this bit to “1” enables the generation of the DONE Interrupt which indicates if the transfer completed successfully.

ENABLE: Setting this bit to 1 enables the channel, clearing this bit disables the channel. The channel must always be enabled after writing the Source/Destination Base address registers and the BCR register. When a channel is disabled, the external peripheral signals will be placed in their inactive state.

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START: Start Transfer. When this bit is set, the DMA begins M2M transfer in accordance with the values in the control registers. START is cleared automatically after one clock cycle and is always read as a logic 0. This bit, in effect, provides a “Software-triggered DMA capability”. A channel must be configured and enabled before setting the START bit. This bit is not used for external M2P/P2M transfers, or for SSP transfers. For a double-buffer software triggered DMA transfer, the START bit need only be set once, that is, at the very beginning of transfer. It is sufficient for software to program the ‘other’ buffer descriptor only, in order to guarantee rollover to the second buffer when the byte count of the first buffer has been reached.

BWC: Bandwidth Control. These 4 bits are used to indicate the number of bytes in a block transfer. When the BCR register value is within 15 bytes of a multiple of the BWC value, the DMA releases the bus by negating the AHB bus request strobe allowing lower priority masters to be granted control of the bus. BWC = 0000 specifies the maximum transfer rate: other values specify a transfer rate limit.

The BWC bits should only be set for software triggered M2M transfers, where **HREQ** stays asserted throughout the transfer. For transfer to/from external peripherals **HREQ** is released after every transfer, and so bandwidth control is not needed.

The BWC bits are ignored when in external M2P/P2M transfer mode.

Example: if BWC = 1010b (indicating 1024 bytes, see Table 7-9, below), the DMA relinquishes control of the bus on completion of the current burst transfer after BCR values which are within 15 bytes of multiples of 1024.

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Table 7-9: BWC Decode Values

BWC	Bytes
0000	Full DMA transfer completes
0001	16
0010	16
0011	16
0100	16
0101	32
0110	64
0111	128
1000	256
1001	512
1010	1024
1011	2048
1100	4096
1101	8192
1110	16384
1111	32768

PW: Peripheral Width. For external M2P/P2M transfers, these bits are used to program the DMA to request byte/halfword/word wide AHB transfers, depending on the width of the external peripheral. These bits are not used for software triggered M2M transfers.

00 - Byte (8 bits)
01 - Halfword (16 bits)
10 - Word (32 bits)
11 - Not used

For word accesses the lower 2 bits of the source/destination address are ignored.

For halfword accesses the lower bit of the source/destination address is ignored.

DAH: Destination Address Hold - This bit is used for external M2P transfers where the external memory destination is a memory-mapped FIFO-based peripheral (with one address location) or for internal peripheral transfers (M2P) to the peripheral's FIFO buffer.
1 - Hold the destination address throughout the transfer (do not increment).
0 - Increment the destination address after each transfer in the transaction.

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SAH: Source Address Hold - This bit is used for external P2M transfers where the external memory source is a memory-mapped FIFO-based peripheral (with one address location) or for internal peripheral transfers (P2M) to the peripheral's FIFO buffer.
1 - Hold the source address throughout the transfer (do not increment).
0 - Increment the source address after each transfer in the transaction.

TM: Transfer Mode:
00 - Software initiated M2M transfer.
01 - Hardware initiated external M2P transfer, that is, transfer from memory to external peripheral or to SSP.
10 - Hardware initiated external P2M transfer, that is, transfer from external peripheral (or SSP) to memory.
11 - Not used.

ETDP: End-of-Transfer/Terminal Count pin Direction & Polarity:
00 - The **DEOT/TC** pin is programmed as an active low end-of-transfer input.
01 - The **DEOT/TC** pin is programmed as an active high end-of-transfer input.
10 - The **DEOT/TC** pin is programmed as an active low terminal count output.
11 - The **DEOT/TC** pin is programmed as an active high terminal count output.

DACKP: DMA Acknowledge pin Polarity:
0 - **DACK** is active low.
1 - **DACK** is active high.

DREQP: DMA Request pin Polarity. These bits must be set before the channels ENABLE bit is set. Otherwise the reset value, "00", will cause the DMA to look for an active low, level sensitive **DREQ**.
00 - **DREQ** is active low, level sensitive.
01 - **DREQ** is active high, level sensitive.
10 - **DREQ** is active low, edge sensitive.
11 - **DREQ** is active high, edge sensitive.

NFBIntEn: Setting this bit to "1" enables the generation of the NFB interrupt in the DMA_BUF_ON state of the DMA channel buffer state machine. Setting this bit to zero disables generation of the NFB Interrupt. Normally when the channel is enabled, this bit should be 1. However in the case where the current buffer is the last, then this bit can be cleared to prevent the generation of an interrupt while the DMA State machine is in the DMA_BUF_ON state.

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RSS: Request Source Selection.
00 - External DReq.
01 - Internal SSPRx.
10 - Internal SSPTx.
11 - Reserved.

NO_HDSK: When set, the peripheral doesn't require the regular handshake protocol. This is optional for external peripherals, but this bit needs to be set for SSP operations. Setting this bit will imply the use of a wait state counter that will mask hardware requests after each DMA write.

PWSC: Peripheral Wait States Count. Gives the latency (in HCLK cycles) needed by the peripheral to de-assert its request line once the M2M transfer is finished.During this latency period, the DMA channel will not consider any request. This wait state count is triggered after each peripheral width transfer, right after the DMA write phase.In the case of internal peripherals, this means that the count will start when the DMA has had confirmation from AHB that the write is accepted and done. In the case of an external peripheral that doesn't use a handshaking protocol, the count will start when the DMA has received the acknowledge of the write from the SMC.If the acknowledge from the SMC takes too long to arrive, the processor can still cancel the counter stall by writing the CONTROL register.

INTERRUPT

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													NFBint	DONEInt	STALLInt

Address:

Channel Base Address + 0x0004 - Read/Write

Definition:

This is the interrupt status register. The register is read to obtain interrupt status for enabled interrupts. An interrupt is enabled by writing the corresponding bits in the CONTROL register.

Write this location once to clear the interrupt. (See the Interrupt Register Bit Descriptions for the bits where this applies.)

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Bit Descriptions:

RSVD: Reserved. Unknown During Read.

STALLInt: Indicates channel has stalled. This interrupt is generated on a Channel State machine transition from MEM_RD (memory read) or MEM_WR (memory write) to the STALL state, assuming STALLIntEn set. The interrupt is cleared by either disabling the channel or by triggering a new transfer.

DONEInt: Transaction is done. When enabled, this interrupt is set when all DMA controller transactions complete normally, as determined by the transfer count/external peripheral **DEOT** signal. When a transfer completes, software must clear the DONE bit before reprogramming the DMA, by writing either a “0” or “1” to this bit. This must be done even if the DMA interrupt is disabled. The DMA will ignore any additional DREQs that it receives from the external peripheral (if operating in external peripheral mode) until the software clears the DONE interrupt and reprograms the DMA with new BCRx values.

NFBInt: Indicates that a channels buffer descriptor is free for update. This interrupt is generated if NFBIntEn is set, when a transfer begins using the second buffer of the double-buffer set, thus informing software that it can now set up the other buffer. The interrupt is cleared by either disabling the channel or writing a new BCR value to set up a new buffer descriptor. The interrupt is not generated for a single-buffer transfer. In software triggered M2M mode, servicing of the NFB interrupt is dependent on the system level AHB arbitration since the DMA’s **HREQ** (AHB request) may be continuously held high.

STATUS

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD		DREQS	NB	NFB	EOTS		TCS		DONE	CurrentState					STALL

Address:

Channel Base Address + 0x000C - Read/Write

Definition:

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This is the channel status register, used to provide status information with respect to the DMA channel. All register bits are read-only except for the DREQS status bit which can be cleared by a write (either a “0” or a “1”) to this register.

Write this location once to clear the interrupt (see Interrupt Register Bit Descriptions for which bits this rule applies to).

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

Stall: A “1” indicates channel is stalled and cannot currently transfer data because the START bit has not been programmed or an external peripheral has not asserted **DREQ**. When the channel is first enabled, the Stall bit is suppressed until the first buffer has been transferred, that is, no stall interrupt generated when STALL state entered from IDLE state, only when entered from MEM_WR State. The STALL state can be cleared by:

- Setting the START bit
- An external peripheral requesting service (depending on transfer mode)
- Disabling the DMA channel
- A request from SSP

CurrentState: Indicates the states that the M2M Channel Control FSM and M2M Buffer FSM are currently in:

CurrentState[2:0] - These indicate the state of M2M Channel Control FSM:
000 - DMA_IDLE
001 - DMA_STALL
010 - DMA_MEM_RD
011 - DMA_MEM_WR
100 - DMA_BWC_WAIT

CurrentState[4:3] - These indicate the state of M2M Buffer FSM:
00 - DMA_NO_BUF
01 - DMA_BUF_ON
10 - DMA_BUF_NEXT

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DONE: Transfer completed successfully. The transfer is terminated on the occurrence of DEOT being asserted by the peripheral or the byte count expiring, whichever happens sooner. When a transfer completes, software must clear the Interrupt.DONEInt bit before reprogramming the DMA, by writing either “0” or “1” to this bit. The DMA will ignore any more **DREQ**s that it receives from the external peripheral (if operating in external peripheral mode) until such time that software clears the DONE interrupt and reprograms the DMA with new BCRx values, and this even if the DMA interrupt is disabled.

TCS: Terminal Count status. This status bit reflects whether or not the actual byte count has reached the programmed limit for buffer descriptor “0” or “1” respectively:
00 - Terminal Count has not been reached for either buffer descriptor 1 or 0.
01 - Terminal Count has not been reached for buffer 1 and has been reached for buffer descriptor 0.
10 - Terminal Count has been reached for buffer 1 and has not been reached for buffer descriptor 0.
11 - Terminal Count has been reached for both buffer descriptors.

The TCS status bit for a buffer descriptor is cleared when the BCR register of that buffer descriptor has been programmed with a new value.

EOTS: End-Of-Transfer status (valid only if the **DEOT/TC** pin has been programmed for the DEOT function, that is, the control reg bit ETDP[1] = 0) for buffer descriptor 1 or 0 respectively.

00 - End of transfer has not been requested by external peripheral for either buffer descriptor.
01 - End of transfer has been requested by external peripheral for buffer descriptor 0 only.
10 - End of transfer has been requested by external peripheral for buffer descriptor 1 only.
11 - End of transfer has been requested by external peripheral for both buffer descriptors.

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NFB: A “1” indicates that the channel is currently transferring data from a DMA buffer but the next byte count register for the next buffer in the transfer has not been programmed, and may now be programmed. This interrupt is generated when the DMA buffer state machine moves from the DMA_BUF_NEXT state to the DMA_BUF_ON state, that is, when transfer begins using the second buffer of the double buffer pair. Thus for a double-buffer transfer both BCR registers must be programmed once before the NFB status bit can be used to determine when the next BCR register should be programmed.
0 - Not ready for next buffer update.
1 - Ready for next buffer updates. NFB interrupt generated if not masked.

NB: NextBuffer status bit - Informs the NFB service routine, after a NFB interrupt, which pair of SAR_BASEx/DAR_BASEx/BCRx registers is free for update.
0 - Update SAR_BASE0/DAR_BASE0/BCR0
1 - Update SAR_BASE1/DAR_BASE1/BCR1

The NextBuffer bit gets set to “1” when a write occurs to BCR0 and it gets set to “0” when a write occurs to BCR1. This bit alone cannot be used to determine which of the two buffers is currently being transferred to - for example if BCR0 is written, then NextBuffer gets set to “1” and transfers will occur using buffer0. If, during this transfer BCR1 gets written, then NextBuffer gets set to “0”, but the current transfer will continue using buffer0 until it terminates. Then the DMA switches over to using buffer1 at which time the NFB interrupt is generated and software reads the NextBuffer status bit to determine what buffer descriptor is now free for update - in this case it is buffer0.

The NextBuffer status bit can be used in conjunction with the CurrentState status bits to determine the active buffer according to the following rules:

If CurrentState[4:3] = DMA_BUF_ON and NextBuffer = 1

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then Buffer0 is the active buffer.

If CurrentState[4:3] = DMA_BUF_ON and NextBuffer = 0 then Buffer1 is the active buffer.

If CurrentState[4:3] = DMA_BUF_NEXT and NextBuffer = 0 then Buffer0 is the active buffer.

If CurrentState[4:3] = DMA_BUF_NEXT and NextBuffer =1 then Buffer1 is the active buffer.

DREQS: **DREQ** Status - This bit reflects the status of the synchronized external peripherals DMA Request signal or SSP requests:
0 - No external peripheral DMA request is pending or, in the case of a transfer without handshaking, the request is not validated yet, the wait state counter is running.
1 - An external peripheral DMA request or a validated SSP or external peripheral without handshaking request is pending.

DREQS can be polled by software at any time. It can, for example, be used to determine whether or not the DMA needs to be set up for a transfer when the DMA is in the STALL state and is receiving DREQs, but the BCRx registers have not been programmed. It is important to notice that, in the case of a transfer without handshaking (external peripheral or SSP), DREQS might be clear if a request is pending but is not validated as a result of a wait state counter still running.

When the channel STATUS register is written with any 32-bit value, this will cause the DREQS bit of the STATUS register to be cleared. A write to the STATUS register only affects the DREQS bit. If an edge is detected on **DREQ** when no previous request is still pending in the DMA (that is, DREQS clear), then the DREQS bit is set by the DMA to indicate that the external peripheral has requested service. The STATUS register is written by software to clear the DREQS status bit, thus causing the DMA to ignore the request.

For level-sensitive **DREQ** mode, do not attempt to clear the DREQS status bit, as the request will keep coming from the external peripheral. The hardware ensures that a write to the STATUS register has no effect when in level-sensitive mode.

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BCRx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
BCRx															

Address:

BCR0: Channel Base Address + 0x0010 - Read/Write
BCR1: Channel Base Address + 0x0014 - Read/Write

Definition:

The Channel Bytes Count Register contains the number of bytes yet to be transferred for a given block of data in a M2M transfer. Only the lower 16 bits are valid.

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Bit Descriptions:

RSVD: Reserved. Unknown During Read.

BCRx: x = “0” or “1” representing the double buffer per channel. The BCR register must be loaded with the number of byte transfers to occur. It decrements on the successful completion of the address transfer during the write-to-memory state of the M2M transfer. At least 1 of the BCRx registers must be programmed to a non-zero value before the ENABLE bit and the START bit (in the case of software-trigger M2M mode) are set in the Control register. Writing to a BCRx register causes a next buffer update, that is, only the BCR of the buffer descriptor has to be written to in order to use that buffer since the SAR_BASEx and DAR_BASEx registers do not have to be continuously updated.

For a double/multiple buffer transfer, the second buffer descriptor can be programmed while the transfer using the first buffer is being carried out (thus reducing software latency impact). The NFB interrupt is generated when transfer begins using the second buffer. The NFB interrupt service routine can then be used to update the free buffer descriptor (in the case where a third buffer is required).

If BCRx = 0 when the transfer is triggered, then NO transfers will occur, that is, the DMA will stay in the STALL state.

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SAR_BASEx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SAR_BASEx															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SAR_BASEx															

Address:

SAR_BASE0: Channel Base Address + 0x0018 - Read/Write
SAR_BASE1: Channel Base Address + 0x001C - Read/Write

Definition:

This register contains the base memory address from which the DMA controller requests data.

Bit Descriptions:

SAR_BASEx: x = “0” or “1” representing the double buffer per channel. This register contains the base memory address from which the DMA controller requests data. At least 1 of the SAR_BASEx registers must be programmed before the ENABLE bit and the START bit (in the case of software-trigger M2M mode) are set in the Control register, and also before the corresponding BCRx register is programmed. The second buffer descriptor can be programmed while the transfer using the “other” buffer is being carried out (thus reducing software latency impact). When transferring from external peripheral to memory, the SAR_BASEx will contain the base address of the memory mapped peripheral.

DAR_BASEx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAR_BASEx															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAR_BASEx															

Address:

DAR_BASE0: Channel Base Address + 0x002C- Read/Write
DAR_BASE1: Channel Base Address + 0x0030 - Read/Write

Definition:

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This register contains the base memory address to which the DMA controller transfers data.

Bit Descriptions:

DAR_BASEx: x = 0 or 1 representing the double buffer per channel. This register contains the base memory address to which the DMA controller sends data. At least 1 of the DAR_BASEx registers must be programmed before the ENABLE bit and the START bit (in the case of software trigger M2M mode) are set in the Control register, and also before the corresponding BCRx register is programmed. The second buffer descriptor can be programmed while the transfer using the 'other' buffer is being carried out (thus reducing software latency impact). When transferring from memory to external peripheral, the DAR_BASEx will contain the base address of the memory mapped peripheral.

7 SAR_CURRENTx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SAR_CURRENTx															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SAR_CURRENTx															

Address:

SAR_CURRENT0: Channel Base Address + 0x0024 - Read Only
SAR_CURRENT1: Channel Base Address + 0x0028 - Read Only

Definition:

This is the Channel Current Source Address Register.

Bit Descriptions:

SAR_CURRENTx: Returns the current value of the channel source address pointer. Upon writing the BCRx register, the contents of the SAR_BASEx register is loaded into the SAR_CURRENTx register and the x buffer becomes active. Following completion of a transfer from a buffer, the post-incremented address is stored in this register so that a software service routine can detect the point in the buffer at which transfer was terminated.

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DAR_CURRENTx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DAR_CURRENTx															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DAR_CURRENTx															

Address:

DAR_CURRENT0: Channel Base Address + 0x0044 - Read Only
DAR_CURRENT1: Channel Base Address + 0x003C - Read Only

Definition:

This is the Channel Current Destination Address Register.

Bit Descriptions:

DAR_CURRENTx: Returns the current value of the channel destination address pointer. Upon writing the BCRx register the contents of the DAR_BASEx register is loaded into the DAR_CURRENTx register and the x buffer becomes active. Following completion of a transfer from a buffer, the post-incremented address is stored in this register so that a software service routine can detect the point in the buffer at which transfer was terminated.

DMAGIInt

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Address:

0x8000_03C0 - Read/Write

Definition:

DMA Global Interrupt Register. This register indicates which channels have an active interrupt. It is a read only register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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D0 - D1: These interrupts are per channel interrupts, as shown in Table 7-10. Each bit is a logical OR of the INTERRUPT register per channel. There are no dedicated storage of these channel interrupts. Once each Channel's Interrupts' are clear, the associated channel interrupt is clear.

Note: The order of the internal M2P channel interrupts is for compatibility reasons with previous versions of software.

Table 7-10: DMA Global Interrupt (DMAGIInt) Register

Bit No.	Description
D[31:12]	RSVD
D11	M2M Channel 1 Interrupt
D10	M2M Channel 0 Interrupt
D9	M2P Channel 8 Interrupt
D8	M2P Channel 9 Interrupt
D7	M2P Channel 6 Interrupt
D6	M2P Channel 7 Interrupt
D5	M2P Channel 4 Interrupt
D4	M2P Channel 5 Interrupt
D3	M2P Channel 2 Interrupt
D2	M2P Channel 3 Interrupt
D1	M2P Channel 0 Interrupt
D0	M2P Channel 1 Interrupt

DMAChArb

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															CHARB

Address:

0x8000_0380 - Read/Write

Definition:

DMA Channel Arbitration Register. This bit controls the DMA channel arbitration.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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CHARB: This bit controls DMA channel arbitration. It is reset to “0”, thus giving a default setting of internal Memory-to-Peripheral channels having a higher priority than Memory-to-Memory channels. This bit can be set to “1” to reverse the default order, that is, giving M2M transfers a higher priority than internal M2P.

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Chapter 8

Universal Serial Bus Host Controller

8.1 Introduction

The EP9301 Universal Serial Bus (USB) Host Controller enables communication to USB 2.0 low-speed (1.2 Mbps) and full-speed (12 Mbps) devices. The controller supports two root hub ports and complies with the Open Host Controller Interface (OpenHCI) specification, version 1.0a. (For additional information, see “Reference Documents”, item 9, on page 5.)

8.1.1 Features

The features of the USB Host Controller are:

- Open Host Controller Interface Specification (OpenHCI) Rev 1.0 compliant.
- Universal Serial Bus Specification Rev. 2.0 compliant.
- Support for both low speed and full speed USB devices.
- Root Hub has two downstream ports
- Master and Slave AHB interfaces
- USB Host test register block for test and software use.
- DMA functionality

The USB Host Controller is partitioned into the key sub blocks as indicated in Figure 8-7.

8.2 Overview

Figure 8-1 shows four main focus areas of a USB system. These areas are:

- Client Software/USB Driver
- Host Controller Driver (HCD)
- Host Controller (HC)
- USB Device.

The Client Software/USB Device and Host Controller Driver are implemented in software. The Host Controller and USB Device are implemented in

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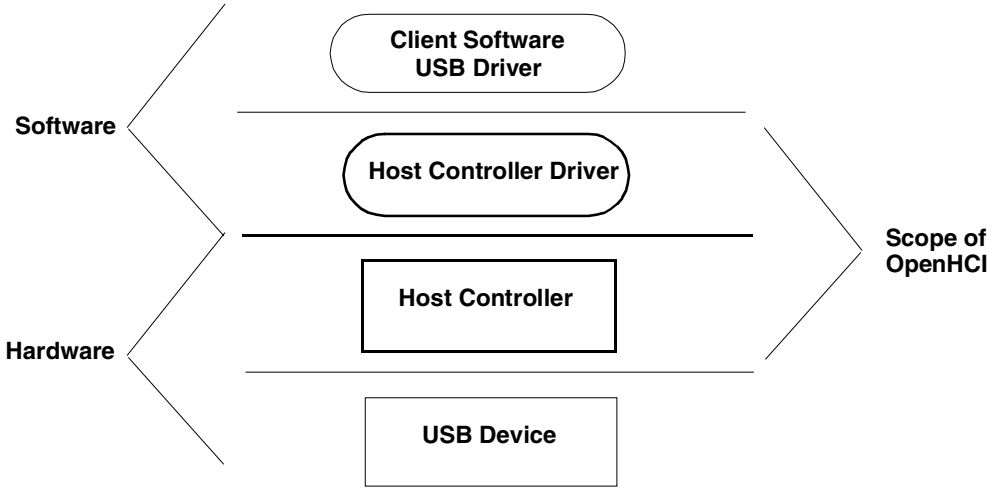
hardware. OpenHCI specifies the interface between the Host Controller Driver and the Host Controller and describes the fundamental operation of each.

Figure 8-1. USB Focus Areas



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The Host Controller Driver and Host Controller work in tandem to transfer data between client software and a USB device. Data is translated from shared-memory data structures at the client software end to USB signal protocols at the USB device end, and vice-versa.

8.2.1 Data Transfer Types

There are four data transfer types defined in USB. Each type is optimized to match the service requirements between the client software and the USB device. The four types are:

- Interrupt Transfers - Small data transfers used to communicate information from the USB device to the client software. The Host Controller Driver polls the USB device by issuing tokens to the device at a periodic interval sufficient for the requirements of the device.
- Isochronous Transfers - Periodic data transfers with a constant data rate. Data transfers are correlated in time between the sender and receiver.
- Control Transfers - Nonperiodic data transfers used to communicate configuration/command/status type information between client software and the USB device.
- Bulk Transfers - Nonperiodic data transfers used to communicate large amounts of information between client software and the USB device.

In OpenHCI the data transfer types are classified into two categories: periodic and nonperiodic. Periodic transfers are interrupt and isochronous since they are scheduled to run at periodic intervals. Nonperiodic transfers are control

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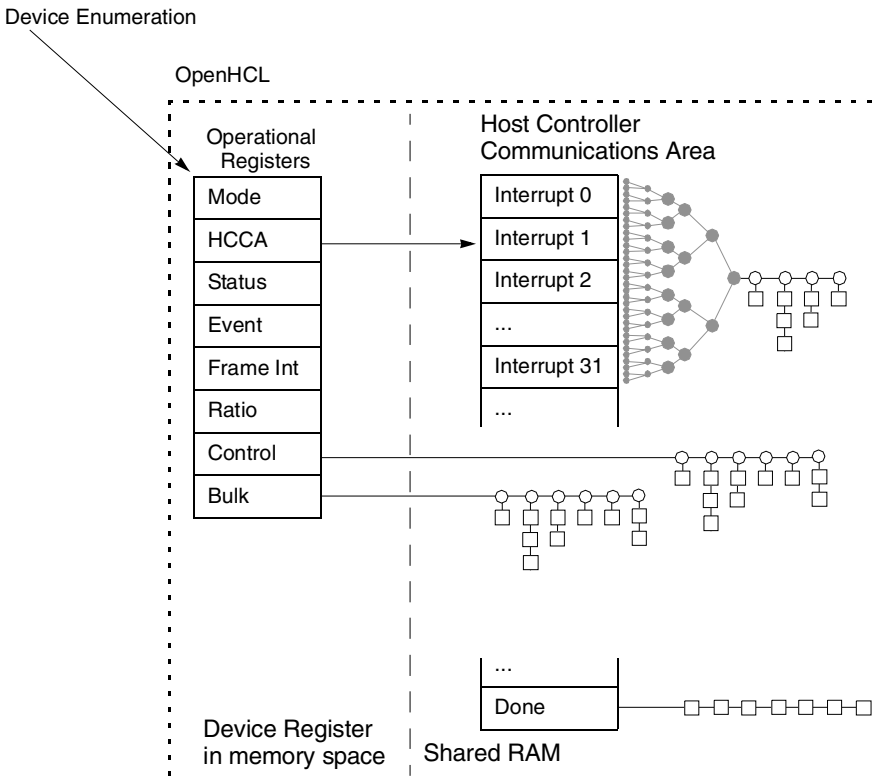
and bulk since they are not scheduled to run at any specific time, but rather on a time-available basis.

8.2.2 Host Controller Interface

8.2.2.1 Communication Channels

There are two communication channels between the Host Controller and the Host Controller Driver. The first channel uses a set of operational registers located on the HC. The Host Controller is the target for all communication on this channel. The operational registers contain control, status, and list pointer registers. Within the operational register set is a pointer to a location in shared memory named the Host Controller Communications Area (HCCA). The HCCA is the second communication channel. The Host Controller is the master for all communication on this channel. The HCCA contains the head pointers to the interrupt Endpoint Descriptor lists, the head pointer to the done queue, and status information associated with start-of-frame processing. Figure 8-2 on page 265 shows the communication channels.

Figure 8-2. Communication Channels



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8.2.2.2 Data Structures

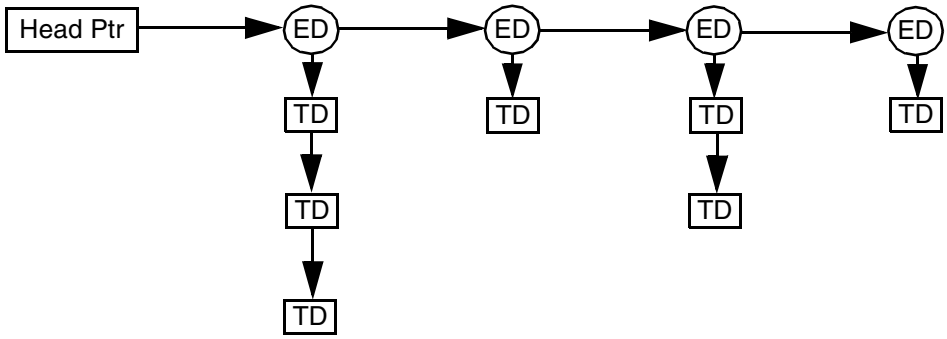
The basic building blocks for communication across the interface are the Endpoint Descriptor (ED) and Transfer Descriptor (TD).

The Host Controller Driver assigns an Endpoint Descriptor to each endpoint in the system. The Endpoint Descriptor contains the information necessary for the Host Controller to communicate with the endpoint. The fields include the maximum packet size, the endpoint address, the speed of the endpoint, and the direction of data flow. Endpoint Descriptors are linked in a list.

A queue of Transfer Descriptors is linked to the Endpoint Descriptor for the specific endpoint. The Transfer Descriptor contains the information necessary to describe the data packets to be transferred. The fields include data toggle information, shared memory buffer location, and completion status codes. Each Transfer Descriptor contains information that describes one or more data packets. The data buffer for each Transfer Descriptor ranges in size from 0 to 8192 bytes with a maximum of one physical page crossing. Transfer Descriptors are linked in a queue: the first one queued is the first one processed.

Each data transfer type has its own linked list of Endpoint Descriptors to be processed. Figure 8-3, Typical List Structure, is a representation of the data structure relationships.

Figure 8-3. Typical List Structure



The head pointers to the bulk and control Endpoint Descriptor lists are maintained within the operational registers in the HC. The Host Controller Driver initializes these pointers prior to the Host Controller gaining access to them. Should these pointers need to be updated, the Host Controller Driver may need to halt the Host Controller from processing the specific list, update the pointer, then re-enable the HC.

The head pointers to the interrupt Endpoint Descriptor lists are maintained within the HCCA. There is no separate head pointer for isochronous transfers. The first isochronous Endpoint Descriptor simply links to the last interrupt Endpoint Descriptor. There are 32 interrupt head pointers. The head pointer

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used for a particular frame is determined by using the last 5 bits of the Frame Counter as an offset into the interrupt array within the HCCA.

The interrupt Endpoint Descriptors are organized into a tree structure with the head pointers being the leaf nodes. The desired polling rate of an Interrupt Endpoint is achieved by scheduling the Endpoint Descriptor at the appropriate depth in the tree. The higher the polling rate, the closer to the root of the tree the Endpoint Descriptor will be placed since multiple lists will converge on it. Figure 8-4 illustrates the structure for Interrupt Endpoints. The Interrupt Endpoint Descriptor Placeholder indicates where zero or more Endpoint Descriptors may be enqueued. The numbers on the left are the index into the HCCA interrupt head pointer array.

Figure 8-4. Interrupt Endpoint Descriptor Structure

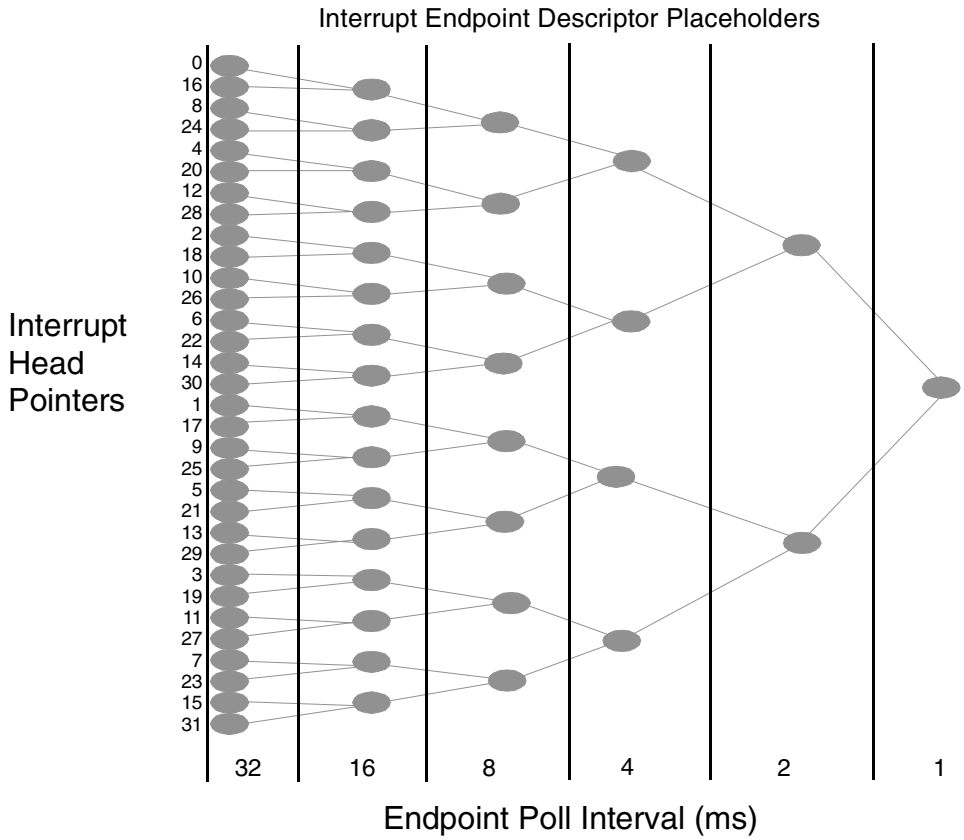

Figure 8-5 is a sample Interrupt Endpoint schedule. The schedule shows two Endpoint Descriptors at a 1 ms poll interval, two Endpoint Descriptors at a 2 ms poll interval, one Endpoint at a 4 ms poll interval, two Endpoint Descriptors at an 8 ms poll interval, two Endpoint Descriptors at a 16 ms poll interval, and two Endpoint Descriptors at a 32 ms poll interval. Note that in this example unused Interrupt Endpoint Placeholders are bypassed and the link is connected to the next available Endpoint in the hierarchy.

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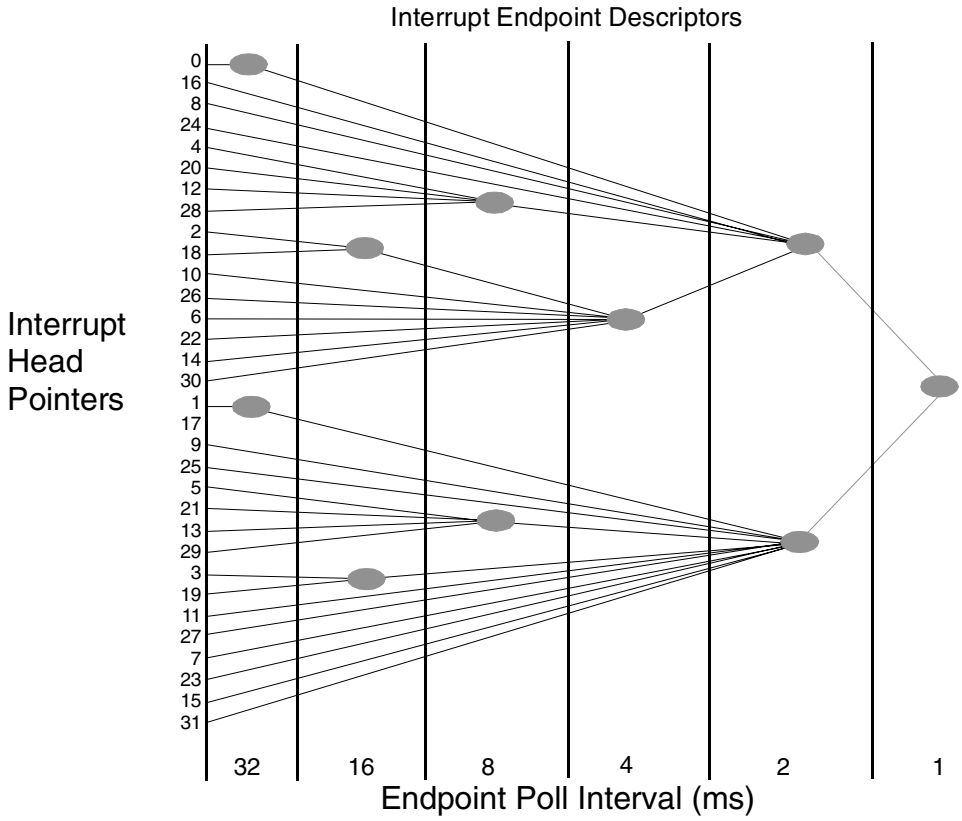
Figure 8-5. Sample Interrupt Endpoint Schedule



8

8.2.3 Host Controller Driver Responsibilities

This section summarizes the Host Controller Driver (HCD) responsibilities.

8.2.3.1 Host Controller Management

The Host Controller Driver manages the operation of the Host Controller (HC). It does so by communicating directly to the operational registers in the Host Controller and establishing the interrupt Endpoint Descriptor list head pointers in the HCCA.

The Host Controller Driver maintains the state of the HC, list processing pointers, list processing enables, and interrupt enables.

8.2.3.2 Bandwidth Allocation

All access to the USB is scheduled by the Host Controller Driver. The Host Controller Driver allocates a portion of the available bandwidth to each periodic endpoint. If sufficient bandwidth is not available, a newly-connected periodic endpoint will be denied access to the bus.

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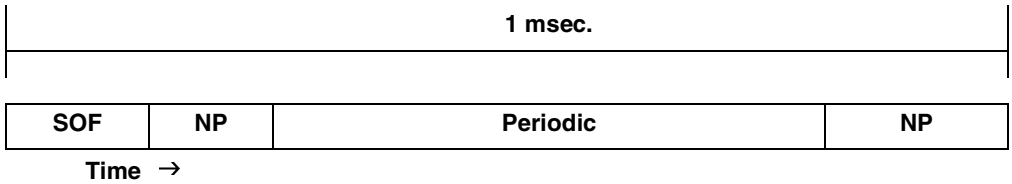
A portion of the bandwidth is reserved for nonperiodic transfers. This ensures that some amount of bulk and control transfers will occur in each frame period. The frame period is defined for USB to be 1.0 ms.

The bandwidth allocation policy for OpenHCI is shown in Figure 8-6. Each frame begins with the Host Controller sending the Start of Frame (SOF) synchronization packet to the USB bus. This is followed by the Host Controller servicing nonperiodic transfers until the frame interval counter reaches the value set by the Host Controller Driver, indicating that the Host Controller should begin servicing periodic transfers. After the periodic transfers complete, any remaining time in the frame is consumed by servicing nonperiodic transfers once more.

Figure 8-6. Frame Bandwidth Allocation



8.2.3.3 List Management

The transport mechanism for USB data packets is via Transfer Descriptor queues linked to Endpoint Descriptor lists. The Host Controller Driver creates these data structures then passes control to the Host Controller for processing.

The Host Controller Driver is responsible for enqueuing and dequeuing Endpoint Descriptors. Enqueuing is done by adding the Endpoint Descriptor to the tail of the appropriate list. This may occur simultaneously with the Host Controller processing the list without requiring any lock mechanism. Before dequeuing an Endpoint Descriptor, the Host Controller Driver may disable the Host Controller from processing the entire Endpoint Descriptor list of the data type being removed to ensure that the Host Controller is not accessing the Endpoint Descriptor.

The Host Controller Driver is also responsible for enqueuing Transfer Descriptors to the

appropriate Endpoint Descriptor. Enqueuing is done by adding the Transfer Descriptor to the tail of the appropriate queue. This may occur simultaneously to the Host Controller processing the queue without requiring any lock mechanism. Under normal operation, the Host Controller dequeues the Transfer Descriptor. However, the Host Controller Driver dequeues the Transfer Descriptor when the Transfer Descriptor is being canceled due to a request from the client software or certain error conditions. In this instance, the Endpoint Descriptor is disabled prior to the Transfer Descriptor being dequeued.

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8.2.3.4 Root Hub

The Root Hub is integrated into the HC. The internal registers of the Root Hub are exposed to the Host Controller Driver which is responsible for providing the proper hub-class protocol with the USB Driver and proper control of the Root Hub.

8.2.4 Host Controller Responsibilities

This section summarizes the Host Controller (HC) responsibilities.

8.2.4.1 USB States

There are four USB states defined in OpenHCI: *UsbOperational, UsbReset, UsbSuspend,* and *UsbResume*. The Host Controller puts the USB bus in the proper operating mode for each state.

8.2.4.2 Frame management

The Host Controller keeps track of the current frame counter and the frame period. At the beginning of each frame, the Host Controller generates the Start of Frame (SOF) packet on the USB bus and updates the frame count value in system memory. The Host Controller also determines if enough time remains in the frame to send the next data packet.

8.2.4.3 List Processing

The Host Controller operates on the Endpoint Descriptors and Transfer Descriptors enqueued by the Host Controller Driver.

For interrupt and isochronous transfers, the Host Controller begins at the Interrupt Endpoint Descriptor head pointer for the current frame. The list is traversed sequentially until one packet transfer from the first Transfer Descriptor of all interrupt and isochronous Endpoint Descriptors scheduled in the current frame is attempted.

For bulk and control transfers, the Host Controller begins in the respective list where it last left off. When the Host Controller reaches the end of a list, it loads the value from the head pointer and continues processing. The Host Controller processes *n* control transfers to 1 bulk transfer where the value of *n* is set by the Host Controller Driver.

When a Transfer Descriptor completes, either successfully or due to an error condition, the Host Controller moves it to the Done Queue. Enqueuing on the Done Queue occurs by placing the most recently completed Transfer Descriptor at the head of the queue. The Done Queue is transferred periodically from the Host Controller to the Host Controller Driver via the HCCA.

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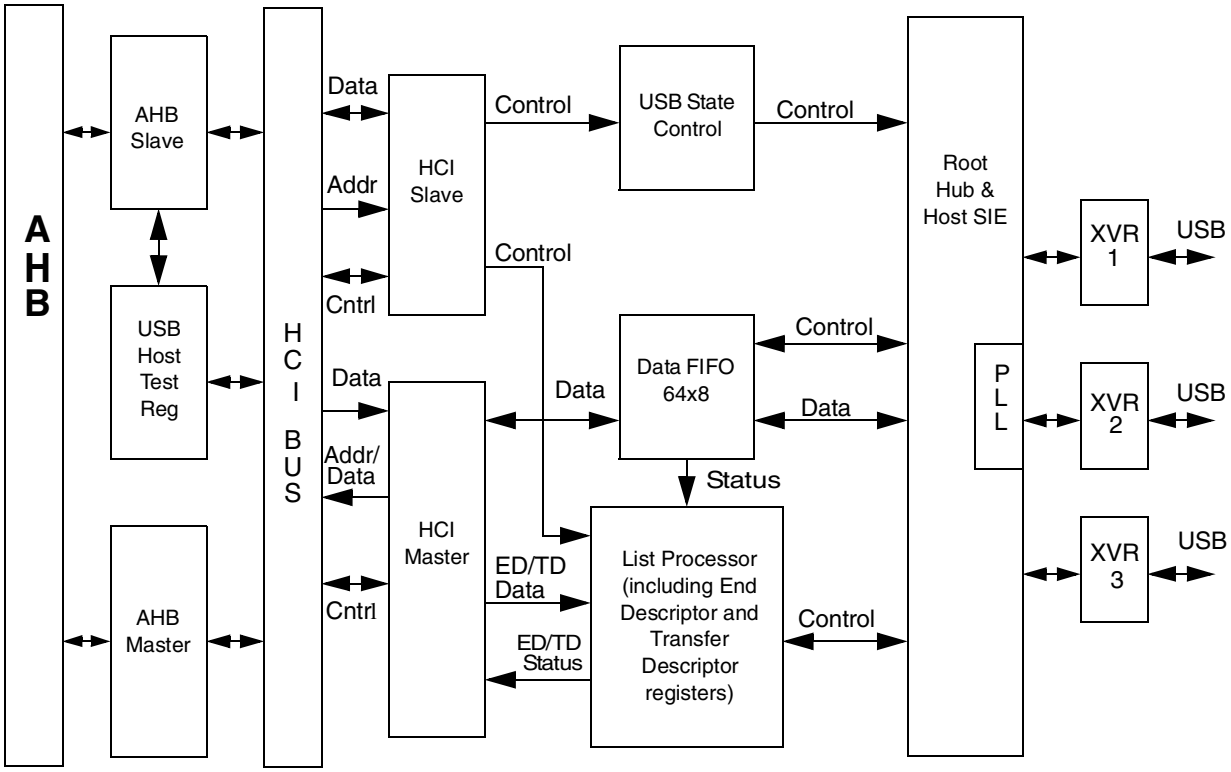
Figure 8-7. USB Host Controller Block Diagram



8.2.5 USB Host Controller Blocks

8.2.5.1 AHB Slave

This block allows access to the OHCI operational registers from/to the AHB via the HCI Bus.

8.2.5.2 AHB Master

This block enables the USB Host Controller to be an AHB Master peripheral and interfaces with the HCI Master block via the HCI Bus.

The AHB Master includes a Data FIFO which will use a 44x37 bit Data FIFO. 32-bit data, 4-bit HCI_MBeN[3:0] (byte lane enables) and HCI_MWBstOnN (burst on) make up the width of the Data FIFO.

8.2.5.3 HCI Slave Block

This block contains the OHCI operational registers, which are programmed by the Host Controller Driver (HCD).

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8.2.5.4 HCI Master Block

The HCI Master Block handles read/write requests to system memory that are initiated by the List Processor while the Host Controller (HC) is in the operational state and is processing the lists queued in by HCD. It generates the addresses for all the memory accesses, which is the DMA functionality. The major tasks handled by this block are:

- Fetching Endpoint Descriptors (ED) and Transfer Descriptors (TD)
- Read/Write endpoint data from/to system memory
- Accessing HC Communication Area (HCCA)
- Write Status and Retire TDs

8.2.5.5 USB State Control

This block implements:

- The USB operational states of the Host Controller, as defined in the OHCI Specification.
- It generates SOF tokens every 1 ms
- It triggers the List Processor while HC is in the operational states.

8.2.5.6 Data FIFO

This block contains a 64x8 FIFO to store the data returned by endpoints on IN tokens, and the data to be sent to the endpoints on OUT Tokens. The FIFO is used as a buffer in case the HC does not get timely access to the host bus.

8.2.5.7 List Processor

The List Processor processes the lists scheduled by HCD according to the priority set in the operational registers.

8.2.5.8 Root Hub and Host SIE

The Root Hub propagates Reset and Resume to downstream ports and handles port connect and disconnect. The Host Serial Interface Engine (HSIE) converts parallel to serial, serial to parallel, Non-Return to Zero Interface (NRZI) encoding/decoding and manages USB serial protocol.

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8.3 Registers

The Host Controller (HC) contains a set of on-chip operational registers that are used by the Host Controller Driver (HCD). According to the function of these registers, they are divided into four partitions, specifically for Control and Status, Memory Pointer, Frame Counter and Root Hub. All of the registers should be read and written as Dwords. The memory map is shown in Table 8-1.

Table 8-1: OpenHCI Register Addresses

Address	Register Name
0x8002_0000	HcRevision
0x8002_0004	HcControl
0x8002_0008	HcCommandStatus
0x8002_000C	HcInterruptStatus
0x8002_0010	HcInterruptEnable
0x8002_0014	HcInterruptDisable
0x8002_0018	HcHCCA
0x8002_001C	HcPeriodCurrentED
0x8002_0020	HcControlHeadED
0x8002_0024	HcControlCurrentED
0x8002_0028	HcBulkHeadED
0x8002_002C	HcBulkCurrentED
0x8002_0030	HcDoneHead
0x8002_0034	HcFmInterval
0x8002_0038	HcFmRemaining
0x8002_003C	HcFmNumber
0x8002_0040	HcPeriodicStart
0x8002_0044	HcLSThreshold
0x8002_0048	HcRhDescriptorA
0x8002_004C	HcRhDescriptorB
0x8002_0050	HcRhStatus
0x8002_0054	HcRhPortStatus[1]
0x8002_0058	Reserved
0x8002_005C	HcRhPortStatus[2]
0x8002_0080	USBCfgCtrl *
0x8002_0084	USBHCISts *

*Note: * - Registers in address space 0x8002_0080 - 0x8002_0084 are not OHCI implementation specific, they are for test software use in EP9301.*

Note: Important - Before setting up any of the Host controller registers it is necessary to set the USH_EN bit (bit 28 of the PwrCnt register).

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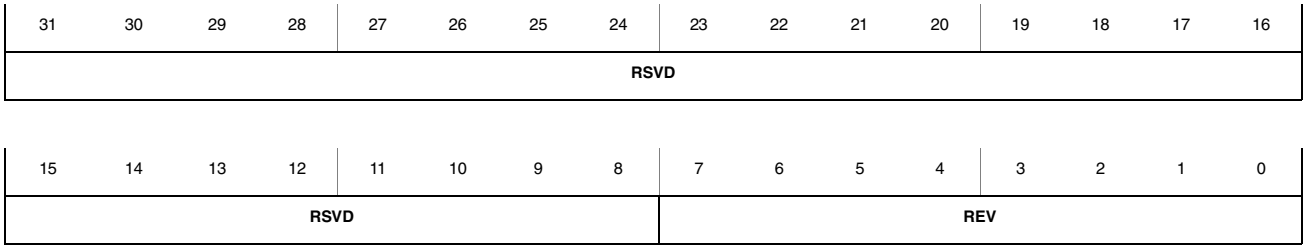
OpenHCI Implementation Specific Registers

The Root Hub partition contains registers that have power-on reset values that are implementation specific. The values for the EP9301 are indicated in the Default field for each register, below.

HcRevision



Address:

0x8002_0000

Default:

0x0000_0010

Definition:

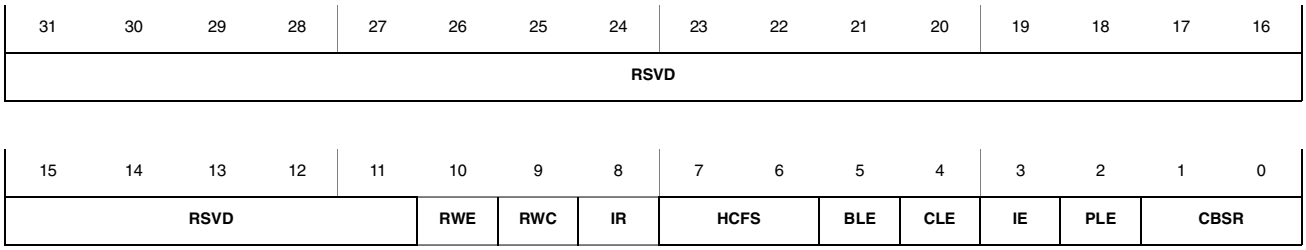
Defines the revision of the OHCI specification with which this implementation is compatible.

Bit Description:

RSVD: Reserved. Unknown During Read.

REV: This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC.
0x10 = Compatible with OHCI 1.0.

HcControl



Address:

0x8002_0004

Default:

0x0000_0000

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Definition:

Controls the host controller's operating modes.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

CBSR: ControlBulkServiceRatio:
This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value.
0 0 = 1:1
0 1 = 2:1
1 0 = 3:1
1 1 = 4:1

PLE: PeriodicListEnable:
This bit is set to enable the processing of the periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.

IE: IsochronousEnable:
This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).

CLE: ControlListEnable:
This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.

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BLE: BulkListEnable:
This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.

HCFS: HostControllerFunctionalState:
A transition to USBOPERATIONAL from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartofFrame field of HcInterruptStatus. This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signaling from a downstream port. HC enters USBSUSPEND after a software reset, whereas it enters USBRESET after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.
0 0 = USBRESET
0 1 = USBRESUME
1 0 = USBOPERATIONAL
1 1 = USBSUSPEND

IR: InterruptRouting:
This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.

RWC: RemoteWakeupConnected:
This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system it is the responsibility of system firmware to set this bit during POST. HC clears the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.

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RWE: RemoteWakeupEnable:
This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.

HcCommandStatus

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD														SOC	

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												OCR	BLF	CLF	HCR

Address:
0x8002_0008

Default:
0x0000_0000

Definition:
Provides current controller status and accepts controller commands.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

HCR: HostControllerReset:
This bit is set by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBSUSPEND state in which most of the operational registers are reset except those stated otherwise; e.g., the InterruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.

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CLF: ControlListFilled:
This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.

BLF: BulkListFilled:
This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.

OCR: OwnershipChangeRequest:
This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwnershipChange field in HcInterruptStatus. After the changeover, this bit is cleared and remains so until the next request from OS HCD.

SOC: SchedulingOverrunCount:
These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in HcInterruptStatus has already been set. This is used by HCD to monitor any persistent scheduling problems.

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HcInterruptStatus

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	OC	RSVD													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									RHSC	FNO	UE	RD	SF	WDH	SO

Address:

0x8002_000C

Default:

0x0000_0000

Definition:

Provides interrupt status information.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

SO: SchedulingOverrun. This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be incremented.

WDH: WritebackDoneHead. This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.

SF: StartofFrame. This bit is set by HC at each start of a frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.

RD: ResumeDetected. This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the USBRESUME state.

UE: UnrecoverableError. This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.

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FNO: FrameNumberOverflow. This bit is set when the MSB of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.

RHSC: RootHubStatusChange. This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.

OC: OwnershipChange. This bit is set by HC when HCD sets the OwnershipChangeRequest field in HcCommandStatus. This event, when unmasked, will always generate a System Management Interrupt (SMI) immediately. This bit is tied to 0b when the SMI pin is not implemented.

HcInterruptEnable

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIE	OC	RSVD													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									RHSC	FNO	UE	RD	SF	WDH	SO

Address:

0x8002_0010

Default:

0x0000_0000

Definition:

Enables interrupt sources.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

SO: SchedulingOverrun. Enable interrupt generation due to Scheduling Overrun.

WDH: WritebackDoneHead. Enable interrupt generation due to HcDoneHead Writeback.

SF: StartofFrame. Enable interrupt generation due to Start of Frame.

RD: ResumeDetected. Enable interrupt generation due to Resume Detect.

UE: UnrecoverableError. Enable interrupt generation due to Unrecoverable Error.

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FNO: FrameNumberOverflow. Enable interrupt generation due to Frame Number Overflow.

RHSC: RootHubStatusChange. Enable interrupt generation due to Root Hub Status Change.

OC: OwnershipChange. Enable interrupt generation due to Ownership Change.

MIE: Master Interrupt Enable. A zero written to this field is ignored by HC. A one written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as a Master Interrupt Enable.

HcInterruptDisable

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
MIE	OC	RSVD													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									RHSC	FNO	UE	RD	SF	WDH	SO

Address:

0x8002_0014

Default:

0x0000_0000

Definition:

Disables interrupt sources.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

SO: SchedulingOverrun: Disable interrupt generation due to Scheduling Overrun.

WDH: WritebackDoneHead: Disable interrupt generation due to HcDoneHead Writeback.

SF: StartofFrame: Disable interrupt generation due to Start of Frame.

RD: ResumeDetected: Disable interrupt generation due to Resume Detect.

UE: UnrecoverableError: Disable interrupt generation due to Unrecoverable Error.

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FNO: FrameNumberOverflow: Disable interrupt generation due to Frame Number Overflow.

RHSC: RootHubStatusChange: Disable interrupt generation due to Ownership Change.

OC: OwnershipChange. Enable interrupt generation due to Ownership Change.

MIE: Master Interrupt Enable: A zero written to this field is ignored by HC. A one written to this field disables interrupt generation due to events specified in the other bits of this register. This field is set after a hardware or software reset.

HcHCCA

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD								RSVD							

Address:

0x8002_0018

Default:

0x0000_0000

Definition:

Base physical address of the Host Controller Communication Area.

Bit Description:

RSVD: Reserved. Unknown During Read.

AD: HCCA. Base physical address of the Host Controller Communication Area.

HcPeriodCurrentED

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AD												RSVD			

Address:

0x8002_001C

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Default:

0x0000_0000

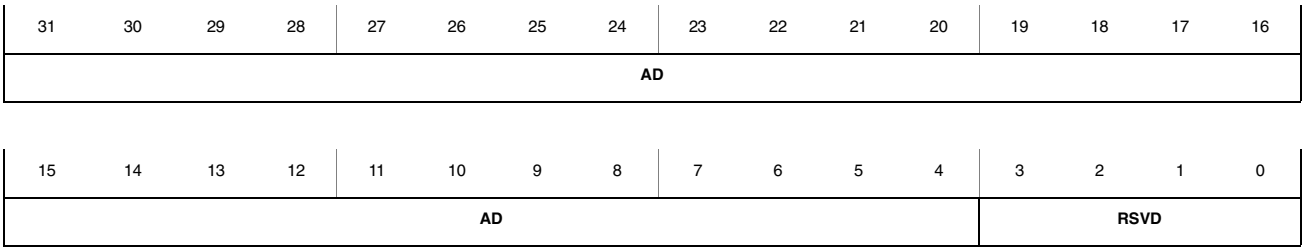
Definition:

Physical address of the current isochronous or interrupt endpoint descriptor.

Bit Description:

RSVD:	Reserved. Unknown During Read.
AD:	PeriodCurrentED. This is used by HC to point to the head of one of the Periodic lists which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.

HcControlHeadED



Address:

0x8002_0020

Default:

0x0000_0000

Definition:

Physical address of the first endpoint descriptor of the control list.

Bit Description:

RSVD:	Reserved. Unknown During Read.
AD:	ControlHeadED. HC traverses the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.

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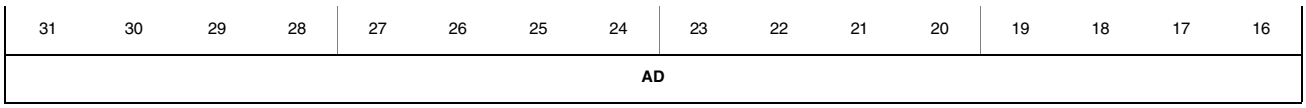
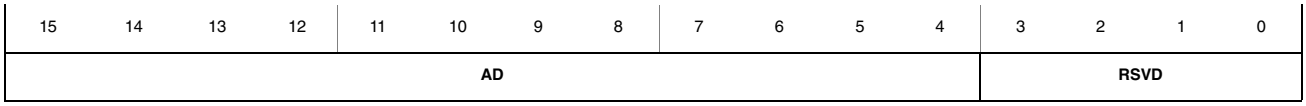
HcControlCurrentED





Address:

0x8002_0024

Default:

0x0000_0000

Definition:

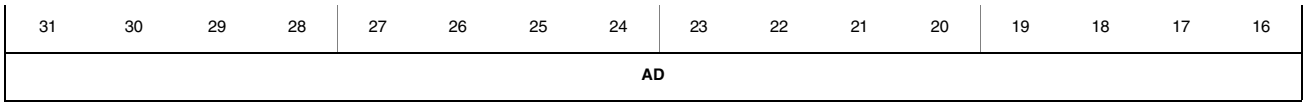
Physical address of the current endpoint descriptor of the control list.

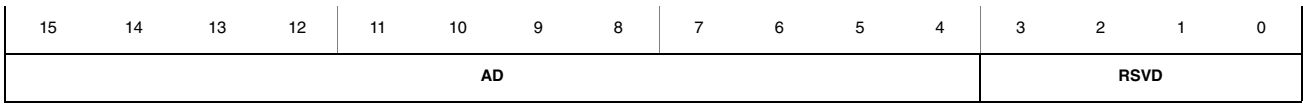
Bit Description:

RSVD: Reserved. Unknown During Read.

AD: ControlCurrentED. This pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentEDand clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.

HcBulkHeadED





Address:

0x8002_0028

Default:

0x0000_0000

Definition:

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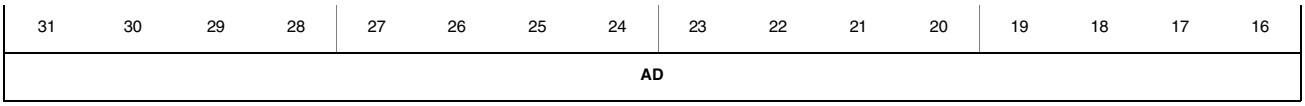
Physical address of the first endpoint descriptor of the bulk list.

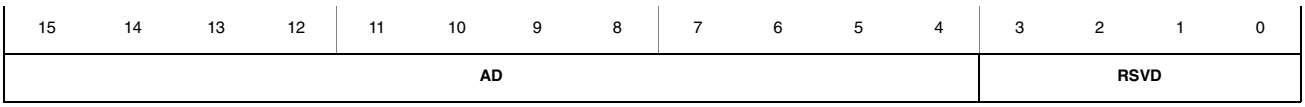
Bit Description:

RSVD: Reserved. Unknown During Read.

AD: BulkHeadED. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.

HcBulkCurrentED





Address:

0x8002_002C

Default:

0x0000_0000

Definition:

Physical address of the current endpoint descriptor of the bulk list.

Bit Description:

RSVD: Reserved. Unknown During Read.

AD: BulkCurrentED. This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.

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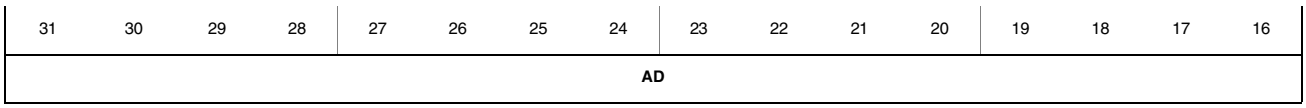
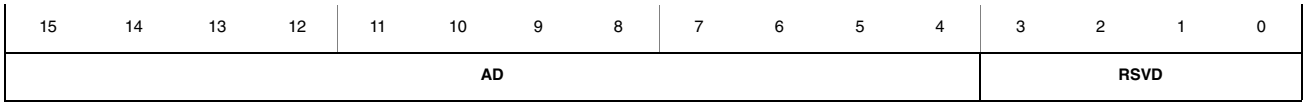
HcDoneHead





Address:

0x8002_0030

Default:

0x0000_0000

Definition:

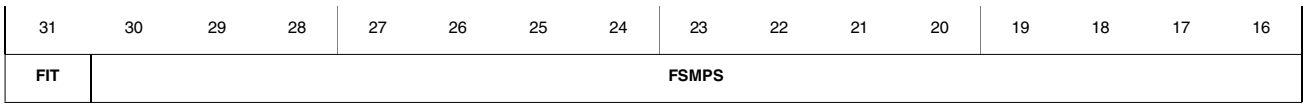
Physical address of the last completed transfer descriptor that was added to the done list.

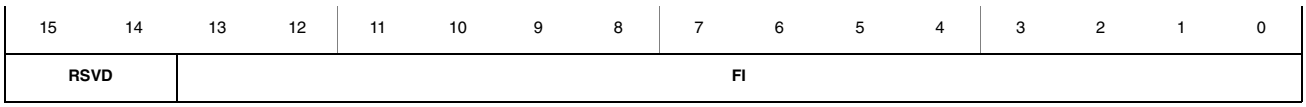
Bit Description:

RSVD: Reserved. Unknown During Read.

AD: DoneHead. When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus.

HcFmInterval





Address:

0x8002_0034

Default:

0x0000_2EDF

Definition:

Describes the bit time interval in a frame and the full speed maximum packet size.

Bit Descriptions:

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RSVD: Reserved. Unknown During Read.

FI: FrameInterval. This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.

FSMPS: FSLargestDataPacket. This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.

FIT: FrameIntervalToggle. HCD toggles this bit whenever it loads a new value to FrameInterval.

HcFmRemaining

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
FRT	RSVD														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				FR											

Address:

0x8002_0038

Default:

0x0000_0000

Definition:

Contains the time remaining in the current frame.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

FR: FrameRemaining. This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of HcFmInterval and uses the updated value from the next SOF.

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FRT: FrameRemainingToggle. This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.

HcFmNumber

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FN															

Address:

0x8002_003C

Default:

0x0000_0000

Definition:

Contains a 16-bit counter used as a timing reference between the host controller and its driver.

Bit Description:

RSVD: Reserved. Unknown During Read.

FN: FrameNumber. This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0x0 after 0xFFFF. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in HcInterruptStatus.

HcPeriodicStart

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				PS											

Address:

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0x8002_0040

Default:

0x0000_0000

Definition:

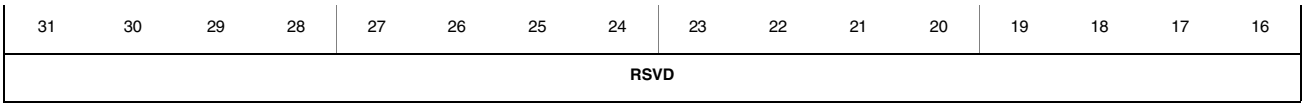
Defines the earliest time the host controller should start processing the periodic list.

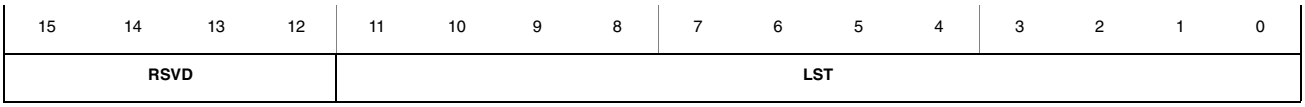
Bit Description:

RSVD: Reserved. Unknown During Read.

PS: PeriodicStart. After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 0x03E67. When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

HcLSThreshold





Address:

0x8002_0044

Default:

0x0000_0628

Definition:

Contains a value used by the host controller to determine whether to commit to the transfer of a maximum 8-byte LS packet before EOF.

Bit Description:

RSVD: Reserved. Unknown During Read.

LST: LSThreshold. This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining >= this field. The value is calculated by HCD with the consideration of transmission and setup overhead.

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HcRhDescriptorA

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
P								RSVD							

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD			NOCP	OCPM	DT	NPS	PSM	NDP							

Address:

0x8002_0048

Default:

0x0200_1203

Definition:

Describes the root hub.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

NDP: NumberDownstreamPorts. These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported by OpenHCI is 15.
0x03 = 3 downstream ports.

PSM: PowerSwitchingMode. This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared.
0: All ports are powered at the same time.
1: Each port is powered individually.

This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, the port is controlled only by the global power switch (Set/ClearGlobalPower).

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NPS: NoPowerSwitching. These bits are used to specify whether power switching is supported or port are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching.
0: Ports are power switched
1: Ports are always powered on when the HC is powered on.

DT: DeviceType. This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.

OCPM: OverCurrentProtectionMode. This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, this fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared.
0: Over-current status is reported collectively for all downstream ports
1: Over-current status is reported on a per-port basis.

NOCP: NoOverCurrentProtection. This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting.
0: Over-current status is reported collectively for all downstream ports
1: No overcurrent protection supported

P: PowerOnToPowerGoodTime. This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as P[7:0] * 2 ms. 0x05 = 10 ms

HcRhDescriptorB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD												PPCM			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												DR			

Address:

0x8002_004C

Default:

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0x0000_0000

Definition:

Describes the root hub.

Bit Descriptions

RSVD: Reserved. Unknown During Read.

DR: DeviceRemovable. Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable.
bit 0: Reserved
bit 1: Device attached to Port #1
bit 2: Device attached to Port #2
bit 3: Device attached to Port #3

PPCM: PortPowerControlMask: Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode=0), this field is not valid.
bit 0: Reserved
bit 1: Ganged-power mask on Port #1
bit 2: Ganged-power mask on Port #2
bit 3: Ganged-power mask on Port #3

HcRhStatus

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CRWE	RSVD													CCIC	LPSC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DRWE	RSVD													OCI	LPS

Address:

0x8002_0050

Default:

0x0000_0000

Definition:

Root hub status.

Bit Descriptions:

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RSVD: Reserved. Unknown During Read.

LPS: (READ) LocalPowerStatus. The Root Hub does not support the local power status feature; thus, this bit is always read as “0”.

(WRITE) ClearGlobalPower: In global power mode (PowerSwitchingMode=0), this bit is written to “1” to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a “0” has no effect.

OCI: OverCurrentIndicator. This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always “0”

DRWE: (READ) DeviceRemoteWakeupEnable. This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt.
0 = ConnectStatusChange is not a remote wakeup event.
1 = ConnectStatusChange is a remote wakeup event.

(WRITE) SetRemoteWakeupEnable: Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect.

LPSC: (READ) LocalPowerStatusChange. The Root Hub does not support the local power status feature; thus, this bit is always read as “0”.

(WRITE) SetGlobalPower. In global power mode (PowerSwitchingMode=0), This bit is written to “1” to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a “0” has no effect.

CCIC: OverCurrentIndicatorChange. This bit is set by hardware when a change has occurred to the OCI field of this register. The HCD clears this bit by writing a “1”. Writing a “0” has no effect.

CRWE: (WRITE) ClearRemoteWakeupEnable. Writing a '1' clears DeviceRemoveWakeupEnable. Writing a '0' has no effect.

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HcRhPortStatus1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD											PRSC	OCIC	PSSC	PESC	CSC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						LSDA	PPS	RSVD			PRS	POCI	PSS	PES	CCS

Address:

HcRhPortStatus1 - 0x8002_0054

Default:

0x0000_0100

Definition:

Control/status for root hub port 1.

Bit Descriptions:

8

CCS: (READ) CurrentConnectStatus: This bit reflects the current state of the downstream port.
0 = no device connected
1 = device connected

(WRITE) ClearPortEnable: The HCD writes a “1” to this bit to clear the PortEnableStatus bit. Writing a “0” has no effect. The CurrentConnectStatus is not affected by any write.

Note: This bit is always read “1” when the attached device is nonremovable (DeviceRemoveable.NDP).

PES: (READ) PortEnableStatus. This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set.
0 = port is disabled
1 = port is enabled

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(WRITE) SetPortEnable. The HCD sets PortEnableStatus by writing a “1”. Writing a “0” has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected port.

PSS: (READ) PortSuspendStatus. This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.
0 = port is not suspended
1 = port is suspended

(WRITE) SetPortSuspend. The HCD sets the PortSuspendStatus bit by writing a “1” to this bit. Writing a “0” has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.

POCI: (READ) PortOverCurrentIndicator. This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal
0 = no overcurrent condition.
1 = overcurrent condition detected.

(WRITE) ClearSuspendStatus. The HCD writes a “1” to initiate a resume. Writing a “0” has no effect. A resume is initiated only if PortSuspendStatus is set.

PRS: (READ) PortResetStatus. When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared.
0 = port reset signal is not active
1 = port reset signal is active

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(WRITE) SetPortReset. The HCD sets the port reset signaling by writing a “1” to this bit. Writing a “0” has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.

PPS: (READ) PortPowerStatus. This bit reflects the port’s power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NDP].

In global switching mode (PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.
0 = port power is off
1 = port power is on

(WRITE) SetPortPower: The HCD writes a “1” to set the PortPowerStatus bit. Writing a “0” has no effect.

Note: This bit is always reads “1” if power switching is not supported.

LSDA: (READ) LowSpeedDeviceAttached. This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set.
0 = full speed device attached
1 = low speed device attached

(WRITE) ClearPortPower. The HCD clears the PortPowerStatus bit by writing a “1” to this bit. Writing a “0” has no effect.

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CSC: ConnectStatusChange. This bit is set whenever a connect or disconnect event occurs. The HCD writes a “1” to clear this bit. Writing a “0” has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected.
0 = no change in CurrentConnectStatus
1 = change in CurrentConnectStatus

Note: If the DeviceRemovable.NDP bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.

PESC: PortEnableStatusChange. This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a “1” to clear this bit. Writing a “0” has no effect.
0 = no change in PortEnableStatus
1 = change in PortEnableStatus

PSSC: PortSuspendStatusChange. This bit is set when the full resume sequence has been completed. This sequence includes the 20 ms resume pulse, LS EOP, and 3 ms re-synchronization delay. The HCD writes a “1” to clear this bit. Writing a “0” has no effect. This bit is also cleared when ResetStatusChange is set.
0 = resume is not completed
1 = resume completed

OCIC: PortOverCurrentIndicatorChange. This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a “1” to clear this bit. Writing a “0” has no effect.
0 = no change in PortOverCurrentIndicator
1 = PortOverCurrentIndicator has changed

PRSC: PortResetStatusChange. This bit is set at the end of the 10 ms port reset signal. The HCD writes a “1” to clear this bit. Writing a “0” has no effect.
0 = port reset is not complete
1 = port reset is complete

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HcRhPortStatus2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD											PRSC	OCIC	PSSC	PESC	CSC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						LSDA	PPS	RSVD			PRS	POCI	PSS	PES	CCS

Address:

HcRhPortStatus2 - 0x8002_005C

Default:

0x0000_0100

Definition:

Control/status for root hub port 2.

Bit Descriptions:

8

CCS: (READ) CurrentConnectStatus: This bit reflects the current state of the downstream port.
0 = no device connected
1 = device connected

(WRITE) ClearPortEnable: The HCD writes a “1” to this bit to clear the PortEnableStatus bit. Writing a “0” has no effect. The CurrentConnectStatus is not affected by any write.

Note: This bit is always read “1” when the attached device is nonremovable (DeviceRemoveable.NDP).

PES: (READ) PortEnableStatus. This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set.
0 = port is disabled
1 = port is enabled

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(WRITE) SetPortEnable. The HCD sets PortEnableStatus by writing a “1”. Writing a “0” has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected port.

PSS: (READ) PortSuspendStatus. This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.
0 = port is not suspended
1 = port is suspended

(WRITE) SetPortSuspend. The HCD sets the PortSuspendStatus bit by writing a “1” to this bit. Writing a “0” has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.

POCI: (READ) PortOverCurrentIndicator. This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal
0 = no overcurrent condition.
1 = overcurrent condition detected.

(WRITE) ClearSuspendStatus. The HCD writes a “1” to initiate a resume. Writing a “0” has no effect. A resume is initiated only if PortSuspendStatus is set.

PRS: (READ) PortResetStatus. When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared.
0 = port reset signal is not active
1 = port reset signal is active

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(WRITE) SetPortReset. The HCD sets the port reset signaling by writing a “1” to this bit. Writing a “0” has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.

PPS: (READ) PortPowerStatus. This bit reflects the port’s power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NDP].

In global switching mode (PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.
0 = port power is off
1 = port power is on

(WRITE) SetPortPower: The HCD writes a “1” to set the PortPowerStatus bit. Writing a “0” has no effect.

Note: This bit is always reads “1” if power switching is not supported.

LSDA: (READ) LowSpeedDeviceAttached. This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set.
0 = full speed device attached
1 = low speed device attached

(WRITE) ClearPortPower. The HCD clears the PortPowerStatus bit by writing a “1” to this bit. Writing a “0” has no effect.

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CSC: ConnectStatusChange. This bit is set whenever a connect or disconnect event occurs. The HCD writes a “1” to clear this bit. Writing a “0” has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected.
0 = no change in CurrentConnectStatus
1 = change in CurrentConnectStatus

Note: If the DeviceRemovable.NDP bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.

PESC: PortEnableStatusChange. This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a “1” to clear this bit. Writing a “0” has no effect.
0 = no change in PortEnableStatus
1 = change in PortEnableStatus

PSSC: PortSuspendStatusChange. This bit is set when the full resume sequence has been completed. This sequence includes the 20 ms resume pulse, LS EOP, and 3 ms re-synchronization delay. The HCD writes a “1” to clear this bit. Writing a “0” has no effect. This bit is also cleared when ResetStatusChange is set.
0 = resume is not completed
1 = resume completed

OCIC: PortOverCurrentIndicatorChange. This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a “1” to clear this bit. Writing a “0” has no effect.
0 = no change in PortOverCurrentIndicator
1 = PortOverCurrentIndicator has changed

PRSC: PortResetStatusChange. This bit is set at the end of the 10 ms port reset signal. The HCD writes a “1” to clear this bit. Writing a “0” has no effect.
0 = port reset is not complete
1 = port reset is complete

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USBCfgCtrl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD											TRCS	TPOC			RSVD

Address:

0x8002_0080 - Read/Write

Default:

0x0000_0000

Definition:

Used to implement some input signals to USB host controller for configuration through software.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TPOC: When asserted by software, the corresponding port will enter DISCONNECT state. These bits must be cleared before the ports can be reused.

TRCS: Inverted internally and sent out as APP_CntSelN signal to uhostc_top. Internally known as TicRegCntSel. APP_CntSelN is used for selecting the counter value for either simulation or real-time for the 1 ms frame duration used internally. It should be usually set to “0”. Setting it to “1” will cause the internal counter count to be a partial full count.

USBHCISts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													RWU	MSN	MBA

Address:

0x8002_0084 - Read/Write

Default:

0x0000_0000

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Definition:

Host Controller Interface. Some status bits reporting from USB host controller to software.

Bit Descriptions:

RSVD:	Reserved. Unknown During Read.
MBA:	Host controller buffer access indication. When asserted, it indicates that currently host controller is accessing data buffer. It is a status bit reporting to software and software does not need to take any action.
MSN:	Host controller new frame. Software does not need to take any action because it is a status about a new frame that is generated.
RWU:	Host controller remote wakeup. Software action when this bit is asserted is implementation specific. It is a status bit reporting a transition of internal state.

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Chapter 9

Static Memory Controller

9.1 Introduction

The Static Memory Controller (SMC) is accessed as an AHB slave device and can be used to provide an interface between the AMBA AHB system bus and external (off-chip) memory devices.

The SMC provides support for up to eight independently configurable memory banks simultaneously. Each memory bank is capable of supporting:

- SRAM
- ROM
- FLASH EPROM
- Burst ROM memory

Each memory bank may use devices using either 8 or 16-bit external memory data paths. The SMC is configured to support little endian operation.

The memory banks can be configured to support:

- The SMC controller can support two external peripherals that use the DMA handshake lines (DMARQ and DMAACK) to control data flow.
- Non-burst read and write accesses only to high-speed CMOS static RAM.
- Non-burst write accesses, non-burst read accesses and asynchronous page mode read accesses to fast-boot block FLASH memory.

The Static Memory Controller has six main functions:

- Memory bank select
- Access sequencing
- Wait states generation
- Byte lane write control
- External bus interface

The Static Memory Controller also supports external wait cycle extension (**WAITn**):

- Each bank of the SMC has a programmable number of wait states. The SMC also supports an external **WAITn** input that can be used by an

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external device to extend the wait time. If there are N (1<N<32) wait cycles, then the SMC holds its bus state for N clock cycles or until WAITn is sampled as being inactive, whichever happens last, with a minimum of N=2 wait cycles for synchronization.

Additional points to note:

- The SMC captures the read data on the system clock edge prior to the de-assertion of **nCSx**. The **nCSx** signal and the address are removed one cycle later.
- If the external memory interface is not as wide as the AHB transfer request, the SMC issues successive external read bus cycles and buffers the data before it is presented to the AHB. In addition, the AHB remains unavailable for any other purpose until the read request has been completed.

9.2 Static Memory Controller Operation

The SMC controller provides access to static memory devices on the external bus, and can be used to interface to a wide variety of external device types, including SRAM and ROM.

Six memory spaces are provided, each with a set of registers determining the timing characteristics of accesses made to that space. These are general purpose and provided with external chip select signals.

Figure 9-1. 16-bit read, 16-bit Memory, 0 wait cycles, RBLE = 1, WAITn Inactive

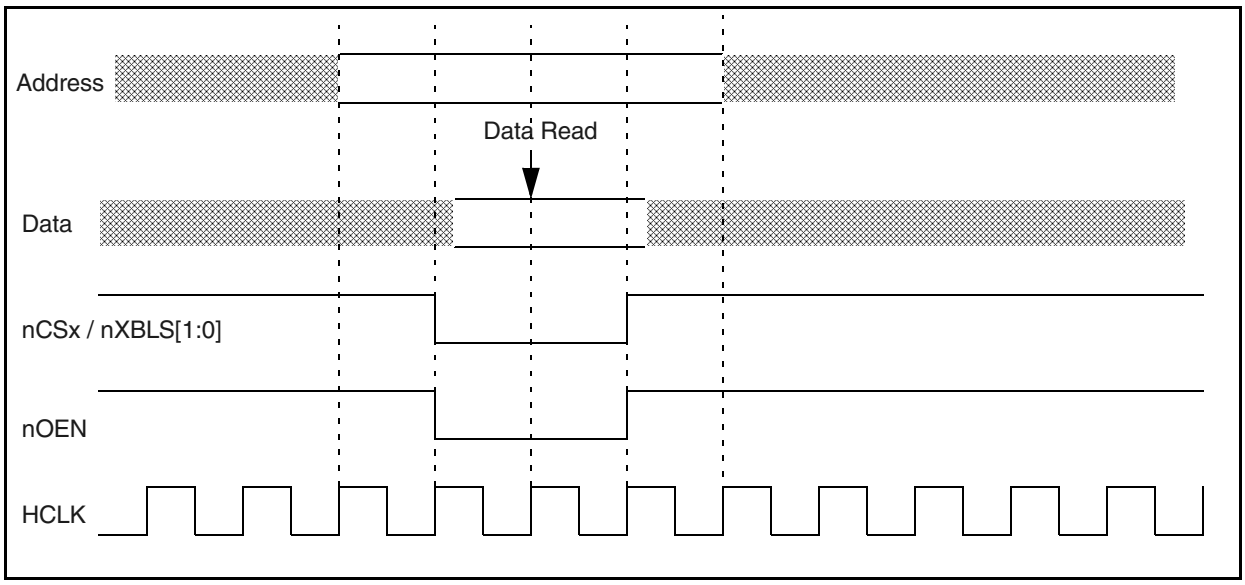

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Figure 9-2. 16-bit write, 16-bit Memory, 0 wait cycles, RBLE = 1, WAITn Inactive

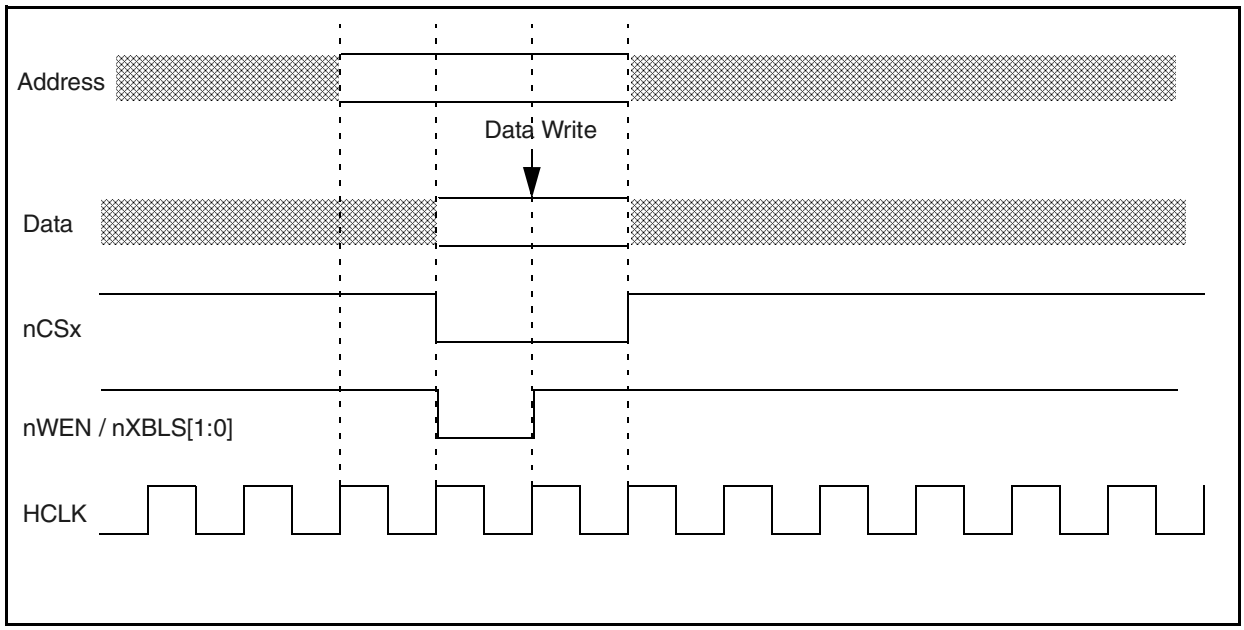

Figure 9-3. 16-bit read, 16-bit Memory, RBLE = 1, WAITn Active

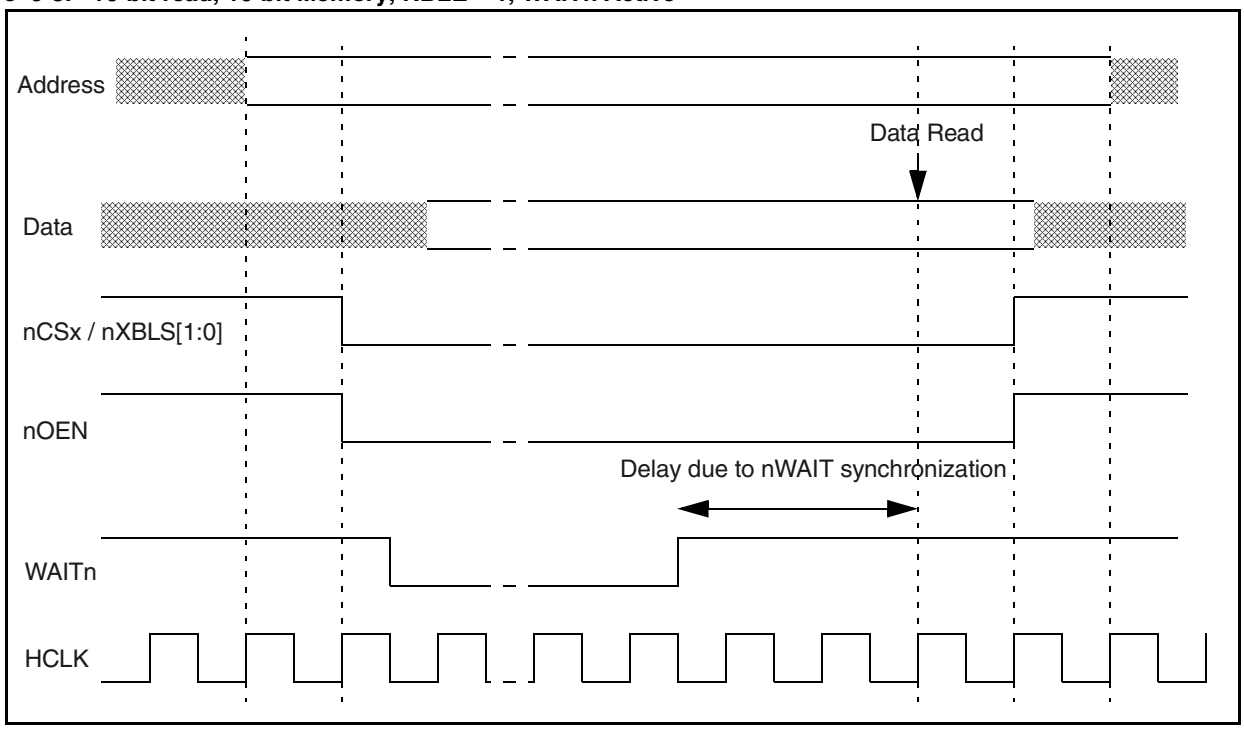

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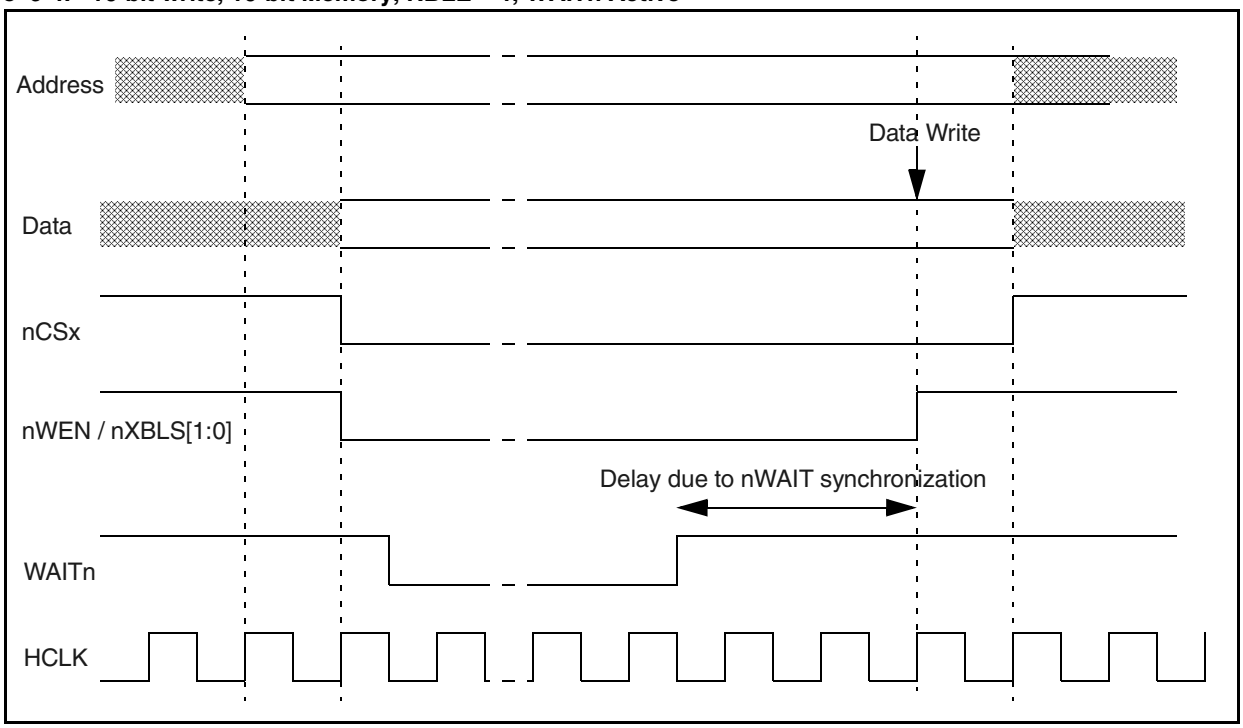
Figure 9-4. 16-bit write, 16-bit Memory, RBLE = 1, WAITn Active



9

9.3 Byte Lane Write / Read Control

The Byte Lane Write/Read Control controls **nXBLS[1:0]** according to AMBA transfer width (indicated by **HSIZE[1:0]**), external memory width, **HADDR[1:0]** and the access sequencing.

A dedicated write enable **nXWEN** and read enable **nXOEN** are used to access the external memory in tandem with the byte lane selection lines **nXBLS[1:0]**.

The **nBYTE** signal is clear when the current memory bank access is programmed for an 8-bit external data system and is set for all other configurations.

Multiplexing is allowed as some signals become redundant depending on the memory bank configuration. The multiplexing control depends on the external memory system being accessed as shown in Table 9-1.

Table 9-1: nXBLS[1:0] Multiplexing

Multiplex Function	8 bit external system (nXBLS[1] redundant)	16 bit external system
nXBLS[1]	Unused	nXBLS[1]
nXBLS[0]	nXBLS[0]	nXBLS[0]

Table 9-2 shows the basic coding for writing to 8 or 16-bit external memory systems:

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Table 9-2: WRITING to an External Memory System

Access	LS Address bits	8 bit external system	16 bit external system
HSIZE[1:0]	HADDR [1:0]	nByte, A1, A0, nXBLS[0] (little-endian)	nByte, A1, nXBLS[1:0] (little-endian)
10 (word)	XX	0,11,0 0,10,0 0,01,0 0,00,0	1,1,00 1,0,00
01 (half word)	1X	0,11,0 0,10,0	1,1,00
01 (half word)	0X	0,01,0 0,00,0	1,0,00
00 (byte)	11	0,11,0	1,1,01
00 (byte)	10	0,10,0	1,1,10
00 (byte)	01	0,01,0	1,0,01
00 (byte)	00	0,00,0	1,0,10

Word transfers are the largest size transfers supported by the SMC, any access attempted with a size greater than a word will cause the ERROR response to be generated.

For READ accesses, depending on the external memory set-up, it is necessary to drive all the **nXBLS[1:0]** lines either all HIGH or all LOW. The control for this is performed using the RBLE (Read byte lane enable) bit within each memory block configuration register, that is:

- RBLE = 0 implies that all **nXBLS[1:0]** lines are driven HIGH during READ accesses.
- RBLE = 1 implies that all **nXBLS[1:0]** lines are driven LOW during READ accesses.

In general, if the byte lane select lines **nXBLS[1:0]** are used as write enables (**nXWEN** unused) then the RBLE bit should be clear.

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9.4 Registers

Table 9-3: SMC Register Map

Address	Read Location	Write Location
0x8008_0000	SMCBCR0 (Bank config register 0)	SMCBCR0 (Bank config register 0)
0x8008_0004	SMCBCR1 (Bank config register 1)	SMCBCR1 (Bank config register 1)
0x8008_0008	SMCBCR2 (Bank config register 2)	SMCBCR2 (Bank config register 2)
0x8008_000C	SMCBCR3 (Bank config register 3)	SMCBCR3 (Bank config register 3)
0x8008_0010	Reserved	Reserved
0x8008_0014	Reserved	Reserved
0x8008_0018	SMCBCR6 (Bank config register 6)	SMCBCR6 (Bank config register 6)
0x8008_001C	SMCBCR7 (Bank config register 7)	SMCBCR7 (Bank config register 7)
0x8008_0020	Reserved	Reserved
0x8008_0024	Reserved	Reserved
0x8008_0028	Reserved	Reserved
0x8008_002C	Reserved	Reserved
0x8008_0030	Reserved	Reserved
0x8008_0034	Reserved	Reserved
0x8008_0038	Reserved	Reserved
0x8008_003C	Reserved	Reserved
0x8008_0040	Reserved	Reserved

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Register Descriptions

SMCBCR0-3, SMCBCR6-7

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD	EBIBRK DIS	MW		PME	WP	WPERR	RSVD								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
WST2					RBLE	WST1					RSVD	IDCY			

Address:

SMCBCR0: 0x8008_0000 - Read/Write
SMCBCR1: 0x8008_0004 - Read/Write
SMCBCR2: 0x8008_0008 - Read/Write
SMCBCR3: 0x8008_000C - Read/Write
SMCBCR6: 0x8008_0018 - Read/Write
SMCBCR7: 0x8008_001C - Read/Write

Default:

0x2000_FBE0

Definition:

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The SMC Bank configuration registers are used to program the characteristics of each of the SRAM/ROM memory banks.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

IDCY: Idle Cycle
Memory data bus turnaround time, (Read to Write).
The turnaround time is (IDCY + 1) x HCLK.

WST1: Wait State1
This is the read/write access time in the case of SRAM and ROM. This wait state time is (WST1 + 1) x HCLK.
This field defaults to 0x1F to enable booting from ROM memories.

RBLE: Read Byte Lane Enable
0 - nXBLS[1:0] all driven HIGH during memory READS (default at reset for bank 1-3,6,7).
1 - nXBLS[1:0] all driven LOW during memory READS. (default at reset for bank 0).

Note: This should be set to "1" during memory writes.

WST2: Wait State 2
This is sequential access time. This wait state time is (WST2 + 1) x HCLK. This defaults to the slowest access on reset (0x1F).

WPERR: Write Protect Error status flag
0 - No Error
1 - Write Protect Error
Writing to this bit will clear the Write Protect status error

WP: Write Protect
0 - SRAM.
1 - ROM, and Write protected RAM

PME: Page Mode Enable (Burst Mode)
1 - Page Mode enabled. (Provides fast Quad Word accesses by toggling the Least 2 Significant address bits on quad word boundaries).
This bit is reset to 0

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MW: Memory Width
00 - 8-bit
01 - 16-bit
10 - Reserved
11 - Reserved
To support different dimension boot ROMs, this register is automatically configured for /CS0 from the state of the width pins Width[1:0] following power on reset if ASDO is Low.

EBIBRKDIS: EBI Break Disable
0 - The SMC is forced to release its EBI bus request at the end of all accesses to this bank when requested by the EBI.
1 - The SMC will only release its EBI bus request when it has completed all pending accesses for this bank.

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Chapter 10

SDRAM, SyncROM, and SyncFLASH Controller

10.1 Introduction

The SDRAM controller provides a high speed memory interface to a wide variety of Synchronous Memory devices, including SDRAMs, Synchronous FLASH, and Synchronous ROMs.

The Key Features of this block are as follows:

- Up to four synchronous memory banks that can be independently configured.
- Includes special configuration bits for Synchronous ROM operation.
- Ability to program Synchronous FLASH devices using write and erase commands.
- Data is transferred between the controller and the SDRAM in quad word bursts. Longer transfers within the same page are concatenated, forming a seamless burst.
- 16-bit data bus.
- Allows external memory pins (address and data) to be multiplexed with other memory controllers (such as SRAM, ROM, etc.).
- SDRAM contents are preserved over a “soft” reset.
- Power saving Synchronous Memory CKE and external clock modes

10.1.1 Booting (from SROM or SyncFLASH)

If the system is booting up using a Synchronous ROM (on SDRAMDevCfg3 register), then a short configuration sequence is activated before releasing the processor from reset. This ensures that a known configuration (RAS=2, CAS=5, and Burst Length=4) is set for whatever device may be attached, as different SROM’s default to different Burst Lengths.

CAUTION: It is not possible to reconfigure other SDRAM memory banks when running code from SDRAM. Attempting to do this may cause the system to lock-up. It is advised that the boot code copy the SDRAM configuration code to some non-SDRAM memory space, and then set up the SDRAM from that space.

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A similar automatic boot-up sequence will be initiated when booting from Synchronous FLASH, (WBL=1, CAS=3, Burst Length=4).

Table 10-1: Boot Device Selection

Boot modes	CSn7	CSn6	ASDO	EECLK
8-bit ROM	0	0	0	0
16-bit ROM	0	1	0	0
16-bit SFLASH (Initializes Mode Register)	0	0	1	0
16-bit SROM (Initializes Mode Register)	0	1	1	0

The following power-up sequence is executed by an internal state machine after power on reset:

1. Power is applied to the circuit with inputs **CKE** and **DQM** pulled high so that they rise with the supply **VDD** and **VDDQ**.
2. Following power-up, the processor is held in the reset state while the clock runs. The Command pins are put in the NOP condition for 200 µs by setting both the Initialize and MRS bits to 1, while the SROM device is clocked.
3. The default settings are written to the Mode register by setting the Initialize and MRS bits to 0, 1 respectively and reading the appropriate address.
4. After 3 clock cycles from the mode register set cycle, the device is ready for power-up, and all data outputs are in a high impedance state. The processor is released from the reset state.

10.1.1.1 Address Pin Usage

Each of the four SDRAMDevCfg domains can be fitted with a variety of device types, provided the total capacitance on any address/control/data line does not exceed the specified operating limit.

Because of the row/column/bank architecture of Synchronous Memory devices, the mapping of these memories into the EP9301 memory space is not always obvious. Typically, the memory in a SDRAM device will not appear continuous to the EP9301 chip. For example, a 32-Mbyte SDRAM device may be visible as eight 4-Mbyte blocks. In order to understand the reason for this non-continuous memory it is necessary to understand the address pin usage of the EP9301 device. Table 10-2 on page 316 shows address pin usage. The top row in this table shows the address lines connected to the memory device. The remaining rows show how the device's linear address space is mapped into the SDRAM address lines. For each memory device configuration, that is, 16-bit wide SDRAM, SROM etc., there is a row and column line. These lines show the addresses presented to the Synchronous Memory device for row and column access. By taking the number of row and columns in a Synchronous memory device (available in the device datasheet), the actual address lines used in addressing the device can be determined. Because

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some address lines are not used, the memory appears as non-continuous. This is illustrated in Table 10-2 on page 316.

By using address bits **A26** and **A27** as the Bank control pins, the memory map can look the same whether a FLASH device or SROM device is attached. This also helps reduce power consumption by ensuring that multiple banks within a device need not always be activated.

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Table 10-2: Synchronous Memory Address Decoding

Muxing scheme		SYB1	SYB0	SYA13	SYA12	SYA11	SYA10	SYA9	SYA8	SYA7	SYA6	SYA5	SYA4	SYA3	SYA2	SYA1	SYA0
16 bit data	ROW/ BANK	A27	A26	A22	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9
	COLUMN	A27	A26				AP	A25	A24	A8	A7	A6	A5	A4	A3	A2	A1
SROM look alike, 16 bit data	ROW/ BANK	A22	A21	A27	A26	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9
	COLUMN	A22	A21				AP	A25	A24	A8	A7	A6	A5	A4	A3	A2	A1

10.1.1.2 SDRAM Initialization

Following power on, each SDRAM in the system must be initialized before it can be used. The following is a general initialization sequence, individual SDRAM device datasheets should be consulted to ensure compatibility.

Table 10-3: General SDRAM Initialization Sequence

Step	Action	Reason
1	Wait 100 µs	To allow SDRAM power and clocks to stabilize
2	Set SDRAM controller device mode register	This is necessary to tell the SDRAM controller the width of the SDRAM it is talking to (8 or 16- bits)
3	Set Initialize, MRS, and CKE bits in the Global configuration register	To issue continuous NOP commands
4	Wait 200 µs	SDRAM requirement
5	Clear the MRS bit (Initialize and CKE are set)	To issue a Pre-charge All command
6	Write 10 into the refresh timer register	To provide a refresh every 10 clock cycles
7	Wait for at least 80 clock cycles	To provide 8 refresh cycles to all SDRAMs
8	Program the refresh counter with the normal operating value	To establish normal refresh operation
9	Select mode register update mode (Initialise=0, MRS=1), and perform a read from each SDRAM in the memory system. The address that is read defines the value written into the SDRAM mode register (see SDRAM device datasheet). This address is dependent on the configuration of the memory system since the actual SDRAM address pins are mapped differently onto EP9301 address pins for 8 and 16-bit wide memory systems. (This is the reason for step 2).	To set each SDRAM mode register

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Step	Action	Reason
10	Program device configuration registers with parameters corresponding to those programmed into the SDRAM devices mode register	To initialize the SDRAM controller timing
11	Clear the Initialize and MRS bits and set other bits in Configuration register 1 to their normal operating values.	To start normal operation.

10.1.1.3 Programming External Device Mode Register

When setting the MODE Register within a synchronous device, the command word that is placed on the address lines shown in Table 10-4 on page 318 depends on whether a SROM, SDRAM, or SyncFlash is attached. Once the MRS and Initialize bits have been appropriately set, the address of a subsequent read instructions on address lines **A[22:0]** (for 16-bit organization, see row 2 of Table 10-4 on page 318) will be output on **SYA[12:0]** as the Synchronous mode command. Hence the actual Read Address specifies the command word. The four MS address bits, N, will determine which memory bank receives the command word. Hence if booting from SROM or SFLASH then N is 0x0.

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Table 10-4: Mode Register Command Decoding

Address	SYA11	AP/SYA10	SYA9	SYA8	SYA7	SYA6	SYA5	SYA4	SYA3	SYA2	SYA1	SYA0
Mapped addr for default 32-bit wide	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9
SDRAM or SFLASH	RFU	RFU	Write Burst Length	Test Mode	TM	CAS	CAS	CAS	Burst Type	0	1	0
Example: SDRAM with WBL = 0, TM = 0, CAS = 3, Sequential, BL = 4	0	0	0	0	0	0	1	1	0	0	1	0
SROM	RFU	RFU	RFU	RFU	RFU	RAS	CAS	CAS	CAS	Burst Type	0	1
Example: SROM RAS =2, CAS=2, Sequential, BL=4	0	0	0	0	0	1	1	0	0	0	0	1

The Burst Length is always set to 8 for all 16-bit wide memory systems.

Table 10-5, below, and Table 10-6, and Table 10-7 on page 319 show the bit field settings for CAS, RAS, and Burst Length.

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Table 10-5: Sync Memory CAS Settings

CAS Setting	SDRAM	SFLASH	SROM
000	Reserved	Reserved	Reserved
001	Reserved	1	2
010	2	2	3
011	3	3	4
100	Reserved	Reserved	5
101	Reserved	Reserved	6
110	Reserved	Reserved	7
111	Reserved	Reserved	8

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Table 10-6: Sync Memory RAS, (Write) Burst Type Settings

Setting	SDRAM	SFLASH	SROM
RAS = 0	-	-	1 clk
RAS = 1	-	-	2 clk
Burst Type (BT) = 0	Sequential	Sequential	Sequential
BT = 1	Interleaved	Interleaved	Interleaved
WBT = 0	As Programmed (that is, same as read)	As Programmed	As Programmed
WBL = 1	Write Burst = 1	Write Burst = 1	-

The SDRAM controller must specify a number of clocks for RAS which is greater than or equal to the specified RAS time for the memory device.

Table 10-7: Burst Length Settings

Burst Length	SDRAM	SFLASH	SROM
000	1	1	Reserved
001	2	2	4
010	4	4	8
011	8	8	Reserved
100	Reserved	Reserved	---
101	Reserved	Reserved	---
110	Reserved	Reserved	---
111	Full Page or Reserved	Full Page or Reserved	

If using a 16-bit wide external bus, then the following Read addresses *must* be used to set up the specified parameters (Note: H can be 0, C, D, E or F. These are the possible memory mapped chip select addresses.):

- SDRAM default READ Address: 0xH000_6600 (This sets WBL=0, TM=0, CAS=3, Sequential, BL=8)
- SFLASH default READ Address: 0xH004_6600 (This sets WBL=1, TM=0, CAS=3, Sequential, BL=8)
- SROM default READ Address: 0xH000_C400 (This sets RAS=2, CAS=5, Sequential, BL=8)

10.1.1.4 SDRAM Self Refresh

10.1.1.4.1 Entering Self Refresh Mode

When entering low power mode (standby), the following actions are carried out by the synchronous memory controller before the processor is stopped

1. Precharge all active banks
2. Issue NOP
3. Clock Enable Driven Low

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4. Issue AUTO REFRESH command
5. Enter SELF REFRESH Mode

10.1.1.4.2 Exiting Self Refresh Mode

Coming out of Standby the following actions are carried out by the synchronous memory controller before the processor is started.

1. Allow clock stabilization
2. Clock Enable driven high
3. Issue 10 NOP commands
4. Issue AUTO REFRESH command
5. Enter AUTO REFRESH Mode

10.1.1.5 SROM and SyncFlash

10.1.1.5.1 Synchronous FLASH Programming

The Synchronous FLASH Command Register enables erasing and writing of Synchronous FLASH attached to the system. It operates in a similar way to programming the Mode register in that once the LCR bit is set, subsequent read addresses are placed onto the Synchronous Address bus and act as the command word. Thus, the address must match the command word specified in the device datasheet. This cycle happens immediately before the usual ACTIVE command in a synchronous instruction sequence and can only be delayed by NOP cycles.

Note the following about Synchronous FLASH devices

- They use the same combination of the CS, RAS, CAS, and WE signals which would normally put a SDRAM into Auto-Refresh mode.
- They cannot be written in bursts, but only one word at a time. Hence the WBL bit is set to 1, allowing burst Reads and Single Writes. When in this mode, no Auto Refresh cycle will occur to this Chip Select, as it will be assumed that the device is a Synchronous FLASH device
- They require 100 µs to initialize after a Low to High transition on the nRP signal.
- Synchronous FLASH can be set by either programming the Mode Register with a known configuration mode before releasing the processor from reset, or by using the contents of its NonVolatileMODE register, (which must have been previously set).

10.1.1.6 External Synchronous Memory System

The Synchronous Memory system is decoded from the processors physical memory map into four address domains each of 256 Mbytes. The memory

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devices used within an address domain must be all of the same type, but different domains may use different memory devices and timing characteristics.

Since all the memory devices share a common bus, the total number of devices is limited by the maximum allowable bus capacitance regardless of which chip select domain they are attached.

10.1.1.6.1 Chip Select nSDCS[3:0] Decoding

Each of the four addressable regions within Synchronous Memory space has an associated chip select line nSDCS[3:0] in Table 10-8. These are decoded from the top bits of the address bus. nSDCS3 can be configured to select an SROM boot device mapping to the bottom of address space.

Table 10-8: Chip Select Decoding

Boot Option (ASDO)	A31	A30	A29	A28	Chip select
1	0	0	0	0	nSDCS3
0	1	1	1	1	nSDCS3
X	1	1	1	0	nSDCS2
X	1	1	0	1	nSDCS1
X	1	1	0	0	nSDCS0

Each of the four Synchronous Memory domains can be configured to be 16 bits wide and to support word, half-word, and byte transfers from the AHB bus. A 16-bit wide external memory system will require two external bus cycles made for each 32-bit operand required.

10.1.1.6.2 Address/Data/Control Required by Memory System

The device type, bank count and latency timing fields can vary between the Synchronous Memory chip select domains, making it possible to use differing memory devices in the memory systems of each domain.

The Address lines in Table 10-9 on page 322 are those required from the processor to address the dimensions of the memory system in each chip select domain. The memory system is 16 bits wide. **DQM[1]** is used as the memory system's upper data mask (UDQM) and **DQM[0]** is used as the lower data mask (LDQM). Where the operand is 32 bits wide, two memory data phases are required to complete the memory cycles, 16-bit and byte sized operands completing in one data phase. Examples of memory system configurations are found in Table 10-9.

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Table 10-9: Memory System Examples

Memory System	Total Size MBytes	Data Bus	Internal Physical Address Required	Byte Enables
16M by 16 bit	32	D[15:0]	A[24:1]	DQM[1:0]
64M by 16 bit	128	D[15:0]	A[26:1]	DQM[1:0]

The SROM 512 ensures a linear addressing range for highly rectangular organized devices. It must also prevent burst accesses that cross the 512 byte border, as the device cannot support this. (Normally the AHB will not burst across a 1 KByte boundary.)

The following is example of the address usage for 256 Mbit device:

Device: 256 Mbits, 16-bit wide, and 13-row x 9-column x 2-bank address (24 address lines in total). The first entry the table above shows the address mapping for this device.

The relevant part of Table 10-2 is reproduced in Table 10-10. However, in this case the used row, column, and bank sizes of the memory are in italics. It can be seen that address bit **A23** is not used in either of row or column address generation. By not using this address bit, the result is the non-continuous memory map of the SDRAM.

Table 10-10: Memory Address Decoding for 256 Mbit, 16-Bit Wide, and 13-Row x 9-Column x 2-Bank Device

Muxing Scheme		SYB1	SYB0	SYA13	SYA12	SYA11	SYA10	SYA9	SYA8	SYA7	SYA6	SYA5	SYA4	SYA3	SYA2	SYA1	SYA0
16 bits Data	ROW/ BANK	*A27*	*A26*	A22	*A21*	*A20*	*A19*	*A18*	*A17*	*A16*	*A15*	*A14*	*A13*	*A12*	*A11*	*A10*	*A9*
	COLUMN	*A27*	*A26*				AP	A25	*A24*	*A8*	*A7*	*A6*	*A5*	*A4*	*A3*	*A2*	*A1*

Table 10-11 and Table 10-11 on page 322 show the Address Ranges utilized by a variety of different configurations and of differently-sized devices.

Table 10-11: 16-Bit Wide Data Systems

Device Size, Type System	Address Matrix	Total Bank Size	Continuous Address Range (see *Note*)	Size of Segment
64 Mbit (16-bit wide device)	12 x 8 x 4 banks	8 Mbytes	0xN000_0000 - 0xN01F_FFFF 0xN400_0000 - 0xN41F_FFFF 0xN800_0000 - 0xN81F_FFFF 0xNC00_0000 - 0xNC1F_FFFF	2 Mbytes

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Device Size, Type System	Address Matrix	Total Bank Size	Continuous Address Range (see *Note*)	Size of Segment
128 Mbit (16-bit wide device)	12 x 9 x 4 banks	16 Mbytes	0xN000_0000 - 0xN01F_FFFF 0xN100_0000 - 0xN11F_FFFF 0xN400_0000 - 0xN41F_FFFF 0xN500_0000 - 0xN51F_FFFF 0xN800_0000 - 0xN81F_FFFF 0xN900_0000 - 0xN91F_FFFF 0xNC00_0000 - 0xNC1F_FFFF 0xND00_0000 - 0xND1F_FFFF	2 Mbytes
256 Mbit (16-bit wide device)	13 x 9 x 4 banks	32 MBytes	0xN000_0000 - 0xN03F_FFFF 0xN100_0000 - 0xN13F_FFFF 0xN400_0000 - 0xN43F_FFFF 0xN500_0000 - 0xN53F_FFFF 0xN800_0000 - 0xN83F_FFFF 0xN900_0000 - 0xN93F_FFFF 0xNC00_0000 - 0xNC3F_FFFF 0xND00_0000 - 0xND3F_FFFF	4 Mbytes
512 Mbit (16-bit wide device)	13 x 10 x 4 banks	64 MBytes	0xN000_0000 - 0xN03F_FFFF 0xN100_0000 - 0xN13F_FFFF 0xN200_0000 - 0xN23F_FFFF 0xN300_0000 - 0xN33F_FFFF 0xN400_0000 - 0xN43F_FFFF 0xN500_0000 - 0xN53F_FFFF 0xN600_0000 - 0xN63F_FFFF 0xN700_0000 - 0xN73F_FFFF 0xN800_0000 - 0xN83F_FFFF 0xN900_0000 - 0xN93F_FFFF 0xNA00_0000 - 0xNA3F_FFFF 0xNB00_0000 - 0xNB3F_FFFF 0xNC00_0000 - 0xNC3F_FFFF 0xND00_0000 - 0xND3F_FFFF 0xNE00_0000 - 0xNE3F_FFFF 0xNF00_0000 - 0xNF3F_FFFF	4 Mbytes

Note: In this table, the letter "N" represents four additional address bits used for chip select. See Table 10-8 on page 321 for details.

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10.2 Registers

The Synchronous Memory controller has seven registers: a global configuration register, four device configuration registers, a refresh timer register, and a boot status register.

The Configuration registers allow software to set the operating parameters of the Synchronous Memory control engine according to the memory devices being used. The refresh timer sets the time period between successive Synchronous Memory refresh commands, and the boot status allows software to detect the state of the boot configuration pins.

The addresses of these registers are listed in Table 10-12.

Table 10-12: Synchronous Memory Controller Registers

Address	Register
0x8006_0000	Reserved
0x8006_0004	GlConfig
0x8006_0008	RefrshTimr
0x8006_000C	BootSts
0x8006_0010	Device configuration 0 (SDRAMDevCfg0)
0x8006_0014	Device configuration 0 (SDRAMDevCfg1)
0x8006_0018	Device configuration 0 (SDRAMDevCfg2)
0x8006_001C	Device configuration 0 (SDRAMDevCfg3)

GlConfig

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
CKE	Clk Shutdown	RSVD													

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								ReArb En	LCR	SMEM Bust	RSVD			MRS	Initialize

Address:

0x8006_0004 - Read/Write

Default:

0x0000_0000

Definition:

The Global configuration register contains additional control and status bits for use during configuration. The lowest two bits are used in combination to allow access to otherwise unavailable synchronous memory commands required

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during memory initialization. The Synchronous Memory status bit provides an indication of the state of the Synchronous Memory controller and can be monitored to determine when a change of device configuration has taken effect.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

CKE: Synchronous Memory clock enable (CKE) control
0 - The clock enable of all IDEL devices de-asserted to save power
1 - All clock enables are driven high continuously (used when booting from SROM or SFLASH)

ClkShutdown: Synchronous Memory clock shutdown control
0 - The CLK is free-running
1 - The CLK line is gated dynamically when there are no accesses to any device.

Note: Before setting the ClkShutdown bit to 1, the CKE bit will have to be set to "0".

ReArbEn: Rearbitration Controller enable.
When HIGH this bit enables the Rearbitration Controller in the SDRAM Arbiter, which changes the default port priority in the SDRAM Arbiter if a Port request is split. By default, this Controller is disabled.

LCR: Load Command Register (for Programming FLASH Devices)
If this bit is set, then the address of subsequent read instructions on lines A[23:10] is output as the FLASH Load Command on SYA[13:0]. The four MS address bits will determine which memory bank the read instruction.
0 - See Table 10-13 on page 326
1 - See Table 10-13 on page 326

SMEMBust: Synchronous Memory engine status bit
0 - Synchronous Memory engine is idle
1 - Synchronous Memory engine is busy

MRS: Synchronous Memory Mode Register.
If this bit is set, then the address of subsequent read instructions on lines A[23:10] is output as the Synchronous Mode command on SYA[13:0]. The four MS address bits will determine which memory bank receives the read instruction.
0 - See Table 10-13 on page 326
1 - See Table 10-13 on page 326

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Initialize: Initialize bit.
Only used as part of the initialization routine.
0 - See Table 10-13
1 - See Table 10-13

The Initialize and MRS bits are used in combination to access Synchronous Memory commands unavailable during normal read and write cycles (Mode Register Set, NOP, PrechargeALL). The LCR bit is used to enable erasing and writing of FLASH memory devices via the Load Command Register. The bits are encoded as described in Table 10-13:

Table 10-13: Synchronous Memory Command Encoding

Initialize	MRS	LCR	Synchronous Memory Command
1	1	0	Issue NOP to Synchronous Memory
1	0	0	Issue PreALL (Pre-charge All) to SDRAM
0	1	0	Enable access to Synchronous Memory device mode register
0	1	1	Enable access to Synchronous FLASH Memory devices Load Command registers
0	0	1	UNDEFINED. Do not use.
1	0	1	UNDEFINED. Do not use.
1	1	1	UNDEFINED. Do not use.
0	0	0	Normal operation

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RefrshTimr

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Refcnt															

Address:

0x8006_0008 - Read/Write

Default:

0x0000_0080

Definition:

The refresh timer register is used to set the period between refresh cycles in multiples of the bus clock period (HCLK). For Example, to generate a 16 ms refresh period, the counter should be set to 800 if the clock period is 20 ns. On reset, the refresh counter is set to 128 but the register must be set by software during the SDRAM initialization routine to the correct value for the memory system. If the Refresh count field is clear, no refresh cycles are initiated.

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Bit Descriptions:

RSVD: Reserved. Unknown During Read.

Refcnt: Refresh Count

BootSts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													Latched ASDO	Width	

Address:

0x8006_000C - Read Only

Default:

0x0000_0000

Definition:

The contents of this register reflect the state of the boot mode option pins, allowing software to determine what the configuration of the device is following boot. The values in this register reflect the levels latched at reset for the given pins.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

Latched ASDO: Boot Media
1 - Synchronous ROM
0 - Asynchronous ROM

Width: Boot memory width
Asynchronous
11 - Reserved
10 - Reserved
01 - 16-bit
00 - 8-bit

Synchronous
11 - Reserved
10 - Reserved
01 - 16-bit SROM (RAS=2, CAS=5, BL=8)
00 - 16-bit SFLASH (WBL=1, CAS=3, BL=4)

Note: SROM is not supported at 8 bits wide.

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*Note: If booting from Asynchronous ROM then the asynchronous memory bank zero **(nCS0)** is mapped to address 0x0000_0000. If booting from Synchronous ROM then synchronous memory bank three (SDRAMDevCfg3), is mapped to address 0x0000_0000. This mapping of **nCS0** and SDRAMDevCfg3 does not change until the chip is reset.*

SDRAMDevCfgx

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD							Auto Precharge	RSVD		RasToCas		WBL	CasLat		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								SFConfig Addr	2K PAGE	SROMLL	SROM512	Bank Count	1	RSVD	

Address:

SDRAMDevCfg0: 0x8006_0010 - Read/Write
SDRAMDevCfg1: 0x8006_0014 - Read/Write
SDRAMDevCfg2: 0x8006_0018 - Read/Write
SDRAMDevCfg3: 0x8006_001C - Read/Write

Default:

0x0122_0008

Definition:

The four device configuration registers define the characteristics of the external Synchronous Memory devices connected to each of the four Synchronous Memory chip select lines. This allows for different device characteristics in each region.

The values set in these registers must correspond with the values programmed into the SDRAM/SROM device mode registers for correct operation. Changes made to these registers only have an effect when the Synchronous Memory controller becomes or is idle to ensure that the Synchronous Memory engine remains synchronized to the state of the synchronous memory. The Synchronous device Mode registers should only be changed when interrupts and DMA operations are disabled to ensure correct programming results.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

AutoPrecharge: 0 - No auto pre-charge
1 - Auto pre-charge

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RasToCas: Synchronous Memory RAS to CAS Latency
00 - Reserved
01 - Reserved
10 - RAS latency = 2
11 - RAS latency = 3
Defaults to RAS latency of 2 to support booting from SROM

Note: RasToCas has one additional clock cycle over the programmed value when performing a Write operation.

WBL: Write Burst Length (See Note, below)
0 - Same as Read Burst Length (that is, 4)
1 - Burst Read but Single Writes (for Sync FLASH support). No refresh to the bank. Setting this bit, SDRAM controller will not support burst write access from the AHB bus. If there is burst write from AHB with WBL=1, data loss may occur. It is intended to support SyncFLASH in this mode.

Note: In order to program sync FLASH memories that do not support Burst writes, you must perform single word writes to the FLASH device using the "str" ARM assembly instruction. Setting WBL will not prevent a burst writes if an "stm" instruction is used. Also, only use the ARM bus master to perform writes to syncFLASH.

CasLat: Synchronous Memory CAS Latency
Defaults to CAS latency of 3 unless booting from SROM, when it is 5.

CasLat[2:0]	Cas Latency
000	Reserved
001	2
010	3 - Default
011	4
100	5 - boot from SROM
101	6
110	7
111	8

SFConfigAddr: Configuration Address Register Read
0 Normal operation
1 Reading of Config. Addr. Reg. of SyncFLASH.

Note: While reading Configuration Address register, the AP bit (bit 24) of this register should be cleared.

2KPAGE: Synchronous Memory 2 KByte Page mode
0 - Sync Memory page depth, not 2 KByte Page mode
1 - Sync Memory has page depth of 2 KByte

Note: Only one of SROM512, SROMLL and 2KPAGE bits (4, 5 and 6) can be set at

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any one time. With the exception of SROMLL, they always operate in 32-bit data width mode regardless of the setting of External Bus Width (bit 2).

SROMLL: SROM Lookalike mode
When this bit is set the muxing will swap its Bank BA0 and BA1 pin signals with Synchronous address pins A12 and A13 respectively. This will allow a Synchronous FLASH to mimic a SROM device. Note that this also uses Bit 2 to determine the data width and *must* be set for 16 bit memory devices.

Note: Only one of SROM512, SROMLL and 2KPAGE bits (4, 5 and 6) can be set at any one time. With the exception of SROMLL, they always operate in 32-bit data width mode regardless of the setting of External Bus Width (bit 2).

SROM512: SROM maximum burst size = 512
0 - Sync memory does not have page depth of 512
1 - Sync Memory has page depth of 512

Note: Only one of SROM512, SROMLL and 2KPAGE bits (4, 5 and 6) can be set at any one time. With the exception of SROMLL, they always operate in 32-bit data width mode regardless of the setting of External Bus Width (bit 2).

BankCount: BankCount indicates the number of banks in SDRAM on SDRAMDevCfgx
1 - Four-bank devices
0 - Two-bank devices

1: Must be written to “1”.

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Chapter 11

UART1 With HDLC and Modem Control Signals

11

11.1 Introduction

UART1 is the collection of a UART block along with a block to support a 9 pin modem interface and a block to support synchronous and asynchronous HDLC protocol support for full duplex transmit and receive. The following sections address each of these blocks.

11.2 UART Overview

Transmit and Receive data transfers through UART1 can either be managed by the DMA, interrupt driven, or CPU polled operations. A loopback control bit is available to enable system testing by routing the transmit data stream into the receiver.

The UART performs:

- Serial-to-parallel conversion on data received from a peripheral device.
- Parallel-to-serial conversion on data transmitted to the peripheral device.

The CPU reads and writes data and control/status information via the AMBA APB interface. The transmit and receive paths are buffered with internal FIFO memories allowing up to 16 bytes to be stored independently in both transmit and receive modes.

The UART:

- Includes a programmable baud rate generator which generates a common transmit and receive internal clock from the UART internal reference clock input, UARTCLK.
- Offers similar functionality to the industry-standard 16C550 UART device.
- Supports baud rates of up to 115.2 Kbits/s and beyond, subject to UARTCLK reference clock frequency.

The UART operation and baud rate values are controlled by the line control register (UART1LinCtrl).

The UART can generate:

- Four individually-maskable interrupts from the receive, transmit and modem status logic blocks.
- A single combined interrupt so that the output is asserted if any of the

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individual interrupts are asserted and unmasked.

If a framing, parity or break error occurs during reception, the appropriate error bit is set, and is stored in the FIFO. If an overrun condition occurs, the overrun register bit is set immediately and FIFO data is prevented from being overwritten.

The FIFOs can be programmed to be 1 byte deep providing a conventional double-buffered UART interface.

The modem status input signals Clear To Send (**CTS**), Data Carrier Detect (**DCD**) and Data Set Ready (**DSR**) are supported. The additional modem status input Ring Indicator (**RI**) is not supported. Output modem control lines, such as Request To Send (**RTS**) and Data Terminal Ready (**DTR**), are not explicitly supported. Note that the separate modem block described later in this chapter does provide support for **RI**, **RTS**, and **DTR**.

11.2.1 UART Functional Description

A diagrammatic view of the UART is shown in Figure 11-1.

11.2.1.1 AMBA APB Interface

The AMBA APB interface generates read and write decodes for accesses to status and control registers and transmit and receive FIFO memories.

The AMBA APB is a local secondary bus which provides a low-power extension to the higher bandwidth Advanced High-performance Bus (AHB) within the AMBA system hierarchy. The AMBA APB groups narrow-bus peripherals to avoid loading the system bus and provides an interface using memory-mapped registers which are accessed under program control.

11.2.1.2 DMA Block

The DMA interface passes data between the UART FIFOs and an external DMA engine as an alternative to AMBA APB accesses. (See Chapter 7, “DMA Controller” on page 213 for additional details.) It may be configured to automatically move characters from the DMA engine to the transmit FIFO and from the receive FIFO to the DMA engine. The DMA engine may also indicate certain error conditions in the receive data to the DMA engine. Note that the DMA interface only supports 8-bit accesses to the FIFOs; status information in the receive FIFO is not passed to the DMA engine.

The UART1DMACtrl register controls the private interface between the DMA engine and the UART. Setting bit TXDMAE enables the transmit channel, while setting bit RXDMAE enables the receive channel. Setting bit DMAERR allows the UART to communicate certain error conditions to the DMA engine via RxEnd on the DMA channel. These conditions include receiving a break, a parity error, or a framing error. Note that configuration of the DMA channels in the DMA engine is also required for DMA operation with the UART.

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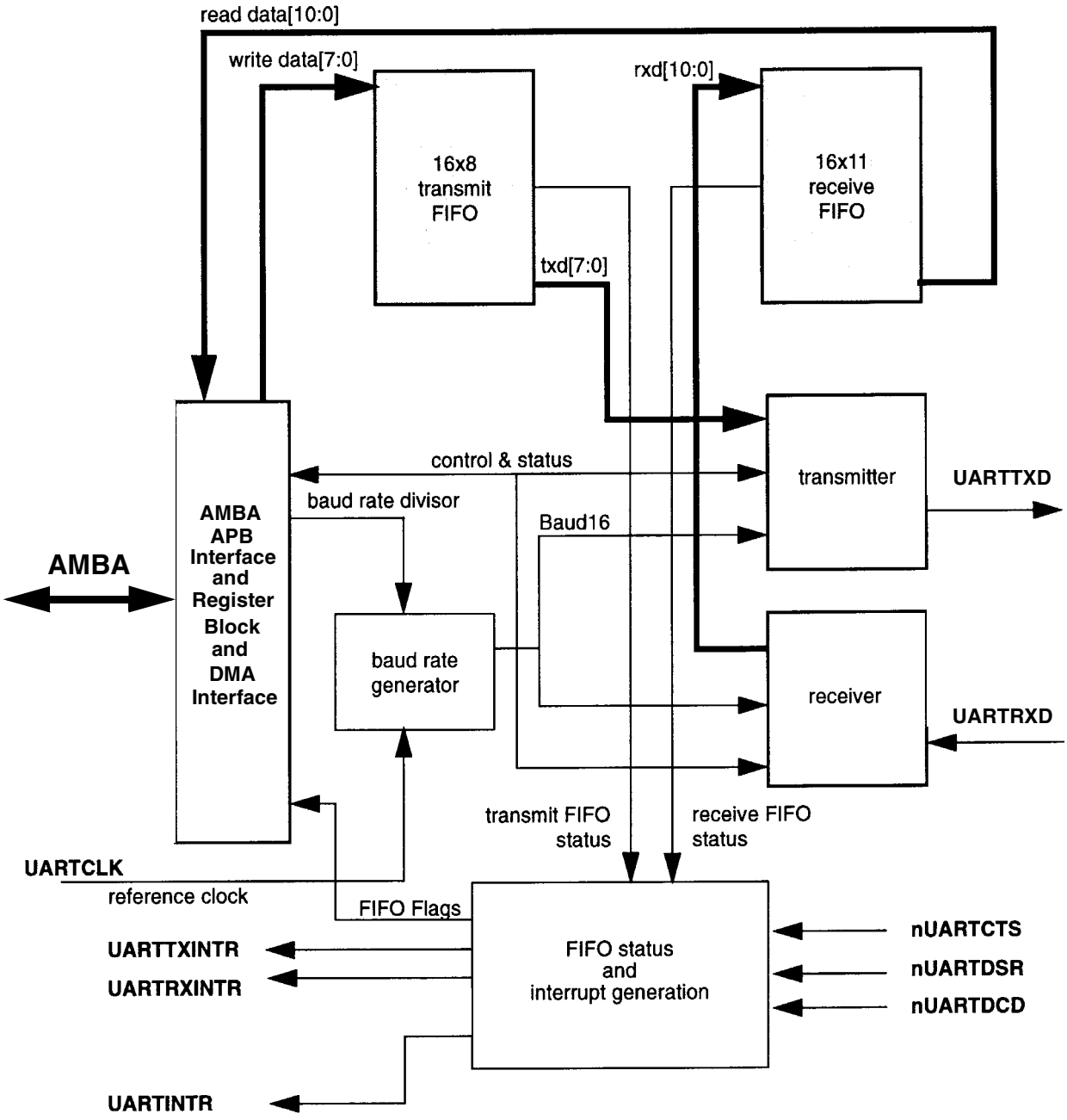
11.2.1.3 Register Block

The register block stores data written or to be read across the AMBA APB interface.

Figure 11-1. UART Block Diagram



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11.2.1.4 Baud Rate Generator

The baud rate generator contains free-running counters which generate the internal x16 clocks and the Baud16 signal. Baud16 provides timing information for UART transmit and receive control. Baud16 is a stream of pulses with a width of one UARTCLK clock period and a frequency of sixteen times the baud rate.

11.2.1.5 Transmit FIFO

The transmit FIFO is an 8-bit wide, 16-entry deep, first-in, first-out memory buffer. CPU data written across the APB interface and data written across the DMA interface is stored in the FIFO until read out by the transmit logic. The transmit FIFO can be disabled to act as a one-byte holding register.

11.2.1.6 Receive FIFO

The receive FIFO is an 11-bit wide, 16-entry deep, FIFO memory buffer. Received data, and corresponding error bits, are stored in the receive FIFO by the receive logic until read out by the CPU across the APB interface or across the DMA interface. The FIFO can be disabled to act as a one-byte holding register.

11.2.1.7 Transmit Logic

The transmit logic performs parallel-to-serial conversion on the data read from the transmit FIFO. Control logic outputs the serial bit stream beginning with a start bit, data bits, least significant bit (LSB) first, followed by parity bit, and then stop bits according to the programmed configuration in control registers.

11.2.1.8 Receive Logic

The receive logic performs serial-to-parallel conversion on the received bit stream after a valid start pulse has been detected. Parity, frame error checking and line break detection are also performed, and the data with associated parity, framing and break error bits is written to the receive FIFO.

11.2.1.9 Interrupt Generation Logic

Four individual maskable active HIGH interrupts are generated by the UART, and a combined interrupt output is also generated as an OR function of the individual interrupt requests.

The single combined UART interrupt (**UARTINTR**) is routed to the system interrupt controller. In addition, a separate receive FIFO interrupt **UARTRXINTR** and a transmit FIFO interrupt **UARTTXINTR** are routed to the system interrupt controller. (See Chapter 5, “Vectored Interrupt Controller” on page 99 for additional details.) Separate receive and transmit FIFO status signals indicate to the DMA interface when there is room in the transmit FIFO for more data and when there is data in the receive FIFO.

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11.2.1.10 Synchronizing Registers and Logic

The UART supports both asynchronous and synchronous operation of the clocks, PCLK and UARTCLK. Synchronization registers and handshaking logic have been implemented, and are active at all times. This has a minimal impact on performance or area. Synchronization of control signals is performed on both directions of data flow, that is, from the PCLK to the UARTCLK domain and from the UARTCLK domain to the PCLK.

11.2.2 UART Operation

Control data is written to the UART line control register, UARTLCR. This register is 23 bits wide internally, but is externally accessed through the AMBA APB bus by three 8-bit wide register locations, UARTLCR_H, UARTLCR_M and UARTLCR.L.

UARTLCR defines the baud rate divisor and transmission parameters, word length, buffer mode, number of transmitted stop bits, parity mode and break generation.

The baud rate divisor is a 16-bit number used by the baud rate generator to determine the bit period. The baud rate generator contains a 16-bit down counter, clocked by the UART reference clock. When the value of the baud rate divisor has decremented to zero, the value of the baud rate divisor is reloaded into the down counter, and an internal clock enable signal, Baud16, is generated. This signal is then divided by 16 to give the transmit clock. A low number in the baud rate divisor gives a short bit period and vice versa.

Data received or transmitted is stored in two 16-byte FIFOs, though the receive FIFO has an extra three bits per character for status information.

For transmission, data is written into the transmit FIFO. This causes a data frame to start transmitting with the parameters indicated in UARTLCR. Data continues to be transmitted until there is no data left in the transmit FIFO. The **BUSY** signal goes HIGH as soon as data is written to the transmit FIFO (that is, the FIFO is non-empty) and remains asserted HIGH while data is being transmitted. **BUSY** is negated only when the transmit FIFO is empty, and the last character has been transmitted from the shift register, including the stop bits. **BUSY** can be asserted HIGH even though the UART may no longer be enabled.

When the receiver is idle (**UARTRXD** continuously 1, in the marking state) and a LOW is detected on the data input (a start bit has been received), the receive counter, with the clock enabled by Baud16, begins running and data is sampled on the eighth cycle of that counter (half way through a bit period).

The start bit is valid if **UARTRXD** is still LOW on the eighth cycle of Baud16, otherwise a false start bit is detected and it is ignored.

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If the start bit was valid, successive data bits are sampled on every 16th cycle of Baud16 (that is, one bit period later) according to the programmed length of the data characters. The parity bit is then checked if parity mode was enabled.

Lastly, a valid stop bit is confirmed if **UARTRXD** is HIGH, otherwise a framing error has occurred. When a full word has been received, the data is stored in the receive FIFO, with any error bits associated with that word (see Table 2-1).

11.2.2.1 Error Bits

Three error bits are stored in bits [10:8] of the receive FIFO, and are associated with a particular character. There is an additional error which indicates an overrun error but it is not associated with a particular character in the receive FIFO. The overrun error is set when the FIFO is full and the next character has been completely received in the shift register. The data in the shift register is overwritten but it is not written into the FIFO.

Table 11-1: Receive FIFO Bit Functions

FIFO bit	Function
10	Break error
9	Parity error
8	Framing error
7:0	Received data

11.2.2.2 Disabling the FIFOs

Additionally, it is possible to disable the FIFOs. In this case, the transmit and receive sides of the UART have 1-byte holding registers (the bottom entry of the FIFOs). The overrun bit is set when a word has been received and the previous one was not yet read. In this implementation, the FIFOs are not physically disabled, but the flags are manipulated to give the illusion of a 1-byte register.

11.2.2.3 System/diagnostic Loopback Testing

It is possible to perform loopback testing for UART data by setting the Loop Back Enable (LBE) bit to 1 in the control register UARTxCtrl (bit 7).

Data transmitted on **UARTTXD** output will be received on the **UARTRXD** input.

11.2.2.4 UART Character Frame

The UART character frame is shown in Figure 11-2:

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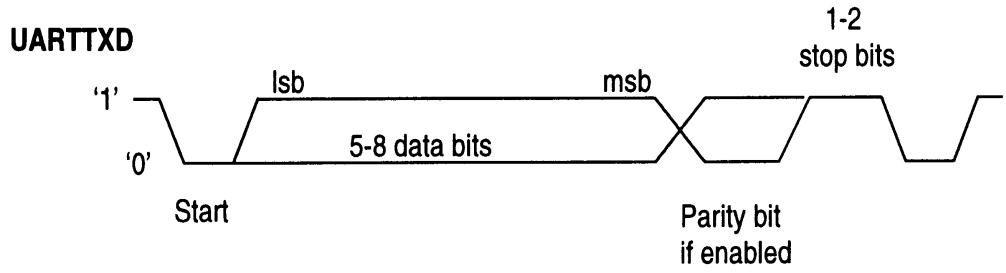
Figure 11-2. UART Character Frame



11.2.3 Interrupts

There are five interrupts generated by the UART. Four of these are individual maskable active HIGH interrupts:

- **UARTMSINTR**
- **UARTRXINTR**
- **UARTRTINTR**
- **UARTTXINTR**

The interrupts are also output as a combined single interrupt **UARTINTR**.

Each of the four individual maskable interrupts is enabled or disabled by changing the mask bits in UARTCR. Setting the appropriate mask bit HIGH enables the interrupt.

The transmit and receive dataflow interrupts **UARTRXINTR** and **UARTTXINTR** have been separated from the status interrupts. This allows **UARTRXINTR** and **UARTTXINTR** to be used in a DMA controller, so that data can be read or written in response to just the FIFO trigger levels. The status of the individual interrupt sources can be read from UARTIIR.

11.2.3.1 UARTMSINTR

The modem status interrupt is asserted if any of the modem status lines (**nUARTCTS, nUARTDCD** and **nUARTDSR**) change. It is cleared by writing to the UART1IntIDIntClr register.

This interrupt is not independently connected to the system interrupt controller.

11.2.3.2 UARTRXINTR

The receive interrupt changes state when one of the following events occurs:

If the FIFOs are enabled and the receive FIFO is half or more full (it contains eight or more words), then the receive interrupt is asserted HIGH. The receive interrupt is cleared by reading data from the receive FIFO until it becomes less than half full.

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If the FIFOs are disabled (have a depth of one location) and data is received thereby filling the location, the receive interrupt is asserted HIGH. The receive interrupt is cleared by performing a single read of the receive FIFO.

This interrupt is connected to the system interrupt controller.

11.2.3.3 UARTTXINTR

The transmit interrupt changes state when one of the following events occurs:

- If the FIFOs are enabled and the transmit FIFO is at least half empty (it has space for eight or more words), then the transmit interrupt is asserted HIGH. It is cleared by filling the transmit FIFO to more than half full.
- If the FIFOs are disabled (have a depth of one location) and there is no data present in the transmitters single location, the transmit FIFO is asserted HIGH. It is cleared by performing a single write to the transmitter FIFO.

The transmit interrupt **UARTTXINTR** is not qualified with the UART Enable signal, which allows operation in one of two ways. Data can be written to the transmit FIFO prior to enabling the UART and the interrupts. Alternatively, the UART and interrupts can be enabled so that data can be written to the transmit FIFO by an interrupt service routine.

This interrupt is connected to the system interrupt controller.

11.2.3.4 UARTRTINTR

The receive timeout interrupt is asserted when the receive FIFO is not empty and no further data is received over a 32-bit period. The receive timeout interrupt is cleared when the FIFO becomes empty through reading all the data (or by reading the holding register).

This interrupt is not independently connected to the system interrupt controller.

11.2.3.5 UARTINTR

The interrupts are also combined into a single output which is an OR function of the individual masked sources. This output is connected to the system interrupt controller to provide another level of masking on a individual peripheral basis. The combined UART interrupt is asserted if any of the four individual interrupts above are asserted and enabled.

11.3 Modem

The modem hardware adds modem control signals **RTSn**, **DTRn**, and **RI**. Two modem support registers provide a 16550 compatible modem control interface.

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11.4 HDLC

The HDLC receiver handles framing, address matching, CRC checking, control-octet transparency or bit-stuffing, and optionally passes the CRC to the CPU at the end of the packet. The HDLC transmitter handles framing, CRC generation, and control-octet transparency or bit-stuffing. The CPU must assemble the frame in memory before transmission. The HDLC receiver and transmitter use the UART FIFOs to buffer the data streams.

When entering HDLC mode, always enable HDLC transmit and/or receive first by setting the TXE and/or RXE bit in the UART1HDLCCtrl, and then enable the UART. When leaving HDLC mode, disable the UART first, and then disable HDLC transmit and/or receive by clearing the TXE and/or RXE bit. This insures that no bytes are sent by the UART transmitter without proper HDLC framing, and that no bytes are received via the UART receiver without proper HDLC decoding. In HDLC mode, the UART should be configured to use 8-bit characters and no parity bit.

11.4.1 Overview of HDLC Modes

HDLC may operate in one of two basic modes, synchronous or asynchronous. Most configuration options affect both modes identically. Setting the UART1HDLCCtrl.SYNC bit selects synchronous mode and clearing it selects asynchronous mode. In asynchronous mode, each byte is transmitted using standard UART protocol framing (that is, start bit, data, parity, stop bit(s)). In synchronous mode, UART framing is bypassed.

The synchronous HDLC bit stream may be either a NRZ or Manchester encoded. In NRZ mode, both the transmitter and receiver may be synchronized to either an external or internal clock running at one cycle per bit period. The transmitter and receiver may operate independently in any of the four modes:

- Simple NRZ mode
- Manchester encoded
- NRZ mode with an internal clock
- NRZ mode with an external clock

In the first NRZ mode, the data stream does not contain an explicit or implicit clock, so synchronization between an HDLC transmitter and receiver cannot be guaranteed. A data bit value of “1” is encoded as a one in the bit stream, and a value of “0” as a zero.

The second mode, Manchester encoding, combines the HDLC data and clock into a single bit stream. In Manchester encoding, a transition always occurs in the middle of a transmitted bit and the value after this transition is the actual value of the bit. That is, a “0” bit is represented by a transition from high to low, and a “1” bit by a transition from low to high. Because a transition always

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occurs in the middle of a bit, the receiver can always extract the proper data after a suitable period of synchronization, provided the signal quality is good.

The third and fourth modes utilize NRZ encoding of the data accompanied by a separate clock signal. The period of the clock signal is one bit period. When using an internal clock, the HDLC transmitter generates a clock such that the data is stable at the clock's rising edge. Hence, an external receiver may sample each data bit at the rising edge of the clock. The internal receiver will also use the same clock to sample input data if programmed to do so.

The internal transmitter and/or receiver may also synchronize to an external, rather than internal, clock. The internal receiver gets this clock along with the incoming HDLC data, allowing it to always sample bits at the right time. In addition, the internal transmitter will synchronize the data it transmits to this clock if programmed to do so. The transmitter will insure that its data is valid before the rising edge of the clock, and the receiver expects the same of the incoming bit stream.

11.4.2 Selecting HDLC Modes

By default, HDLC is NRZ-encoded. Set bit UART1HDLCCtrl.TXENC to force Manchester encoding in the transmitter, and set bit UART1HDLCCtrl.RXENC to make the receiver expect Manchester encoding.

The receiver utilizes a digital PLL to synchronize to the incoming encoded bit stream. The digital PLL should always successfully lock on to an incoming data stream within two bytes provided that the first two bits of the first byte are either "01" or "10". Hence, at a minimum, two bytes must precede the final opening flag to insure that the HDLC receiver sees the packet. To meet this requirement, the simplest approach is to insure that at least three opening flags are received if the packet is Manchester encoded. (Note that to meet this requirement when transmitting, field HDLC1Ctrl.FLAG should be set to 0010b.)

Three bits in various combination determine how an external or internal clock may be used along with NRZ data. The clock will have a period equal to the bit period of the data stream, and it is expected that the internal or external receiver will sample the bit at or near the rising edge of this clock.

To generate an internal clock suitable for sending along with the transmitted data, set UART1HDLCCtrl.TXCM and UART1HDLCCtrl.CMAS. To make the receiver use the same internal clock, set UART1HDLCCtrl.RXCM. To make the receiver use an externally generated clock, clear UART1HDLCCtrl.CMAS, but set UART1HDLCCtrl.RXCM.

To force the transmitter to use the same external clock, also set UART1HDLCCtrl.TXCM. The clock is either internal or external, that is, the receiver cannot use an external clock while the transmitter generates and sends an internal one. Refer to the documentation for the DeviceCfg register

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in Syscon for the use and routing of HDLC clocks to or from external pins on the device.

The internal clock is generated by the transmitter only while it is sending data or flags; the clock is not generated while the transmitter is idle. For this reason, another transmitter which expects to use this clock to at any time send its own packets cannot reliably do so. To insure that a clock is continuously generated, the IDLE bit in the UART1HDLCCtrl register may be set, which causes this transmitter to continously send flags between packets instead of going idle.

Table 11-2 summarizes the legal HDLC mode configurations.

Table 11-2: Legal HDLC Mode Configurations

UART1HDLCCtrl Bits Set						Transmit Mode	Receive Mode
CMAS	TXCM	RXCM	TXENC	RXENC	SYNC		
-	-	-	-	-	-	Asynchronous NRZ	Asynchronous NRZ
-	-	-	-	-	1	Synchronous NRZ	Synchronous NRZ
-	-	-	-	1	1	Synchronous NRZ	Manchester
-	-	-	1	-	1	Manchester	Synchronous NRZ
-	-	-	1	1	1	Manchester	Manchester
-	-	1	-	-	1	Synchronous NRZ	External clock
-	-	1	1	-	1	Manchester	External clock
-	1	-	-	-	1	External clock	Synchronous NRZ
-	1	-	-	1	1	External clock	Manchester
1	1	-	-	-	1	Internal clock	Synchronous NRZ
1	1	-	-	1	1	Internal clock	Manchester
-	1	1	-	-	1	External clock	External clock
1	1	1	-	-	1	Internal clock	Internal clock

11.4.3 HDLC Transmit

In normal operation, the HDLC transmitter either continuously sends flags or holds the transmit pin in a marking state, depending on the setting of the UART1HDLCCtrl.IDLE bit. When data appears in the transmit FIFO, it begins sending a packet. If in the marking state, it sends from 1 to 16 opening flags, as specified by the UART1HDLCCtrl.FLAG field. If already sending flags, it ensures that at least the specified number have been sent. It then begins sending the bytes in the FIFO, inserting and modifying the data depending on the HDLC mode.

In asynchronous HDLC, the transmitter enforces control-octet transparency. Whenever a flag byte (01111110b) or an escape byte (01111101b) appears in the data, the transmitter inverts the fifth bit and precedes it with an escape byte.

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In synchronous HDLC, the transmitter performs bit-stuffing (except for flags). Whenever five consecutive “1” bits appear in the transmitted bit stream, a “0” bit is inserted, preventing six ones from appearing consecutively.

When the transmit FIFO underruns, the HDLC transmitter does one of two things (depending on the setting of the UART1HDLCCtrl.TUS bit). If the TUS bit is zero, the transmitter first sends the CRC (if CRC is enabled) and then sends from 1 to 16 closing flags, as specified in the UART1HDLCCtrl.FLAG field, terminating the packet.

If TUS is one, the transmitter aborts the packet. In synchronous HDLC, it sends a byte of all ones (since seven consecutive ones signifies an abort), following by at least one closing flag. In asynchronous HDLC, it sends an escape and then at least one closing flag. The number of closing flags is from 1 to 16, as specified in the UART1HDLCCtrl.FLAG field.

When a packet ends, the UART1HDLCSts.TFC bit is set, and if UART1HDLCCtrl.TFCEN is set, an interrupt is generated. When a packet is aborted, the UART1HDLCCtrl.TAB bit is set, also generating an interrupt if UART1HDLCCtrl.TABEN is set.

11.4.4 HDLC Receive

The HDLC receiver continuously reads bytes from the UART receiver until it finds a flag followed by a byte other than a flag. Then, if in asynchronous mode, it processes the incoming bytes (including the first after the flag), reversing control-octet transparency, or, if in synchronous mode, it reverses bit-stuffing. Processed bytes are placed in the receive FIFO. When programmed to receive a Manchester encoded bit stream, UART1HDLCSts.PLLCS indicates whether the DPLL in the receiver has locked on to the carrier.

When the last byte of data for a packet is read from the receive FIFO, the HDLC logic sets a number of bits in the UART1HDLCSts depending on the state of the system and the way the packet was terminated. In all cases, the RFC bit and EOF bit are set. If the receive FIFO overflowed while the packet was being received, the ROR bit is also set. If CRC is enabled and the received CRC does not match the calculated one, the CRE bit is set. The RFC bit is set and, if UART1HDLCCtrl.RFCEN is set, an interrupt is generated. If the packet was aborted, the RAB bit is set, and an interrupt generated if the UART1HDLCCtrl.RABEN bit is set. If using Manchester encoding and the packet was aborted due to losing synchronization with the encoded clock, the UART1HDLCCtrl.PLLE bit is set.

Besides setting bits in the UART1HDLCSts and possibly causing interrupts, reading the last byte of a packet also loads the UART1HDLCRXInfoBuf register with data describing the packet. BRAB, BCRE, BROR, and BPLLE are copied from RAB, CRE, ROR, and PLLE in the UART1HDLCSts. BFRE is copied from the FE bit in the UART1RXSts. BC is set to the number of bytes in

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the packet that were read from the FIFO. Whenever this register is written by the receiver and has not been read since previously it was previously written, the UART1HDLCSts.RIL bit is set, and, if UART1HDLCSts.RILEN is set, an interrupt is generated.

If a new packet is received and the first byte of that packet cannot be written into the receive FIFO because it has overflowed, the UART1HDLCSts.RFL bit is set and the packet is discarded. An interrupt is generated if the UART1HDLCCtrl.RFLEN bit is also set.

11.4.5 CRCs

Several bits in the UART1HDLCCtrl determine how CRCs are generated by the transmitter and processed by the receiver. By setting the CRCE bit, the HDLC transmitter will calculate and append a CRC to each packet. The CRC may be either 16-bit or 32-bit, depending on the CRCS bit. Furthermore, it will be inverted prior to transmission if the CRCN bit is set. If CRCs are enabled, the receiver will expect the same type of CRC that the transmitter sends. It will automatically calculate the CRC for the received packet in the fly, and if the calculated CRC does not match the received one, the UART1RXSts.CRE bit will be set when the last byte of the received packet is read from the UART1Data. The receiver does not pass the CRC to the CPU unless the CRCApd bit is set.

11.4.6 Address Matching

When address matching is enabled, the HDLC receiver will ignore any packet whose address does not match the programmed configuration. Address matching is enabled and address size specified by the UART1HDLCCtrl.AME bits. The UART1HDLCAddMtchVal specifies the addresses that are compared while the UART1HDLCAddMask controls which bits in each address are compared If one-byte addressing is used, each byte in UART1HDLCAddMtchVal specifies an address to match, while the corresponding byte in UART1HDLCAddMask specifies which bits of each address must match. If two-byte addressing is used, each halfword in UART1HDLCAddMtchVal specifies an address to match and the corresponding halfword in UART1HDLCAddMask specifies which bits of each address to match. Hence, up to four different one-byte addresses and two different two-byte addresses may be specified. An incoming address consisting entirely of “1”s, that is, 0xFF or 0xFFFF, will always match, as it is expected to be the broadcast address. For packets whose addresses do not match, the HDLC receiver will generate no interrupts, modify no status bits, and place no data in the receive FIFO.

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Table 11-3: HDLC Receive Address Matching Modes

AME	Match Function	Address Match Test
00	No matching	
01	One byte address	***NOT***((AMV[31:24] ***XOR*** ADDR) ***AND*** AMSK[31:24]) ***OR*** ***NOT***((AMV[23:16] ***XOR*** ADDR) ***AND*** AMSK[23:16]) ***OR*** ***NOT***((AMV[15:8] ***XOR*** ADDR) ***AND*** AMSK[15:8]) ***OR*** ***NOT***((AMV[7:0] ***XOR*** ADDR) ***AND*** AMSK[7:0]) ***OR*** ADDR = 0xFF
10	Two byte address	***NOT***((AMV[31:16] ***XOR*** ADDR) ***AND*** AMSK[31:16]) ***OR*** ***NOT***((AMV[15:0] ***XOR*** ADDR) ***AND*** AMSK[15:0]) ***OR*** ADDR = 0xFFFF
11	Undefined	

11.4.7 Aborts

If a packet is aborted or is too short, or if using Manchester encoding and the receiver DPLL loses the carrier signal, the CPU will see at least some part of the packet in the receive FIFO. In all cases, reading the last byte of the packet from the receive FIFO will set the EOF and RAB bits in the UART1HDLCSts (and possibly generate an interrupt). In the case of an abort indicated by an HDLC transmitter, that is, an escape-closing flag sequence in asynchronous mode or an all “1”s byte in synchronous mode, all bytes received in the frame will appear in the receive FIFO.

In asynchronous mode, if the abort is caused by a framing error (a missing stop bit), all bytes up to and including the misframed byte will appear in the receive FIFO. Reading the last byte will also set the UART1HDLCSts.FRE bit.

In synchronous mode, if the abort is caused by a misaligned flag or a series of seven consecutive “1”s, all bytes except the one containing the bit after the sixth “1” will appear in the receive FIFO. If the abort is caused by the receiver DPLL losing synchronization with a Manchester encoded bit stream, the UART1HDLCSts.DPLLE bit is set.

Finally, if the packet is too short, that is, there are not enough received bytes to hold the specified number of address and CRC bytes, the entire packet will appear in the receive FIFO. In all cases, the packet is illegal and will be ignored by the CPU.

11.4.8 DMA

The DMA engine may be used with the UART when transmitting and receiving HDLC packets. The transmit and receive channels may operate completely independently.

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When receiving data in HDLC mode, the DMA channel reads the packet data byte by byte from the RX FIFO. When it reads the final byte, the HDLC RFC interrupt will occur if enabled. However, the DMA channel, which buffers the data, may not write all of the data to memory. To insure that the DMA channel dumps the data, the interrupt handling routine must do the following:

1. Note the values in the MAXCNTx and REMAIN registers for the DMA channel. The difference is the number of bytes read from the UART, which is the size of the HDLC packet. Call this difference N. Note that the BC field of the UART1HDLCRXInfoBuf register should also be N.
2. Temporarily disable the UART DMA RX interface by clearing the RXDMAE bit in the UART1DMACtrl register.
3. Wait until the difference between the CURRENTx and BASEx registers in the DMA channel is equal to N + 1.

An extra byte will be read from the UART by the DMA channel. It should be ignored.

Note that if the DMAERR bit in the UART1DMACtrl register is set and the HDLC receiver is in asynchronous mode, if the receiver sees a break, parity, or framing error, it will indicate an error condtion via RxEnd on the DMA channel.

11.4.9 Writing Configuration Registers

It is assumed that various configuration registers for the UART/HDLC are not written more than once in quick succession, in order to insure proper synchronization of configuration information across the implementation. Such registers include UART1Ctrl and UART1LinCtrlHigh as well as UART1HDLCCtrl, UART1HDLCAddMtchVal, UART1HDLCAddMask. These registers should not change often in typical use.

The simplest way to fulfill this requirement with respect to writing the UART1Ctrl and UART1HDLCCtrl registers is to insure that the HDLC transmitter is enabled before the UART transmit logic. This will ensure that the UART does not transmit incorrect characters or unexpectedly transmit characters with UART framing,

First the UART1HDLCCtrl register should be written, setting the TXE bit. Then the UART1Ctrl register should be written, setting the UARTE bit. In between the two writes, at least two UARTCLK periods must occur. Under worst case conditions, at least 55 HCLK periods must separate the two writes. The simplest way to due this is separate the two writes by 55 NOPs.

11.5 UART1 Package Dependency

UART1 uses package pins **RXD0**, **TXD0**, **CTSn**, **DSRn**, **DTRn**, **RTSn**, **EGPIO[3]**, and **EGPIO[0]**, which are described in Table 11-4.

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Table 11-4: UART1 Pin Functionality

PIN	Description
RXD0	UART1 input pin
TXD0	UART1 output pin
CTSn	Modem input: Clear To Send
DSRn	Modem input: Data Set Ready (also used for DCDn Data Carrier Detect)
EGPIO[0]	Modem input RIn: Ring Indicator if Syscon register DeviceCfg[25] MODonGPIO is set. Otherwise, RIn is driven low.
DTRn	Modem output Data Terminal Ready if Syscon register TESTCR[27] RTConGPIO is clear.
RTSn	Modem output: Ready To Send
EGPIO[3]	HDLC clock

The use of **EGPIO[3]** is determined by several bits in Syscon register DeviceCfg. See Table 11-5.

Table 11-5: DeviceCfg Register Bit Functions

bit 13 HC1IN	bit 12 HC1EN	Function
0	x	External HDLC clock input is driven low.
1	1	External HDLC clock input is driven by EGPIO[3].
0	1	Internal HDLC clock output drives EGPIO[3].

11.5.1 Clocking Requirements

There are two clocks, PCLK and UARTCLK.

UARTCLK frequency must accommodate the desired range of baud rates:

$$F_{UARTCLK_{MIN}} \geq 32 \times baudrate_{MAX}$$

$$F_{UARTCLK_{MAX}} \leq 32 \times 65536 \times baudrate_{MIN}$$

The frequency of UARTCLK must also be within the required error limits for all baud rates to be used.

To allow sufficient time to write the received data to the receive FIFO, UARTCLK must be less than or equal to four times the frequency of PCLK:

$$F_{UARTCLK} \leq 4 \times F_{PCLK}$$

11.5.2 Bus Bandwidth Requirements

There are two basic ways of moving data to and from the UART FIFOs:

- Direct DMA interface - This permits byte-wide access to the UART without using the APB. The DMA block will pack or unpack individual bytes so that it reads or writes full 32-bit words rather than individual bytes.

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- Accessing the UART via the APB - This requires APB/AHB bus bandwidth. Then, both a read and write are required for each 8-bit data byte.

Bandwidth requirements also depend on the selected baud rate, character size, parity selection, number of stop bits, and spacing between characters (if receiving).

For example, assume transmission protocols of 115,200 baud, 8-bit characters, even parity, one stop bit, no space between characters. There are 11 bits per character, so 115,200 / 11 = 10,473 characters per second. If both transmitting and receiving, 20,945 characters per second pass through the UART. Accessing the UART through the DMA interface requires one access per 32-bits, implying only 20,945 / 4 = 5,236 AHB accesses per second. Accessing the UART through the APB requires two accesses per byte, implying 20,945 APB bus accesses.

As another example, assume 230,400 baud (the maximum with a UARTCLK equal to 7.3728 Mhz), 5-bit characters, no parity, one stop bit, and no space between characters. There are 7 bits per character, so 230,400 / 7 = 32,914 characters per second. Simultaneous transmitting and receiving implies 65,829 characters per second. Using the DMA interface would result in 16,457 AHB accesses per second, while using the APB to access the UART leads to 65,829 bus accesses per second.

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11.6 Registers

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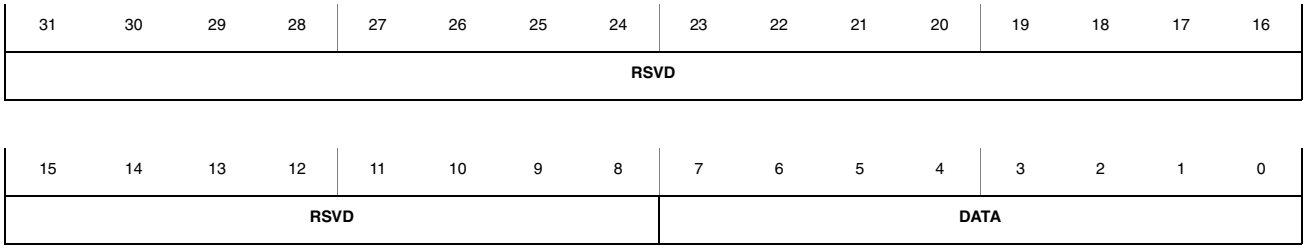
UART Register Descriptions

UART1Data



Address:

0x808C_0000 - Read/Write

Default:

0x0000_0000

Definition:

UART Data Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

DATA: UART Data: read for receive data, write for transmit data
For words to be transmitted:
• if the FIFOs are enabled, data written to this location is pushed onto the transmit FIFO
• if the FIFOs are not enabled, data is stored in the transmitter holding register (the bottom word of the transmit FIFO). The write operation initiates transmission from the UART. The data is prefixed with a start bit, appended with the appropriate parity bit (if parity is enabled), and a stop bit. The resultant word is then transmitted.

For received words:
• if the FIFOs are enabled, the data byte is extracted, and

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a 3-bit status (break, frame and parity) is pushed onto the 11-bit wide receive FIFO
• if the FIFOs are not enabled, the data byte and status are stored in the receiving holding register (the bottom word of the receive FIFO).

The received data byte is read by performing reads from the UART1Data register while the corresponding status information can be read by a successive read of the UART1RXSts register.

UART1RXSts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												OE	BE	PE	FE

Address:

0x808C_0004 - Read/Write

Default:

0x0000_0000

Definition:

UART1 Receive Status Register/Error Clear Register. Provides receive status of the data value last read from the UART1Data. A write to this register clears the framing, parity, break and overrun errors. The data value is not important. Note that BE, PE and FE are not used for synchronous HDLC.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

OE: Overrun Error. This bit is set to “1” if data is received and the FIFO is already full. This bit is cleared to “0” by a write to UART1RXSts. The FIFO contents remain valid since no further data is written when the FIFO is full. Only the contents of the shift register are overwritten. The data must be read in order to empty the FIFO.

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BE: Break Error. This bit is set to 1 if a break condition was detected, indicating that the received data input was held LOW for longer than a full-word transmission time (defined as start, data, parity and stop bits). This bit is cleared to 0 after a write to UART1RXSts. In FIFO mode, this error is associated with the character at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character is only enabled after the receive data input goes to a 1 (marking state) and the next valid start bit is received.

PE: Parity Error. When this bit is set to 1, it indicates that the parity of the received data character does not match the parity selected in UART1LinCtrlHigh (bit 2). This bit is cleared to 0 by a write to UART1RXSts. In FIFO mode, this error is associated with the character at the top of the FIFO.

FE: Framing Error. When this bit is set to 1, it indicates that the received character did not have a valid stop bit (a valid stop bit is “1”). This bit is cleared to 0 by a write to UART1RXSts. In FIFO mode, this error is associated with the character at the top of the FIFO.

UART1LinCtrlHigh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									WLEN		FEN	STP2	EPS	PEN	BRK

Address:

0x808C_0008 - Read/Write

Default:

0x0000_0000

Definition:

UART1 Line Control Register High. UART1LinCtrlHigh, UART1LinCtrlMid and UART1LinCtrlLow form a single 23-bit wide register (UART1LinCtrl) which is updated on a single write strobe generated by an UART1LinCtrlHigh write. In order to internally update the contents of UART1LinCtrlMid or UART1LinCtrlLow, a UART1LinCtrlHigh write must always be performed at the end.

To update the three registers there are two possible sequences:

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- UART1LinCtrlLow write, UART1LinCtrlMid write and UART1LinCtrlHigh write
- UART1LinCtrlMid write, UART1LinCtrlLow write and UART1LinCtrlHigh write.

To update UART1LinCtrlLow or UART1LinCtrlMid only:

- UART1LinCtrlLow write (or UART1LinCtrlMid write) and UART1LinCtrlHigh write.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

WLEN: Number of bits per frame:
11 = 8 bits
10 = 7 bits
01 = 6 bits
00 = 5 bits

FEN: FIFO Enable.
1 - Transmit and receive FIFO buffers are enabled (FIFO mode).
0 - The FIFOs are disabled (character mode) that is, the FIFOs become 1-byte-deep holding registers.

STP2: Two Stop Bits Select.
1 - Two stop bits are transmitted at the end of the frame.
0 - One stop bit is transmitted at the end of the frame.
The receive logic does not check for two stop bits being received.

EPS: Even Parity Select.
1 - Even parity generation and checking is performed during transmission and reception, which checks for an even number of “1”s in data and parity bits.
0 - Odd parity checking is performed, which checks for an odd number of “1”s.
This bit has no effect when parity is disabled by Parity Enable (bit 1) being cleared to 0.

PEN: Parity Enable.
1 - Parity checking and generation is enabled,
0 - Parity checking and generation is disabled and no parity bit is added to the data frame.

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BRK: Send Break.
1 - A low level is continually output on the **UARTTXD** output, after completing transmission of the current character. This bit must be asserted for at least one complete frame transmission time in order to generate a break condition. The transmit FIFO contents remain unaffected during a break condition.
0 - For normal use, this bit must be cleared.

UART1LinCtrlMid

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								BR							

Address:
0x808C_000C - Read/Write

Default:
0x0000_0000

Definition:
UART Line Control Register Middle.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

BR: Baud Rate Divisor bits [15:8]. Most significant byte of baud rate divisor. These bits are cleared to 0 on reset.

UART1LinCtrlLow

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								BR							

Address:
0x808C_0010 - Read/Write

Default:
0x0000_0000

Definition:

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UART Line Control Register Low.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

BR: Baud Rate Divisor bits [7:0]. Least significant byte of baud rate divisor. These bits are cleared to 0 on reset. The baud rate divisor is calculated as follows:

Baud rate divisor
$BAUDDIV = (F_{UARTCLK} / 16 * \text{Baud rate})) - 1$

where $F_{UARTCLK}$ is the UART reference clock frequency. A baud rate divisor of zero is not allowed and will result in no data transfer.

UART1Ctrl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								LBE	RTIE	TIE	RIE	MSIE	RSVD		UARTE

Address:

0x808C_0014 - Read/Write

Default:

0x0000_0000

Definition:

UART1 Control Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

LBE: Loopback Enable. If this bit is set to 1, data sent to **TXD** is received on **RXD**. This bit is cleared to 0 on reset, which disables the loopback mode.

RTIE: Receive Timeout Enable. If this bit is set to 1, the receive timeout interrupt is enabled.

TIE: Transmit Interrupt Enable. If this bit is set to 1, the transmit interrupt is enabled.

RIE: Receive Interrupt Enable. If this bit is set to 1, the receive interrupt is enabled.

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MSIE: Modem Status Interrupt Enable. If this bit is set to 1, the modem status interrupt is enabled.

UARTE: UART Enable. If this bit is set to 1, the UART is enabled. Data transmission and reception occurs for UART signals.

UART1Flag

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								TXFE	RXFF	TXFF	RXFE	BUSY	DCD	DSR	CTS

Address:

0x808C_0018 - Read Only

Default:

0x0000_0000

Definition:

UART Flag Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TXFE: Transmit FIFO Empty. The meaning of this bit depends on the state of the FEN bit in the UART1LinCtrlHigh register. If the FIFO is disabled, this bit is set when the transmit holding register is empty. If the FIFO is enabled, the TXFE bit is set when the transmit FIFO is empty.

RXFF: Receive FIFO Full. The meaning of this bit depends on the state of the FEN bit in the UART1LinCtrlHigh register. If the FIFO is disabled, this bit is set when the receive holding register is full. If the FIFO is enabled, the RXFF bit is set when the receive FIFO is full.

TXFF: Transmit FIFO Full. The meaning of this bit depends on the state of the FEN bit in the UART1LinCtrlHigh register. If the FIFO is disabled, this bit is set when the transmit holding register is full. If the FIFO is enabled, the TXFF bit is set when the transmit FIFO is full.

RXFE: Receive FIFO Empty. The meaning of this bit depends on the state of the FEN bit in the UART1LinCtrlHigh register. If the FIFO is disabled, this bit is set when the receive holding register is empty. If the FIFO is enabled, the RXFE bit is set when the receive FIFO is empty.

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BUSY: UART Busy. If this bit is set to 1, the UART is busy transmitting data. This bit remains set until the complete byte, including all the stop bits, has been sent from the shift register. This bit is set as soon as the transmit FIFO becomes non-empty (regardless of whether the UART is enabled or not).

DCD: Data Carrier Detect status. This bit is the complement of the UART data carrier detect (**nUARTDCD**) modem status input. That is, the bit is 1 when the modem status input is 0.

DSR: Data Set Ready status. This bit is the complement of the UART data set ready (**nUARTDSR**) modem status input. That is, the bit is 1 when the modem status input is 0.

CTS: Clear To Send status. This bit is the complement of the UART clear to send (**nUARTCTS**) modem status input. That is, the bit is 1 when the modem status input is 0.

UART1IntIDIntClr

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												RTIS	TIS	RIS	MIS

Address:

0x808C_001C - Read/Write

Default:

0x0000_0000

Definition:

UART Interrupt Identification and Interrupt Clear Register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RTIS: Receive Timeout Interrupt Status. This bit is set to 1 if the **UARTRTINTR** receive timeout interrupt is asserted. This bit is cleared when the receive FIFO is empty or the receive line goes active.

TIS: Transmit Interrupt Status.
1 - The **UARTTXINTR** transmit interrupt is asserted, which occurs when the transmit FIFO is not full.
0 - The transmit FIFO is full.

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RIS: Receive Interrupt Status.
1 - The **UARTRXINTR** receive interrupt is asserted, which occurs when the receive FIFO is not empty.
0 - The receive FIFO is empty.

MIS: Modem Interrupt Status. This bit is set to 1 if the **UARTMSINTR** modem status interrupt is asserted. This bit is cleared by writing any value to this register.

UART1DMACtrl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													DMAERR	TXDMAE	RXDMAE

Address:
0x808C_0028 - Read/Write

Default:
0x0000_0000

Definition:
UART DMA Control Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

DMAERR: RX DMA error handing enable. If 0, the RX DMA interface ignores error conditions in the UART receive section. If 1, the DMA interface stops and notifies the DMA block when an error occurs. Errors include break errors, parity errors, and framing errors.

TXDMAE: TX DMA interface enable. Setting to 1 enables the private DMA interface to the transmit FIFO.

RXDMAE: RX DMA interface enable. Setting to 1 enables the private DMA interface to the receive FIFO.

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Modem Register Descriptions

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UART1ModemCtrl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								0	0	0	LOOP	OUT2	OUT1	RTS	DTR

Address:

0x808C_0100 - Read/Write

Default:

0x0000_0000

Definition:

Modem Control Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

0: Must be written as “0”.

LOOP: Activate internal modem control loopback function. This internal loopback only affects the hardware handshake signals. Use the UART1Ctrl LBE bit to loopback the serial data.
When high, modem control outputs **RTSn** and **DTRn** are forced high (inactive), and modem control inputs are driven by outputs:
DSR = DTR
CTS = RTS
RI2 = OUT1
DCD = OUT2

OUT2: OUT2 function. Used for internal loopback.

OUT1: OUT1 function. Used for internal loopback.

RTS: RTS output signal:
1 - **RTSn** pin low
0 - **RTSn** pin high

DTR: DTR output signal:
1 - **DTRn** pin low
0 - **DTRn** pin high

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UART1ModemSts

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								DCD	RI	DSR	CTS	DDCD	TERI	DDSR	DCTS

Address:

0x808C_0104 - Read Only

Default:

0x0000_0000

Definition:

Modem Status Register

Bit Descriptions:

RSVD:	Reserved. Unknown During Read.
DCD:	Inverse of **DCDn** input pin. Note that this is identical to the **DSR** device pin.
RI:	Inverse of **RI** input pin.
DSR:	Inverse of the **DSRn** pin. Note that this is identical to the **DCD** device pin
CTS:	Inverse **CTSn** input pin.
DDCD:	Delta **DCD** - **DCDn** pin changed state since last read.
TERI:	Trailing Edge Ring Indicator. **RI** input pin has changed from low to high.
DDSR:	Delta **DSR** - **DSRn** pin has changed state since last read.
DCTS:	Delta **CTS** - **CTSn** pin has changed state since last read.

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HDLC Register Descriptions

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UART1HDLCCtrl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD				CMAS	TXCM	RXCM	TXENC	RXENC	SYNC	TFCEN	TABEN	RFCEN	RILEN	RFLEN	RTOEN

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FLAG				CRCN	CRCApd	IDLE	AME		IDLSpc	CRCZ	RXE	TXE	TUS	CRCE	CRCS

Address:

0x808C_020C - Read/Write

Default:

0x0000_0000

Definition:

HDLC Control Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

CMAS: Clock Master:
1 - Transmitter and/or receiver use 1x clock generated by the internal transmitter.
0 - Transmitter and/or receiver use 1x clock generated externally.

TXCM: Transmit Clock Mode.
1 - Generate 1x clock when in synchronous HDLC mode using NRZ encoding.
0 - Do not generate clock.
This bit has no effect unless TXENC is clear and synchronous HDLC is enabled.

RXCM: Receive Clock Mode.
1 - Use external 1x clock when in synchronous HDLC mode using NRZ encoding.
0 - Do not use external clock.
This bit has no effect unless RXENC is clear and synchronous HDLC is enabled.

TXENC: Transmit Encoding method.
1 - Use Manchester bit encoding.
0 - Use NRZ bit encoding.
This bit has no effect unless synchronous HDLC is enabled

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RXENC: Receive Encoding method.
1 - Use Manchester bit encoding.
0 - Use NRZ bit encoding.
This bit has no effect unless synchronous HDLC is enabled.

SYNC: Synchronous / Asynchronous HDLC Enable.
0 - Select asynchronous HDLC for TX and RX.
1 - Select synchronous HDLC for TX and RX.

TFCEN: Transmit Frame Complete Interrupt Enable.
0 - TFC interrupt will not occur.
1 - TFC interrupt will occur whenever TFC bit is set.

TABEN: Transmit Frame Abort Interrupt Enable.
0 - TAB interrupt will not occur.
1 - TAB interrupt will occur whenever TAB bit is set.

RFCEN: Receive Frame Complete Interrupt Enable.
0 - RFC interrupt will not occur.
1 - RFC interrupt will occur whenever RAB bit or EOF bit is set.

RILEN: Receive Information Lost Interrupt Enable.
0 - RIL interrupt will not occur.
1 - RIL interrupt will occur whenever RIL bit is set.

RFLEN: Receive Frame Lost Interrupt Enable.
0 - RFL interrupt will not occur.
1 - RFL interrupt will occur whenever RFL bit is set.

RTOEN: Receiver Time Out Interrupt Enable.
0 - RTO interrupt will not occur.
1 - RTO interrupt will occur whenever RTO bit is set.

FLAG: Minimum number of opening and closing flags for HDLC TX. The minimum number of flags between packets is this 4-bit value plus one. Hence, 0000b forces at least one opening flag and one closing flag for each packet, and 1111b forces at least 16 opening and closing flags. The closing flags of one packet may also be the opening flags of the next one if the transmit line does not go idle in between. Note that HDLC RX does not count flags; only one is necessary (or three in Manchester mode).

CRCN: CRC polarity control.
0 - CRC transmitted not inverted.
1 - CRC transmitted inverted.

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CRCApd: CRC pass through.
0 - Do not pass received CRC to CPU.
1 - Pass received CRC to CPU.

IDLE: Idle mode.
0 - Idle-in Mark mode - When HDLC is idle (not transmitting starting/stop flags or packets), hold the transmit data pin high.
1 - Idle-in Flag mode - When HDLC is idle, transmit continuous flags.

AME: Address Match Enable. Activates address matching on received frames.
00 - No address matching
01 - 4 x 1 byte matching
10 - 2 x 2 byte matching
11 - Undefined, no matching

IDLSpc: Idle in space
0 - TX idle in mark (normal)
1 - TX idle in space
RX will receive Manchester encoded data whether it idles in mark or space.

CRCZ: CRC zero seed
0 - Seed CRC calculations with all ones; that is, 0xFFFF for 16 bit words and 0xFFFF_FFFF for 32 bit words.
1 - Seed CRC calculations with all zeros.
Applies to both RX and TX.

RXE: HDLC Receive Enable.
0 - Disable HDLC RX. If UART is still enabled, UART may still receive normally.
1 - Enable HDLC RX.

TXE: HDLC Transmit Enable.
0 - Disable HDLC TX. If UART is still enabled, UART may still transmit normally.
1 - Enable HDLC TX.

TUS: Transmit FIFO Underrun Select
0 - TX FIFO underrun causes CRC (if enabled) and stop flag to be transmitted.
1 - TX FIFO underrun causes abort (escape-flag) to be transmitted.

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CRCE: CRC enable.
0 - No CRC is generated by TX or expected by RX.
1 - HDLC TX automatically generates and sends a CRC at the end of a packet, and HDLC RX expects a CRC at the end of a packet.

CRCS: CRC size.
0 - CRC-CCITT (16 bits): $x^{16} + x^{12} + x^5 + 1$
1 - CRC-32: $x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1$
If inverted (see CRCN bit) the CRC-16 check value is 0x1D0F and the CRC-32 check value is 0xC704_DD7B. Otherwise the check value is zero.

UART1HDLCAddMtchVal

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AMV															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AMV															

Address:
0x808C_0210 - Read/Write

Default:
0x0000_0000

Definition:
HDLC Address Match Value

Bit Descriptions:

AMV: Address match value. Supports 8-bit and 16-bit address matching. If UART1HDLCCtrl.AME[1:0] is 00b or 11b, this register is not used.

UART1HDLCAddMask

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
AMSK															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AMSK															

Address:

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0x808C_0214 - Read/Write

Default:

0x0000_0000

Definition:

HDLC Address Mask

Bit Descriptions:

AMSK: Address mask value. Supports 8-bit and 16-bit address masking. If UART1HDLCCtrl.AME[1:0] is 00b or 11b, this register is not used.

UART1HDLCRXInfoBuf

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD														BPLLE	RSVD

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	BC											BFRE	BROR	BCRE	BRAB

Address:

0x808C_0218 - Read Only

Default:

0x0000_0000

Definition:

HDLC Receive Information Buffer Register. This register is loaded when the last data byte in a received frame is read from the receive FIFO. The CPU has until the end of the next frame to read this register, or the RIL bit in the HDLC Status Register is set.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

BPLLE: Buffered Digital PLL Error.
1 - Receiver aborted last frame because DPLL lost the carrier.
0 - Receiver did not abort because DPLL lost the carrier.
This bit is only valid when receiving Manchester-encoded synchronous HDLC.

BC: Received frame Byte Count.
The total number of valid bytes read from the RX FIFO during the last HDLC frame.

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BFRE: Buffered Framing Error.
0 - No framing errors were encountered in the last frame.
1 - A framing error occurred during the last frame, causing the remainder of the frame to be discarded.

BROR: Buffered Receiver Over Run.
0 - The RX buffer did not overrun during the last frame.
1 - The receive FIFO did overrun during the last frame. The remainder of the frame was discarded.

BCRE: Buffered CRC Error.
0 - No CRC check errors occurred in the last frame.
1 - The CRC calculated on the incoming data did not match the CRC value contained in the last frame.

BRAB: Buffered Receiver Abort.
0 - No abort occurred in the last frame.
1 - The last frame was aborted.

UART1HDLCSts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD														PLLE	PLLCC

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
LNKIDL	CRE	ROR	TBY	RIF	RSVD	RAB	RTO	EOF	RFL	RIL	RFC	RFS	TAB	TFC	TFS

Address:

0x808C_021C - Read/Write

Default:

0x0000_0000

Definition:

HDLC Status Register. The TFS and RFS bits in this register are replicas of bits in the UART status register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PLLE: Digital PLL Error. (Read Only)
1 - A frame receive was aborted because the DPLL lost synchronization with the carrier.
0 - DPLL has not lost carrier during frame reception.
This bit is only valid when set up to receive Manchester-encoded synchronous HDLC.

Note: This bit reflects the status associated with the last character read from the RX FIFO. It changes with reads from the RX FIFO.

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PLLCC: Digital PLL Carrier Sense. (Read Only)
1 - DPLL tacked onto a carrier.
0 - DPLL does not sense a carrier.

LNKIDL: Link Idle. (Read Only)
0 - RX data signal has changed within two bit periods
1 - RX data signal has not changed within two bit periods. This bit is only valid when set up to receive Manchester-encoded synchronous HDLC.

CRE: CRC Error. (Read Only)
0 - No CRC check errors encountered in incoming frame.
1 - CRC calculated on the incoming data does not match CRC value contained within the received frame. This bit is set with the last data in the incoming frame along with EOF.

Note: This bit reflects the status associated with the last character read from the RX FIFO. It changes with reads from the RX FIFO.

ROR: Receive FIFO Overrun. (Read Only)
0 - RX FIFO has not overrun.
1 - RX logic attempted to place data in the RX FIFO while it was full. The most recently read data is the last valid data before the overrun. The rest of the incoming frame is dropped. EOF is also set.

Note: This bit reflects the status associated with the last character read from the RX FIFO. It changes with reads from the RX FIFO.

TBY: Transmitter Busy. (Read Only)
0 - TX is idle, disabled, or transmitting an abort.
1 - TX is currently sending a frame (address, control, data, CRC or start/stop flag).

RIF: Receiver In Frame. (Read Only)
0 - RX is idle, disabled, or receiving start flags.
1 - RX is receiving a frame.

RAB: Receiver Abort. (Read Only)
0 - No abort has been detected for the incoming frame.
1 - Abort detected during receipt of incoming frame. The most recently read data is the last valid data before the abort. EOF is also set.

Note: This bit reflects the status associated with the last character read from the RX FIFO. It changes with reads from the RX FIFO.

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RTO: Receiver Time Out.
Set to “1” whenever the HDLC RX has received four consecutive flags, or four character times of idle or space. Cleared by writing a “1” to this bit.

EOF: End of Frame (read only).
0 - Current frame has not been received completely.
1 - The data most recently read from the RX FIFO is the last byte of data within the frame.

Note: This bit reflects the status associated with the last character read from the RX FIFO. It changes with reads from the RX FIFO.

RFL: Receive Frame Lost. (Read/Write)
Set to “1” when an ROR occurred at the start of a new frame, before any data for the frame could be put into the RX FIFO. Cleared by writing a “1” to this bit.

RIL: Receive Information buffer Lost. (Read/Write)
Set to “1” when the last data for a frame is read from the RX FIFO and the UART1HDLCRXInfoBuf has not been read since the last data of the previous frame was read. That is, the information loaded into the UART1HDLCRXInfoBuf about the previous frame was never read and has been overwritten. Cleared by writing a “1” to this bit.

RFC: Received Frame Complete. (Read/Write)
Set to “1” when the last data byte for the frame is read from the RX FIFO (this also triggers an update of the UART1HDLCRXInfoBuf). Cleared by writing to a “1” to this bit.

RFS: Receive FIFO Service request. (Read Only)
This bit is a copy of the RIS bit in the UART interrupt identification register.
0 - RX FIFO is empty or RX is disabled.
1 - RX FIFO not empty and RX enabled.
May generate an interrupt and signal a DMA service request.

TAB: Transmitted Frame Aborted. (Read/Write)
Set “1” when a transmitted frame is terminated with an abort. Cleared by writing to a “1” to this bit.

TFC: Transmit Frame Complete. (Read/Write)
Set to “1” whenever a transmitted frame completes, whether terminated normally or aborted. Cleared by writing to a “1” to this bit.

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TFS: Transmit FIFO Service request. (Read Only)
This bit is a copy of the TIS bit in the UART interrupt identification register.
0 - TX FIFO is full or TX disabled.
1 - TX FIFO not full and TX enabled. May generate an interrupt and signal a DMA service request.

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Chapter 12

UART2

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12.1 Introduction

UART2 implements a UART interface identical to that of UART1. UART2 does *not* implement a modem or HDLC interface. For additional details about UART1, refer to Chapter 11, “UART1 With HDLC and Modem Control Signals” on page 331.

UART2 and the IrDA blocks cooperatively implement a Slow Infrared (SIR) interface. The register interface for each block is separate. The UART2 control registers are at base address 0x808D_0000 and the IrDA controller registers are at base address 0x808B_0000. For additional details about IrDA, refer to Chapter 13, “IrDA” on page 387. The UART SIR interface is described below.

12.2 IrDA SIR Block

The IrDA SIR block contains an IrDA SIR protocol Encoder/decoder. The SIR protocol Encoder/decoder can be enabled for serial communication via signals **nSIROUT** and **SIRIN** to an infrared transducer instead of using the UART signals **UARTTXD** and **UARTRXD**.

If the SIR protocol Encoder/decoder is enabled, the **UARTTXD** line is held in the passive state (HIGH) and transitions of the modem status or the **UARTRXD** line will have no effect. The SIR protocol Encoder/decoder can both receive and transmit, but it is half-duplex only, so it cannot receive while transmitting, or vice versa.

The IrDA SIR physical layer specifies a minimum 10 ms delay between transmission and reception.

12.2.1 IrDA SIR Encoder/decoder Functional Description

The IrDA SIR Encoder/decoder comprises:

- IrDA SIR transmit encoder
- IrDA SIR receive decoder

This is shown in Figure 12-1, below.

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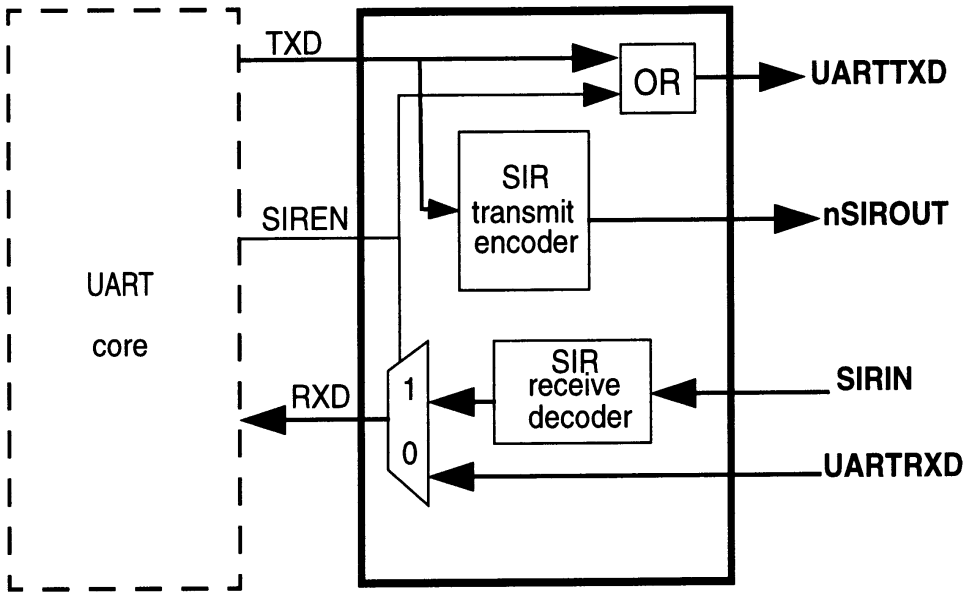
Figure 12-1. IrDA SIR Encoder/decoder Block Diagram



12.2.1.1 IrDA SIR Transmit Encoder

The SIR transmit encoder modulates the Non Return-to-Zero (NRZ) transmit bit stream output from the UART. The IrDA SIR physical layer specifies use of a Return To Zero, Inverted (RZI) modulation scheme which represents logic 0 as an infrared light pulse. The modulated output pulse stream is transmitted to an external output driver and infrared Light Emitting Diode (LED).

In normal mode, the transmitted pulse width is specified as three times the period of the internal x16 clock (Baud16), that is, 3/16 of a bit period.

In low-power mode, the transmit pulse width is specified as 3/16 of a 115.2 Kbits/s bit period. This is implemented as three times the period of a nominal 1.8432 MHz clock (IrLPBaud16) derived by dividing down the UARTCLK clock. The frequency of IrLPBaud16 is set up by writing the appropriate divisor value to UARTILPR. The active low encoder output is normally LOW for the marking state (no light pulse). The encoder outputs a high pulse to generate a infrared light pulse representing a logic “0” or spacing state.

12.2.1.2 IrDA SIR Receive Decoder

The SIR receive decoder demodulates the return-to-zero bit stream from the infrared detector and outputs the received NRZ serial bit stream to the UART received data input. The decoder input is normally HIGH (marking state) in the idle state (the transmit encoder output has the opposite polarity to the decoder input).

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A start bit is detected when the decoder input is LOW.

Regardless of being in normal or low-power mode, a start bit is deemed valid if the decoder is still LOW, one period of IrLPBaud16 after the LOW was first detected. This allows a normal-mode UART to receive data from a low-power mode UART, which may transmit pulses as small as 1.41 µsec.

12.2.2 IrDA SIR Operation

The IrDA SIR Encoder/decoder provides functionality which converts between an asynchronous UART data stream and half-duplex serial SIR interface. No analog processing is performed on-chip. The role of the SIR encoder/decoder is only to provide a digital encoded output and decoded input to the UART. There are two modes of operation:

- In normal IrDA mode, a zero logic level is transmitted as high pulse of $3/16^{th}$ duration of the selected baud rate bit period on the **nSIROUT** signal, while logic one levels are transmitted as a static LOW signal. These levels control the driver of an infrared transmitter, sending a pulse of light for each zero. On the reception side, the incoming light pulses energize the photo transistor base of the receiver, pulling its output LOW. This then drives the **SIRIN** signal LOW.
- In low-power IrDA mode, the width of the transmitted infrared pulse is set to 3 times the period of the internally generated IrLPBaud16 signal (1.63 ns assuming a nominal 1.8432MHz frequency) by changing the appropriate bit in UARTCR.

In both normal and low-power IrDA modes, during transmission, the UART data bit is used as the base for encoding, while during reception the decoded bits are transferred to the UART receive logic.

The IrDA SIR physical layer specifies a half duplex communication link with a minimum 10ms delay between transmission and reception. This delay must be generated by software since it is not supported by the UART. The delay is required since the Infrared receiver electronics may become biased or even saturated from the optical power coupled from the adjacent transmitter LED. This delay is known as latency or receiver setup time. Shorter delays may be able to be used when the link first starts up.

The IrLPBaud16 signal is generated by dividing down the UARTCLK signal according to the low-power divisor value written to UARTILPR.

The low-power divisor value is calculated as:

$$\text{Low-power divisor} = (\text{FUARTCLK} / \text{FirLPBaud16}) - 1$$

where FirLPBaud16 is nominally 1.8432 MHz.

The divisor must be chosen so that 1.42 MHz < IrLPBaud16 < 2.12 MHz.

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12.2.2.1 System/diagnostic Loopback Testing

It is possible to perform loopback testing for SIR data by setting the Loop Back Enable (LBE) bit to 1 in the control register UARTCR (bit 7), and setting the SIRTEST bit to 1 in the test register UARTTMR (bit 1).

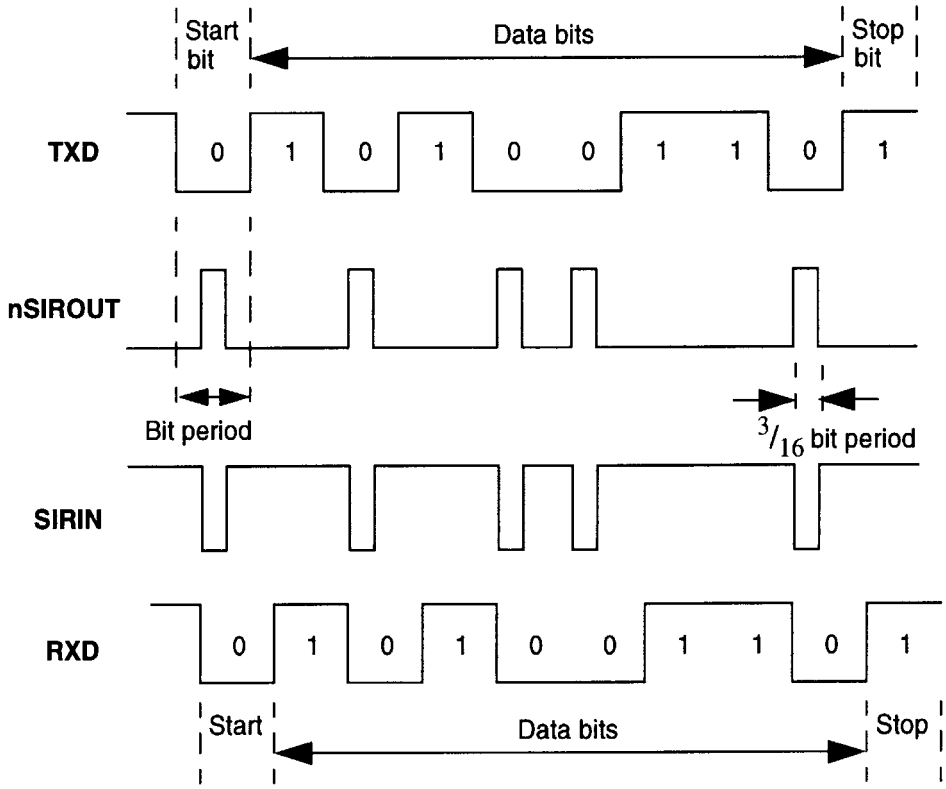
Data transmitted on nSIROUT will be received on the SIRIN input.

Note: UART2TMR is the only occasion that a test register needs to be accessed during normal operation.

12.2.3 IrDA Data Modulation

The effect of IrDA 3/16 data modulation can be seen in Figure 12-2, below.

Figure 12-2. IrDA Data Modulation (3/16)



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12.2.4 Enabling Infrared (Ir) Modes

Table 12-1: UART2 / IrDA Modes

Mode	DeviceCfg Register		UART2Ctrl Register		IrEnable Register	
	U2EN	IonU2	SirEn	UARTE	EN[1]	EN[0]
Disabled	0	x	0	0	0	0
UART2	1	0	0	1	0	0
SIR	1	1	1	1	0	1
MIR	x	1	0	0	1	0
FIR	x	1	0	0	1	1

12.3 UART2 Package Dependency

UART2 uses package pins **RXD1** and **TXD1**. Pin **RXD1** drives both the UART2 UART input and the UART2 SIR input.

However, Syscon register DeviceCfg[28] (IonU2) controls what drives pin **TXD1**. See Table 12-2.

Table 12-2: IonU2 Pin Function

IonU2	Pin TXD1 Function
0	UART2 UART is the output signal
1	Logical OR of IrDA output signal and UART2 SIR output signal

Therefore, to use any IrDA mode, FIR, MIR or SIR, set IonU2. To use UART2 as a UART, clear IonU2.

12.3.1 Clocking Requirements

There are two clocks, PCLK and UARTCLK.

UARTCLK frequency must accommodate the desired range of baud rates:

Fuartclk(min) >= 32 x baud_rate(max)

Fuartclk(max) <= 32 x 65,536 x baud_rate(min)

The frequency of UARTCLK must also be within the required error limits for all baud rates to be used.

To allow sufficient time to write the received data to the receive FIFO, UARTCLK must be less than or equal to four times the frequency of PCLK:

Fuartclk <= 4 x Fpclk

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If the IrDA SIR functionality is required, UARTCLK must have a frequency between 2.7 MHz and 542.7 MHz to ensure that the low-power mode transmit pulse duration complies with the IrDA SIR specification.

12.3.2 Bus Bandwidth Requirements

There are two basic ways of moving data to and from the UART FIFOs:

- Direct DMA interface - this permits byte-wide access to the UART without using the APB. The DMA block will pack/unpack individual bytes so that it reads or writes full 32-bit words rather than individual bytes.
- Accessing the UART via the APB - this requires APB/AHB bus bandwidth. Then, both a read and write are required for each 8-bit data byte.

Bandwidth requirements also depend on the selected baud rate, character size, parity selection, number of stop bits, and spacing between characters (if receiving).

For example, assume 115,200 baud, 8-bit characters, even parity, one stop bit, no space between characters. There are 11 bits per character, so 115,200 / 11 = 10473 characters per second. If both transmitting and receiving, 20,945 characters per second pass through the UART. Accessing the UART through the DMA interface requires one access per 32 bits, implying only 20,945 / 4 = 5,236 AHB accesses per second. Accessing the UART through the APB requires two accesses per byte, implying 20,945 APB bus accesses.

As another example, assume 230,400 baud (the maximum with a UARTCLK equal to 7.3728 Mhz), 5-bit characters, no parity, one stop bit, and no space between characters. There are 7 bits per character, so 230400 / 7 = 32,914 characters per second. Simultaneous transmitting and receiving implies 65829 APB characters per second. Using the DMA interface would result in 16457 AHB accesses per second, while using the APB to access the UART leads to 65829 bus accesses per second.

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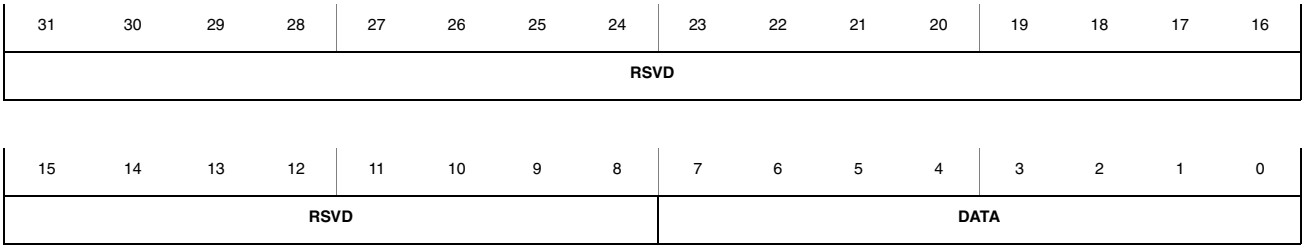
12.4 Registers

Register Descriptions

UART2Data



Address:

0x808D_0000 - Read/Write

Default:

0x0000_0000

Definition:

UART Data Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

DATA: UART Data, read for receive data, write for transmit data
For words to be transmitted:
• if the FIFOs are enabled, data written to this location is pushed onto the transmit FIFO
• if the FIFOs are not enabled, data is stored in the transmitter holding register (the bottom word of the transmit FIFO). The write operation initiates transmission from the UART. The data is prefixed with a start bit, appended with the appropriate parity bit (if parity is enabled), and a stop bit. The resultant word is then transmitted.
For received words:
• if the FIFOs are enabled, the data byte is extracted, and a 3-bit status (break, frame and parity) is pushed onto the 11-bit wide receive FIFO
• if the FIFOs are not enabled, the data byte and status are stored in the receiving holding register (the bottom word of the receive FIFO).

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UART2RXSts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												OE	BE	PE	FE

Address:

0x808D_0004 - Read/Write

Default:

0x0000_0000

Definition:

UART Receive Status Register and Error Clear Register. Provides receive status of the data value last read from the UART2Data. A write to this register clears the framing, parity, break and overrun errors. The data value is not important.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

OE: Overrun Error. This bit is set to “1” if data is received and the FIFO is already full. This bit is cleared to 0 by a write to UART2RXSts. The FIFO contents remain valid since no further data is written when the FIFO is full, only the contents of the shift register are overwritten. The CPU must now read the data in order to empty the FIFO.

BE: Break Error. This bit is set to “1” if a break condition was detected, indicating that the received data input was held LOW for longer than a full-word transmission time (defined as start, data, parity and stop bits). This bit is cleared to 0 after a write to UART2RXSts. In FIFO mode, this error is associated with the character at the top of the FIFO. When a break occurs, only one 0 character is loaded into the FIFO. The next character is only enabled after the receive data input goes to a “1” (marking state) and the next valid start bit is received.

PE: Parity Error. When this bit is set to “1”, it indicates that the parity of the received data character does not match the parity selected in UART2LinCtrlHigh (bit 2). This bit is cleared to 0 by a write to UART2RXSts. In FIFO mode, this error is associated with the character at the top of the FIFO.

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FE: Framing Error. When this bit is set to “1”, it indicates that the received character did not have a valid stop bit (a valid stop bit is “1”). This bit is cleared to 0 by a write to UART2RXSts. In FIFO mode, this error is associated with the character at the top of the FIFO.

UART2LinCtrlHigh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									WLEN		FEN	STP2	EPS	PEN	BRK

Address:

0x808D_0008 - Read/Write

Default:

0x0000_0000

Definition:

UART - High. UART2LinCtrlHigh, UART2LinCtrlMid and UART2LinCtrlLow form a single 23-bit wide register (UART2LinCtrl) which is updated on a single write strobe generated by an UART2LinCtrlHigh write. So, in order to internally update the contents of UART2LinCtrlMid or UART2LinCtrlLow, a UART2LinCtrlHigh write must always be performed at the end.

To update the three registers there are two possible sequences:
• UART2LinCtrlLow write, UART2LinCtrlMid write and UART2LinCtrlHigh write
• UART2LinCtrlMid write, UART2LinCtrlLow write and UART2LinCtrlHigh write.

To update UART2LinCtrlLow or UART2LinCtrlMid only:
• UART2LinCtrlLow write (or UART2LinCtrlMid write) and UART2LinCtrlHigh write.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

WLEN: Number of bits per frame:
11 = 8 bits
10 = 7 bits
01 = 6 bits
00 = 5 bits

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FEN: FIFO Enable.
1 - Transmit and receive FIFO buffers are enabled (FIFO mode).
0 - The FIFOs are disabled (character mode). (That is, the FIFOs become 1-byte-deep holding registers.)

STP2: Two Stop Bits Select.
1 - Two stop bits are transmitted at the end of the frame.
0 - One stop bit is transmitted at the end of the frame.
The receive logic does not check for two stop bits being received.

EPS: Even Parity Select.
1 - Even parity generation and checking is performed during transmission and reception (this checks for an even number of “1”s in data and parity bits).
0 - Odd parity is performed (this checks for an odd number of “1”s).
This bit has no effect when parity is disabled by Parity Enable (bit 1) being cleared to 0.

PEN: Parity Enable.
1 - Parity checking and generation is enabled,
0 - Parity checking is disabled and no parity bit added to the data frame.

BRK: Send Break.
1 - A low level is continually output on the **UARTTXD** output, after completing transmission of the current character. This bit must be asserted for at least one complete frame transmission time in order to generate a break condition. The transmit FIFO contents remain unaffected during a break condition.
0 - For normal use, this bit must be cleared.

UART2LinCtrlMid

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								BR							

Address:

0x808D_000C - Read/Write

Default:

0x0000_0000

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Definition:

UART Line Control Register Middle.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

BR: Baud Rate Divisor bits [15:8]. Most significant byte of baud rate divisor. These bits are cleared to 0 on reset.

UART2LinCtrlLow

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								BR							

Address:

0x808D_0010 - Read/Write

Default:

0x0000_0000

Definition:

UART Line Control Register Low.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

BR: Baud Rate Divisor bits [7:0]. Least significant byte of baud rate divisor. These bits are cleared to 0 on reset. The baud rate divisor is calculated as follows:

Baud rate divisor BAUDDIV = ($F_{UARTCLK}$ / (16 * Baud rate)) –1

where $F_{UARTCLK}$ is the UART reference clock frequency. A baud rate divisor of zero is not allowed and will result in no data transfer.

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UART2Ctrl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								LBE	RTIE	TIE	RIE	MSIE	SIRLP	SIREN	UARTE

Address:

0x808D_0014 - Read/Write

Default:

0x0000_0000

Definition:

UART Control Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

LBE: Loopback Enable, for SIR and UART only.
1 - If the SIR Enable bit is also set to “1”, and register UART2TMR bit 1 (SIRTEST) is set to “1”, the SIR output path is inverted and fed through to the SIR input path. The SIRTEST bit in the test register must be set to “1” to override the normal half-duplex SIR operation. This should be the requirement for accessing the test registers during normal operation, and SIRTEST must be cleared to “0” when loopback testing is finished. This feature reduces the amount of external coupling required during system test.
0 - This bit is cleared to “0” on reset, which disables the loopback mode.

RTIE: Receive Timeout Enable. If this bit is set to “1”, the receive timeout interrupt is enabled.

TIE: Transmit Interrupt Enable. If this bit is set to “1”, the transmit interrupt is enabled.

RIE: Receive Interrupt Enable. If this bit is set to “1”, the receive interrupt is enabled.

MSIE: Modem Status Interrupt Enable. If this bit is set to “1”, the modem status interrupt is enabled.

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SIRLP: SIR Low Power Mode. This bit selects the IrDA encoding mode. If this bit is cleared to 0, low level bits are transmitted as an active high pulse with a width of 3/16th of the bit period. If this bit is set to “1”, low level bits are transmitted with a pulse width which is 3 times the period of the IrLPBaud16 input signal, regardless of the selected bit rate. Setting this bit uses less power, but may reduce transmission distances.

SIREN: SIR Enable. If this bit is set to “1”, the IrDA SIR encoder/decoder is enabled. This bit has no effect if the UART is not enabled by bit 0 being set to “1”. When the IrDA SIR encoder/decoder is enabled, data is transmitted and received on **nSIROUT** and **SIRIN**. **UARTTXD** remains in the marking state (set to “1”). Signal transitions on **UARTRXD** or modem status inputs will have no effect. When the IrDA SIR encoder/decoder is disabled, **nSIROUT** remains cleared to 0 (no light pulse generated), and signal transitions on **SIRIN** will have no effect.

UARTE: UART Enable. If this bit is set to “1”, the UART is enabled. Data transmission and reception occurs for UART signals.

UART2Flag

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								TXFE	RXFF	TXFF	RXFE	BUSY	DCD	DSR	CTS

Address:

0x808D_0018 - Read/Write

Default:

0x0000_0000

Definition:

UART Flag Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TXFE: Transmit FIFO Empty. The meaning of this bit depends on the state of the FEN bit in the UART2LinCtrlHigh register. If the FIFO is disabled, this bit is set when the transmit holding register is empty. If the FIFO is enabled, the TXFE bit is set when the transmit FIFO is empty.

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RXFF: Receive FIFO Full. The meaning of this bit depends on the state of the FEN bit in the UART2LinCtrlHigh register. If the FIFO is disabled, this bit is set when the receive holding register is full. If the FIFO is enabled, the RXFF bit is set when the receive FIFO is full.

TXFF: Transmit FIFO Full. The meaning of this bit depends on the state of the FEN bit in the UART2LinCtrlHigh register. If the FIFO is disabled, this bit is set when the transmit holding register is full. If the FIFO is enabled, the TXFF bit is set when the transmit FIFO is full.

RXFE: Receive FIFO Empty. The meaning of this bit depends on the state of the FEN bit in the UART2LinCtrlHigh register. If the FIFO is disabled, this bit is set when the receive holding register is empty. If the FIFO is enabled, the RXFE bit is set when the receive FIFO is empty.

BUSY: UART Busy. If this bit is set to “1”, the UART is busy transmitting data. This bit remains set until the complete byte, including all the stop bits, has been sent from the shift register. This bit is set as soon as the transmit FIFO becomes non-empty (regardless of whether the UART is enabled or not).

DCD: Data Carrier Detect status. This bit is the complement of the UART data carrier detect (**nUARTDCD**) modem status input. That is, the bit is “1” when the modem status input is 0.

DSR: Data Set Ready status. This bit is the complement of the UART data set ready (**nUARTDSR**) modem status input. That is, the bit is “1” when the modem status input is 0.

CTS: Clear To Send status. This bit is the complement of the UART clear to send (**nUARTCTS**) modem status input. That is, the bit is “1” when the modem status input is 0.

UART2IntIDIntClr

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												RTIS	TIS	RIS	MIS

Address:

0x808D_001C

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Default:

0x0000_0000

Definition:

UART Interrupt Identification and Interrupt Clear Register. Interrupt status is read from UART2IntIDIntClr. A write to UART2IntIDIntClr clears the modem status interrupt. All the bits are cleared to 0 when reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

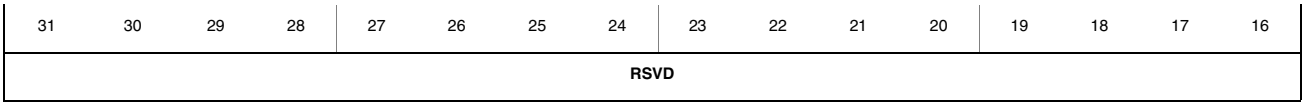
RTIS: Receive Timeout Interrupt Status. This bit is set to “1” if the receive timeout interrupt is asserted.

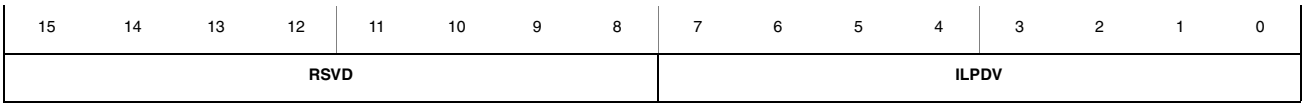
TIS: Transmit Interrupt Status. This bit is set to “1” if the transmit interrupt is asserted.

RIS: Receive Interrupt Status. This bit is set to “1” if the receive interrupt is asserted.

MIS: Modem Interrupt Status. This bit is set to “1” if the modem status interrupt is asserted.

UART2IrLowPwrCntr





Address:

0x808D_0020 - Read/Write

Default:

0x0000_0000

Definition:

UART IrDA Low Power Divisor Register. This is an 8-bit read/write register that stores the low-power counter divisor value used to generate the **IrLPBaud16** signal by dividing down of UARTCLK. All the bits are cleared to 0 when reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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ILPDV: IrDA Low Power Divisor bits [7:0]. 8-bit low-power divisor value. These bits are cleared to 0 at reset. The divisor must be chosen so that the relationship 1.42 MHz < **IrLPBaud16** < 2.12 MHz is maintained, which results in a low power pulse duration of 1.41–2.11 µs (three times the period of **IrLPBaud16**). The minimum frequency of **IrLPBaud16** ensures that pulses less than one period of **IrLPBaud16** are rejected, but that pulses greater than 1.4 µs are accepted as valid pulses. **Zero is an illegal value. Programming a zero value will result in no IrLPBaud16 pulses being generated.**

UART2DMACtrl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													DMAERR	TXDMAE	RXDMAE

Address:

0x808D_0028 - Read/Write

Default:

0x0000_0000

Definition:

UART DMA Control Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

DMAERR: RX DMA error handing enable. If 0, the RX DMA interface ignores error conditions in the UART receive section. If “1”, the DMA interface stops and notifies the DMA block when an error occurs. Errors include break errors, parity errors, and framing errors.

TXDMAE: TX DMA interface enable. Setting to “1” enables the private DMA interface to the transmit FIFO.

RXDMAE: RX DMA interface enable. Setting to “1” enables the private DMA interface to the receive FIFO.

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UART2TMR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								0						SIRTEST	0

Address:

0x808D_0084 - Read/Write

Default:

0x0000_0000

Definition:

UART SIR Loopback Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

0: Must be written as “0”. Unknown During Read.

SIRTEST: SIR test enable. Setting this bit to “1” enables the receive data path during IrDA transmission (testing requires SIR to be configured in full-duplex mode). This bit must be set to “1” to enable SIR system loopback testing, when the normal mode control register UART2Ctrl bit 7, Loop Back Enable (LBE), has been set to “1”. Clearing this bit to 0 disabled the receive logic when the SIR is transmitting (normal operation). This bit defaults to 0 for normal (half-duplex) operation.

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Chapter 13

IrDA

13.1 Introduction

This module implements the physical layer of an infrared serial port that is compliant with Version 1.1 of the Infrared Data Association (IrDA) standard. It supports communication speeds of up to 4 MBit/s. When combined with analog transducer components, it provides a complete interface between infrared media and an AMBA compliant peripheral bus (APB).

Three different encoder/decoder units implement the supported modulation schemes and data encoding systems defined by the IrDA standard:

- Slow Infrared (SIR) - This interface attaches to the output of UART2. The UART2 registers handle the data and control for this interface, though the IrDA interface enable register selects the SIR function.
- Medium Infrared (MIR) - Transmission/reception rates can be 0.576 or 1.152 Mb/s.
- Fast Infrared (FIR) - Transmission/reception rate is 4 Mb/s.

13.2 IrDA Interfaces

The Infrared Interface Module implements in hardware the physical layer of an infrared serial port, compliant with version 1.1 of the IrDA standard. Communication speeds of up to 4 Mbit/sec are supported. When combined with analog transducer components, it provides a complete interface between infrared media and an AMBA compliant peripheral bus (APB).

The Module comprises three separate encoder/decoder units for implementing three different combinations of modulation scheme and data encoding system defined by the IrDA standard. These are:

- Slow Infrared - SIR - This interface attaches to the output of a UART. All data and control for this interface is done through the UART registers. The SIR encoder function is selected using the IrDA interface enable register.
- Medium Infrared - MIR - This interface is independent of a UART. Transmission/reception rates can be 0.576 or 1.152 Mbit/sec.
- Fast Infrared - FIR - This interface is independent of a UART. Transmission/reception rates can be 4 Mbit/sec.

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13.3 Shared IrDA Interface Feature

This section describes features common to the MIR and FIR interfaces (the SIR interface has been designed to share the enable register and device pins but is otherwise a separate interface assumed to be controlled by UART2).

13.3.1 Overview

The Slow Infrared (SIR) Encoder/Decoder is used to modulate and demodulate serial data using the Hewlett-Packard Serial Infrared standard (HP-SIR) for bit encoding. Serial transmit data from UART2 is modulated using return-to-zero (RTZ) encoding to produce an output to drive the Ir transmitter LED, while data received from the Ir detector is converted into a serial bit stream to drive a UART's serial input. The SIR supports data rates up to 115.2 kbit/s.

The Medium Speed Infrared (MIR) Encoder/Decoder encodes/decodes peripheral bus data according to a modified HDLC standard, using flag characters, bit stuffing and a 16 bit CRC checker. MIR uses the same RTZ modulation and demodulation scheme used by the SIR. Two signal bit rates are supported: 0.576 Mbit/s and 1.152 Mbit/s.

The Fast Infrared Encoder/Decoder (FIR) operates at a fixed bit rate of 4 Mbit/s. Modulation/demodulation is by a phase shift key scheme called pulse position modulation (4 PPM). One of four signalling symbols represent each possible pair of data bits. Data encoding uses a packet format that prefixes bit and symbol synchronization flags to data and appends a 32-bit CRC and stop flag to the end of each packet. The start and stop flags use signalling symbols that are not used to encode data, hence bit stuffing of data is not required in this mode.

Only one of the Encoder/Decoder modules can be enabled to transmit and receive data from the IrDA transducers at one time Selection of an Ir sub-module is by means of the IrEnable register. The MIR and FIR sub-modules can be regarded by programmers as independent entities which are operated using common control and data registers, but which report status data via separate read registers.

Detailed descriptions of the MIR and FIR are given in the following sections. The SIR, however, has no data or control registers. It interfaces directly to a UART's serial stream. With the exception of the IrEnable register, it has no presence on the memory map and has no interface to the APB via the Infrared interface.

13.3.2 Functional Description

This section gives a programmer's guide to operating the IrDA interface. It includes detail on the general configuration and the transmit and receive processes.

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13.3.2.1 General Configuration

13.3.2.1.1 Select Ir Mode

The IrEnable register selects which of the three Ir sub-modules is used to operate the IrDA interface. Only one of the three may be active at any one time. The reset value for this register is zero, which disables all three encoder/decoder modules. The bottom two bits of this register select the encoder/decoder module according to the tabulated values:

Table 13-1: Bit Values to Select Ir Module

IrEnable EN1	IrEnable EN0	Encoder Selected
0	0	None
0	1	SIR
1	0	MIR
1	1	FIR

SIR does not use the data transfer mechanism described in this section. After selecting SIR mode, all data transfer operations are made through a UART, as if connection is through a serial cable without handshake lines. The features described below are implemented for the MIR and FIR modes.

13.3.2.1.2 Select Data Rate

The data rates for MIR and FIR are as follows:

- MIR - Clear BRD bit in IrControl (IrCon) for 0.576 Mbit/sec, Set BRD bit in IrCon for 1.152 Mbit/sec.
- FIR - Fixed at 4 Mbit/sec.

13.3.2.2 Transmitting Data

13.3.2.2.1 Initialization

The principal method of data transfer from memory to the active IrDA encoder (MIR or FIR) is by DMA. Typically DMA can be used to transfer data of any length into the transmit FIFO when requested by the infrared peripheral. When polling or interrupts are used to perform the data transfer, a mechanism exists for transmitting data packets that are not a multiple of 4 bytes in length. This uses a register called IrDataTail and its use is described in the next section.

The DMA route is usually provided to overcome any large interrupt response times that may exist in the SoC where the Infrared module is going to be used. These large interrupt response times can make programmed I/O an impractical method for transferring large Ir data packets.

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13.3.2.2.2 The Transmit Process

This section describes the transmission process in detail.

Is last transmission complete? - Ensure that the Infrared peripheral is not currently receiving or transmitting data by reading the RSY (for half-duplex communications) and TBY bits in the IrFlag register. If either is set, postpone the start of transmission.

Disable IrDA - If you are changing Ir mode, first disable Ir. To disable IrDA, first clear IrCtrl.RXE and IrCtrl.TXE. Secondly, clear the IrEnable.EN field to be “00”.

Disabling UART2 for MIR and FIR - For MIR and FIR, disable UART2 by writing “0” to UART2Ctrl and 0 to IrCtrl.

Set up the DMA Engine - If DMA is being used, set up the DMA engine by setting up the registers of the DMA block.

Enabling Clocks - For MIR, set up the MIR clock in MIRClkDiv. Select 0.576 or 1.152 Mbps mode by clearing or setting IrCtrl.BRD. For FIR, enable the FIR clock by setting PwrCnt.FIR_EN.

Select Ir Mode - Select SIR, MIR, or FIR mode by writing the IrEnable.EN bit field to be “01”, “10”, or “11”.

Clear Interrupt Sticky Bits - For MIR, write the MISR register, setting the TFC, TAB, RFL, and RIL bits to clear them. Then read the IrRIB register to clear the RFC bit. For FIR, write the FISR register, setting the TFC, TAB, RFL, and RIL bits to clear them. Then read the IrRIB register to clear the RFC bit.

Select Transmit Underrun Action - When DMA is used, the TUS bit should be cleared.

Enable Transmit - Set the IrCtrl.TXE Transmit Enable bit. Also set IrCtrl.RXE if receive is to be enabled. If DMA is used, also set IrDMACR.TXDMAE (and IrDMACR.RXDMAE if receive is to be enabled).

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Preloading the Transmit FIFO - Copy the first two full words of data into the transmit FIFO by writing them into the IrData register. The Ir encode block can hold up to 11 bytes of data (two words in the FIFO plus up to three bytes in the IrDataTail register). If this is sufficient to hold the complete transmission data packet, DMA will not be needed. The IrCon.TUS bit should be cleared. This will cause the Ir encoder to correctly send the CRC and end of frame flag. **Note:** Prefilling the FIFO must happen immediately after enabling MIR or FIR. Preloading the FIFO is unnecessary for SIR. Also note that preloading the FIFO is unnecessary for MIR and FIR if DMA is used.

Loading the IrDataTail Register - In the PIO and IRQ case, once the FIFO has been preloaded, the IrDataTail register can be loaded. The IrDataTail register contains the last bytes in the frame (1, 2 or 3 bytes left over from the last whole word provided by PIO or IRQ). **Note:** If DMA is used, loading the IrDataTail register is unnecessary, as the IrDataTail register is disabled in that case.

Send out the data - If DMA is being used, everything is now enabled for the transmission process to begin. If PIO or IRQ is being used, data should be written to the IrData register.

13.3.2.2.3 Sending Packets Which are Not a Multiple of 4 Bytes In Length

The transmit FIFO is 32 bits wide. When using polling or interrupts to effect the transfer, loading the FIFO with less than 32 bits would cause extraneous zero bits to be transmitted. This is taken care of automatically by DMA and needs no special action in that case. However in the case of polling or interrupt-driven transfers, the IrDataTail register is the mechanism used to preload the last 1, 2 or 3 bytes of a frame. When the transfer is complete and the FIFO is empty, any bytes stored in the IrDataTail register are transmitted before the Ir encoder sends the CRC and end-of-frame flags. There are three distinct addresses to write the end of frame data to. This allows a single word write to specify the data to be transmitted and the number of trailing bytes to send.

Table 13-2: Address Offsets for End-of-frame Data

Bytes to transmit	Address offset to use
1	0x014
2	0x018
3	0x01C

If there is a single trailing byte to transmit, write to address offset 0x014, for two bytes write to 0x018 and if there are three trailing bytes write to 0x01 C.

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13.3.2.2.4 End of Frame Interrupt

Once all the data sent to the FIFO has been taken by the Ir interface, the FIFO will underrun. When this occurs any data that has been preloaded into the IrDataTail register will be used and the Transmitted Frame Complete (TFC) interrupt will be generated.

13.3.2.2.5 Disable Transmit Circuitry

To save power, the Transmit Enable (TXE) bit can be cleared in the IrEnable register if there are no frames that need to be sent.

13.3.2.2.6 Error conditions

Transmitted frame abort is only signalled if IrCon register bit TUS is set to 1.

13.3.2.3 Receiving Data

The end of a reception frame will cause an interrupt, which may be masked using the mask register (MIMR/FIMR). The end of frame interrupt occurs after the last data value has been transferred, including any odd bytes in the frame tail.

13.3.2.3.1 Initialization

Address Matching — To use Address Match filtering, set the local 8 bit address in the Address Match Value Register and set the Address Match Enable bit in the IrCon register.

Set up DMA — Set up a DMA buffer (the buffer should be greater than twice the maximum possible size of received frames). Enable DMA.

Alternatively, two buffers maybe used which are each the maximum possible frame size long. The DMA would then be programmed to switch between the two buffers.

Enable Ir Receive — Set the Receive Enable bit (RXE) in IrEnable.

13.3.2.3.2 End of Frame Interrupt

The Receive Frame Complete (RFC) interrupt is generated when the last data in a frame is read from the receive FIFO. To check whether the frame was received correctly (no errors) and for information on frame size the Receive Information Buffer register (IrRIB) must be read by the interrupt service routine (this also clears the RFC interrupt condition).

Note: By the time the processor responds to this interrupt the interface may have already started reception of a new frame.

13.3.2.3.3 End of Frame: Using Programmed I/O

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If interrupt driven programmed I/O is used instead of DMA, every time the Receive Buffer Service (RFS) interrupt is serviced the IrFlag register must be read before the IrData register, if the IrFlag values are needed. Their Flag register gives information about error conditions that correspond to the data value at the head of the receive FIFO.

Note: The IrRIB registers stores status flags for a complete frame.

13.3.2.3.4 Error Conditions

Receive error conditions do not generate interrupts. Reading the IrData word clears the IrFlag register bits listed below.

Receiver Abort Detected When set, this indicates that the transmitter sent an abort signal during frame transmission.

Receiver Overrun This indicates that data has not been read for the IrData register in time and has resulted in data loss from the frame. When this occurs the interface automatically discards the remainder of the incoming frame.

CRC Error If the CRC for the received data does not match the CRC value contained in the incoming data stream this condition will occur.

Frame Error (FIR only) This indicates that a framing error has been detected.

The data word and flags are held in the 39-bit wide receiver FIFO. Reading an IrData word removes both the data and its associated flag bits from the FIFO causing the next word in the FIFO (if present) to be transferred into the IrFlag and data registers. However, all error conditions encountered during a frame are remembered. At the end of frame they can be read form the IrRIB register.

When a receive overrun (ROR) or FIR framing error (FRE) is detected the remainder of the frame will be discarded by the receive logic (not put into the receive FIFO). In the case of receive overruns, if the end of frame (EOF) bit in the last entry in the FIFO is clear then the Receive Buffer Overrun (ROR) and EOF bits will be set. If an overrun occurs and the last entry in the FIFO already has the EOF bit set then the RFL interrupt will be triggered. In the case of a framing error an extra entry will be put into the FIFO with FIR Framing Error (FRE) and EOF set, this entry will not contain any valid data.

If programmed IO is used to service the IrDA interface instead of DMA a similar process occurs. Interrupt requests to service the receive FIFO will not occur until the rest of the frame has been discarded.

At the end of a frame, a valid end of frame (EOF) or an abort (RAB), a DMA request corresponding to the last word (which may hold 1, 2, 3, or 4 bytes of valid data) of the received frame will be raised. DMA will take the word. At that point the receive FIFO should be empty and the DMA request may be deasserted. The DMA request will be reasserted when data for a following frame is loaded into the receive FIFO.

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The above behavior means there is no need for processor intervention to service the IrDA interface between successive receive frames.

13.3.2.4 Special Conditions

13.3.2.4.1 Early Termination of Transmission

Clearing IrCon.TXE (transmit enable bit) stops transmission immediately. All data within the FIFO, transmit buffer and serial output shifter is cleared.

13.3.2.4.2 Early Termination of Reception

Clearing IrCon.RXE receive enable bit stops reception immediately. All data within the receive buffer, serial input shifter and FIFO is cleared.

13.3.2.4.3 Changing IrDA Mode

Poll the Transmitter Disabled bits – FD or MD bits – in IrEnable register until end of transmission is indicated. The new mode can then be set as described in *4.2.1General Configuration*.

13.3.2.4.4 Loopback Mode

For test purposes, data will be looped back – internally – from the output of the transmit serial shifter into the input of the receive serial shifter when IrEnable.LBM is set.

13.3.3 Control Information Buffering

The processor needs several items of information about a received frame that are not held in data DMAed from the receive FIFO, or stored in the DMA controller itself (because the DMA unit may be receiving the next frame by the time the processor starts to work on the frame just completed). The additional information is as follows:

- A receive overrun or framing error occurred during frame reception.
- The frame failed the CRC check at the end of reception.
- Transmission of the frame was aborted.
- The number of bytes of valid data received in the frame (i.e. up to the end of frame or the overrun/framing error condition).

A control information buffer register is loaded whenever an end of received frame condition occurs. This event also generates an interrupt, which must be serviced before the end of the next received frame (at which point the buffered control information would be overwritten). The interrupt may be cleared by reading from the control information buffer register or by writing a ‘1’ to its status bit position.

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13.4 Medium IrDA Specific Features

The MIR comprises a dedicated serial port and RZI modulator/demodulator supporting the Infrared Data Association (IrDA) standard for transmission/reception at 0.576 and 1.152 Mb/s.

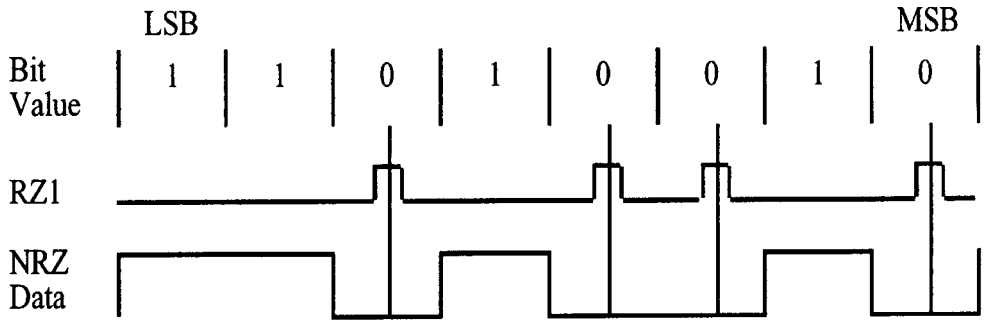
Frames contain an 8 bit address, an optional control field, a data field of any size that is a multiple of 8 bits and a 16-bit CRC-CCITT. The start/stop flag and CRC generation/checking is performed in the hardware. Data can be selectively saved in the receive buffer by programming an address with which to compare against all incoming frames. Interrupts are signalled when CRC checks performed on received data indicate an error, when a receiver abort occurs, when the transmit buffer underruns during an active frame and is aborted, when the receive buffer overruns and data is lost.

13.4.1 Introduction

13.4.1.1 Bit Encoding

The MIR bit encoding uses an RZI modulation scheme where a “0” is represented by a light pulse. For both 0.576 and 1.152 Mbit/sec data rates, the optical pulse duration is normally 1/4 of a bit duration. For example, if the data frame (in the order of transmission) is 11010010b, then Figure 13-1 represents the signal that is actually transmitted.

Figure 13-1. RZ1/NRZ Bit Encoding Example



13.4.1.2 Frame Format

MIR uses a flag (reserved bit pattern) to denote the beginning and end of a frame of information and to synchronize frame transmission. A double flag is used to indicate the start of a frame and a single flag the end. The flag contains eight bits, which start and end with a zero and contain six sequential ones in the middle (01111110b). This sequence of six ones is unique because all data between the start and stop flag is prohibited from having more than five consecutive ones. Data that violates this rule is altered before transmission by automatically inserting a zero after five consecutive ones are detected in the transmitted bit stream. This technique is commonly referred to

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as “bit stuffing” and is transparent to the user. The information field within a MIR frame is placed between the start and stop flags, consisting of an 8 bit address, an optional 8 bit control field, a data field containing any multiple of 8 bits and a 16 bit cyclic redundancy check (CRC-CCITT). Note that each byte within the address, control and data fields is transmitted and received LSB first, ending with the byte’s MSB. However, the CRC is transmitted and received MSB first. The MIR frame format is outlined below in Table 13-3.

Table 13-3: MIR Frame Format

8 Bits	8 Bits	8 Bits	8 Bits (optional)	Any multiple of 8 Bits	16 Bits	8 Bits
Start Flag 0111 1110	Start Flag 0111 1110	Address	Control	Data	CRC-CCITT	Stop Flag 0111 1110

13.4.1.2.1 Address Field

The 8 bit address field is used by a transmitter to target a select group of receivers when multiple stations are connected using the infrared link. The address allows up to 255 stations to be uniquely addressed (00000000b to 11111110b). The global address (11111111b) is used to broadcast messages to all stations. The serial port contains an 8 bit register that is used to program a unique address for broadcast recognition as well as a control bit to enable/disable the address match function. Note that the address of received frames is stored in the receive buffer along with normal data and that it is transmitted and received starting with its LSB and ending with its MSB.

13.4.1.2.2 Control Field

The MIR control field is typically 8 bits, but can be any length. The serial port does not provide any hardware decode support for the control byte, but instead treats all bytes between the address and the CRC as data. Thus any control bits appear as data to the programmer. Note that the control field is transmitted and received starting with its LSB and ending with its MSB.

13.4.1.2.3 Data Field

The data field can be any length that is a multiple of 8 bits, including zero. The user determines the data field length according to the application requirements and transmission characteristics of the target system. Usually a length is selected which maximizes the amount of data that can be transmitted per frame, while allowing the CRC checker to be able to consistently detect all errors during transmission. All data fields must be a multiple of 8 bits. If a data field that is not a multiple of 8 bits is received, an abort is signalled and the end of frame tag is set within the receive buffer. Also note that each byte within the data field is transmitted and received starting with its LSB and ending with its MSB.

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13.4.1.2.4 CRC Field

MIR uses the established CCITT cyclical redundancy check (CRC) to detect bit errors that occur during transmission. A 16 bit CRC-CCITT is computed using the address, control and data fields and is included in each frame. A separate CRC generator is implemented in both the transmit and receive logic. The transmitter calculates a CRC while data is actively transmitted and places the 16 bit value at the end of each frame before the stop flag is transmitted. The receiver calculates a CRC for each received data frame and compares the calculated CRC to the expected CRC value contained within the end of each received frame. If the calculated value does not match the expected value, an interrupt is signalled. The CRC computation logic is preset to all ones before reception/transmission of each frame. Note that the CRC is transmitted and received starting with its MSB and ending with its LSB. The CRC uses the four term polynomial:

$$CRC(x) = (x^{16} + x^{12} + x^5 + 1)$$

13.4.2 Functional Description

Following reset, the MIR is disabled. Reset also causes the transmit and receive buffers and tail register to be flushed (buffers marked as empty). To transmit data in MIR mode, use the following procedure:

1. Set the EN bits in the IrEnable register to 10b for MIR mode. Do not begin data transmission.
2. Before enabling the MIR, the user must first clear any writable or “sticky” status bits that are set by writing a one to each bit. (A sticky bit is a readable status bit that may be cleared by writing a one to its location.) Set the TAB and TFC bits in the MISR register, then read the MISR register to clear all interrupts.
3. Next, the desired mode of operation is programmed in the control register. Set the TXE and RXE bits in the IrCtrl register.
4. Write 1 to 3 bytes to the appropriate IrDataTail register.
5. Once the MIR is enabled, transmission/reception of data can begin on the transmit and receive pins.

13.4.2.1 Baud Rate Generation

The baud or bit rate is derived by dividing down an 18.423MHz clock. The clock is divided down by either 1 (BRD=1) or 2 (BRD=0) and then by a fixed value of four, generating the transmit clock for 1.152Mb/s and 0.576Mb/s data rates, respectively. The receive clock is generated by the receiver Digital Phase Locked Loop (DPLL). The DPLL uses a sample clock that is undivided. A sample rate counter (incremented at the sample clock rate) is used to generate a receive clock at the nominal data rate (sample clock divided by 41

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and two-thirds). The sample rate counter is reset on the detection of each positive-going data transition (indicating the RZI encoding of a “0”) to ensure that synchronization with the incoming data stream is maintained.

13.4.2.2 Receive Operation

Once the MIR receiver is enabled it enters hunt mode, searching the incoming data stream for the flag (01111110b). The flag serves to achieve bit synchronization, denotes the beginning of a frame and delineates the boundaries of individual bytes of data. The end of the second flag denotes the beginning of the address byte. Once the flag is found, the receiver is synchronized to incoming data and hunt mode is exited.

After each bit is decoded, a serial shifter is used to receive the incoming data a byte at a time. Once the flag is recognized, each subsequent byte of data is decoded and placed within a two byte temporary buffer. A temporary buffer is used to prevent the CRC from being placed within the receive buffer. When the temporary buffer is filled, data values are pushed out one by one to the receive buffer. The first byte of a frame is the address. If receiver address matching is enabled, the received address is compared to the address programmed in the address match value field in a control register. If the two values are equal or if the incoming address contains all ones, all subsequent data bytes including the address byte are stored in the receive buffer. If the values do not match, the receive logic does not store any data in the receive buffer, ignores the remainder of the frame and begins to search for the stop flag. The second byte of the frame can contain an optional control field that must be decoded in software (There is no hardware support within the MIR). Use of a control byte is determined by the user.

When the receive buffer contains a word of data, an interrupt or DMA request is signalled. If the data is not removed soon enough and the buffer is completely filled, an overrun error is generated when the receive logic attempts to place additional data into the full buffer. If this occurs all subsequent data in the frame is discarded by the interface and the last valid entry in the buffer is marked with the ROR and EOF bits. The interface will stall in this state until the receive buffer is emptied.

Frames can contain any amount of data in multiples of 8 bits. Although the MIR protocol does not limit frame size, in practice they tend to be implemented in numbers ranging from hundreds to a couple of thousand bytes. In general this interface expects received frame size to be limited to 2047 bytes. However, the interface can continue to operate past this limit provided that software drivers are written that carefully check the indicated frame length with the amount of data transferred (in the DMA case this is a little more difficult).

The receive logic continuously searches for the stop flag at the end of the frame. Once it is recognized, the last byte that was placed within the receive buffer is flagged as the last byte of the frame and the two bytes remaining within the temporary buffer are removed and used as the 16 bit CRC value for

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the frame. Instead of placing this in the receive buffer, the receive logic compares it to the CRC-CCITT value which is continuously calculated using the incoming data stream. If they do not match, the last byte that was placed within the receive buffer is also flagged with a CRC error. The CRC value is not placed in the receive buffer.

The MIR protocol permits back to back frames to be received. When this occurs, three flags separate back to back frames.

Most commercial IrDA transceivers can generate an abort (7 to 13 ones) when their transmit buffer underruns. The receive logic contains a counter that increments each time a one is decoded before entering the serial shifter and is reset any time a zero is decoded. When seven or more ones are detected, a receiver abort occurs. Note that data is moved from the serial shifter to the temporary buffer a byte at a time and seven consecutive ones may bridge two bytes. For this reason, after an abort is detected, the remaining data in the serial shifter is discarded along with the most recent byte of data placed in the temporary buffer. After this data is discarded, the oldest byte of data in the temporary buffer is placed in the receive buffer, the EOF tag is set within the top entry of the buffer (next to the byte transferred from the temporary buffer), the receiver abort interrupt is signalled and the receiver logic enters hunt mode until it recognizes the next flag.

This interface also generates an abort condition when a stop flag is received that is not byte aligned with the rest of the data in the frame. In this case the over flow data bits past the last byte boundary are discarded. It is not possible for the programmer to distinguish this condition for an normal abort condition.

If the user disables the receiver during operation, reception of the current data byte is stopped immediately, the serial shifter and receive buffer are cleared and all clocks used by the receive logic are automatically shut off to conserve power.

13.4.2.3 Transmit Operation

Immediately after enabling the MIR for transmission, the user may either “prime” the transmit buffer by filling it with data (see section “Functional Description” on page 397 for details) or allow service requests to cause the CPU or DMA to fill the buffer once the MIR is enabled. Once enabled, the transmit logic issues a service request if its buffer is empty. A Serial Infrared Interaction Pulse (SIP) is transmitted in order to guarantee non-disruptive co-existence with slower (up to 115.2 kbit/sec) systems, for example another device attempting to use its SIR. This is followed by continuous transmission of flags until valid data resides within the buffer. Once a byte of data resides at the bottom of the transmit buffer, it is transferred to the serial shifter, is encoded and shifted out onto the transmit pin clocked by the programmed baud rate clock. Note that the flags and CRC value are automatically transmitted and need not be placed in the transmit buffer.

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When the transmit buffer has space for another word, an interrupt and/or DMA service request is signalled. If new data is not supplied soon enough, the buffer is completely emptied and the transmit logic attempts to take additional data from the empty buffer, one of two actions can be taken as programmed by the user. An underrun can either signal the normal completion of a frame or an unexpected termination of a frame in progress.

When normal frame completion is selected and an underrun occurs, the transmit logic transmits the 16 bit CRC value calculated during the transmission of all data within the frame (including the address and control bytes), followed by a flag to denote the end of the frame. The transmitter then transmits an SIP, followed by a continuous transmission of flags until data is once again available within the buffer. Once data is available, the transmitter begins transmission of the next frame.

When unexpected frame termination is selected and an underrun occurs, the transmit logic outputs an abort and interrupts the CPU. An abort continues to be transmitted until data is once again available in the transmit buffer. The MIR then transmits an SIP, followed by a double flag and starts the new frame. The off-chip receiver may choose to ignore the abort and continue to receive data, or to signal the serial port to retry transmission of the aborted frame. If the user disables the transmitter during operation, transmission of the current data byte is stopped immediately, the serial shifter and transmit buffer are cleared and all clocks used by the transmit logic are automatically disabled to conserve power.

13.5 Fast IrDA Specific Features

The Fast Infrared port (FIR) operates at half-duplex and provides direct connection to commercially available Infrared Data Association (IrDA) compliant LED transceivers. The FIR supports the 4.0 Mbps IrDA standard, using four pulse position modulation (4 PPM) and a specialized serial packet protocol developed expressly for IrDA transmission.

13.5.1 Introduction

13.5.1.1 4PPM Modulation

Four position pulse modulation (4PPM) is used for the high-speed transmission rate of 4.0 Mbps. Payload data is divided into data bit pairs (DBPs) for encoding with LSBs transmitted first. Each DBP is represented by one of four symbols (DDs) comprising a single 125 ms pulse within a 500 ms symbol period. The 125 ms quarters of a symbol are known as “chips”. The resulting signal waveform for the four data DDs is shown in Figure 13-2 and Figure 13-3 and shows modulation of the byte, 10110001b which is constructed using four DBPs.

Note: 1. Bits within each DBP are not reordered, but the least significant DBP is

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transmitted first.

Note: 2. A "chip" in the context of the FIR is one time slice in the Position Modulation (PPM) symbol.

Figure 13-2. 4PPM Modulation Encoding

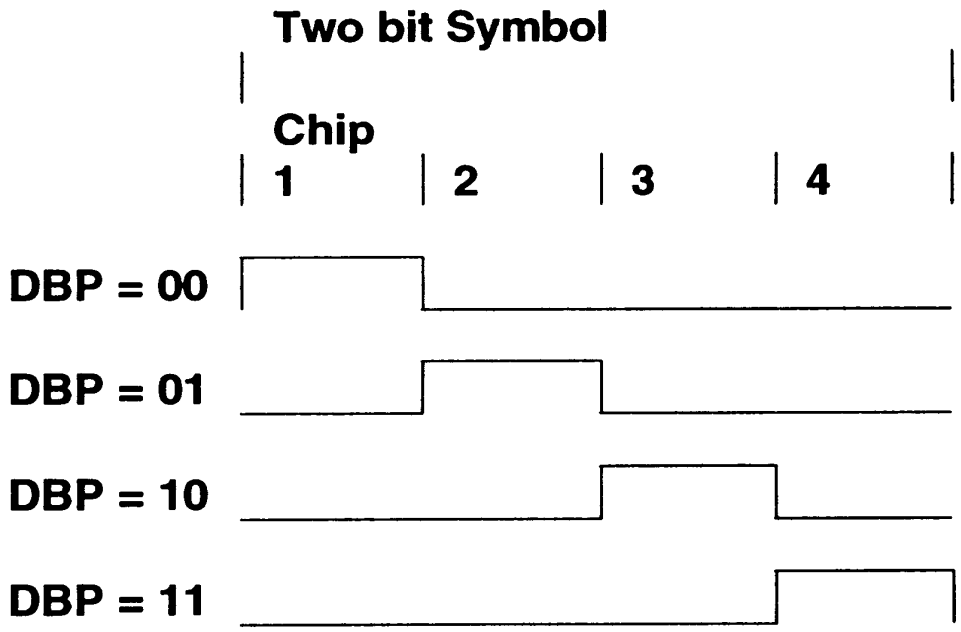
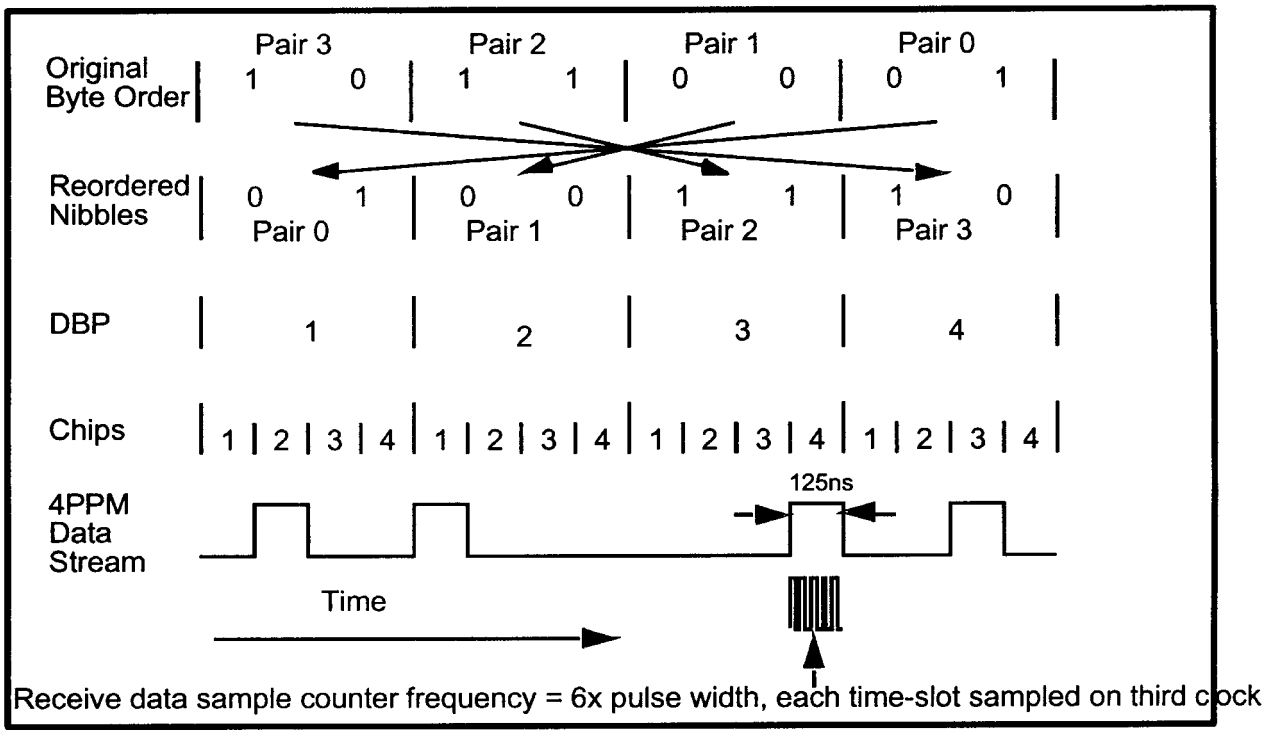


Figure 13-3. 4PPM Modulation Example



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13.5.1.2 4.0 Mbps FIR Frame Format

When the 4.0 Mbps transmission rate is used, the high-speed serial/parallel (FIR) interface within the FIR is used along with the 4PPM bit encoding. The high-speed frame format shown in Figure 13-4 shown below, is similar to the SDLC format with several minor modifications: the start/stop flags and CRC are twice as long and instead of one start flag, a preamble and start flag of differing length are used.

Figure 13-4. IrDA (4.0 Mbps) Transmission Format

64 symbols	8 symbols	4 DDs (8 bits)	4 DDs (8 bits)	8180 DDs max (2045 bytes)	16 DDs (32 bits)	8 symbols
Preamble	**Start Flag**	**Address**	**Control (optional)**	**Data**	**CRC-32**	**Stop Flag**

Start Flag	|0000|1100|0000|1100|0110|0000|0110|0000|	
	|0000|1100|0000|1100|0000|0110|0000|0110|	**Stop Flag**
Preamble	|1000|0000|1010|1000|... repeated 16 times	

The preamble, start and stop flags are a mixture of symbols which contain either 0, 1, or 2 pulses within the four time slots. Symbols with 0 and 2 pulses are used to construct flags since they represent invalid data bit pairings (one pulse required per symbol to represent one of four bit pairs). The preamble contains sixteen repeated transmissions of the four symbols: **1000 0000 1010 1000**, the start flag contains one transmission of eight symbols: **0000 1100 0000 1100 0110 0000 0110 0000** and the stop flag contains one transmission of eight symbols: **0000 1100 0000 1100 0000 0110 0000 0110**. The address, control, data and CRC-32 all use the standard 4PPM DDs described above.

13.5.1.2.1 Address Field

The 8 bit address field is used by a transmitter to target a select group of receivers when multiple stations are connected to the same set of serial lines. The address allows up to 255 stations to be uniquely addressed (00000000b to 11111110b). The global address (11111111b) is use to broadcast messages to all stations. Serial port 1 contains an 8 bit register which is used to program a unique address for broadcast recognition as well as a control bit to enable/disable the address match function. Note that the address of received frames is stored in the receive buffer along with normal data and that it is transmitted and received starting with its LSB and ending with its MSB.

13.5.1.2.2 Control Field

The IPC control field is 8 bits and is optional (as defined by the user). The FIR does not provide any hardware decode support for the control byte, but instead treats all bytes between the address and the CRC as data. Note that

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the control field is transmitted and received starting with its LSB and ending with its MSB.

13.5.1.2.3 Data Field

The data field can be any length which is a multiple of 8 bits, from 0 to 2045 bytes. The user determines the data field length according to the application requirements and transmission characteristics of the target system. Usually a length is selected which maximizes the amount of data which can be transmitted per frame, while allowing the CRC checker to be able to consistently detect all errors during transmission. Note that the serial port does not contain any hardware which restricts the maximum amount of data transmitted or received. It is up to the user to maintain these limits. If a data field which is not a multiple of 8 bits is received an abort is signalled. Also note that each byte within the data field is transmitted and received starting with its LSB and ending with its MSB.

13.5.1.2.4 CRC Field

The FIR uses the established 32 bit cyclical redundancy check (CRC-32) to detect bit errors which occur during transmission. A 32 bit CRC is computed using the address, control and data fields and is included in each frame. A separate CRC generator is implemented in both the transmit and receive logic. The transmitter calculates a CRC while data is actively transmitted byte shifting each byte transmitted through its serial shifter LSB first, then places the inverse of the resultant 32 bit value at the end of each frame before the flag is transmitted. In a similar manner, the receiver also calculates a CRC for each received data frame and compares the calculated CRC to the expected CRC value contained within the end of each received frame. If the calculated value does not match the expected value, an interrupt is signalled. The CRC computation logic is preset to all ones before reception/transmission of each frame and the result is inverted before it used for comparison or transmission. Note that unlike the address, control and data fields, the 32 bit inverted CRC value is transmitted and received from least significant byte to most significant and within each byte the least significant nibble is encoded/decoded first. The cyclical redundancy checker uses the 32 term polynomial:

$$CRC(x) = (x^{32} + x^{26} + x^{23} + x^{22} + x^{16} + x^{12} + x^{11} + x^{10} + x^8 + x^7 + x^5 + x^4 + x^2 + x + 1)$$

13.5.2 Functional Description

Following reset, the FIR is disabled. Reset also causes the transmit and receive buffers and tail register to be flushed (buffers marked as empty). To transmit data in FIR mode, use the following procedure:

1. Set the EN bits in the IrEnable register to 11b for FIR mode. Do not begin data transmission.

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2. Before enabling the FIR, the user must first clear any writable or “sticky” status bits that are set by writing a one to each bit. (A sticky bit is a readable status bit that may be cleared by writing a one to its location.) Set the TAB and TFC bits in the FISR register, then read the FISR register to clear all interrupts.
3. Next, the desired mode of operation is programmed in the control register. Set the TXE and RXE bits in the IrCtrl register.
4. Write 1 to 3 bytes to the appropriate IrDataTail register.
5. Once the FIR is enabled, transmission/reception of data can begin on the transmit and receive pins.

13.5.2.1 Baud Rate Generation

The baud rate is derived by dividing down a fixed 48 MHz clock. The 8 MHz baud (time-slot) clock for the receiver is synchronized with the 4 PPM data stream each time a transition is detected on the receive data line using a digital PLL. To encode a 4.0 Mbps data stream, the required “symbol” frequency is 2.0 MHz, with four chips per symbol at a frequency of 8.0 MHz. Receive data is sampled half way through each time-slot period by counting three out of the six 48 MHz clock periods which make up each chip. Refer to Figure 13-3 on page 401. The symbols are synchronized during preamble reception. Recall that the preamble consists of four symbols repeated sixteen times. This repeating pattern is used to identify the first time-slot or beginning of a symbol and resets the two bit chip counter logic, such that the 4 PPM data is properly decoded.

13.5.2.2 Receive Operation

The IrDA standard specifies that all transmission occurs at half-duplex. This restriction forces the user to enable one direction at a given time; either the transmit or receive logic, but not both. However, the FIR’s hardware does not impose such a restriction. The user may enable both the transmitter and receiver at the same time. Although forbidden by the IrDA standard, this feature is particularly useful when using the FIR’s loop back mode, which internally connects the output of the transmit serial shifter to the input of the receive serial shifter.

After the FIR is enabled for 4.0 Mbps transmission, the receiver logic begins by selecting an arbitrary symbol boundary, receives four incoming 4 PPM symbols from the input pin using a serial shifter and latches and decodes the symbols one at a time. If the symbols do not decode to the correct preamble, the chip counter’s clock is forced to skip one 8MHz period, effectively delaying the chip count by one. This process is repeated until the preamble is recognized, signifying that the chip counter is synchronized. The preamble may be repeated as few as sixteen times, or may be continuously repeated to indicate an idle receive line.

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At any time after the transmission of sixteen preambles, the start flag may be received. The start flag is eight symbols long. If any portion of the start flag does not match the standard encoding, the receiver signals a framing error and the receive logic once again begins to look for the frame preamble.

Once the correct start flag is recognized, each subsequent grouping of four DDs is decoded into a data byte, placed within a five byte temporary buffer which is used to prevent the CRC from being placed within the receive buffer. When the temporary buffer is filled, data values are pushed out one by one to the receive buffer. The first data byte of a frame is the address. If receiver address matching is enabled, the received address is compared to the address programmed in the address match value field in one of the control registers. If the two values are equal or if the incoming address contains all ones, all subsequent data bytes including the address byte are stored in the receive buffer. If the values do not match, the receiver logic does not store any data in the receive buffer, ignores the remainder of the frame and begins to search for the next preamble. The second data byte of the frame can contain an optional control field as defined by the user and must be decoded in software (there is no hardware support within the FIR).

Frames can contain any amount of data in multiples of 8 bits up to a maximum of 2047 bytes (including the address and control byte). In general this interface expects received frame size to be limited to 2047 bytes. However, the interface can continue to operate past this limit, thus it is the responsibility of the user to check that the size of each incoming frame does not exceed the IrDA protocol's maximum allowed frame size. The BC field in the IrRIB register can not be used for this since it will over flow (and wrap), the true frame length can be deduced from the DMA buffer position in combination with the BC field.

When the receive buffer contains a word of data, an interrupt or DMA request is signalled. If the data is not removed soon enough and the buffer is completely filled, an overrun error is generated when the receive logic attempts to place additional data into the full buffer. If this occurs all subsequent data in the frame is discarded by the interface and the last valid entry in the buffer is marked with the ROR and EOF bits. The interface will stall in this state until the receiver buffer is emptied.

When a framing error is detected all subsequent data in the frame is discarded by the interface and an entry is put into the buffer with the FRE and EOF bits set The data in this buffer entry is invalid.

If any two sequential symbols within the data field do not contain pulses (are 0000b), the frame is aborted. The oldest byte in the temporary buffer is moved to the receive buffer (the remaining four buffer entries are discarded). The end of frame (EOF) tag is set within the same buffer entry where the last "good" byte of data resides and the receiver logic begins to search for the preamble. An abort occurs if any data symbol contains 0011b, 1010b, 0101b, or 1001b (invalid symbols which do not occur in the stop flag).

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The receiver continuously searches for the 8 symbol stop flag. Once it is recognized, the last byte placed within the receive buffer is flagged as the last byte of the frame and the data in the temporary buffer is removed and used as the 32 bit CRC value for the frame. Instead of placing this in the receive buffer, the receiver compares it to the CRC-32 value which is continuously calculated using the incoming data stream. If they do not match, the last byte which was placed in the receiver buffer is also tagged with a CRC error. The CRC value is not placed in the receive buffer.

If the user disables the FIR's receiver during operation, reception of the current data byte is stopped immediately, the serial shifter and receive buffer are cleared and all clocks used by the receive logic are automatically shut off to conserve power.

13.5.2.3 Transmit Operation

Immediately after enabling the FIR for transmission, the user may either "prime" the transmit buffer by filling it with data (see section "Functional Description" on page 403 for details) or allow service requests to cause the CPU or DMA to fill the buffer once the FIR is enabled. Once enabled, the transmit logic issues a service request if its buffer is empty. For each frame output, a minimum of sixteen preambles are transmitted. If data is not available after the sixteenth preamble, additional preambles are output until a byte of valid data resides within the bottom of the transmit buffer. The preambles are then followed by the start flag and then the data from the transmit buffer. Four symbols (8 bits) are encoded at a time and then loaded into a serial shift register. The contents are shifted out onto the transmit pin clocked by the 8 MHz baud clock. Note that the preamble, start and stop flags and CRC value is automatically transmitted and need not be placed in the transmit buffer.

When the transmit buffer is emptied, an interrupt and/or DMA service request is signalled. If new data is not supplied quickly enough and the transmit logic attempts to take additional data from the empty buffer, one of two actions can be taken as programmed by the user. An underrun can either signal the normal completion of a frame or an unexpected termination of a frame in progress.

When normal frame completion is selected and an underrun occurs, the transmit logic transmits the 32 bit CRC value calculated during the transmission of all data within the frame (including the address and control bytes), followed by the stop flag to denote the end of the frame. The transmitter then continuously transmits preambles until data is once again available within the buffer. Once data is available, the transmitter begins transmission of the next frame.

When unexpected frame termination is selected and an underrun occurs, the transmit logic outputs an abort and interrupts the CPU. An abort continues to be transmitted until data is once again available in the transmit buffer. The FIR

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then transmits 16 preambles, a start flag and starts the new frame. The remote receiver may choose to ignore the abort and continue to receive data, or to signal the FIR to retry transmission of the aborted frame.

At the end of each frame transmitted, the FIR outputs a pulse called the serial infrared interaction pulse (SIP). A SIP is required at least every 500 ms to keep slower speed devices (115.2 kbps and slower) from colliding with the higher speed transmission. The SIP simulates a start bit which causes all low speed devices to stay off the bus for at least another 500 ms. Transmission of the SIP pulse causes the transmit pin to be forced high for a duration of 1.625 µs and low for 7.375 µs (total SIP period = 9.0 µs). After the 9.0 µs elapses, the preamble is then transmitted continuously to indicate to the remote receiver that the FIR's transmitter is in the idle state. The preamble continues to be transmitted until new data is available within the transmit buffer, or the FIR's transmitter is disabled. Note that it is the responsibility of the user to ensure that a frame completes once every 500 ms such that a SIP pulse is produced keeping all low speed devices from interrupting transmission. Because most IrDA compatible devices produce a SIP after each frame transmitted, the user may only need to ensure that a frame is either transmitted or received by the FIR every 500 ms.

Note that frame length does not represent a significant portion of the 500 ms time frame in which a SIP must be produced. At 4.0 Mbps, the longest frame allowed is 16,568 bits, which takes just over 4 ms to transmit. Also note that the FIR issues a SIP when the transmitter is first enabled, to ensure all low speed devices are silenced before transmitting it's first frame.

If the user disables the FIR's transmitter during operation, transmission of the current data byte is stopped immediately, the serial shifter and transmit buffer are cleared. All clocks used by the transmit logic are automatically shut off to conserve power.

13.5.3 IrDA Connectivity

The IrDA controller uses package pins **RXD1** and **TXD1**. The IrDA input signal is always **RXD1**. Syscon register DeviceCfg.IonU2 controls what drives bit **TXD1**. See Figure 13-4 on page 407.

Table 13-4: DeviceCfg.IonU2 Pin Function

DeviceCfg.IonU2	Pin TXD1 Function
0	UART2 is the output signal
1	Logical OR of IrDA output signal and UART2 SIR output signal

Therefore, to use any IrDA mode, FIR, MIR or SIR, set IonU2. To use UART2 as a UART, clear IonU2.

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13.5.4 IrDA Integration Information

13.5.4.1 Enabling Infrared Modes

Table 13-5: UART2 / IrDA Modes

Mode	DeviceCfg Register		UART2Ctrl Register		IrEnable Register	
	U2EN	IonU2	SIREn	UARTE	EN[1]	EN[0]
Disabled	0	x	0	0	0	0
UART2	1	0	0	1	0	0
SIR	1	1	1	1	0	1
MIR	x	1	0	0	1	0
FIR	x	1	0	0	1	1

13.5.4.2 Clocking Requirements

There are four clocks, PCLK, MIRCLK, FIRCLK, and UARTCLK.

Version 1.1 of the Infrared Data Association standard indicates the following:

- FIRCLK must by 48.0 MHz with a tolerance of 0.01%.
- MIRCLK must be 18.432 MHz with a tolerance of 0.1%.

The worst case ratio that can be supported for PCLK:FIRCLK is a ratio of 1:5. The maximum that PCLK can be is 66 MHz, therefore:

$$\frac{1}{5}F_{FIRCLK} < F_{PCLK} < 66.0MHz$$

Any frequencies outside the above range are not supported and will result in incorrect behavior of the FIR mode of the infrared peripheral.

Since MIRCLK is 18.432 MHz, PCLK can be as low as 3.68 MHz and as high as 66 MHz. Any PCLK frequency in this range is allowable. Any PCLK frequencies outside the range are not supported and will result in incorrect behavior of the MIR mode of the infrared peripheral, therefore:

$$3.68MHz \leq F_{PCLK} \leq 66.0MHz$$

The tolerance of UARTCLK is defined by the UART to which it is connected.

UARTCLK frequency must accommodate the desired range of baud rates:

$$F_{UARTCLK_{MIN}} \geq 32 \times baudrate_{MAX}$$

$$F_{UARTCLK_{MAX}} \leq 32 \times 65536 \times baudrate_{MIN}$$

The frequency of UARTCLK must also be within the required error limits for all baud rates to be used.

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To allow sufficient time to write the received data to the receive FIFO, UARTCLK must be less than or equal to four times the frequency of PCLK:

$$F_{UARTCLK} \leq 4 \times F_{PCLK}$$

If the IrDA SIR functionality is required, UARTCLK must have a frequency between 2.7 MHz and 542.7 MHz to ensure that the low-power mode transmit pulse duration complies with the IrDA SIR specification.

13.5.4.3 Bus Bandwidth Requirements

There are four different IrDA modes with different bandwidth requirements. Furthermore, there are two basic ways of moving data to or from the IrDA FIFOs:

- Direct DMA interface - this permits byte-wide access to the IrDA without using the APB. The DMA block will pack/unpack individual bytes so that it reads or writes full 32-bit words rather than individual bytes.
- Accessing the IrDA via the APB - this requires APB/AHB bus bandwidth. Then, both a read and write are required for each 32-bit data word.

Assuming most bytes in a packet are moved either via the DMA interface or via 32-bit word accesses to the IrDA controller on the APB, the following table indicates the maximum average number of memory accesses per second to service IrDA TX or RX:

Table 13-6: IrDA Service Memory Accesses / Second

Infrared Mode	Bit Rate (bits / second)	Bus accesses / second	
		DMA	APB
SIR	115,200	3,600	7,200
Slow MIR	576,000	18,000	36,000
Fast MIR	1,152,000	36,000	72,000
FIR	4,000,000	125,000	250,000

Note that the SIR mode bit rate is a worst case value.

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13.6 Registers

Register Descriptions

IrEnable

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31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD											FD	MD	LBM	EN	

Address:

0x808B_0000 - Read/Write

Default:

0x0000_0018

Definition:

IrDA Enable Register. This register selects which Infrared interface module is active. The Medium and Fast modules share common control, flag, and data interfaces while maintaining separate status registers.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

FD: Fast done status. Read-only bit indicating that the FIR transmit module has completed transition of the current frame and that it is safe to disable the module using the EN control bits.

MD: Medium done status. Read-only bit indicating that the MIR transmit module has completed transmission of the current frame and that it is safe to disable the module using the EN control bits.

LBM: Loopback Mode, for MIR and FIR operation.
0 - Normal operation.
1 - Loopback active, the transmit serial shifter is directly connected to the receive serial shifter.

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EN: Enable value:
00 - No encoder selected
01 - SIR, 0 to 0.1152Mbit/s data rate, using the UART2 interface
10 - MIR, 0.576 or 1.152Mbit/s data rate, using IrDA interface
11 - FIR, 4.0Mbit/s data rate, using IrDA interface.

Note: While the FIR transmit section is enabled, the FD bit is low, and while the MIR transmit section is enabled, the MD bit is low. In FIR mode, the FD bit does not go high until the TXE bit in the IrCtrl register is cleared, and in MIR mode, the same bit must be cleared for MD to go high. Monitor the TBY bit in the IrFlag register to discover whether a packet is fully transmitted before clearing TXE.

IrCtrl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								AME	RXP	TXP	RXE	TXE	TUS	BRD	0

Address:
0x808B_0004

Default:
0x0000_0000

Definition:
IrDA Control Register. This register selects various operating parameters. Note that the RXE and TXE bit must be cleared before selecting a different interface with the IrEnable register EN bits. The other bits in this register may be changed while the interface is active.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

AME: Address Match Enable.
0 - Disable receiver address match function, store data from all incoming frames in the receive buffer.
1 - Enable receiver address match function, do not buffer data unless address is recognized or incoming address contains all ones.

RXP: Receive Polarity Control.
0 - Data input is not inverted before decoding.
1 - Data input is inverted before decoding.

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TXP: Transmit Polarity Control.
0 - Encoded data is not inverted before being passed to the pins.
1 - Encoded data is inverted before being passed to the pins.

RXE: Receive Enable.
0 - Ir receive logic is disabled and clocks are stopped.
1 - Ir receive logic is enabled.

TXE: Transmit Enable.
0 - Transmit logic is disabled and clocks are stopped.
1 - Transmit logic is enabled.

TUS: Transmit buffer Underrun Select.
0 - Transmit buffer underrun causes CRC, stop flag, and SIP to be transmitted.
1 - Transmit buffer underrun causes an abort to be transmitted.

BRD: MIR Bit rate select.
0 - MIR data rate is 0.576 Mbit/s.
1 - MIR data rate is 1.152 Mbit/s.

0: Must be written to “0”.

IrAdrMatchVal

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								AMV							

Address:

0x808B_0008 - Read/Write

Default:

0x0000_0000

Definition:

IrDA Address Match Value Register contains the 8 bit address match value field which is used by the receiver to selectively store only the data within the receive frames which have the same address. For incoming frames which have the same address value as the AMV field, the frame’s address, control and data is stored in the receive buffer. For those that do not match, the remainder of the frame is ignored and the receive logic searches for the beginning of the next frame. This register is used for both MIR and FIR. The AME bit in IrCtrl must be set to enable this function. Frames containing an

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address of all ones are broadcast frames, and are always matched regardless of the value in the AMV. The AMV may be written at any time, allowing the address match value to be changed during active receive operation.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

AMV: Address Match Value.

IrFlag

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD						TBY	RIF	RSY	EOF	WST	WST	FRE	ROR	CRE	RAB

Address:

0x808B_008B - Read Only

Default:

0x0000_0000

Definition:

IrDA Flag Register. Contains the nine read only flags which indicate the current state of the IrDA Interface.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TBY: Transmitter Busy Flag.
0 - Transmitter is idle, or disabled, or an abort is being transmitted.
1 - Transmit logic is currently transmitting a frame.

RIF: Receiver In Frame.
0 - Receiver is in preamble/start flag or is in hunt mode.
1 - Receiver is in a frame.

RSY: Receiver Synchronized Flag.
0 - Receiver is in hunt mode.
1 - Receiver logic is synchronized within the incoming data.

EOF: End of Frame.
0 - Current frame is not completed.
1 - The word in the receive buffer contains the last byte of data within the frame. When the last word in the current frame is read this bit is cleared.

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WST: Width Status.
00 - All four bytes in receive buffer are valid.
01 - Least significant byte is valid only.
10 - Least significant two bytes are valid only.
11 - Least significant three bytes are valid only.

FRE: FIR Framing Error.
0 - No framing errors encountered in the receipt of FIR data.
1 - Framing error occurred, FIR preamble followed by something other than another preamble or FIR start flag. The data in the buffer is invalid.

ROR: Receive buffer Overrun.
0 - Receive buffer has not experienced an overrun.
1 - Receive logic attempted to place data into receive buffer while it was full. The next data value in the buffer is the last piece of “good” data before the buffer was overrun.

CRE: CRC Error.
0 - No CRC check errors encountered in the data.
1 - CRC calculated on the incoming data does not match CRC value contained within the received frame.

RAB: Receiver Abort.
0 - No abort has been detected for the incoming frame.
1 - Abort detected during receipt of the incoming frame, EOF bit set in receive buffer next to the last piece of “good” data received before abort.

IrData

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
DATA															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															

Address:

0x808B_0010 - Read/Write

Default:

0x0000_0000

Definition:

IrDA Data Register. Provides access to the transmit and receive buffers used by the MIR and FIR interfaces.

Bit Descriptions:

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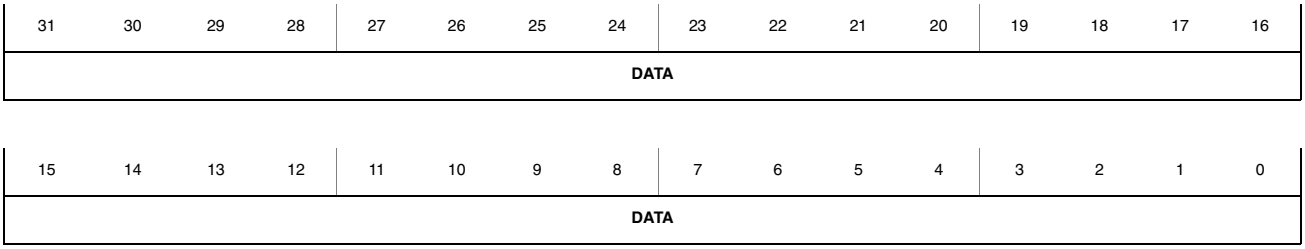
DATA: IrDA data word. Values written and sent to the transmit FIFO. Values read are from the receiver FIFO.

IrDataTail



Address:

0x808B_0014, 0x808B_0018, 0x808B_001C - Write Only

Default:

0x0000_0000

Definition:

IrDA Data Tail Register. This is a 24-bit write only register used for transmitting frames whose payload data is not an integer multiple of 4 bytes long. The bit locations are cleared when read by the transmit logic or when the TXE control bit is clear. The IrData Tail register may be written using one of three addresses. Bits two and three of the address determine how many bytes within the word are significant, that is, are intended for transmission. If none of the address is written, the register remains marked as empty and payload data will be read by the transmit logic from the 32-bit FIFO only. The status of this register does not affect the TFS flag, nor does it cause interrupts or DMA requests to be generated.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

DATA: IrDA transmit payload data. Write to address 0x014, least significant byte is transmitted. Write to address 0x018, least significant two bytes are transmitted. Write to address 0x01C, least significant three bytes are transmitted.

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IrRIB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD	BC											BFRE	BROR	BCRE	BRAB

Address:

0x808B_0020 - Read Only

Default:

0x0000_0000

Definition:

IrDA Receive Information Register. This register contains 15 read only bits that identify flag and byte count values from the last received frame. The bits are copied from the flag register when the last data in a frame is read from the receive FIFO.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

BC: Byte Count. The total number of valid bytes read from the interface during the last frame. If the total number of bytes is greater than 2047, only the lower eleven bits are presented.

BFRE: Buffered Framing Error.
0 - No framing errors were encountered during the last frame.
1 - A framing error occurred during the last frame causing the remainder of the frame to be discarded.

BROR: Buffered Receive buffer Overrun.
0 - The receive buffer did not overrun during the last frame.
1 - Receive logic attempted to place data into receive buffer while it was full during the last frame causing the remainder of the frame to be discarded.

BCRE: Buffered CRC Error.
0 - No CRC check errors encountered in the last frame.
1 - CRC calculated on the incoming data did not match CRC value contained within the received frame for the last frame.

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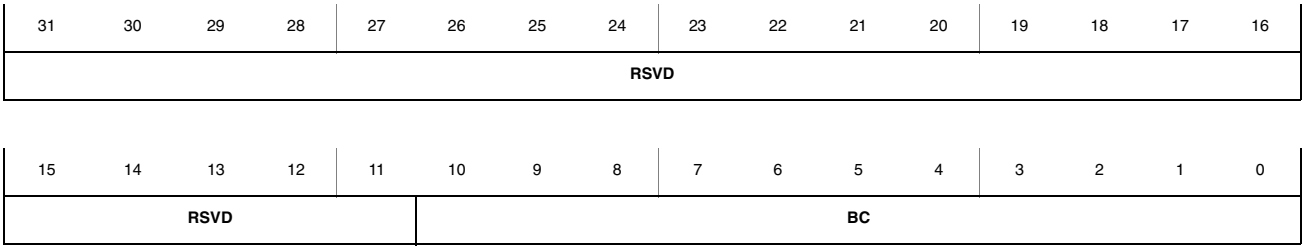
BRAB: Buffered Receiver Abort.
0 - No abort was detected in the last frame.
1 - The last frame was terminated with an abort condition.

IrTR0



Address:
0x808B_0024 - Read Only

Default:
0x0000_0000

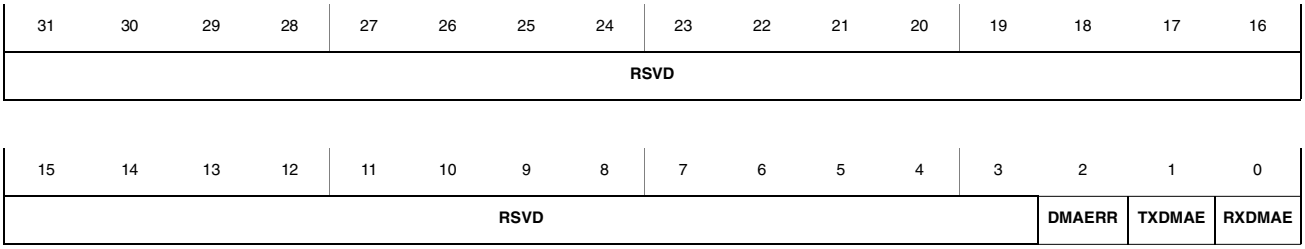
Definition:
IrDA Test Register 0. This register indicates the received byte count.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

BC: Byte Count. The total number of valid bytes read by the receiver.

IrDMACR



Address:
0x808B_0028 - Read/Write

Default:
0x0000_0000

Definition:
IrDA DMA Control Register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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DMAERR: RX DMA error handing enable. If 0, the RX DMA interface ignores error conditions in the IrDA receive section. If “1”, the DMA interface stops and notifies the DMA block when an error occurs. Errors include framing errors, receive abort, and CRC mismatch.

TXDMAE: TX DMA interface enable. Setting to “1” enables the private DMA interface to the transmit FIFO.

RXDMAE: RX DMA interface enable. Setting to “1” enables the private DMA interface to the receive FIFO.

SIRTR0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								SIREN	SIROUT	TXD	RXD	SIRT	SIRIN	S16CLK	TSIRC

Address:

0x808B_0030 - Read/Write

Default:

0x0000_0000, except that bit 4 is unknown at reset

Definition:

IrDA Slow InfraRed Test Register 0.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

SIREN: The state of the **SIREN** after synchronization. Read only.

SIROUT: The state of **SIROUT** output from the InfraRed block. Read only.

TXD: The state of the **TXD** input to the InfraRed block from UART2. Read only.

RXD: The state of the **RXD** output from the InfraRed block to UART2. Read only.

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MISR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									RFL	RIL	RFC	RFS	TAB	TFC	TFS

Address:

0x808B_0080 - Read/Write

Default:

0x0000_0000

Definition:

MIR Status Register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RFL: Receive Frame Lost. Set to a “1” when a ROR occurred at the start of a new frame, before any data for the frame could be put into the receive FIFO. This bit is cleared by writing a “1” to this bit. This occurs if the last entry in the FIFO already contains a valid EOF bit from a previous frame when a FIFO overrun occurs. The ROR bit cannot be placed into the FIFO and all data associated with the frame is lost.

RIL: Receive Information Buffer Lost. Set to a “1” when the last data for a frame is read from the receive FIFO and the RFC bit is still set from a previous end of frame. This bit is cleared by writing a “1” to this bit. This is triggered if the RFC bit is already set before the last data from a frame is read from the IrData register. It indicates that the data from the IrRIB register was lost. This can occur if the CPU does not respond to the RFC interrupt before another (short) frame completes and is read from the IrData register by the DMA controller.

RFC: Received Frame Complete. Set to “1” when the last data for a frame is read from the receive FIFO (via the IrData register). This event also triggers the IrRIB to load the IrFlag and byte count. This bit is cleared when the IrRIB register is read.

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RFS: Receive buffer Service Request (read only).
0 - Receive buffer is empty or the receiver is discarding data or the receiver is disabled.
1 - Receive buffer is not empty and the receiver is enabled, DMA service request signaled.

TAB: Transmit Frame Aborted. Set to “1” when a transmitted frame is terminated with an abort. This will only occur if the TUS bit is set in the IrCtrl register. Writing a “1” to this bit clears it.

TFC: Transmitted Frame Complete. Set to “1” whenever a transmitted frame completes, whether it is terminated with a CRC followed by a stop flag or terminated with an abort. Writing a “1” to this bit clears it.

TFS: Transmit buffer Service Request (read only).
0 - Transmit buffer is full or transmitter disabled.
1 - Transmit buffer is not full and the transmitter is enabled, DMA service is signaled.
The bit is automatically cleared after the buffer is filled.

MIMR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									RFL	RIL	RFC	RFS	TAB	TFC	TFS

Address:
0x808B_0084 - Read/Write

Default:
0x0000_0000

Definition:
MIR Interrupt Mask Register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RFL: RFL mask bit. When high, the MIR RFL status can generate an interrupt.

RIL: RIL mask bit. When high, the MIR RIL status can generate an interrupt.

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RFC: RFC mask bit. When high, the MIR RFC status can generate an interrupt.

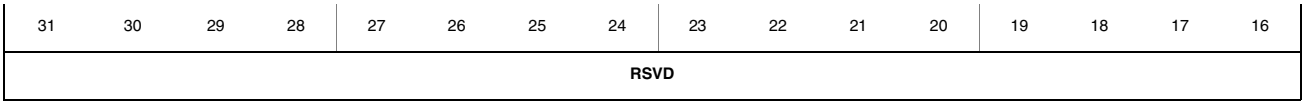
RFS: RFS mask bit. When high, the MIR RFS status can generate an interrupt.

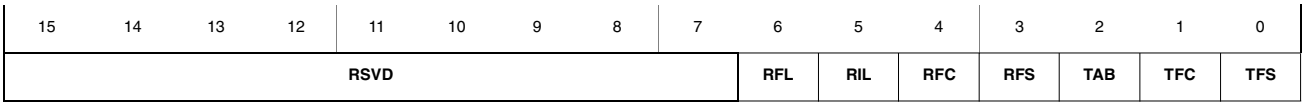
TAB: TAB mask bit. When high, the MIR TAB status can generate an interrupt.

TFC: TFC mask bit. When high, the MIR TFC status can generate an interrupt.

TFS: TFS mask bit. When high, the MIR TFS status can generate an interrupt.

MIIR





Address:

0x808B_0088 - Read Only

Default:

0x0000_0000

Definition:

MIR Interrupt Register. The IrDA interrupt is asserted if any bit in the MIIR is high.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RFL: Logical AND of MIR RFL status bit and RFL mask bit.

RIL: Logical AND of MIR RIL status bit and RIL mask bit.

RFC: Logical AND of MIR RFC status bit and RFC mask bit.

RFS: Logical AND of MIR RFS status bit and RFS mask bit.

TAB: Logical AND of MIR TAB status bit and TAB mask bit.

TFC: Logical AND of MIR TFC status bit and TFC mask bit.

TFS: Logical AND of MIR TFS status bit and TFS mask bit.

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FISR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									RFL	RIL	RFC	RFS	TAB	TFC	TFS

Address:

0x808B_0180 - Read/Write

Default:

0x0000_0000

Definition:

FIR Status Register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RFL: Receive Frame Lost. Set to a “1” when a ROR occurred at the start of a new frame, before any data for the frame could be put into the receive FIFO. This bit is cleared by writing a “1” to this bit. This occurs if the last entry in the FIFO already contains a valid EOF bit from a previous frame when a FIFO overrun occurs. The ROR bit cannot be placed into the FIFO and all data associated with the frame is lost.

RIL: Receive Information Buffer Lost. Set to a “1” when the last data for a frame is read from the receive FIFO (via the IrData register) and the RFC bit is still set from a previous end of frame. It indicates that data in the IrRIB register for the previous frame was lost. This can occur if the CPU does not respond to the RFC interrupt before another frame completes and is read from the IrData register by the DMA controller. This bit is cleared by writing a “1” to this bit.

RFC: Received Frame Complete. Set to “1” when the last data for a frame is read from the receive FIFO (via the IrData register). This event also triggers the IrRIB to load the IrFlag and byte count. This bit is cleared when the IrRIB register is read.

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RFS: Receive buffer Service Request (read only).
0 - Receive buffer is empty or the receiver is discarding data or the receiver is disabled.
1 - Receive buffer is not empty and the receiver is enabled, DMA service request signaled.
The bit is automatically cleared when the receive buffer is emptied.

TAB: Transmit Frame Aborted. Set to “1” when a transmitted frame is terminated with an abort. This will only occur if the TUS bit is set in the IrCtrl register. The bit is cleared by writing a “1” to this bit.

TFC: Transmitted Frame Complete. Set to “1” whenever a transmitted frame completes (whether it is terminated with a CRC followed by a stop flag or terminated with an abort). This bit is cleared by writing a “1” to this bit.

TFS: Transmit buffer Service Request (read only).
0 - Transmit buffer is full or transmitter disabled.
1 - Transmit buffer is not full and the transmitter is enabled, DMA service is signaled.
The bit is automatically cleared after the buffer is filled.

FIMR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									RFL	RIL	RFC	RFS	TAB	TFC	TFS

Address:
0x808B_0184 - Read/Write

Default:
0x0000_0000

Definition:
FIR Interrupt Mask Register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RFL: RFL mask bit. When high, the FIR RFL status can generate an interrupt.

RIL: RIL mask bit. When high, the FIR RIL status can generate an interrupt.

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RFC: RFC mask bit. When high, the FIR RFC status can generate an interrupt.

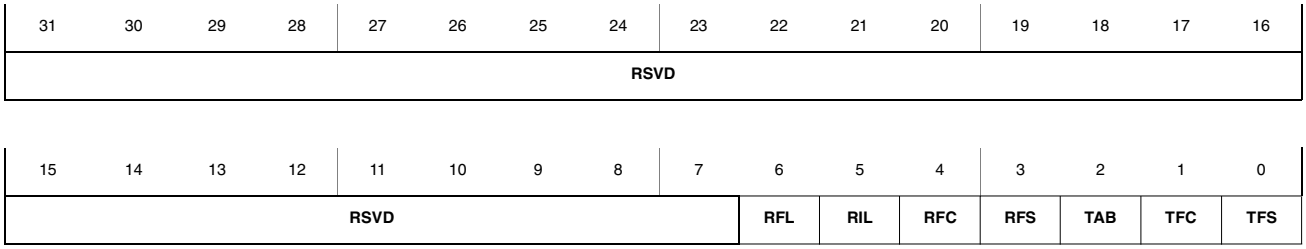
RFS: RFS mask bit. When high, the FIR RFS status can generate an interrupt.

TAB: TAB mask bit. When high, the FIR TAB status can generate an interrupt.

TFC: TFC mask bit. When high, the FIR TFC status can generate an interrupt.

TFS: TFS mask bit. When high, the FIR TFS status can generate an interrupt.

FIIR



Address:

0x808B_0188 - Read Only

Default:

0x0000_0000

Definition:

FIR Interrupt Register. An interrupt is signalled from this block if any bit is high in the FIIR.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RFL: Logical AND of FIR RFL status bit and RFL mask bit.

RIL: Logical AND of FIR RIL status bit and RIL mask bit.

RFC: Logical AND of FIR RFC status bit and RFC mask bit.

RFS: Logical AND of FIR RFS status bit and RFS mask bit.

TAB: Logical AND of FIR TAB status bit and TAB mask bit.

TFC: Logical AND of FIR TFC status bit and TFC mask bit.

TFS: Logical AND of FIR TFS status bit and TFS mask bit.

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Chapter 14

Timers

14.1 Introduction

The timers are used to control timed events in the system. For example, a wait can be inserted by setting the timer value to an appropriate value and waiting for the timer interrupt.

The Timers block contains two 16-bit timers, one 32-bit timer and one 40-bit time stamp debug timer.

14.1.1 Features

The EP9301 has the following timer features:

- Two 16-bit timers
  - Free running
  - Load based
- One 32-bit timer
  - Free running
  - Load based
- One 40-bit timer
  - Free running

14.1.2 16 and 32-bit Timer Operation

The two 16-bit timers are referred to as TC1 and TC2. Each of these timers has an associated 16-bit read/write data register and a control register. Each counter is loaded with the value written to the data register immediately. This value will then be decremented on the next active clock edge to arrive after the write. When the timer counter decrements to “0”, it will assert the appropriate interrupt. The timer counters can be read at any time. The clock source and mode is selectable by writing to various bits in the system control register. Clock sources are 508 kHz and 2 kHz. Both of these clock sources are synchronized to the main system AHB bus clock (HCLK).

Timer 3 (TC3) has the exact same operation as TC1 and TC2, but it is a 32-bit counter. It has the same register arrangement as TC1 and TC2, providing a

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load, value, control and clear register. The 16 and 32-bit timer counters can operate in two modes, free running mode or pre-load mode.

14.1.2.1 Free Running Mode

In free running mode, counters TC1 and TC2 will wrap to 0xFFFF when they reach zero (underflow), and continue counting down. Counter TC3 will wrap to 0xFFFFFFFF when it underflows, and continues counting down.

14.1.2.2 Pre-load Mode

In pre-load (periodic) mode, the value written to the TC1, TC2 or TC3 Load registers is automatically re-loaded when the counter underflows. This mode can be used to generate a programmable periodic interrupt.

14.1.3 40-bit Timer Operation

The time stamp debug timer is a 40-bit up-counter used only for long term debugging (TC4). Its clock source is the 14.7456 MHz clock, divided by 15 to give a 983.04 kHz reference. The timer value may be read at any time by reading the lower 32-bit word first and then the high byte. Dividing the result by 983 yields a timestamp in milliseconds. The debug timer does not cause an interrupt. The timer is controlled by a single enable bit. When the timer is enabled, it begins counting from zero and when it is disabled, it is cleared back to zero. When it reaches its maximum value (0xFF_FFFF_FFFF) it wraps around to zero and continues counting upwards.

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14.2 Registers

Table 14-1: Timers Register Map

Address	Read Location	Write Location	Size	Reset Value
0x8081_0000	Timer1Load	Timer1Load	16 bits	0
0x8081_0004	Timer1Value	-	16 bits	0
0x8081_0008	Timer1Control	Timer1Control	8 bits	0
0x8081_000C	Reserved	Timer1Clear	1 bit	-
0x8081_0020	Timer2Load	Timer2Load	16 bits	0
0x8081_0024	Timer2Value	-	16 bits	0
0x8081_0028	Timer2Control	Timer2Control	8 bits	0
0x8081_002C	Reserved	Timer2Clear	1 bit	-
0x8081_0060	Timer4ValueLow	-	32	0
0x8081_0064	Timer4Enable / Timer4ValueHigh	Timer4Enable	9	0
0x8081_0080	Timer3Load	Timer3Load	32 bits	0
0x8081_0084	Timer3Value	-	32 bits	0
0x8081_0088	Timer3Control	Timer3Control	32 bits	0
0x8081_008C	Reserved	Timer3Clear	1 bit	-
0x8081_0010	Reserved	Reserved	-	-
0x8081_0030	Reserved	Reserved	-	-
0x8081_0040	Reserved	Reserved	-	-
0x8081_0090	Reserved	Reserved	-	-

Register Descriptions

Timer1Load, Timer2Load

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Load															

Address:

Timer1 - 0x8081_0000 - Read/Write
Timer2 - 0x8081_0020 - Read/Write

Reset Value:

0x0000_0000

Definition:

The Load register contains the initial value of the timer and is also used as the reload value in periodic timer mode. The timer is loaded by writing to the Load register when the timer is disabled. The Timer Value register is updated with the Timer Load value as soon as the Timer Load register is written. The Load

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register should not be written after the Timer is enabled because this causes the Timer Value register to be updated with an undetermined value.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

Load: Initial load value of the timer.

Timer3Load

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Load															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Load															

Address:

Timer3 - 0x8081_0080 - Read/Write

Reset Value:

0x0000_0000

Definition:

The Load register contains the initial value of the timer and is also used as the reload value in periodic timer mode. The timer is loaded by writing to the Load register when the timer is disabled. The Timer Value register is updated with the Timer Load value as soon as the Timer Load register is written to. The Load register should not be written to after the Timer is enabled as this causes the Timer Value register to be updated with an undetermined value.

Bit Descriptions:

Load: Initial load value of the timer.

Timer1Value, Timer2Value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															

Address:

Timer1 - 0x8081_0004 - Read Only
Timer2 - 0x8081_0024 - Read Only

Reset Value:

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0x0000_0000

Definition:

The Value location gives the current value of the timer. When the Timer Load register is written to, the Value register is also updated with this Load value.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

Value: Current value of the timer.

Timer3Value

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Value															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															

Address:

Timer3 - 0x8081_0084 - Read Only

Reset Value:

0x0000_0000

Definition:

The Value location gives the current value of the timer. When the Timer Load register is written to, the Value register is also updated with this Load value.

Bit Descriptions:

Value: Current value of the timer.

Timer1Clear, Timer2Clear, Timer3Clear

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															

Address:

Timer1 - 0x8081_000C - Write Only
Timer2 - 0x8081_002C - Write Only
Timer3 - 0x8081_008C - Write Only

Reset Value:

Not defined.

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Definition:

Writing any value to the Clear location clears an interrupt generated by the timer.

Bit Descriptions:

RSVD: This register has no readable bits. It is just a write trigger.

Timer1Control, Timer2Control, Timer3Control

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								ENABLE	MODE	RSVD		CLKSEL	RSVD		

Address:

Timer1 - 0x8081_0008 - Read/Write
Timer2 - 0x8081_0028 - Read/Write
Timer3 - 0x8081_0088 - Read/Write

Reset Value:

0x0000_0000

Definition:

The Control register provides enable/disable and mode configurations for the timer.

Bit Descriptions:

RSVD: Reserved. Unknown during a Read operation.

ENABLE: Timer enable bit. This bit must be set to “1” to enable the timer. When the timer is disabled, its clock sources are turned off. Before re-enabling the timer, its Load register must be written to again.

MODE: This bit sets the mode of operation of the timer. When set to 1, the timer is in periodic timer mode and when set to “0”, the timer is in free running mode.

CLKSEL: When set to “1”, the 508 kHz clock is selected and when set to “0”, the 2 kHz clock is selected.

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Timer4ValueLow

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Value															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Value															

Address:

Timer4 - 0x8081_0060 - Read Only

Reset Value:

0x0000_0000

Definition:

This read-only register contains the low word of the time stamp debug timer (Timer4). When this register is read, the high byte of the Timer4 counter is saved in the Timer4ValueHigh register.

Bit Descriptions:

Value: Read Only Low Word of the Timer4 counter.

Timer4ValueHigh

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD							Enable	Value							

Address:

Timer4 - 0x8081_0064 - Read/Write

Reset Value:

0x0000_0000

Definition:

This is a 9-bit read/write register.

Enable is the only bit that matters during a register write. When set to “1”, the timer is enabled and begins to count upwards.

Timer4ValueHigh is a read-only value and contains the high byte of the Timer4 counter. Note that the Timer4ValueLow register must first be read to store the high byte of the TC4 in Timer4ValueHigh register.

Bit Descriptions:

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RSVD: Reserved. Unknown during a Read operation.

Enable: Read/Write. Enable for Timer4.

Value: Read only. High Byte of the Timer4 counter.

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Chapter 15

Watchdog Timer

15.1 Introduction

The Watchdog Timer provides a mechanism for generating a system-wide reset should the system hang. This functionality allows the Watchdog to recover the system and report the recovery to software. To prevent system-wide reset, software must periodically reset the Watchdog via an APB write operation. It is possible to disable the Watchdog through either hardware or software.

The Watchdog timer circuitry consists of a 7-bit counter. The most significant bit of the counter is used to trigger the **WATCHDOG_RESETn** output signal to the system control module for generating **HRESETn**.

The amount of time before a **WATCHDOG_RESETn** is initiated as well as the duration of the reset pulse is as follows:

- Time-out or **WATCHDOG_RESETn**
  duration = 64 / WATCHDOG_CLK frequency (units are seconds).
- For a 256 Hz WATCHDOG_CLK, time-out and reset pulse duration are 64 / 256 = 250 msec.

To keep the reset pulse from occurring, SW must reset the Watchdog timer (sometimes known as “kick the dog”) to a predetermined count on a periodic basis. This resets the counter, which prevents the **WATCH_RESETn** from activating. The counter is reset by writing 0x5555 to the Watchdog register. The Watchdog should be reset at least 2 WATCHDOG_CLK periods earlier than the time-out calculation would indicate, due to clock synchronization and handshaking circuitry.

Once a Watchdog reset occurs, the timer also provides a 250 msec duration reset pulse. The Watchdog also defaults to providing the pulse duration when the reset is from other sources such as user reset (external reset on **RSTOn**), AMBA bus reset (**HRESETn**), or power on reset (internal chip voltage detect power on signal **PWR_RESETn**). The reset pulse duration can be disabled by pulling the **CSn[2]** (**HW_RSTPULSE_DISABLEn**) signal low during the bus reset (**HRESETn** low). This immediately frees the Watchdog reset output line when reset becomes inactive. In either case, if the reset pulse duration is provided or not, the Watchdog counter will start over after the **WATCHDOG_RESETn** output becomes inactive. This begins a new 250 msec cycle after reset becomes inactive before software must reset the counter.

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15.1.1 Watchdog Activation

The Watchdog circuitry may be disabled via software for test purposes on products that do not wish to use a Watchdog timer by writing 0xAA55 to the Watchdog register. The Watchdog may also be re-enabled via software by writing 0xAAAA to the Watchdog register.

The Watchdog circuitry may be disabled via hardware on products that do not need to use a Watchdog timer, by applying an external pull down on the **CSn[1]** (**HW_WATCHDOG_DISABLEn**) signal during reset. This will allow the block to detect the presence of the resistor during the bus reset (**HRESETn** low) and disable the counter. During reset, the chip will disable the output driver and provide a weak pull-up resistor on this pad.

15.1.2 Clocking Requirements

The WATCHDOG_CLK for stepping the counter in the Watchdog has a frequency that is nominally 256 Hz, for generating a 250 ms time-out and a 250 ms reset pulse duration.

15.1.3 Reset Requirements

The Watchdog block has the following four reset inputs:

- **HRESETn**: This is the AHB bus reset signal from the Syscon block, which includes a software reset.
- **USR_RESETn**: This is the external user reset input, and its status is kept in register Watchdog[2].
- **PWR_RESETn**: This is the power-on-reset input for resetting everything including reset status bits. The power-on-reset is generated by a combination of the external **PRSTn** pin and the on chip voltage monitor/power up detector.

15.1.4 Watchdog Status

The Watchdog timer register can be read to determine the cause of a reset. The register contains user reset status (external reset on **RSTOn**) and Watchdog reset status bits (reset caused by **WATCHDOG_RESETn**). The state of these bits determines if the reset condition was the result of a user reset, a power on reset, or a watch dog time-out. The status of these bits can only be cleared by a power on reset (internal chip voltage detect power on signal **PWR_RESETn**). An additional 7-bit status register is provided in the Watchdog module as WDSTAT. This status value is held through all resets but power on reset. The system can be reset by a user reset or a Watchdog reset without losing the contents of this register.

Note: A software reset can reset the system without this register losing its contents.

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15.2 Registers

Table 15-1: Register Memory Map

Address	Name	SW locked	Type	Size	Description
0x8094_0000	Watchdog	No	Read/Write	16/3 bits	Watchdog Control Register
0x8094_0004	WDStatus	No	Read/Write	7 bits	Watchdog Status Storage Register

Note: Watchdog registers are intended to be word-accessed only. Since the least significant bytes of the address bus are not decoded, byte and half word accesses are not allowed and may have unpredictable results.

Register Descriptions

Watchdog

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CTL								CTL/PLSDSN	CTL/OVRID	CTL/SWDIS	CTL/HWDIS	CTL/URST	RSVD		CTL/WD

Address:

0x8094_0000 - Read/Write

Default:

0x0000_0000

Definition:

Watchdog control register.

Bit Descriptions:

RSVD: Reserved. Unknown during read.

WRITE ONLY BIT FIELDS

CTL: Watchdog control bits. The processor writes 0x5555 to this hword to periodically restart the watchdog timer. Writing 0xAA55 to this hword will disable the watchdog timer. Writing 0xAAAA to this hword will re-enable the watchdog timer.

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READ ONLY BIT FIELDS

PLSDSN: Pulse Disable Not. The Watchdog internal PLSDIS bit monitors the **HW_PULSE_DISABLEn** latch status in the watchdog module. This provides status of the hardware pulse duration disable function. Active low means that the reset pulse is disabled.

OVRID: Software Override of the hardware watchdog disable. The OVRID bit monitors the SW_OVERIDE_HW_DISABLE register status in the watchdog module. This provides status of the watchdog software disable overriding the hardware disable function. This bit is active high when the software disable is overriding the hardware disable.

SWDIS: Software Watchdog Disable. The SWDIS bit monitors the SW_WATCHDOG_DISABLE register status in the watchdog module. This provides status of the watchdog software disable function. This bit is active high when the watchdog is software disabled.

HWDIS: Hardware Watchdog Disable. The HWDIS bit monitors the **HW_WATCHDOG_DISABLEN** latch status in the watchdog module. This provides status of the watchdog hardware disable function. This bit is active high when the watchdog is hardware disabled.

URST: User Reset Status flip flop. Read only. When “1”, this bit indicates that the last reset was generated by the user reset signal (externally on **RSTOn**). This bit is not cleared by any resets other than power on reset, **PWR_RESETn**.

WD: Watchdog Reset Status flip flop. Read only. When “1”, this bit indicates that the last reset was generated because of a watch dog time out. This bit is not cleared by any resets other than power on reset, **PWR_RESETn**.

WDStatus

Address:

0x8094_0004 - Read/Write

Default:

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0x0000_0000

Definition:

Watchdog status storage register. It can be used for storing your own status, and it can only be cleared by power-on-reset.

Bit Descriptions:

RSVD: Reserved. Unknown during read.

STAT: Watchdog Status bits. This is a watchdog status storage register that is not cleared by any resets other than power-on-reset and **PWR_RESETn**. The system can be reset by a user reset or a watchdog reset without losing the contents of this register.

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Chapter 16

Real Time Clock With Software Trim

16.1 Introduction

The Real Time Clock (RTC) is a circuit within the EP9301 that keeps track of the system date and time. The RTC operates from the normal device power supply and the 32 kHz input clock. The RTC circuit operates whenever power is applied to the device and the 32 kHz input clock is running.

The Real Time Clock section is composed of two blocks - Real Time Clock and the RTC TRIM.

The RTC module provides second level precision for internal time keeping. In addition, the block provides an interrupt based on a comparison register. The Real Time Clock block operates whenever power is applied and the 32 kHz input clock is running. However, the RTC cannot be used to wake the system via it's interrupt when the system is in a STANDBY or HALT state, where PCLK is inactive.

The RTC TRIM block takes the 32,768 Hz clock from the RTC oscillator and creates a digitally compensated 1 Hz reference clock for use by the time keeping functions.

Note: The 32,768 Hz clock is referred to as the 32 kHz clock throughout the text.

16.1.1 Software Trim

The Real Time Clock oscillator software compensation circuitry allows software controlled digital compensation of a 32.768 kHz crystal oscillator. Typically, crystal oscillators must be externally compensated using discrete components. They are mechanically calibrated during manufacture. Software controlled digital compensation allows the oscillator to be electronically calibrated by automatic test equipment during manufacture. The circuit also enables readjustment in the field under software control.

The RTCSWComp register value is determined by manufacturing during board initialization to adjust the frequency of the 1 Hz clock. Refer to "Software Compensation" on page 440 for details on how to calculate the value in this register. This value is then stored in FLASH memory for retrieval when the product is first enabled in the field. The compensation values need to be restored once the RTC is permanently enabled for field use.

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The compensation value consists of two parts: a counter preload value to act as an integer divider, (RTCSWComp.INT[15:0]), and the number of 32.768 kHz clocks to delete on a periodic interval (RTCSWComp.DEL[4:0]).

16.1.1.1 Software Compensation

The 1 Hz clock is generated by running a programmable counter clocked by the 32.768 KHZ crystal oscillator reference. If the crystal reference and oscillator were perfect, a counter that counted 32768 clocks would provide a 1 Hz reference. However, the counter pre-load value is programmable to allow inaccuracies in the crystal and oscillator circuit. Simply allowing a different counter pre-load value only gives an accuracy of:

(½LSB / 32768 bits) x (3600 sec / 1 hr) x (24hrs/day) x (30 days/month)
~= +/- 40 sec per month

To further increase the accuracy, a fractional compensation is needed. This compensation mechanism provides a much better nominal RTC accuracy. The 1 Hz clock feeding the RTC is obtained by dividing the output of the 32.768 KHZ oscillator by an integer value. However, factors such as inaccuracy of the crystal, varying capacitance of the board traces, leads, and connections, etc., will cause the reference frequency to be inaccurate. This is corrected in software by adjusting the 1 Hz clock period through an integer compensation (by adjusting the counter preload) and with a fractional compensation (via deleting clocks at a fixed interval). By measuring the frequency of the reference crystal, and setting the RTCSWComp register value, the clock can be adjusted to a nominal accuracy of better than +/- 5 seconds per month.

16.1.1.2 Oscillator Frequency Calibration

Manufacturing can use a high precision frequency counter to measure the RTC 32.768 kHz reference clock via the **EGPIO[1]** pin when the RSTCR.RonG bit is set. This mode isolates the measurement of the oscillator circuit during manufacturing test to avoid disturbing the crystal reference frequency through added probe capacitance, etc. The compensation is accomplished by dividing the output of the oscillator by a integer value (with a pre-loadable counter) and then doing a fractional adjustment by periodically deleting clocks to the counter.

16.1.1.3 RTCSWComp Value Determination

After the true frequency of the oscillator is known, it is separated into integer and fractional portions. The integer portion of the frequency (less one) is set as the counter pre-load value. When the counter reaches zero, a carry pulse is generated and the counter is pre-loaded again. The carry pulse is used as the RTC 1 Hz signal reference.

The fractional part of the adjustment is done by deleting clocks from the clock stream feeding the integer counter. The period interval between deleting

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clocks is 32 seconds. The number of clocks deleted is set by RTCSWComp.DEL[4:0].

16.1.1.4 Example - Measured Value Split Into Integer and Fractional Component

The manufacturing tester measures the oscillator output to be 33,455.870 Hz. For the integer portion, 33,455 - 32,768 is 687 cycles over the nominal frequency of the crystal. The integer pre-load value for the counter should always be chosen so that the actual clock frequency is faster than the value needed to generate a 1 Hz reference. Therefore, the RTCSWComp.INT[15:0] value is loaded with the binary equivalent of 33,455-1 or 0x82AE.

The fractional component of the oscillator output was measured to be 0.870 Hz. Software must adjust the clock so that the average number of cycles that are counted before generating one 1 Hz clock is 33 455-1.

Because the clock frequency is 0.870 Hz faster than the integer value, the 1 Hz clock generated by just the integer compensation is slightly faster than needed and may be slowed down by deleting clocks.

The fractional compensation value must be programmed to delete 0.870 Hz on average to bring the 1 Hz output frequency down to the proper value. Since the compensation procedure is performed only every 32 seconds, the value must be set to delete (0.870*32) = 27.84 which, when rounded, is 28 clocks every 32 seconds. The rounded 0.16 cycles per 32 seconds (or 0.005 Hz) represents the error in compensation. The RTCSWComp.DEL[4:0] fractional compensation value should be loaded with the hexadecimal equivalent of 28 - 1 or 0x1B.

16.1.1.5 Maximum Error Calculation vs. Real Time Clock Accuracy

The maximum error is 0.5½ clocks per 32 seconds. Therefore at 32.768 kHz, the maximum error is:

(0.5½ clock / 32 sec) x (1 sec / 32,768 clocks nominal) x
(2592000 sec/1month) = 1.24 seconds/month maximum error

To maintain an accuracy of +/- 5 seconds per month the required interval is calculated to be:

(5 seconds/1 month) x (1 month/2,592,000 seconds) = 1.93E-6

= (1 second/32,768 clocks) x (½clock / X-interval seconds)

X-interval = 7.9 seconds

Therefore to maintain a 5-second-per-month accuracy the compensation circuit only has to adjust within ½ of a 32.768 KHZ clock every 7.9 seconds. This could be done with a 3 bit clock delete value and an 8 second (3 bits clocked by 1 Hz) counter. However, the 1.24 second per month number is better and has been implemented in this device.

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16.1.1.6 Real-Time Interrupt

To allow a Real Time Interrupt to be generated, VIC2 **INT[10]** has been connected to the 1 Hz clock. This interrupt should be configured as edge-triggered.

16.1.2 Reset Control

The RTC block level reset operation is a bit complicated. The reset strategy is for the time-keeping part of the RTC to survive a system reset, and only be initialized by a power-on reset. The RTC interrupt enable is cleared by a user reset, so that a time count match (alarm interrupt) would disable with system reset.

The following register is initialized only by **PRSTn**: RTCSWComp

The following registers are initialized by **PRSTn**: RTCData, RTCMatch, RTCLoad, and RTCCtrl.

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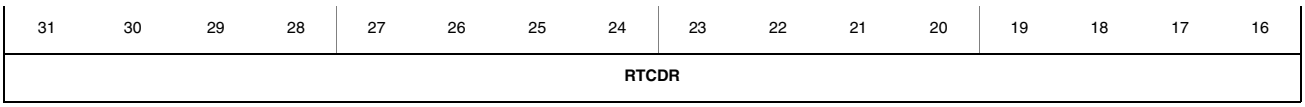
16.2 Registers

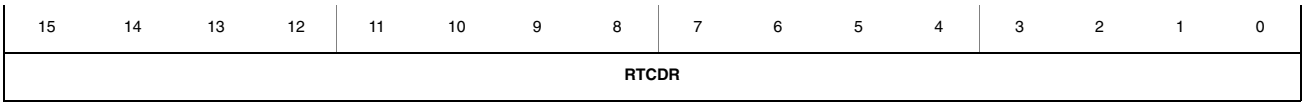
Table 16-1: Register Memory Map

Address	Name	Description
0x8092_0000	RTCData	RTC Data Register
0x8092_0004	RTCMatch	RTC Match Register
0x8092_0008	RTCSts	RTC Status/EOI Register
0x8092_000C	RTCLoad	RTC Load Register
0x8092_0010	RTCCtrl	RTC Control Register
0x8092_0108	RTCSWComp	RTC Software Compensation

Register Descriptions

RTCData





Address:

0x8092_0000 - Read Only

Default:

0x0000_0000

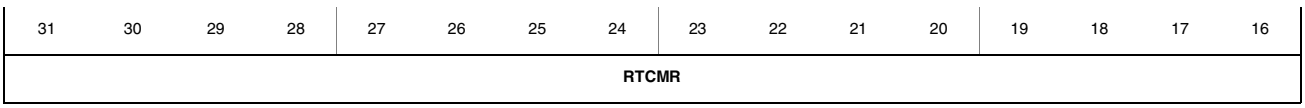
Definition:

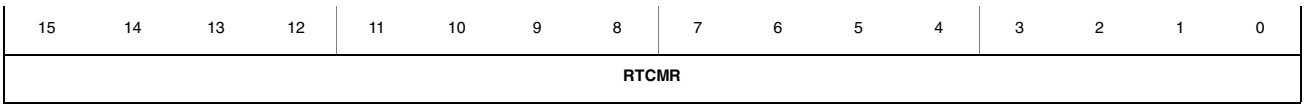
RTC Data Register. Contains the 32 bit RTC counter value. This counter is incremented by the 1 Hz clock output from the RTC Trim module.

Bit Descriptions:

RTCDR: Counter value.

RTCMatch





Address:

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0x8092_0004 - Read/Write

Default:

0x0000_0000

Definition:

RTC Match Register. Contain the 32 bit match value. When the RTCData value equals the RTCMatch value the RTC will generate an interrupt if the RTCCtrl.MIE bit is set to “1”.

Bit Descriptions:

RTCMR: Match value.

RTCSts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															INTR

Address:

0x8092_0008 - Read/Write

Default:

0x0000_0000

Definition:

RTC Interrupt Status and End Of Interrupt Register. Writing to this register clears the asserted interrupt.

Bit Descriptions:

RSVD: Reserved, unknown during read.

INTR: Interrupt status,
1 - RTC interrupt is asserted
0 - no interrupt.

RTCLoad

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RTCLR															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RTCLR															

Address:

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0x8092_000C - Read/Write

Default:

0x0000_0000

Definition:

RTC Load Register. Contains the 32 bit load value. Data written to this register is transferred to the RTCData on the next 1 Hz tick.

Bit Descriptions:

RTCLR: Load value.

RTCCtrl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															MIE

Address:

0x8092_0010 - Read/Write

Default:

0x0000_0000

Definition:

RTC Interrupt Control Register. Contains the interrupt enable control bit.

Bit Descriptions:

RSVD: Reserved, unknown during read.

MIE: Match Interrupt Enable,
1 - RTC match interrupt is enabled
0 - interrupt disabled.

RTCSWComp

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD										0	DEL				

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
INT															

Address:

0x8092_0108 - Read/Write

Default:

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0x0000_7FFF

Mask:

003F_FFFF

Definition:

RTC Software Compensation Register.

Bit Descriptions:

RSVD:	Reserved. Unknown During Read.
0:	Must be written as “0”.
DEL:	Number of clocks to delete. This value determines the number of 32.768 KHZ clocks to delete every 32 seconds for compensating the oscillator. The value defaults to 0x0 which deletes no clock pulses.
INT:	Counter pre-load Integer value. This value is pre-loaded into the counter as the integer divide portion of the oscillator compensation. If set to 0x0000, no integer divide occurs and no clock pulses are deleted. The value defaults to 0x7FFF which causes the divider to divide by exactly 32,768 to generate a 1 Hz clock.

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Chapter 17

I²S Controller

17.1 Introduction

The I²S controller is used to stream serial audio data between the external I²S CODEC's ADCs/DACs and the ARM processor. It consists of a stereo transmitter channel and a stereo receiver channel. The transmitter and receiver are completely independent of each other and are programmed separately. Each channel (RX and TX) has its own set of addressable registers which allows access through the ARM APB or DMA accesses.

Figure 17-1 on page 448 gives an architectural overview of the I²S controller.

The i2s_audioclk_mux section performs gating on the incoming audio clocks based on the settings within the TX and RX clock configuration registers and delivers a known clock definition to the rest of the I²S controller.

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Figure 17-1. Architectural Overview of the I2S Controller

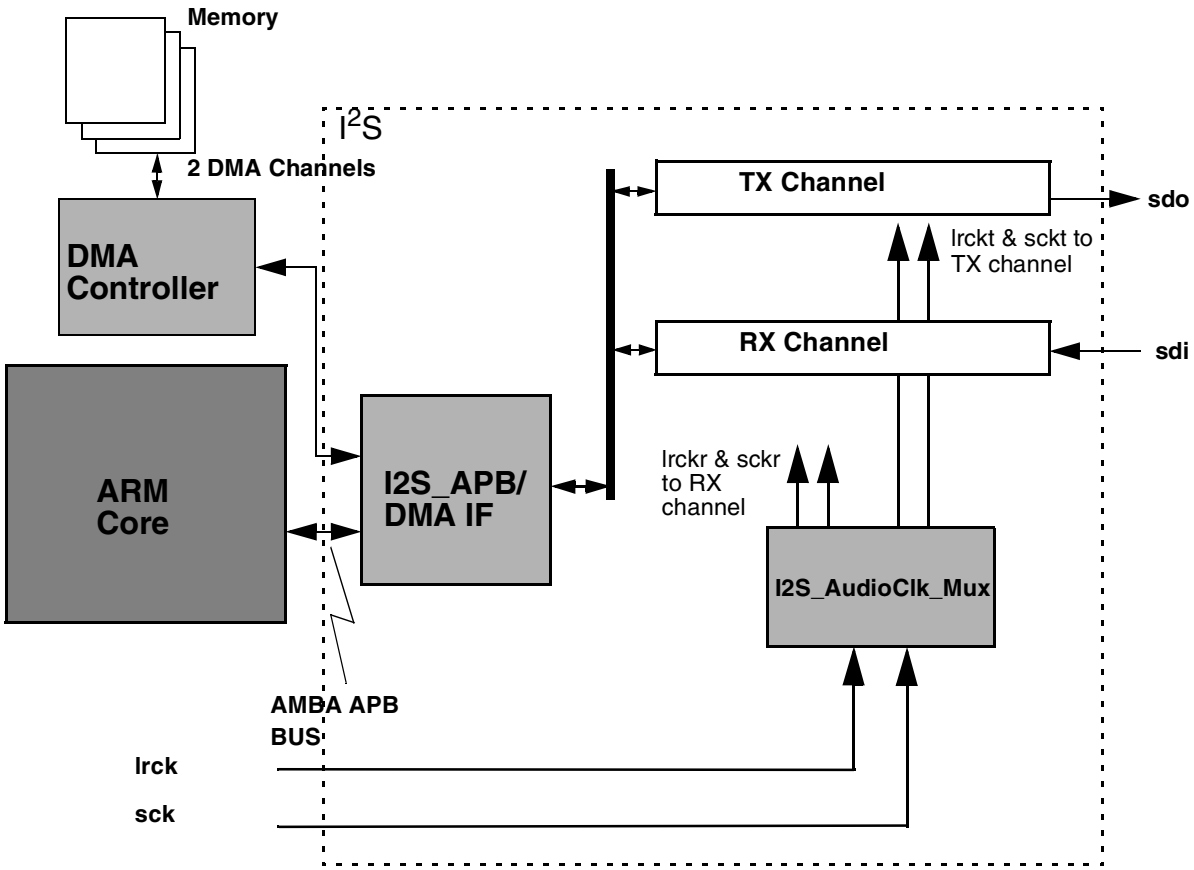

Table 17-1: I2S Controller Input and Output Signals

Signal Name	Type	Description
Irck	IN	Left/right Word Audio slave clock.
sck	IN	Audio bit slave clock.
sdi	IN	Serial data input
sdo	OUT	Serial data output

The I2S port and the I2S clocks are multiplexed and can be assigned to either the SSP pins or the AC'97 pins.

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Table 17-2: Audio Interfaces Pin Assignment

Pin Name	Normal Mode Pin Description	I2S on SSP Mode Pin Description	I2S on AC'97 Mode Pin Description
SCLK1	SPI Bit Clock	I2S Serial Clock	SPI Bit Clock
SFRM1	SPI Frame Clock	I2S Frame Clock	SPI Frame Clock
SSPRX1	SPI Serial Input	I2S Serial Input	SPI Serial Input
SSPTX1	SPI Serial Output	I2S Serial Output	SPI Serial Output
		(No I2S Master Clock)	
ARSTn	AC'97 Reset	AC'97 Reset	I2S Master Clock
ABITCLK	AC'97 Bit Clock	AC'97 Bit Clock	I2S Serial Clock
ASYNC	AC'97 Frame Clock	AC'97 Frame Clock	I2S Frame Clock
ASDI	AC'97 Serial Input	AC'97 Serial Input	I2S Serial Input
ASDO	AC'97 Serial Output	AC'97 Serial Output	I2S Serial Output

17.2 I²S Transmitter Channel Overview

The I²S TX channel provides a single stereo I²S compliant output. The Transmit channel can operate in master or slave mode. Data is transferred between the ARM core and the I²S controller via an interrupt based mechanism or DMA access. The ARM or host processor must write words in multiples of 2 (that is, a left and right stereo pair). These words are serially shifted out, timed with respect to the audio bit clock and word clock (SCLK and LRCK) that are generated (see “Clock Control” on page 69 for additional details). The key features of the I²S transmitter are:

- One stereo transmit data channel, master or slave mode.
- Supports 16/24/32 bit word lengths.
- Programmable left/right word clock polarity on the serial frame.
- Programmable Bit Clock polarity.
- Programmable data validity, that is, data valid on the rising/negative edge of the bit clock.
- Programmable first data bit position (I²S or non-I²S format).
- Programmable Left or Right data word justification
- Programmable data shift direction, that is, MSB or LSB transmitted first.
- Data underflow detection, that is, re-transmission of old data.
- Clock domain synchronization.
- DMA access.

The basic operation of the I²S transmitter is the ARM or host processor writes 2 words (left and right stereo pair) to the I²S channel. These words are serially shifted out, timed with respect to SCLK.

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Figure 17-2. Transmitter FIFO

	Right Sample 7	Byte 7	Byte 6	Byte 5	Byte 4
7	Left Sample 7	Byte 3	Byte 2	Byte 1	Byte 0
	Right Sample 6	Byte 7	Byte 6	Byte 5	Byte 4
:	:	:	:	:	:
:	:	:	:	:	:
	Right Sample 0	Byte 7	Byte 6	Byte 5	Byte 4
1	Left Sample 1	Byte 3	Byte 2	Byte 1	Byte 0
	Right Sample 0	Byte 7	Byte 6	Byte 5	Byte 4
0	Left Sample 0	Byte 3	Byte 2	Byte 1	Byte 0

The TX channel has a 16 deep by 32-bit wide FIFO where the ARM or DMA controller can write up to 8 sets of left/right data pairs before enabling the channel for transmission. In order to fill the FIFO the following sequence of events must be performed by the programmer.

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1. Enable I2S controller: The I2S global control register bit, I2SGlCtrl[0] must be written to in order to turn on the PCLK to the I2S controller. The I2S controller will not function correctly if this is not done.

2. Write to the FIFO: Once the I2S controller is enabled, the TX FIFO may be written to by either the DMA or the ARM.

   The FIFO is split up into 8 locations. Each location consists of 2 X 32-bit register and can hold one left and one right stereo sample (16, 24 or 32 bits per sample). For APB accesses, the left and right samples must be written to different addresses: I2STXLft register address for left samples and I2STXRt register address for right samples (see register definitions).

   In order to fill a FIFO location, the programmer must write two data words, corresponding to left and right stereo data, to the FIFO. Only when both words are written by the programmer will the be FIFO be loaded. Assuming this is the first FIFO write, these two words will occupy positions 0 and 1 in the FIFO. The FIFO now contains one complete left / right stereo sample. The words written by the programmer must always be right justified when writing 16-bit and 24-bit values.

   If the programmer writes another left and right stereo sample to the I2STXLft and I2STXRt registers respectively, these words are loaded into the FIFO and will occupy positions 2 and 3. Subsequent writes will fill positions 4 and 5 and so on. The FIFO full flag is set when all 8 FIFO locations are filled by left / right sample pairs.

   If an attempt is made to write another left / right stereo pair to the FIFO

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while it is full, the new samples are ignored and the FIFO overflow flag is set. (See “Register Descriptions” on page 448 on clearing this flag.) None of the existing FIFO locations are overwritten.

3. Enable the I²S transmit channel

   Once the FIFO has been loaded, the channel enable I2STXEn one-bit register (see “I²S TX Register Descriptions” on page 461) is set. At this point, both the left and right stereo data from the 1st FIFO location are read by the I²S controller and copied into separate left and right holding registers. The left holding register is parallel loaded into a shift register and is serially shifted out the I²S sdo data line. This shifting out process is timed on the I²S audio word and bit clock. Once the left sample is shifted out, the right holding register is parallel loaded into the shift register and is serially shifted out the I²S sdo line.

   If the I²S controller is programmed to transmit 16 or 24 bit words, the lower 16 or 24 bits are taken from the holding registers and loaded into the shift register. The upper bits are ignored by the I²S controller.

When the right sample is loaded into the shift register, the I²S controller reads the next left and right stereo samples from the 2nd FIFO location. After these have been loaded into the shift register in the same manner as above, FIFO location 3 is read and so on. After samples 15 and 16 (FIFO location 7) are taken from the FIFO, the FIFO read pointer will wrap around to location 0 and continue as before as long as the channel is enabled. If the I²S controller is disabled at any point, all FIFO locations are zeroed and the FIFO write and read pointers are reset.

If the transmit channel corresponding to the FIFO is disabled, the I²S controller will stop transmitting the current sample that is in the shift register. The data in the FIFO is not touched and the FIFO read and write pointers stay as they are. Upon re-enabling the channel, the I²S controller will read the next left and right stereo samples from the FIFO currently being pointed to by the read pointer and transmit them. The effect of this is that the data currently residing in the holding registers at the time the channel is disabled is lost.

If the programmer wants to end transmission of data completely while there is data in the FIFO they should first disable the corresponding channel. This action will ensure that the channel’s state machines are reset. The next step should be to disable the I²S controller, which will result in the FIFO being reset. Any samples currently in the FIFO will be lost as a result.

If the control registers are to be changed at any time by the user, the I²S transmit and receive channels should be disabled before doing so. Once the new configuration has been set, the channels can be re-enabled following the specified start order.

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If a channel is enabled while the FIFO is empty, no samples are read from the FIFO. The I2S controller will parallel load whatever is currently in the left holding register into the shift register. Once these contents have been shifted out, the right holding register is then parallel loaded into the shift register and then shifted out. If this occurs after the I2S controller has been reset, these holding registers will contain zero. If the I2S controller has been re-enabled after an earlier transmission, the holding registers will contain the last samples that were copied into them. As before, the I2S controller will attempt to read the FIFO after the right holding register has been loaded into the shift register. At this point, if the FIFO is still empty, the I2S controller will assert the FIFO underflow flag. No attempt is made to read the FIFO by the I2S controller and the read pointer stays pointing to location 0. The underflow will update a status bit in the Global Control Status register, I2SGISts. (See “Register Descriptions” on page 448.) To clear the underflow the programmer must write at least one left and right stereo sample to the FIFO. Disabling the I2S controller will also clear the underflow.

The status of the FIFO is reflected by 5 bits in the Global Control Status register. They are as follows:

- Tx_underflow - Gets set when the I2S controller reads the FIFO when it is empty.
- Tx_overflow - Gets set when the programmer attempts to write to the FIFO when it is full.
- Tx_fifo_empty - Gets set when there no left and right stereo samples in the FIFO.
- Tx_fifo_half_empty - Gets set when there are 4 left and right stereo samples or less in the FIFO.
- Tx_fifo_full - Gets set when there are 8 left and right stereo samples in the FIFO.

17.3 I2S Receiver Channel Overview

The I2S Receiver channel enables audio compression algorithms executing on the ARM core to receive stereo information from external CODECS.

The I2S RX channel provides a single stereo I2S compliant input channel. The Receive channel can operate in master and slave mode. Data is received from the channel input and transferred into two registers, the left and right stereo pair. The ARM can then read the data from the channel. The key features are shown below.

- One stereo Receive data channel, master or slave mode.
- Supports 16/24/32 bit word lengths.
- Programmable left/right word clock polarity on the serial frame.

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- Programmable bit clock polarity.
- Programmable data validity, that is, data valid on the rising/negative edge of the bit clock.
- Programmable first data bit position. that is, I²S or non-I²S format.
- Programmable left or right data word justification.
- Programmable data shift direction, that is, MSB or LSB received first.
- Data overflow detection.
- Clock domain synchronization.
- DMA accesses.

The basic operation of the I²S receiver is that data is serially shifted in to form to a pair of left /right words. These pair of words are written to a FIFO which the ARM will read.

17.3.1 Receiver FIFO

The receiver channel has a 16 deep by 32 bit wide FIFO where the ARM or DMA controller can read up to 8 sets of left / right data pairs. In order to receive left and right stereo data into the FIFO and read this data out from the FIFO, the following sequence of events must be performed by the programmer.

1. Enable the I²S controller.

   The I²S global control register bit, I2SGlCtrl[0], must be written to in order to turn on the PCLK to the I²S controller. The I²S controller will not function correctly if this is not done.

2. Enable the receive channel.

   The channel corresponding to the FIFO must be enabled in order for it to start sampling the data line. After being enabled, the I²S controller will wait until the start of the next incoming left stereo word, which is indicated by the audio word clock. When the start of the left word occurs, the I²S controller will sample the data line and load each bit into a dedicated left shift register. At the end of the left word and start of the right word as indicated by the audio word clock, the contents of the left shift register are loaded into a left data register. The I²S controller will continue to sample the data line loading each bit into a dedicated right shift register. At the end of the right word and start of the next left word, the contents of the right shift register are loaded into a right data register. One complete left and right stereo sample has now been received.

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At this point, the I²S controller signals to the FIFO that there is valid data ready to be written to the FIFO. The I²S controller will then write this stereo sample to FIFO location 0, which consists of 2 x 32 bit registers (assuming that this is the first sample to be received). The FIFO-empty bit in the I²S Global Control Status register, I2SGlSts is now deasserted. As more stereo sample pairs are received, they will be written to locations 1, 2, 3 and so on.

The programmer can determine from the Global Control Status register if the FIFO has any valid left / right stereo samples. These samples are obtained from the FIFO via the APB by reading from the I2SRX0Lft and I2SRX0Rt registers. (See "Register Descriptions" on page 448.) Note that both left and right sample registers must be read in order for the I²S controller to consider the location to be free and modify the internal counter.

If the programmer attempts to read from the FIFO while it is empty, the contents that were last read from the FIFO will be put onto the APB bus. The FIFO read pointer is not updated and stays pointing to the same location. The FIFO underflow flag in the Global Control Status register is asserted. (See "Register Descriptions" on page 448.) If this happens to be the first attempted read by the programmer on the FIFO while the FIFO is still empty, the contents at FIFO location 0 are put onto the APB bus. These contents are zero if the I²S controller has been reset previously.

If the I²S controller signals to the FIFO that new stereo sample pairs have been received and the FIFO is full, the new samples are ignored. The existing contents in FIFO locations 0 to 7 are not touched. An internal Overflow bit is set, marking the FIFO pointer location at which the last good data was received (that is, at [current FIFO pointer location - 1]). When the FIFO pointer eventually points at this location again, after reading all 7 other FIFO locations, the FIFO overflow flag in the Global Control Status Register is asserted (and an interrupt is asserted, if enabled). The Status Register bit (and interrupt) is cleared by reading a left / right stereo sample pair from this FIFO location.

The data in the FIFO is always right justified for word lengths of 16 and 24 bits. The upper bits will be set to zero by the I²S controller in this case.

If the control registers are to be changed at any time by the user, the I²S transmit and receive channels should be disabled before doing so. Once the new configuration has been set, the channels can be re-enabled following the specified start order.

The status of the FIFO is reflected in the Global Control Status register. This register has 5 bits per FIFO that reflect the state of the FIFO. They are:

- Rx_underflow - Gets set when the programmer reads the FIFO when it is empty.

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- Rx_overflow - Gets set when an Rx overflow has occurred, and the FIFO pointer is pointing at the last FIFO location where data was received before the overflow occurred
- Rx_fifo_empty - Gets set when there are no left and right stereo samples in the FIFO.
- Rx_fifo_half_full - Gets set when there are 4 left and right stereo samples or less in the FIFO.
- Rx_fifo_full - Gets set when there are 8 left and right stereo samples in the FIFO.

17.4 I²S Configuration and Status Registers

The I²S deals with the following:

- Generates the clock configuration signals that are used in the i2s_audioclk_mux block. This block uses these to perform the correct audio clock gating.
- Generates the clock configuration signals that can be used or overridden in the Syscon block. Syscon can use these signals to generate the master clocks.
- Selects between master and slave audio clocks.

The following table summarizes the register set in the APB/DMA interface. Each of the registers listed are addressable. The registers can be only accessed through the APB bus. In Master Mode, the clock setting can be overridden by the Syscon register I2SClkDiv.

17.5 I²S Master Clock Generation

The following information is required to generate a set of clocks for the I²S controller. The I²S port i2s_mstr_clk_cfg is used to supply the Syscon block the necessary control information in order to generate a set of audio clocks, LRCK (word clock) and SCLK (bit clock). The control bits required are:

- Master Mode Enable. (i2s_mstr_clk_cfg[0])
- Word Length Control (i2s_mstr_clk_cfg[2:1])
- Bit Clock Polarity (i2s_mstr_clk_cfg[3])
- Not Bit Clock Gating (i2s_mstr_clk_cfg[4]).
- Bit Clock Rate (i2s_mstr_clk_cfg[6:5])

These control bits come from the TX and the RX clock configuration registers and the word length registers. This control is sent out through the i2s_mstr_clk_cfg port of the I²S controller to the audio clock generator. The

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audio clock generator responds with the correct clock definition based on the settings received.

If both the TX and RX are required to be in master mode at the same time, both the RX and TX share the same master audio clocks. The following shows how i2s_mstr_clk_cfg is generated.

- If the Transmitter is enabled, the clock configuration information will always come from I2STXClkCfg register. Therefore, the I2SRXClkCfg (receiver clock configuration) register must be configured to be the same as the I2STXClkCfg (transmitter clock configuration) register in order to ensure correct operation of the receiver. The word lengths for both the TX and RX must be the same.
- If the Transmitter is disabled and the Receiver is required to be in master mode, then the i2s_mstr_clk_cfg output is generated from the I2SRXClkCfg register and the RX word length register.

Please note, the I2SClkDiv (Addr=0x8093_008C) register in the SYSCON block has an effect on I2S clock generation as well. The details are listed in Table 17-3 on page 457. The controlling bitfield for each function is determined by the ORIDE bit in the I2SClkDiv register (I2SClkDiv[29]). This table does not show the details of how to control this function. Please refer to each individual block for a detailed description.

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Table 17-3: I2SClkDiv SYSCON Register Effect on I2S Clock Generation

Function	ORIDE=1	ORIDE=0
SCLK polarity	SPOL (I2SClkDiv[19])	i2s_mstr_clk_cfg[3]
SCLK Speed and Gating	DROP(I2SClkDiv[20]), SDIV(I2SClkDiv[16])	SCLK always is MCLK/2. SCLK is gated when i2s_mstr_clk_cfg[4]=0 **and**, i2s_mstr_clk_cfg[6:5]=0 **and,** i2s_mstr_clk_cfg[2:1]=1, otherwise, SCLK is not gated.
LRCK Speed	LRDIV(I2SClkDiv[18:17])	i2s_mstr_clk_cfg[6:5]
Audio Slave Mode Audio Clock (SCLK, LRCLK) Generation Enable	SLAVE(I2SClkDiv[30]) SENA(I2SClkDiv[31])	i2s_mstr_clk_cfg[0] I2SonAC97 (DeviceCfg[6]) or I2SonSSP (DeviceCfg[7]). If either one is set, it enables the clock generation.
Output Data Bit Align to SCLK Edge	When SPOL=1 and i2s_mstr_clk_cfg[3]=0, transition of output data bit and LRCK align to falling edge of SCLK When SPOL=0 and i2s_mstr_clk_cfg[3]=1, transition of output data bit and LRCK align to rising edge of SCLK;	The output data bit is always a half-cycle later to the SCLK edge which aligns to LRCK transition. If the SCLK rising edge is configured to align to the LRCK transition, then output data is aligned to falling edge of SCLK. If the SCLK falling edge aligns to the LRCK transition, then output data aligns to the SCLK rising edge.

17.6 I²S Bit Clock Rate Generation

Table 17-4: Bit Clock Rate Generation

Word Length	Bit Clock Rate (BCR[1:0])	not Bit Clock Gating (nBCG)	Actual bit clock rate with respect to LRCK
16	00	0 or 1	32x
24	00	0	64x with last 8 cycles gated off in each word.
24	00	1	64x Note the last 8 cycles are not gated off.
32	00	0 or 1	64x
Ignored	01	Ignored	Fixed at 32x
Ignored	10	Ignored	Fixed at 64x
Ignored	11	Ignored	Fixed at 128x

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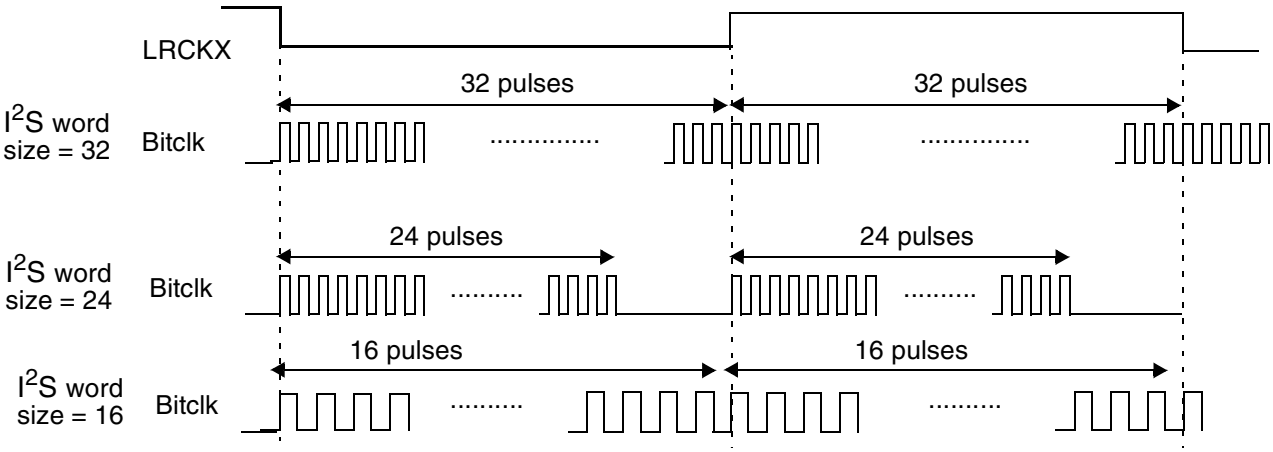
17.6.1 Example of the Bit Clock Generation.

For nBCG = 0 and BCR[1:0] = “10” the bit clock frequency is fixed at 64 times LRCK for word lengths of 32 and 24 and at 32x LRCK for word lengths of 16. In the case of 24 and 32 bit words, this 64x clock is then gating depending on the I2S controller word size. If the I2S controller word size is 32, then all of the 64x clock pulses are passed. If the I2S controller word size is 24, then the last 8 64x clock pulses are gated off in a LRCK cycle. For an I2S controller word size of 16 than all of the 32x clock pulses are passed. This is shown in Figure 17-3.

For other values of nBCG and BCR, the register bit descriptions define the bit clock operation.

Figure 17-3. Bit Clock Generation Example



17.6.2 Example of Right Justified LRCK format

Figure 17-4 shows the frame format for Right Justified data. The word length is 16 in this case and the MSB is transmitted first. The bit clock rate is 64x so the for the first 16 clock cycles in each word there is no data as it is right justified in each word frame.

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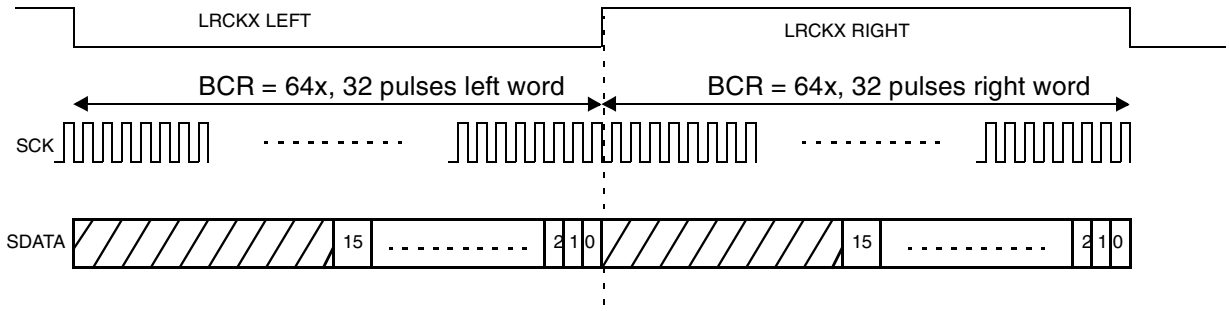
Figure 17-4. Frame Format for Right Justified Data



17.7 Interrupts

The I²S controller generates a single interrupt, I2SINTR to the processor. This interrupt is a combination (logical OR) of all TX and RX internal interrupts.

The transmitter generates 2 internal interrupts within the I²S controller which reflect the status of the TX FIFO. These internal interrupts are as follows:

- TX FIFO empty.
- TX underflow.

The TX FIFO interrupt can have its interrupt level determined by I2STXCtrl[0]. If this bit = 1, then the FIFO empty interrupt will occur when the FIFO is empty. If this bit = 0, then the FIFO empty interrupt will occur when the FIFO is half empty.

These interrupts are combined and are maskable with the TX interrupt register enable bit, I2STXCtrl[1].

The FIFO Empty internal interrupts are cleared if the FIFOs are filled with data or the corresponding channel is disabled.

The TX underflow internal interrupt is cleared by writing to both the left and right data registers the TX channel. This interrupt will also be cleared if the corresponding channel is disabled.

The I²S receiver generates 2 internal interrupts within the I²S controller which reflect the status of the RX FIFO. These internal interrupts are as follows:

- RX FIFO full.
- RX overflow.

These can have their interrupt level determined by I2SRXCtrl[0]. If this bit = 1, then the FIFO full interrupt will occur when the FIFO is full. If this bit = 0, then the FIFO full interrupt will occur when the FIFO is half full.

All four are combined and are maskable with the RX interrupt register enable bit, I2SRXCtrl[1].

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The FIFO Full internal interrupts are cleared if the FIFOs become less than full or the corresponding channel is disabled.

The RX overflow internal interrupt is cleared by reading both the left and right data registers the RX channel. This interrupt will also be cleared if the corresponding channel is disabled.

The RX and TX global interrupts are combined to form the I2S controller Interrupt, I2SINTR.

The following table summarizes which FIFO flags will generate interrupts when set. For example a transmitter FIFO empty flag will result in an interrupt but for a receiver FIFO empty flag a status bit only is set.

The sticky bits refer to bits I2SGlSts[11:6]. A write of zero is required to clear the setting of these bits.

Table 17-5: FIFO Flags

FIFO Flag	Transmitter	Receiver
FIFO empty	Interrupt and status bit	Status bit.
FIFO full	Status	Interrupt and status bit
FIFO overflow	Sticky bit	Interrupt and status bit
FIFO underflow	Interrupt and status bit	Sticky bit

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17.8 Registers

17.8.1 I²S TX Registers

The following table summarizes the register set in the Transmitter. Each of the registers listed are addressable. The left and right data registers can be accessed by both APB and DMA accesses. The remaining registers are concerned with control / status information and can be only accessed through the APB bus.

Table 17-6: I²S TX Registers

Address	Type	Width	Reset Value	Name	Description
0x8082_0010	R/W	32	0x0	I2STX0Lft	Left Transmit data register for channel 0
0x8082_0014	R/W	32	0x0	I2STX0Rt	Right Transmit data register for channel 0
0x8082_0018	-	-	-	-	Reserved
0x8082_001C	-	-	-	-	Reserved
0x8082_0020	-	-	-	-	Reserved
0x8082_0024	-	-	-	-	Reserved
0x8082_0028	R/W	3	0x0	I2STXLinCtrlData	Line Control data register
0x8082_002C	R/W	2	0x0	I2STXCtrl	Control register
0x8082_0030	R/W	2	0x0	I2STXWrdLen	Word Length
0x8082_0034	R/W	1	0x0	I2STX0En	TX0 Channel Enable
0x8082_0038	-	-	-	-	Reserved
0x8082_003C	-	-	-	-	Reserved

I²S TX Register Descriptions

I2STXLft

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
i2s_tx_left															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
i2s_tx_left															

Address:

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0x8082_0010 - Read/Write

Default:

0x0000_0000

Definition:

Transmit left data word.

Bit Descriptions:

i2s_tx_left: Transmit left data word.

I2STXRt

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
i2s_tx_right															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
i2s_tx_right															

Address:

0x8082_0014 - Read/Write

Default:

0x0000_0000

Definition:

Transmit right data word.

Bit Descriptions:

i2s_tx_right: Transmit right data word.

I2STXLinCtrlData

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												Left_Right_Justify	TXUF_REPEAT_SAMPLE		TXDIR

Address:

0x8082_0028 - Read/Write

Default:

0x0000_0000

Definition:

Line Control Data Register

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Bit Descriptions:

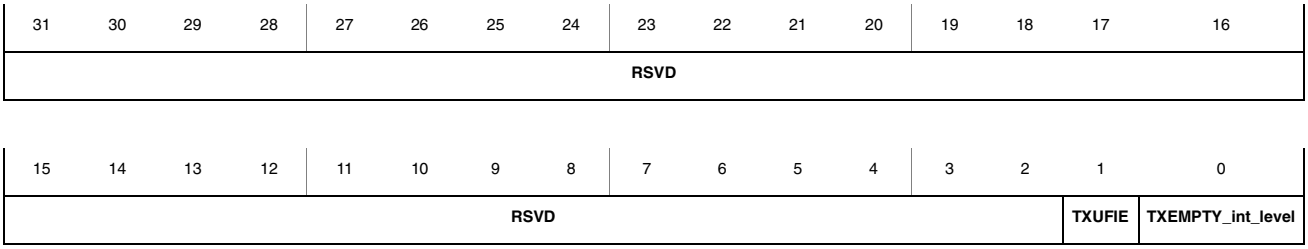
RSVD: Reserved. Unknown During Read.

Left_Right_Justify: Determines how the data word is justified when being transmitted on the sdo line output.
0 - left justified.
1 - right justified

TXUF_REPEAT_SAMPLE:On TX underflow, the I²S controller transmits all zeros if this bit is “1”.
If this bit is “0” the I²S controller repeats the last sample on underflow.

TXDIR: Transmit data shift direction.
0 - MSB first
1 - LSB first

I2STXCtrl



Address:
0x8082_002C - Read/Write

Default:
0x0000_0000

Definition:
Transmit Control Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TXUFIE: Transmit interrupt enable. Active high

TXEMPTY_int_level:Transmit empty interrupt level select.
0 - Generate interrupt when FIFO is half empty.
1 - Generate interrupt when FIFO is empty.

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I2STXWrdLen

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														WL	

Address:

0x8082_0030 - Read/Write

Default:

0x0000_0000

Definition:

Transmit Word Length

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

WL: Transmit Word Length.
00 - 16 bit mode
01 - 24 bit mode
10 - 32 bit mode

I2STXEn

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															i2s_tx_EN

Address:

0x8082_0034 - Read/Write

Default:

0x0000_0000

Definition:

TX Channel Enable

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

i2s_tx_EN: TX Channel Enable

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17.8.2 I²S RX Registers

The following table summarizes the register set in the I²S Receiver block. Each of the registers listed are addressable. The left and right data registers can be accessed by both APB and DMA accesses. The remaining registers are concerned with control/status information and can be only accessed through the APB bus.

Table 17-7: I²S RX Registers

Address	Type	Width	Reset Value	Name	Description
0x8082_0040	R	32	0x0	I2SRXLft	Left Receive data register
0x8082_0044	R	32	0x0	I2SRXRt	Right Receive data register
0x8082_0048	-	-	-	-	Reserved
0x8082_004C	-	-	-	-	Reserved
0x8082_0050	-	-	-	-	Reserved
0x8082_0054	-	-	-	-	Reserved
0x8082_0058	R/W	2	0x0	I2SRXLinCtrlData	Line Control data register
0x8082_005C	R/W	2	0x0	I2SRXCtrl	Control register
0x8082_0060	R/W	2	0x0	I2SRXWrdLen	Word Length
0x8082_0064	R/W	1	0x0	I2SRXEn	RX Channel Enable
0x8082_0068	-	-	-	-	Reserved
0x8082_006C	-	-	-	-	Reserved

I²S RX Register Descriptions

I2SRXLft

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
i2s_rx_left															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
i2s_rx_left															

Address:

0x8082_0040 - Read Only

Default:

0x0000_0000

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Definition:

Receive left data word.

Bit Descriptions:

i2s_rx_left: Receive left data word.

I2SRXRt

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
i2s_rx_right															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
i2s_rx_right															

Address:

0x8082_0044 - Read Only

Default:

0x0000_0000

Definition:

Receive right data word.

Bit Descriptions:

i2s_rx_right: Receive right data word.

I2SRXLinCtrlData

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														Left_Right_Justify	RXDIR

Address:

0x8082_0058 - Read/Write

Default:

0x0000_0000

Definition:

Receive Line Control Data Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read. Must be written as “0”.

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Left_Right_Justify: Receiver Data word Justification when being received on the SDI line input.
0 - Left justification.
1 - Right justification.

RXDIR: Receive data shift direction.
0 - MSB first
1 - LSB first

I2SRXCtrl

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														ROFLIE	RXFull_int_level

Address:
0x8082_005C - Read/Write

Default:
0x0000_0000

Definition:
Control Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read. Must be written as “0”.

ROFLIE: Receive interrupt enable.
Active high

RXFull_int_level: Rx full interrupt level select.
0 - Generate interrupt when FIFO is half full.
1 - Generate interrupt when FIFO is full.

I2SRXWrdLen

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														WL	

Address:
0x8082_0060 - Read/Write

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Default:

0x0000_0000

Definition:

Word Length

Bit Descriptions:

RSVD:	Reserved. Unknown During Read. Must be written as “0”.
WL:	Receive Word Length. 00 - 16 bit mode 01 - 24 bit mode 10 - 32 bit mode

I2SRXEn

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															i2s_rx0_EN

Address:

0x8082_0064 - Read/Write

Default:

0x0000_0000

Definition:

RX Channel Enable

Bit Descriptions:

RSVD:	Reserved. Unknown During Read. Must be written as “0”.
i2s_rx_EN:	RX Channel Enable

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17.8.3 I²S Configuration and Status Registers

Table 17-8: I²S Configuration and Status Registers

Address	Type	Width	Reset Value	Name	Description
0x8082_0000	R/W	7	0x0	I2STXClkCfg	Transmitter clock configuration register.
0x8082_0004	R/W	7	0x0	I2SRXClkCfg	Receiver clock configuration register
0x8082_0008	R/W	20	0x12492	I2SGlSts	I²S Global Status register. This reflects the status of the RX FIFO and the TX FIFO.
0x8082_000C	R/W	2	0x0	I2SGlCtrl	I2S Global Control register.

I²S Configuration and Status Register Descriptions

I2STXClkCfg

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									i2s_tx_bcr		i2s_tx_nbcg	i2s_mstr	i2s_trel	i2s_tckp	i2s_tlrs

Address:

0x8082_0000 - Read/Write

Default

0x0000_0000

Definition:

Transmitter clock configuration register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

i2s_tx_bcr: Defines the TX bit clock rate.
00 - I2STXClkCfg[4] defines the bit clock generation.
01 - Bit clock rate is fixed at 32x. Word length is ignored.
10 - Bit clock rate is fixed at 64x. Word length is ignored.

11 - Bit clock rate is fixed at 128x. Word length is ignored.

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i2s_tx_nbcg: Defines TX not bit clock gating mode.

If I2STXClkCfg[5:6] = 00, this bit defines the bit clock rate, otherwise ignored.

Bit clock rate = 32x if word length is 16.
Bit clock rate = 64x if word length is 32.
Bit clock rate = 64x if word length is 24.

There is a special case when the word length is 24.
If this bit = 0 and the word length is 24, the last 8 cycles are gated off in each word.
If this bit = 1 and the word length is 24, the last 8 cycles are not gated off in each word.

i2s_mstr: Defines if the TX Audio clocks are slave or master.
0 - slave mode.
1 - master mode.

i2s_trel: Determines the timing of the lrckt with respect to the sdox data outputs.

0 - Transition of lrckt occurs together with the first data bit.
1 - Transition of lrckr occurs one bitclk cycle before the first sdox data bit. This is I2S format.

i2s_tckp: Defines polarity of the TX bitclk.

1 - Positive clock polarity. The lrckt and sdox lines change synchronously with the positive edge of the bitclk and are considered valid during negative transitions.
0 - Negative clock polarity. The lrckt and sdox lines change synchronously with the negative edge of the bitclk and are considered valid during positive transitions.

i2s_tlrs: Defines the polarity of lrckt.

0 - if lrckt is low, then it's the left word, if lrckt is high, then it's the right word.
1 - if lrckt is low, then it's the right word, if lrckt is high, then it's the left word.

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I2SRXClkCfg

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									i2s_rx_bcr		i2s_rx_nbcg	i2s_mstr	i2s_rrel	i2s_rckp	i2s_rlrs

Address:

0x8082_0004 - Read/Write

Default:

0x0000_0000

Definition:

Receiver clock configuration register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

i2s_rx_bcr: RX bit clock rate.
00 - I2SRXClkCfg[4] defines the bit clock generation.
01 - Bit clock rate is fixed at 32x. Word length is ignored.
10 - Bit clock rate is fixed at 64x. Word length is ignored.
11 - Bit clock rate is fixed at 128x. Word length is ignored.

i2s_rx_nbcg: Defines RX not bit clock gating mode.

If I2SRXClkCfg[5:6] = 00, this bit defines the bit clock rate, otherwise ignored.

Bit clock rate = 32x if word length is 16.
Bit clock rate = 64x if word length is 32.
Bit clock rate = 64x if word length is 24.

There is a special case when the word length is 24.
If this bit = 0 and the word length is 24, the last 8 cycles are gated off in each word.
If this bit = 1 and the word length is 24, the last 8 cycles are not gated off in each word.

i2s_mstr: Defines if the RX Audio clocks are slave or master.
0 - slave mode.
1 - master mode.

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i2s_rrel: Determines the timing of the lrckr with respect to the sdix data inputs.
0 - Transition of lrckr occurs together with the first data bit.
1 - Transition of lrckr occurs one bitclk cycle before the first sdix data bit.

i2s_rckp: Defines polarity of the RX bitclk.
1 - Positive clock polarity. The lrckr and sdix lines change synchronously with the positive edge of the bitclk and are considered valid during negative transitions.
0 - Negative clock polarity. The lrckr and sdix lines change synchronously with the negative edge of the bitclk and are considered valid during positive transitions.

i2s_rlrs: Defines the polarity or Lrckr.
0 - if lrckr is low then it's the left word, if lrckr is high then it's the right word.
1 - if lrckr is low then it's the right word, if lrckr is high then it's the left word.

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17.8.4 I²S Global Status Registers

I²S Global Status Registers

I2SGISts

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD														rx_fifo_half_full	rx_fifo_empty

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
rx_fifo_full	tx_fifo_half_empty	tx_fifo_empty	tx_fifo_full	RSVD		Rx_underflow	RSVD		Tx_overflow	RSVD		Rx_overflow	RSVD		Tx_underflow

Address:
0x8082_0008 - Read/Write

Default:
0x0001_2492

Definition:
UART Data Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

Tx_underflow: when = 1, TX FIFO has underflowed.

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Rx_overflow: when = 1, RX FIFO has overflowed and the FIFO pointer is currently pointing at the last data received before the overflow occurred.

Tx_overflow: when = 1, the TX FIFO is full and an attempt has been made to write data to it by the APB or DMA. This bit is cleared by writing a 0 to it.

Rx_underflow: when = 1, the RX FIFO is empty and an attempt has been made to read data from it by the APB or DMA. This bit is cleared by writing a 0 to it.

tx_fifo_full: when = 1, FIFO is full, otherwise not full

tx_fifo_empty: when = 1, FIFO is empty, otherwise not empty

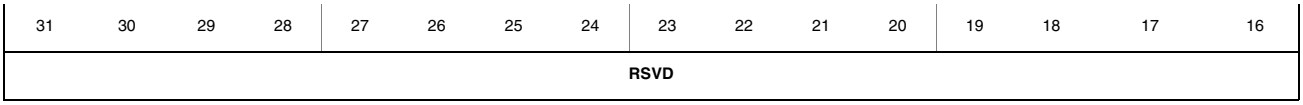
tx_fifo_half_empty: when = 1, FIFO is half empty, otherwise less than half empty

rx_fifo_full: when = 1, FIFO is full, otherwise not full

rx_fifo_empty: when = 1, FIFO is empty, otherwise not empty

rx_fifo_half_full: when = 1, FIFO is half full, otherwise less than half full

I2SGICtrl



Address:

0x8082_000C - Read/Write

Default:

0x0000_0000

Definition:

I2S Global Control Register

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

i2s_ife: Defines if I2S controller is enabled and PCLK is turned on for the I2S controller.
0 - PCLK is off.
1 - PCLK is on.

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i2s_loopback: Defines loopback operation.
0 - not in loopback mode
1 - Loopback mode selected.

The I²S global register deals with enabling the block and whether loopback mode is used. The I²S enable bit determines whether the PCLK is turned on for the I²S. All registers except for the data registers can be written without the I²S PCLK enabled. The ARM provides its own clock cycles when writing to any of the control status registers.

When the I²S controller is required to transmit or receive data, PCLK must be turned on via this register.

The I²S controller loopback mode bit determines if the TX channel is connected to the RX channel. This will allow data be sent in a loop fashion from the transmitter back through the receiver. When loopback is active, data at the receiver input is ignored and transmit data is sent out normally. The transmit section will control the clock configuration during loopback the same as if full-duplex operation was used.

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Chapter 18

AC'97 Controller

18.1 Introduction

The AC'97 Controller includes a 5-pin serial interface to an external audio codec. The AC-Link is a bi-directional, fixed rate, serial PCM (Pulse Code Modulation) digital stream, dividing each audio frame into 12 outgoing and 12 incoming data streams (slots), each with 20-bit sample resolution.

The AC'97 Controller contains logic that controls the AC-Link to the audio codec and an interface to the AMBA APB.

The main features of the AC'97 are:

- Serial-to-parallel conversion on data received from the external codec.
- Parallel-to-serial conversion on data transmitted to the external codec.
- Reception / Transmission of control and status information.
- The transmit and receive paths are buffered with internal FIFO memories allowing data to be stored independently in both transmit and receive modes. The data for the FIFO can be written via either the APB interface or DMA.

Signal Name	Input/Output	Description
SDATAIN	Input	Serial input data stream from the audio codec. It contains status information and digital audio input streams.
BITCLK	Input	Clock from serial codec. Fixed at 12.233 MHz.
SDATAOUT	Output	This serial output transmits the control information and digital audio output streams to the audio codec.
SYNC	Output	Synchronization signal to the external codec. Fixed at 48 kHz. It is also output asynchronously when the audio codec is in warm reset state.
RESET	Output	Asynchronous cold reset (active low, resets codec registers).

The AC'97 pins are multiplexed and may be used for the I^2S controller instead of AC'97 by setting DeviceCfg.I2SonAC97.

The controller consists of a transmit FIFO, a receive FIFO and their associated control logic. The control logic can be configured to allow the FIFO to accept any data to or from any slot in a frame.

The receive channel is controlled via its AC97RXCR register. This register controls the following:

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- Which slot data from the received frame is to be stored in the FIFO. The controller will not store any other slots than those specified in these registers. The user must ensure that all slot data stored in the FIFO is at the same sampling rate.
- The length of time before a timeout interrupt is generated.
- Whether the FIFO is enabled or not.
- The number of bits in the slot that is captured.
- Whether the channel is enabled to receive data or not.

The transmit channel is controlled via its AC97TXCR register. This register controls the following:

- Which slot the data in the FIFO is to be transmitted in, the user must ensure that all the data in the FIFO is intended for slots with the same sampling rate. The data must be supplied lowest slot number first.
- Whether the FIFO is enabled or not.
- The number of bits that need to be appended to the data from the CPU to make the word 20 bits.
- Whether the channel is enabled to transmit data or not.
- The transmit channel also supports variable sample rates via the Data Request Disable Slots from the external codec in slot 1.

Slot 0 for transmission is determined by the controller depending on the values in the AC97TXCR register, the data request bits, and the FIFO having valid data to send. If a slot does not have any data for transmission, the controller will fill the slot with zeros and set the Tag bits as invalid.

If the external codec does not support the Data Request Disable bits/Variable Rate Extension the bits will always be "0" meaning a sample rate of 48 kHz. As slots 1 and 2 are always transmitted at 48 kHz, the external codec does not have Data Request Disable bits for these slots. Data for transmission on slots 1, 2, and 12 can be obtained from either the channels or the registers SLOT1RXTX, AC97S2Data and AC97S12Data. If data for the slots is present in both sources the controller will default to sending the data in the channel first. However this dual source mode of operation is not supported. The user must ensure that the slot data only comes from one source.

If the slot enable bits are set when receiving the data for slots 1, 2, and 12, the data is stored in the channel and not the SLOT1/2/12RX registers. If the slot enable bits are not set, then the data will always go to the registers.

The user should only use the channels to transmit slot 1 and 2 data when they are setting the external codec up for operation. Once the set up of the external codec is complete, the data for slot 1 and 2 should come via the SLOT1/2TX registers. This action frees up the channel.

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18.2 Interrupts

The AC'97 Controller generates individual maskable active HIGH interrupts. Each interrupt may be enabled or disabled using the appropriate enable bit. Setting the bit HIGH enables the corresponding interrupt. This allows for a system interrupt controller to provide the mask registers for each interrupt.

The status of the individual interrupt sources can be read from appropriate register. The interrupts are ORed to create one interrupt (**AC97INTR**) for the AC'97 controller block

18.2.1 Channel Interrupts

The individual interrupts that are generated by the transmit/receive channel are described below. The status of the interrupts can be read from the AC97RISR or AC97ISR registers, and is masked in the AC97IE register.

18.2.1.1 RIS

If the receive FIFO is enabled and the mask bit RIE is set, the FIFO receive interrupt is asserted when the AC'97 Controller receive FIFO is greater than or equal to half full. The receive interrupt is cleared when the FIFO becomes less than half full.

If the receive FIFO is disabled, it has a depth of one location. Any data received will fill that one location, causing the receive interrupt to be asserted high. The receive interrupt is cleared by performing a single read of the receive FIFO.

18.2.1.2 TIS

If the transmit FIFO is enabled and the mask bit TIE is set, the FIFO transmit interrupt is asserted when the AC'97 Controller transmit FIFO is at least half-empty. The FIFO transmit interrupt is cleared by filling the transmit FIFO more than half full.

If the transmit FIFO is disabled (has a depth of one location) and there is no data present in the transmitters single location, the transmit interrupt is asserted high. The transmit interrupt is cleared by performing a single write to the transmit FIFO.

18.2.1.3 RTIS

The receive timeout interrupt is asserted when the receive FIFO is not empty and no further data is received over a number of frames. This number is set by the TOC value in the AC97RXCR register. The receive timeout interrupt is cleared when the FIFO becomes empty through reading all the data.

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18.2.1.4 TCIS

The transmit complete interrupt is asserted when the transmit FIFO is empty and the parallel to serial shifter is empty. This indicates that there is no data left in the FIFO to be sent.

18.2.2 Global Interrupts

The individual interrupts that are global for the AC97 controller are described below. The status of these interrupts can be read from the AC97GIS or AC97RGIS registers, and are masked in the AC97IM register.

18.2.2.1 CODECREADY

The Codec Ready Interrupt is asserted when the codec has indicated that it is ready by setting bit15 of Slot0.

This interrupt is cleared by writing a "1" to the appropriate bit of the AC97EOI register.

18.2.2.2 WINT

The Wakeup interrupt is asserted when a wake-up event will trigger the assertion of **SDATAIN** while the AC-Link is powered down. The wake-up is caused by the external codec's GPIO pins, which have been configured to generate a wake-up event via the codec's GPIO pin Wakeup Control register (0x52). An AC-Link wake-up interrupt is defined as a 0-to-1 transition on SDATAIN when the AC-Link is powered down. The controller knows when the external codec has been powered down as the SLOT1/2TX registers are monitored to check for this condition. When the wake up event has been detected on the **SDATAIN** line, an interrupt is generated to allow the processor to reactivate the link with either a warm or cold reset.

This interrupt is cleared by writing a "1" to the appropriate bit of the AC97EOI register.

18.2.2.3 GPIOINT

The receive GPIOINT interrupt is asserted when bit 0 in slot 12 of the incoming SDATAIN is "1". This bit indicates that one or more of the bits in slot 12 have changed since the last frame. It is up to the interrupt service routine to read the AC97S12Data register in order to clear this interrupt. The external codec register 0x54 GPIO pin Status reflects the state of all the GPIO pins.

18.2.2.4 GPIOTXCOMPLETE

The transmit GPIOTXCOMPLETE interrupt is asserted when all values written to the AC97S12Data have been transmitted. It is cleared when any data is written to the AC97S12Data.

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18.2.2.5 SLOT2INT

The receive SLOT2INT interrupt is asserted when the AC97S2Data register has new data that has not been read. By reading the data in the AC97S2Data register the SLOT2INT interrupt is cleared.

18.2.2.6 SLOT1TXCOMPLETE

The transmit **SLOT1TXCOMPLETE** interrupt is asserted when all values written to the AC97S1Data have been transmitted. It is cleared when any data is written to the AC97S1Data.

18.2.2.7 SLOT2TXCOMPLETE

The transmit **SLOT2TXCOMPLETE** interrupt is asserted when all values written to the AC97S2Data have been transmitted. It is cleared when any data is written to the AC97S2Data.

18.3 System Loopback Testing

A loopback test mode is available for system testing so that data transmitted on **ASDO** can also be received on **ASDI**. Loopback mode is entered when a "1" is written to the LOOP bit in AC97GCR register. For normal operation the LOOP bit must always be "0", which is also the default state at reset.

Note: For this test mode to work, an external bit clock will need to be supplied.

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18.4 Registers

Table 18-1: Register Memory Map

Address	Type	Name	Description
0x8088_0000	Read/Write	AC97DR	Data read or written from/to FIFO
0x8088_0004	Read/Write	AC97RXCR	Control register for receive
0x8088_0008	Read/Write	AC97TXCR	Control register for transmit
0x8088_000C	Read	AC97SR	Status register
0x8088_0010	Read	AC97RISR	Raw interrupt status register
0x8088_0014	Read	AC97ISR	Interrupt Status
0x8088_0018	Read/Write	AC97IE	Interrupt Enable
0x8088_001C	-	-	Reserved
0x8088_0080	Read/Write	AC97S1Data	Data received/transmitted on SLOT1
0x8088_0084	Read/Write	AC97S2Data	Data received/transmitted on SLOT2
0x8088_0088	Read/Write	AC97S12Data	Data received/transmitted on SLOT12
0x8088_008C	Read/Write	AC97RGIS	Raw Global interrupt status register
0x8088_0090	Read	AC97GIS	Global interrupt status register
0x8088_0094	Read/Write	AC97IM	Interrupt mask register
0x8088_0098	Write	AC97EOI	End Of Interrupt register
0x8088_009C	Read/Write	AC97GCR	Main Control register
0x8088_00A0	Read/Write	AC97Reset	RESET control register.
0x8088_00A4	Read/Write	AC97SYNC	SYNC control register.
0x8088_00A8	Read	AC97GCIS	Global channel FIFO interrupt status register.

Register Descriptions

AC97DR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD / DATA (See Definition, below.)												DATA			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															

Address:

AC97DR - 0x8088_0000 - Read/Write

Definition:

The AC97DR register is a read / write data register that is normally 20 bits wide. In 16-bit compact mode, all 32 available bits are used. This register is zero at reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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DATA: Write - Transmit FIFO: The AC97TXCR register qualifies the data within the TX FIFO.
Read - Receive FIFO: The AC97RXCR register qualifies the data within the FIFO.

For words to be transmitted:

- If the FIFO is enabled, data written to this location is pushed onto the transmit FIFO.
- If the FIFO is not enabled, data is stored in the transmitter holding register (the bottom word of the transmit FIFO).

For received words:

- If the FIFO is enabled, the data received is pushed onto the receive FIFO.
- If the FIFO is not enabled, the data received is stored in the receiving holding register (the bottom word of the receive FIFO).

The receive FIFO is 21 bits wide. The 21st bit, the receive overrun error status, can only be read via the AC97ISR registers. The receive overrun error status bit is transferred down to the FIFO buffer along with the overrun data value.

AC97RXCR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD				TOC											FDIS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CM	RSIZE		RX12	RX11	RX10	RX9	RX8	RX7	RX6	RX5	RX4	RX3	RX2	RX1	REN

Address:

AC97RXCR - 0x8088_0004 - Read/Write

Definition:

Receive Control Register. The AC97RXCR register is a 32-bit read/write register. The data contained within the register controls the data slots that are contained within the receive FIFO. The data contained within the RSIZE bits controls the number of zeros that are to be appended to data for a slot to make it 20 bits.

The data from the receive channel is stored in the lowest slot first. If for example the receive FIFO is setup to store slots 3 and 4 then the first data word out of the FIFO will be slot 3 followed by slot 4.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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TOC: Time out count value. The FIFO have the capability of generating a timeout interrupt when the receive FIFO is not empty and no further data is received for a period of time. This time period is specified by the value written here. The value is the number of frames that must occur without any data being received (a count of the SYNC signal). A write of "0" to this value disables the counter, and no timeout interrupt is generated. On reset the value is "0". The maximum count of 4096 will allow the timeout period to be set to 85 msec.

FDIS: FIFO Disable
0 - The FIFO buffer is Enabled (FIFO mode).
1 - The FIFO is disabled (character mode). That is, the FIFO becomes 1-byte-deep holding registers.

CM: Compact mode enable. If the RSIZE value is either "00" or "11" (setting the data word size to 12- or 16-bits) then the CM bit determines whether the two data words are compacted into one 32-bit word, or each is sent in a separate word. If the RSIZE value is either "01" or "10" (setting the data word size to 18- or 20-bits) then the CM bit has no effect. See Table 18-2.
0 - The data is justified into separate 32 bit words
1 - The two data words are compacted into one 32-bit word for reading by the CPU.

RSIZE: Determines how many bits to a data word. See Table 18-2 for details of the interaction between RSIZE and CM.
00 data is 16 bits
01 data is 18 bits
10 data is 20 bits
11 data is 12 bits

Table 18-2: Interaction Between RSIZE and CM

CM	RSIZE		Data to CPU
0	0	0	Justified, one 16 bits
0	1	1	Justified, one 12 bits
1	0	0	Compacted, two 16 bits
1	1	1	Compacted, two 12 bits
X	1	0	Justified, 20 bit
X	0	1	Justified, 18 bit

RX12: FIFO stores SLOT12 data (takes precedence over AC97S12Data)

RX11: FIFO stores SLOT11 data

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RX10: FIFO stores SLOT10 data

RX9: FIFO stores SLOT9 data

RX8: FIFO stores SLOT8 data

RX7: FIFO stores SLOT7 data

RX6: FIFO stores SLOT6 data

RX5: FIFO stores SLOT5 data

RX4: FIFO stores SLOT4 data

RX3: FIFO stores SLOT3 data

RX2: FIFO stores SLOT2 data

RX1: FIFO stores SLOT1 data

REN: A "1" written to this bit enables the receive for this FIFO and enables the PCLK for the respective channel.

AC97TXCR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															FDIS

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CM	TSIZE		TX12	TX11	TX10	TX9	TX8	TX7	TX6	TX5	TX4	TX3	TX2	TX1	TEN

Address:

AC97TXCR - 0x8088_0008 - Read/Write

Definition:

Transmit Control Register. The AC97TXCR register is read/write. The data contained within the register controls the data slots that are contained within the FIFO's transmit register. The data within this FIFO must be of the same sampling frequency, such as all audio slot data at 44.1 kHz. This register is used to create slot 0 for transmitting. If this register specifies that the data within is for Slot1 and 2 this will take precedence over the data in the SLOT1TX and SLOT2TX register.

The data contained within the TSIZE bits controls the number of zeros that are to be appended to data for a slot to make it 20 bits.

The data into the FIFO is stored in the lowest slot first. For example if the FIFO is set up to store in slots 3 and 4, then slot 3 is the first data into the FIFO and slot 4 the second.

Bit Descriptions:

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RSVD: Reserved. Unknown During Read.

FDIS: FIFO Disable
0 - The FIFO buffer is Enabled (FIFO mode).
1 - The FIFO is disabled (character mode). That is, the FIFO becomes 1-byte-deep holding registers.

CM: Compact mode enable. If the RSIZE value is either "00" or "11" (setting the data word size to 12- or 16-bits) then the CM bit determines whether the two data words are compacted into one 32-bit word, or each is sent in a separate word. If the RSIZE value is either "01" or "10" (setting the data word size to 18- or 20-bits) then the CM bit has no effect. See Table 18-3.
0 - The data is justified into one 32 bit word
1 - The two data words are compacted into one 32-bit word for reading by the CPU.

RSIZE: Determines how many bits to a data word. See Table 18-3 for details of the interaction between RSIZE and CM.
00 data is 16 bits
01 data is 18 bits
10 data is 20 bits
11 data is 12 bits

Table 18-3: Interaction Between RSIZE and CM Bits

CM	RSIZE		Data to CPU
0	0	0	Justified, one 16 bits
0	1	1	Justified, one 12 bits
1	0	0	Compacted, two 16 bits
1	1	1	Compacted, two 12 bits
X	1	0	Justified, 20 bit
X	0	1	Justified, 18 bit

TX12: FIFO stores SLOT12 data (takes precedence over AC97S12Data)

TX11: FIFO stores SLOT11 data

TX10: FIFO stores SLOT10 data

TX9: FIFO stores SLOT9 data

TX8: FIFO stores SLOT8 data

TX7: FIFO stores SLOT7 data

TX6: FIFO stores SLOT6 data

TX5: FIFO stores SLOT5 data

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TX4: FIFO stores SLOT4 data

TX3: FIFO stores SLOT3 data

TX2: FIFO contains SLOT2 data (only use if sampling rate is 48 kHz). Takes precedence over AC97S2Data.

TX1: FIFO contains SLOT1 data (only use if sampling rate is 48 kHz). Takes precedence over AC97S1DATA.

TEN: A "1" written to this bit enables the transmit for this FIFO and enables the PCLK for the respective Channel.

AC97SR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									TXUE	RXOE	TXBUSY	TXFF	RXFF	TXFE	RXFE

Address:

AC97SR - 0x8088_000C - Read Only

Definition:

Status Register. The AC'97 Controller status register is a read only register that gives information about the transmit/receive status of the block. After reset, the TXFF, RXFF and TXBUSY are "0", and TXFE and RXFE are "1".

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

TXUE: TX Underrun Error - This bit is set to "1" if an underrun error has been detected, that is, if data is to be transmitted and the FIFO is empty.

This bit is cleared to "0" by writing to the AC97DR register.

Note: Bit will only be set if FIFO had been written to at least once in current data transfer.

RXOE: RX Overrun Error - This bit is set to "1" if an overrun error has been detected. This bit is set to "1" if data is received and the FIFO is already full.

This bit is cleared to "0" by reading the AC97DR register.

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TXBUSY: TXBUSY is set when TEN = "1" AND there is data in the FIFO, OR when data from this FIFO is being sent in the current frame.

TXBUSY is cleared at the start of the next frame following the assertion of the corresponding channels FIFO-empty-flag (the value of TEN is irrelevant).

TXFF: Transmit FIFO full flag, active HIGH.
This bit is asserted HIGH if the transmit FIFO is full.

RXFF: Receive FIFO full flag, active HIGH.
This bit is asserted HIGH if the receive FIFO is full.

TXFE: Transmit FIFO empty flag, active HIGH.
This bit is asserted HIGH if the transmit FIFO is empty.

RXFE: Receive FIFO empty flag, active HIGH.
This bit is asserted HIGH if the receive FIFO is empty.

AC97RISR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												RIS	TIS	RTIS	TCIS

Address:

AC97RISR - 0x8088_0010 - Read Only

Definition:

Raw Interrupt Status. The AC97ISR register is the raw Interrupt status register for the controller FIFO. All bits are cleared to zero on reset except for the TCIS as the FIFO and shift register should both be empty. Any write to this register clears the overrun error.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RIS: RX Interrupt Status - This bit is set to "1" if the receive FIFO becomes half full.

TIS: TX Interrupt Status - This bit is set to "1" if the transmit FIFO becomes half empty.

RTIS: RX Timeout Interrupt Status - If this bit is set to "1", the timeout FIFO interrupt is asserted.

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TCIS: TX complete Interrupt Status - If this bit is set to "1", the transmit FIFO complete interrupt is asserted.

AC97ISR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												RIS	TIS	RTIS	TCIS

Address:

AC97ISR - 0x8088_0014 - Read Only

Definition:

Interrupt Status Register. The AC97ISR register is the Interrupt status register for the controller FIFO. All bits are cleared to zero on reset except for the TCIS as the FIFO and shift register should both be empty.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RIS: RX Interrupt Status - If this bit is set to "1", the receive FIFO interrupt is asserted.

TIS: TX Interrupt Status - If this bit is set to "1", the transmit FIFO interrupt is asserted.

RTIS: RX Timeout Interrupt Status - If this bit is set to "1", the timeout FIFO interrupt is asserted.

TCIS: TX complete Interrupt Status - If this bit is set to "1", the transmit FIFO complete interrupt is asserted.

AC97IE

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												RIE	TIE	RTIE	TCIE

Address:

AC97IE - 0x8088_0018 - Read/Write

Definition:

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Interrupt Enable Register. The AC97IE register controls the Interrupt Enables for the FIFOs within the controller. All bits are cleared on reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

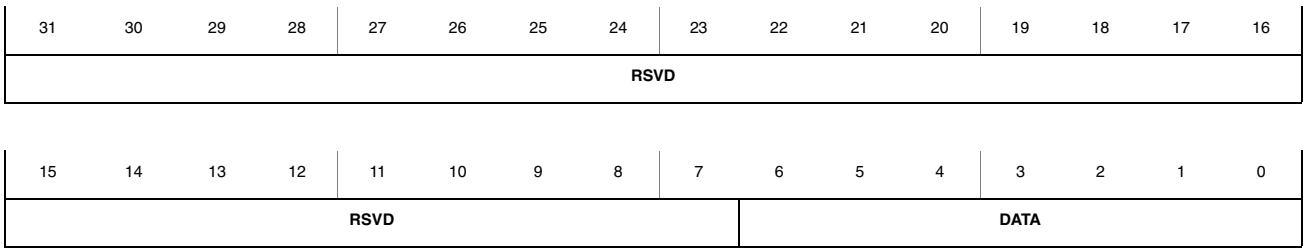
RIE: Receive Interrupt Enable - If this bit is set to "1", the FIFO receive interrupt is enabled.

TIE: Transmit Interrupt Enable - If this bit is set to "1", the FIFO transmit interrupt is enabled.

RTIE: Receive Timeout Interrupt Enable - If this bit is set to "1", the FIFO receive timeout interrupt is enabled.

TCIE: Transmit Complete Interrupt Enable - If this bit is set to "1", the FIFO transmit complete interrupt is enabled.

AC97S1Data



Address:

0x8088_0080 - Read/Write

Definition:

Slot 1 Data Register. The AC97S1Data register is a read / write register. When a write has occurred to this register, the data contained within it is sent on the next available frame in SLOT1. As both the AC97S1Data and AC97S2Data data are required for writes to the external codec, the AC97S2Data data will only become valid for transmission when the AC97S1Data has been written also. In order to perform a write to the external codec, the AC97S1Data register must be written to after the AC97S2Data register is written.

Bit[19] of Slot1 on SDATAOUT from the AC'97 indicates whether a read or a write is being performed to or from the external codec. This bit is generated automatically in the AC'97 as follows:

- When data is written to the AC97S2Data register, the read / write bit is set to "0", that is, a write operation.
- It is set to "1", that is, a read operation, when the slot 2 data has been transmitted.
- It is set to "1", that is, a read operation, when a read occurs from either the AC97S1Data or AC97S2Data register.

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If a power down is required, then the software must write the address 0x26 to this location (for the external device), which will be recorded by the controller. If the AC97S2Data bit 12 is set, then the controller will go into power down mode.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

DATA: Read operation: Read data value of the last value written to this register via the AC-Link interface. The data contained within it is the last valid received slot 1, for example, the slot 0 received tagged slot1 as valid.

Write operation: Write data value to transmit on slot1 on the next available frame. Once the data has been transmitted, it will be marked as invalid.

AC97S2Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															

Address:

0x8088_0084 - Read/Write

Definition:

Slot 2 Data Register. The AC97S2Data register is a read / write register. When a write has occurred to this register, the data contained within it will be sent on the next available frame in SLOT2. In order to perform a write to the external codec, the AC97S2Data register must be written to before the AC97S1Data register is written.

If a power down is required, then the software must write to SLOT1TX location address 0x26, which is recorded by the controller. If the AC97S2Data bit 12 is set, then the controller will go into power down mode.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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DATA: Read operation: Read data value of the last value written to this register via the AC-Link interface.

Write operation: Write data value to transmit on slot 2 on next available frame. Once the data has been transmitted, it will marked as invalid.

AC97S12Data

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD												DATA			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															

Address:

0x8088_0088 - Read/Write

Definition:

Slot 12 Data Register. The AC97S12Data register is a read / write register. Data written to it will be sent on the next available frame in SLOT 12. When this register is read, the data contained within it is the data that was last received for SLOT 12.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

DATA: Read operation: Read data value of the last value received in SLOT 12. Bit 0 is monitored to see if a GPIOINT has occurred.

Write operation: Write data value to transmit on slot 12 on next available frame. Once the data has been transmitted it will marked as invalid.

AC97RGIS

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									SLOT2TX COMPLETE	CODEC READY	WINT	GPIO INT	GPIOTX COMPLETE	SLOT2RX VALID	SLOT1TX COMPLETE

Address:

0x8088_008C - Read Only

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Definition:

Raw Global Interrupt Status Register. The AC'97 raw global interrupt status register is a read/write register that gives the status of various functions outside of the FIFO functionality within the controller.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

SLOT2TXCOMPLETE: Set when the AC97S2Data register has completed transmission. This bit is cleared when data is in the register to be transmitted.

CODECREADY: This bit is set to "1" during a wakeup when the codec indicates that it is ready by setting bit 15 of Slot0. It is cleared by writing to Bit1 of the AC97EOI Register.

WINT: RAW Wakeup Interrupt Status. If this bit is set to "1". The RAW Wakeup interrupt is asserted. This bit is cleared with a write to the AC97EOI register.

GPIOINT: The GPIOINT shows the raw status of the GPIOINT bit (slot 12 bit 0) in the receive frame, which is stored in the AC97S12Data register. This bit is cleared when the AC97S12Data register is read.

GPIOTXCOMPLETE: GPIO Transmission Complete. Set when a new value to the AC97S12Data register has completed transmission. Cleared when data is placed in the register to be transmitted.

SLOT2RXVALID: The AC97S2Data register has new data that has not been read. Reading the data in the AC97S2Data register clears this bit.

SLOT1TXCOMPLETE: Set when the AC97S1Data register has completed transmission. This bit is cleared when data is written to the AC97S1Data register to be transmitted.

AC97GIS

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									SLOT2TX COMPLETE	CODEC READY	WINT	GPIO INT	GPIOTX COMPLETE	SLOT2R XVALID	SLOT1TX COMPLETE

Address:

0x8088_0090 - Read Only

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Definition:

Global Interrupt Status. The AC97GIS register is the global interrupt status register. All bits are cleared to zero on reset. Each bit is the logical AND of the corresponding bits in the AC97RGIS register and the AC97IM register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

SLOT2TXCOMPLETE: If this bit is set to "1", the SLOT2TXCOMPLETE interrupt is asserted.

CODECREADY: This bit is set to "1" during a wakeup when the codec indicates that it is ready by setting bit 15 of Slot0

WINT: Wakeup Interrupt Status: If this bit is set to "1", the Wakeup Interrupt is asserted.

GPIOINT: GPIO Interrupt Status: If this bit is set to "1", the GPIOINT interrupt is asserted.

GPIOTXCOMPLETE: If this bit is set to "1", the GPIOTXCOMPLETE interrupt is asserted.

SLOT2RXVALID: If this bit is set to "1", SLOT2RXVALID interrupt is asserted.

SLOT1TXCOMPLETE: If this bit is set to "1", SLOT1TXCOMPLETE interrupt is asserted.

AC97IM

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									SLOT2TX COMPLETE	CODEC READY	WINT	GPIO INT	GPIOTX COMPLETE	SLOT2RX VALID	SLOT1TX COMPLETE

Address:

0x8088_0094 - Read/Write

Definition:

Controller Interrupt Enable Register. The AC'97 Controller interrupt enable register is a read/write register that controls the interrupt enables for the interrupts outside the FIFO channels. The table below shows the bit details of the register.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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SLOT2TXCOMPLETE: If this bit is set to "1", the SLOT2TXCOMPLETE interrupt is enabled.

CODECREADY: If this bit is set to "1", the Codec Ready Interrupt is enabled.

WINT: If this bit is set to "1", the Wakeup Interrupt is enabled.

GPIOINT: If this bit is set to "1", the GPIO interrupt is enabled.

GPIOTXCOMPLETE: If this bit is set to "1", the GPIOTXCOMPLETE interrupt is enabled.

SLOT2RXVALID: If this bit is set to "1", SLOT2RXVALID interrupt is enabled.

SLOT1TXCOMPLETE: If this bit is set to "1", SLOT1TXCOMPLETE interrupt is enabled.

AC97EOI

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														CODECREADY	WINT

Address:

0x8088_0098 - Write Only

Definition:

End Of Interrupt Register. The AC'97 End Of Interrupt Register is a write-only register that allows the CODECREADY and WIS interrupts to be cleared. A write to this location clears the interrupt.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

CODECREADY: CODECREADY Interrupt Status Clear. A write of "1" to this location will clear the CODECREADY interrupt bit.

WINT: Wakeup Interrupt Status Clear. A write of "1" to this location will clear the WIS interrupt bit.

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AC97GCR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													OCODECReady	LOOP	AC97IFE

Address:

0x8088_009C - Read/Write

Definition:

Global Control Register. The AC97GCR register is the main control register for the AC'97 Controller. All bits are cleared on reset.

The AC97IFE creates the clock enable signal for the clock controller block. It is used to enable/disable both PCLK and AC97LK.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

OCODECReady: If set to "1", this bit will override normal Codec-ready definition.

LOOP: Loopback mode: If this is set to "1", loopback test mode is enabled. Defaults to "0" when reset. Ensure this bit is always "0" for normal operation.

AC97IFE: AC97IF Enable: If this bit is set the AC'97 is enabled. Defaults to "0" on reset. When set to "0", all FIFO are reset to "0".

AC97Reset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													EFORCER	FORCED RESET	TIMED RESET

Address:

0x8088_00A0 - Read/Write

Definition:

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Controller Reset Register. The AC'97 Controller RESET register is a read/write register that controls various functions within the AC'97 Controller of the RESET port. All the register bits are cleared to "0" when reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

EFORCER: Enable for the Forced RESET bit.
1 - FORCEDRESET become active
0 - FORCEDRESET has no effect.

FORCEDRESET: If the EFORCER bit is set to "1", the RESET port will follow whatever value is written to this bit. If this mechanism is used to control the RESET port, it is up to software to ensure that the signal is high long enough to meet the specification of the external device.

This bit has priority over the TIMEDRESET bit.

TIMEDRESET: If this bit is set to "1", the RESET port is forced to "0" for five pulses of the 2.9491 MHz clock (0.339 µs x 5 = 1.695 µs maximum reset pulse and 1.356 µs minimum reset pulse using this 2.9491 MHz clock). After which this bit is zeroed.

AC97SYNC

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													EFORCES	FORCED SYNC	TIMED SYNC

Address:

0x8088_00A4 - Read/Write

Definition:

Sync Control Register. The AC'97 Sync Controller register is a read / write register that controls various functions within the AC'97 Controller of the SYNC port. All the register bits are cleared to "0" when reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

EFORCES: Enable for Forced SYNC bit
1 - FORCEDSYNC become active
0 - FORCEDSYNC has no effect.

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FORCEDSYNC: If EFORCES bit is set to "1", the SYNC port will follow whatever value is written to this bit. If this mechanism is used to control the SYNC port it is up to software to ensure that the signal is high long enough to meet the specification of the external device.

This bit has priority over the TIMEDSYNC bit.

TIMEDSYNC: If this bit is set to "1", the SYNC port is forced to "1" for five pulses of the 2.9491 MHz (0.339 µs x 5 = 1.695 µs maximum SYNC pulse and 1.356 µs minimum SYNC pulse using this clock). After which this bit is zeroed, allowing the SYNC to be controlled via the BITCLK counter.

AC97GCIS

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD												AC97GIS			

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												AC97ISR1			

Address:

0x8088_00A8 - Read Only

Definition:

Global Channel Interrupt Status. The AC97GCIS register (AC'97 Global Channel Interrupt Status) is read only, and echoes all the interrupt status registers in the controller. This register allows the software to read both the interrupt sources with one read.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

AC97GIS: Copy of the AC97GIS register

AC97ISR: Copy of the AC97ISR 1 register

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Chapter 19

Synchronous Serial Port

19.1 Introduction

The Synchronous Serial Port (SSP) is a master or slave interface for synchronous serial communication with slave peripheral devices that have either Motorola® SPI, National Semiconductor® Microwire®, or Texas Instruments® synchronous serial interfaces.

The SSP performs serial-to-parallel conversion on data received from a peripheral device. The CPU or DMA reads and writes data and control and status information. The transmit and receive paths are buffered with internal FIFO memories allowing up to eight 16-bit values to be stored independently in both transmit and receive modes. Serial data is transmitted on **SSPTXD** and received on **SSPRXD**.

19.2 Features

Following is a list of features of the Synchronous Serial Port.

- Master or Slave operation
- Programmable clock bit rate and prescaler
- Separate transmit and receive FIFO memory buffers, 16-bits wide, 8 locations deep
- Programmable data frame size from 4 to 16 bits
- Independent masking of transmit FIFO, receive FIFO and receive overrun interrupts

The SSP has a programmable choice of interfaces: SPI, Microwire, or TI synchronous serial. The features of each of these are listed below.

- SPI features:
  - Full duplex, four-wire synchronous transfers
  - Programmable clock polarity and phase
- The feature of the National Semiconductor Microwire interface is:
  - Half duplex transfer using 8-bit control message
- Texas Instrument synchronous serial interface features:
  - Full duplex four-wire synchronous transfer

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- Transmit data pin can be in high impedance state when not transmitting

19.3 SSP Functionality

The SSP includes a programmable bit rate clock divider and prescaler to generate the serial output clock SCLKOUT from the input clock SSPCLK. Bit rates are supported to 2MHz and beyond, subject to choice of frequency for SSPCLK. The maximum bit rate will usually be determined by peripheral devices.

The SSP operating mode, frame format and size are programmed though the control registers SSPCR0, SSPCR1.

Three individually maskable interrupt outputs, **SSPTXINTR**, **SSPRXINTR** and **SSPRORINTR**, are generated:

- **SSPTXINTR** requests servicing of the transmit buffer
- **SSPRXINTR** requests servicing of the receive buffer
- **SSPRORINTR** indicates an overrun condition in the receive FIFO.

19.4 SSP Pin Multiplex

The SSP pins are multiplexed and may be used for the I^2S controller instead of SSP by setting DeviceCfg.I2SonSSP.

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19.5 Configuring the SSP

Following reset, the SSP logic is disabled and must be configured when in this state. Control registers SSPCR0 and SSPCR1 need to be programmed to configure the peripheral as a master or slave operating under one of the following protocols:

- Motorola SPI
- Texas Instruments SSI
- National Semiconductor.

The bit rate, derived from the external SSPCLK, requires the programming of the clock prescale register SSPCPSR. The following procedure must be used to initialize the SSP function:

1. Set the enable bit (SSE) in register SSPCR1.
2. Write the other SSP configuration registers: SSPCR0 and SSPCPSR.
3. Clear the enable bit (SSE) in register SSPCR1.
4. Set the enable bit (SSE) in register SSPCR1.

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19.5.1 Enabling SSP Operation

You can either prime the transmit FIFO, by writing up to eight 16-bit values when the SSP is disabled, or allow the transmit FIFO service request to interrupt the CPU. Once enabled, transmission or reception of data begins on the transmit (**SSPTXD**) and receive (**SSPRXD**) pins.

19.5.2 Master/Slave Mode

To configure the SSP as a master, clear the SSPCR1 register master or slave selection bit (MS) to 0, which is the default value on reset. Setting the SSPCR1 register MS bit to 1 configures the SSP as a slave. When configured as a slave, enabling or disabling of the SSP **SSPTXD** signal is provided through the SSPCR1 slave mode **SSPTXD** output disable bit (SOD).

19.5.3 Serial Bit Rate Generation

The serial bit rate is derived by dividing down the 7.4 MHz SSPCLK. The clock is first divided by an even prescale value CPSDVSR from 2 to 254, which is programmed in SSPCPSR. The clock is further divided by a value from 1 to 256, which is 1 + SCR, where SCR is the value programmed in SSPCR0. The frequency of the output signal bit clock, **SCLKOUT,** is defined below:

$$F_{sspclkout} = F_{sspclk} / (cpsdvr \times (1 + scr))$$

19.5.4 Frame Format

Each data frame is between 4 and 16 bits long depending on the size of data programmed, and is transmitted starting with the MSB. There are three basic frame types that can be selected:

- Texas Instruments synchronous serial
- Motorola SPI
- National Semiconductor Microwire.

For all three formats, the serial clock (**SCLKOUT**) is held inactive while the SSP is idle, and transitions at the programmed frequency only during active transmission or reception of data. The idle state of **SCLKOUT** is utilized to provide a receive timeout indication that occurs when the receive FIFO still contains data after a timeout period.

For Motorola SPI and National Semiconductor Microwire frame formats, the serial frame (**SFRMOUT**) pin is active LOW, and is asserted (pulled down) during the entire transmission of the frame.

For Texas Instruments synchronous serial frame format, the **SFRMOUT** pin is pulsed for one serial clock period starting at its rising edge, prior to the transmission of each frame. For this frame format, both the SSP and the off-

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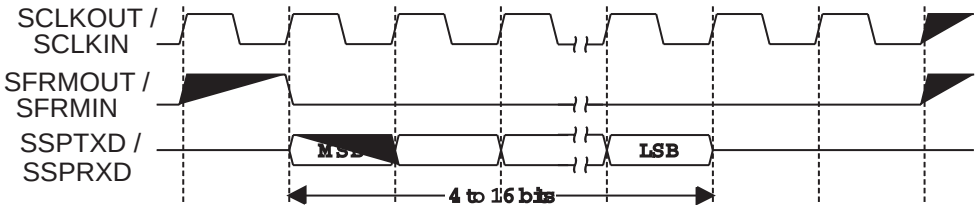
chip slave device drive their output data on the rising edge of **SCLKOUT**, and latch data from the other device on the falling edge.

Unlike the full-duplex transmission of the other two frame formats, the National Semiconductor Microwire format uses a special master-slave messaging technique, which operates at half-duplex. In this mode, when a frame begins, an 8-bit control message is transmitted to the off-chip slave. During this transmit, no incoming data is received by the SSP. After the message has been sent, the off-chip slave decodes it and, after waiting one serial clock after the last bit of the 8-bit control message has been sent, responds with the requested data. The returned data can be 4 to 16 bits in length, making the total frame length anywhere from 13 to 25 bits.

19.5.5 Texas Instruments® Synchronous Serial Frame Format

Figure 19-1 shows the Texas Instruments synchronous serial frame format for a single transmitted frame.

Figure 19-1. Texas Instruments Synchronous Serial Frame Format (Single Transfer)



In this mode, **SCLKOUT** and **SFRMOUT** are forced LOW, and the transmit data line **SSPTXD** is high impedance whenever the SSP is idle. Once the bottom entry of the transmit FIFO contains data, **SFRMOUT** is pulsed HIGH for one **SCLKOUT** period. The value to be transmitted is also transferred from the transmit FIFO to the serial shift register of the transmit logic. On the next rising edge of **SCLKOUT**, the MSB of the 4 to 16-bit data frame is shifted out on the **SSPTXD** pin. Likewise, the MSB of the received data is shifted onto the **SSPRXD** pin by the off-chip serial slave device.

Both the SSP and the off-chip serial slave device then clock each data bit into their serial shifter on the falling edge of each **SCLKOUT**. The received data is transferred from the serial shifter to the receive FIFO on the first rising edge of **SCLKOUT** after the LSB has been latched. Figure 19-2 on page 501 shows the Texas Instruments synchronous serial frame format when back-to-back frames are transmitted.

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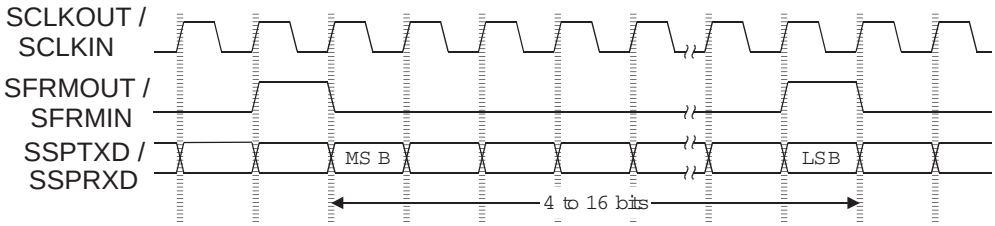
Figure 19-2. TI Synchronous Serial Frame Format (Continuous Transfer)



19.5.6 Motorola® SPI Frame Format

The Motorola SPI interface is a four-wire interface where the **SFRMOUT** signal behaves as a slave select. The main feature of the Motorola SPI format is that the inactive state and phase of the **SCLKOUT** signal are programmable through the SPO and SPH bits within the control register, “SSPCR0” on page 510.

19.5.6.1 SPO Clock Polarity

When the SPO clock polarity control bit is LOW, it produces a steady state low value on the **SCLKOUT** pin. If the SPO clock polarity control bit is HIGH, a steady state high value is placed on the **SCLKOUT** pin when data is not being transferred.

19.5.6.2 SPH Clock Phase

The SPH control bit selects the clock edge that captures data and allows it to change state. It has the most impact on the first bit transmitted by either allowing or not allowing a clock transition before the first data capture edge.

When the SPH phase control bit is LOW, data is captured on the first clock edge transition. If the SPH clock phase control bit is HIGH, data is captured on the second clock edge transition.

19.5.7 Motorola SPI Format with SPO=0, SPH=0

Single and continuous transmission signal sequences for Motorola SPI format with SPO=0, SPH=0 are shown in Figure 19-3 on page 502 and Figure 19-4 on page 502.

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Figure 19-3. Motorola SPI Frame Format (Single Transfer) with SPO=0 and SPH=0

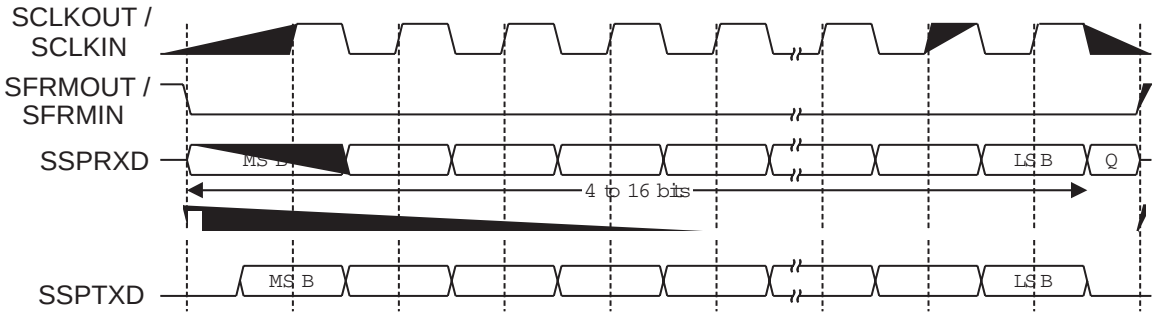
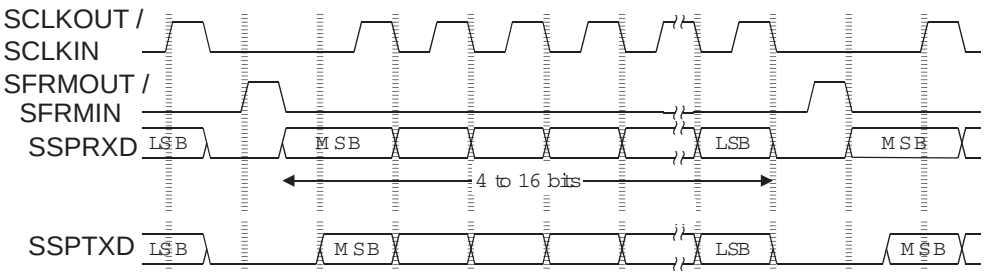


Figure 19-4. Motorola SPI Frame Format (Continuous Transfer) with SPO=0 and SPH=0



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In this configuration, during idle periods:

- the **SCLKOUT** signal is forced LOW
- **SFRMOUT** is forced HIGH
- the transmit data line **SSPTXD** is arbitrarily forced LOW
- when the SSP is configured as a master, the **SSPCTLOE** line is driven LOW, enabling the **SCLKOUT** pad (active LOW enable)
- when the SSP is configured as a slave, the **SSPCTLOE** line is driven HIGH, disabling the **SCLKOUT** pad (active LOW enable).

If the SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the **SFRMOUT** master signal being driven LOW. This causes slave data to be enabled onto the **SSPRXD** input line of the master. The master **SSPTXD** output pad is enabled.

One half **SCLKOUT** period later, valid master data is transferred to the **SSPTXD** pin. Now that both the master and slave data have been set, the **SCLKOUT** master clock pin goes HIGH after one further half **SCLKOUT** period.

The data is now captured on the rising and propagated on the falling edges of the **SCLKOUT** signal.

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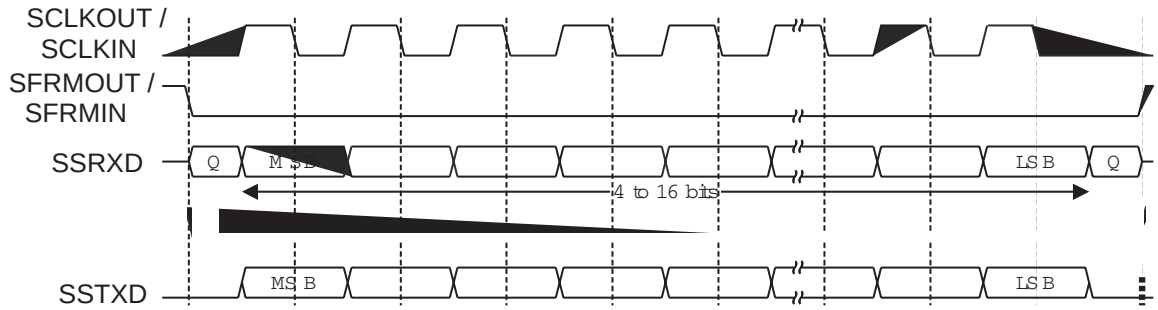
In the case of a single word transmission, after all bits of the data word have been transferred, the **SFRMOUT** line is returned to its idle HIGH state one **SCLKOUT** period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the **SFRMOUT** signal must be pulsed HIGH between each data word transfer. This is because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the SPH bit is logic zero. Therefore the master device must raise the **SFRMIN** pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the **SFRMOUT** pin is returned to its idle state one **SCLKOUT** period after the last bit has been captured.

19.5.8 Motorola SPI Format with SPO=0, SPH=1

The transfer signal sequence for Motorola SPI format with SPO=0, SPH=1 is shown in Figure 19-5, which covers both single and continuous transfers.

Figure 19-5. Motorola SPI Frame Format with SPO=0 and SPH=1



In this configuration, during idle periods:

- the **SCLKOUT** signal is forced LOW
- **SFRMOUT** is forced HIGH
- the transmit data line **SSPTXD** is arbitrarily forced LOW
- when the SSP is configured as a master, the **SSPCTLOE** line is driven LOW, enabling the **SCLKOUT** pad (active LOW enable)
- when the SSP is configured as a slave, the **SSPCTLOE** line is driven HIGH, disabling the **SCLKOUT** pad (active LOW enable).

If the SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the **SFRMOUT** master signal being driven LOW. The master **SSPTXD** output pad is enabled. After a further one half **SCLKOUT** period, both master and slave valid data is enabled onto their respective transmission lines. At the same time, the **SCLKOUT** is enabled with a rising edge transition.

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Data is then captured on the falling edges and propagated on the rising edges of the **SCLKOUT** signal.

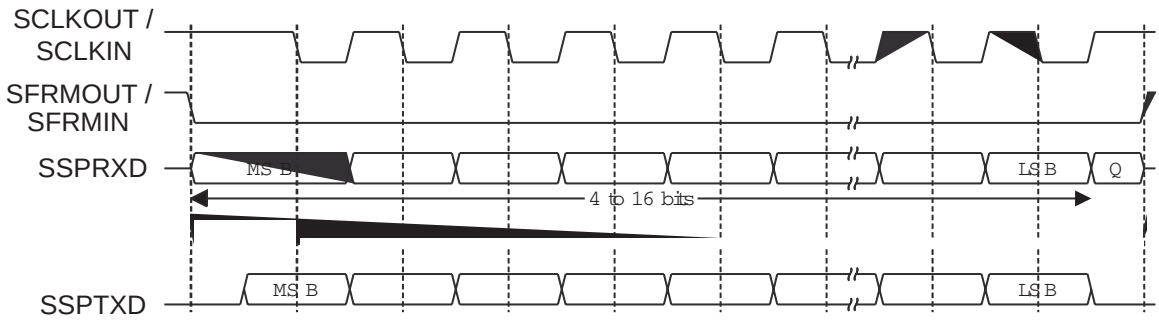
In the case of a single word transfer, after all bits have been transferred, the **SFRMOUT** line is returned to its idle HIGH state one **SCLKOUT** period after the last bit has been captured.

For continuous back-to-back transfers, the **SFRMOUT** pin is held LOW between successive data words and termination is the same as that of the single word transfer.

19.5.9 Motorola SPI Format with SPO=1, SPH=0

Single and continuous transmission signal sequences for Motorola SPI format with SPO=1, SPH=0 are shown in Figure 19-6 and Figure 19-7 on page 505.

Figure 19-6. Motorola SPI Frame Format (Single Transfer) with SPO=1 and SPH=0



Note: In Figure 19-6, Q is an undefined signal.

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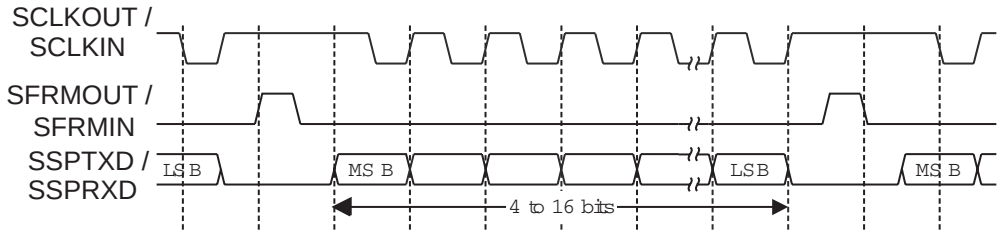
Figure 19-7. Motorola SPI Frame Format (Continuous Transfer) with SPO=1 and SPH=0



In this configuration, during idle periods

- the **SCLKOUT** signal is forced HIGH
- **SFRMOUT** is forced HIGH
- the transmit data line **SSPTXD** is arbitrarily forced LOW
- when the SSP is configured as a master, the **SSPCTLOE** line is driven LOW, enabling the **SCLKOUT** pad (active LOW enable)
- when the SSP is configured as a slave, the **SSPCTLOE** line is driven HIGH, disabling the **SCLKOUT** pad (active LOW enable).

If the SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the **SFRMOUT** master signal being driven LOW, which causes slave data to be immediately transferred onto the **SSPRXD** line of the master. The master **SSPTXD** output pad is enabled.

One half period later, valid master data is transferred to the **SSPTXD** line. Now that both the master and slave data have been set, the **SCLKOUT** master clock pin becomes LOW after one further half **SCLKOUT** period. This means that data is captured on the falling edges and be propagated on the rising edges of the **SCLKOUT** signal.

In the case of a single word transmission, after all bits of the data word are transferred, the **SFRMOUT** line is returned to its idle HIGH state one **SCLKOUT** period after the last bit has been captured.

However, in the case of continuous back-to-back transmissions, the **SFRMOUT** signal must be pulsed HIGH between each data word transfer. This is because the slave select pin freezes the data in its serial peripheral register and does not allow it to be altered if the SPH bit is logic zero. Therefore the master device must raise the **SFRMIN** pin of the slave device between each data transfer to enable the serial peripheral data write. On completion of the continuous transfer, the **SFRMOUT** pin is returned to its idle state one **SCLKOUT** period after the last bit has been captured.

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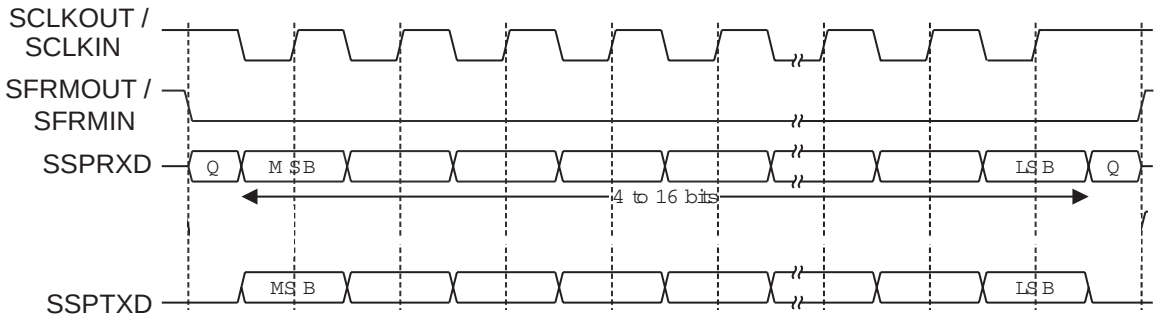
19.5.10 Motorola SPI Format with SPO=1, SPH=1

The transfer signal sequence for Motorola SPI format with SPO=1, SPH=1 is shown in Figure 19-8, which covers both single and continuous transfers.

Figure 19-8. Motorola SPI Frame Format with SPO=1 and SPH=1



Note: Figure 19-8, Q is an undefined signal.

In this configuration, during idle periods:

- the **SCLKOUT** signal is forced HIGH
- **SFRMOUT** is forced HIGH
- the transmit data line **SSPTXD** is arbitrarily forced LOW
- when the SSP is configured as a master, the **SSPCTLOE** line is driven LOW, enabling the **SCLKOUT** pad (active LOW enable)
- when the SSP is configured as a slave, the **SSPCTLOE** line is driven HIGH, disabling the **SCLKOUT** pad (active LOW enable).

If the SSP is enabled and there is valid data within the transmit FIFO, the start of transmission is signified by the **SFRMOUT** master signal being driven LOW. The master **SSPTXD** output pad is enabled. After a further one half **SCLKOUT** period, both master and slave data are enabled onto their respective transmission lines. At the same time, the **SCLKOUT** is enabled with a falling edge transition. Data is then captured on the rising edges and propagated on the falling edges of the **SCLKOUT** signal.

After all bits have been transferred, in the case of a single word transmission, the **SFRMOUT** line is returned to its idle HIGH state one SCLKOUT period after the last bit has been captured.

For continuous back-to-back transmissions, the **SFRMOUT** pins remains in its active LOW state, until the final bit of the last word has been captured, and then returns to its idle state as described above.

For continuous back-to-back transfers, the **SFRMOUT** pin is held LOW between successive data words and termination is the same as that of the single word transfer.

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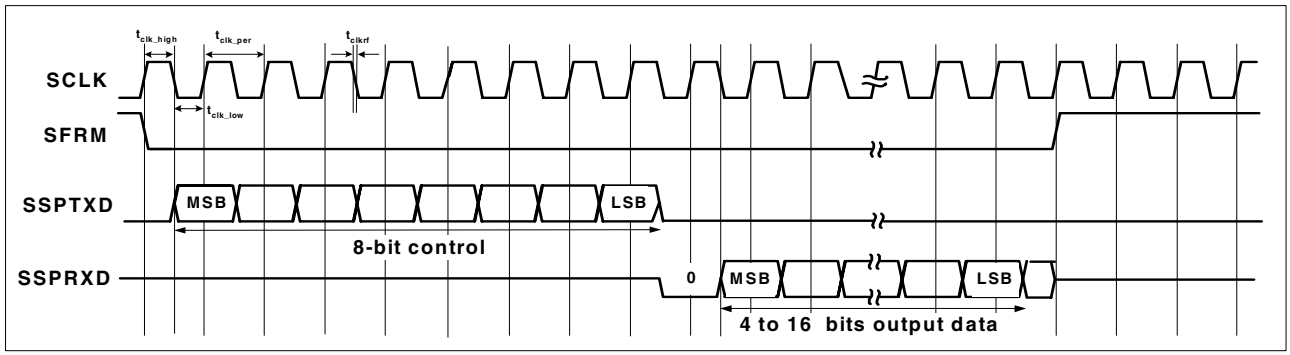
19.5.11 National Semiconductor® Microwire® Frame Format

Figure 19-9 shows the National Semiconductor Microwire frame format, again for a single frame. Figure 19-10 on page 508 shows the same format when back to back frames are transmitted.

Figure 19-9. Microwire Frame Format (Single Transfer)



Microwire format is very similar to SPI format, except that transmission is half-duplex instead of full-duplex, using a master-slave message passing technique. Each serial transmission begins with an 8-bit control word that is transmitted from the SSP to the off-chip slave device. During this transmission, no incoming data is received by the SSP. After the message has been sent, the off-chip slave decodes it and, after waiting one serial clock after the last bit of the 8-bit control message has been sent, responds with the required data. The returned data is 4 to 16 bits in length, making the total frame length anywhere from 13 to 25 bits.

In this configuration, during idle periods:

- the **SCLKOUT** signal is forced LOW
- **SFRMOUT** is forced HIGH
- the transmit data line **SSPTXD** is arbitrarily forced LOW

A transmission is triggered by writing a control byte to the transmit FIFO. The falling edge of **SFRMOUT** causes the value contained in the bottom entry of the transmit FIFO to be transferred to the serial shift register of the transmit logic, and the MSB of the 8-bit control frame to be shifted out onto the **SSPTXD** pin. **SFRMOUT** remains LOW for the duration of the frame transmission. The **SSPRXD** pin remains high impedance during this transmission.

The off-chip serial slave device latches each control bit into its serial shifter on the rising edge of each **SCLKOUT**. After the last bit is latched by the slave device, the control byte is decoded during a one clock wait-state, and the slave responds by transmitting data back to the SSP. Each bit is driven onto **SSPRXD** line on the falling edge of **SCLKOUT**. The SSP in turn latches each bit on the rising edge of **SCLKOUT.** At the end of the frame, for single

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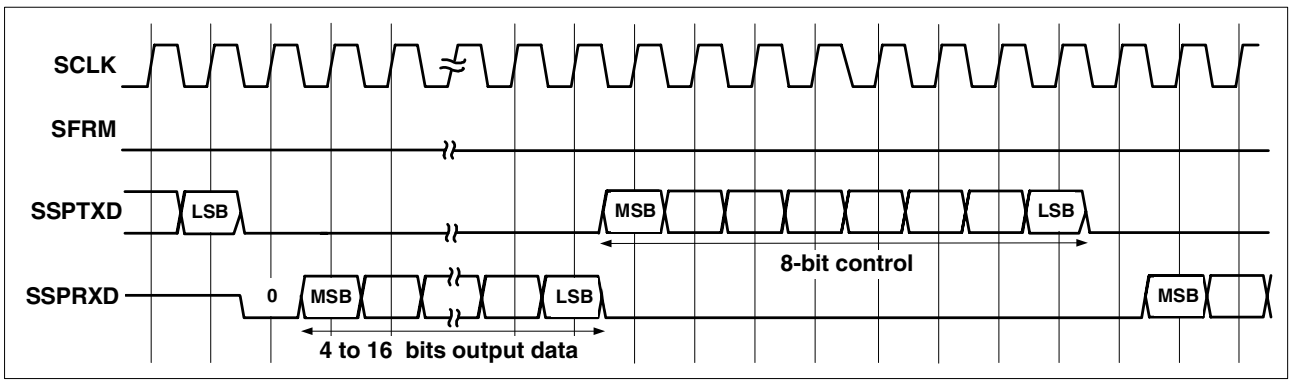
transfers, the **SFRMOUT** signal is pulled HIGH one clock period after the last bit has been latched in the receive serial shifter, that causes the data to be transferred to the receive FIFO.

*Note: The off-chip slave device can drive the receive line to a high impedance state either on the falling edge of **SCLKOUT** after the LSB has been latched by the receive shifter, or when the **SFRMOUT** pin goes HIGH.*

For continuous transfers, data transmission begins and ends in the same manner as a single transfer. However, the **SFRMOUT** line is continuously asserted (held LOW) and transmission of data occurs back to back. The control byte of the next frame follows directly after the LSB of the received data from the current frame. Each of the received values is transferred from the receive shifter on the falling edge **SCLKOUT**, after the LSB of the frame has been latched into the SSP.

Figure 19-10. Microwire Frame Format (Continuous Transfers)



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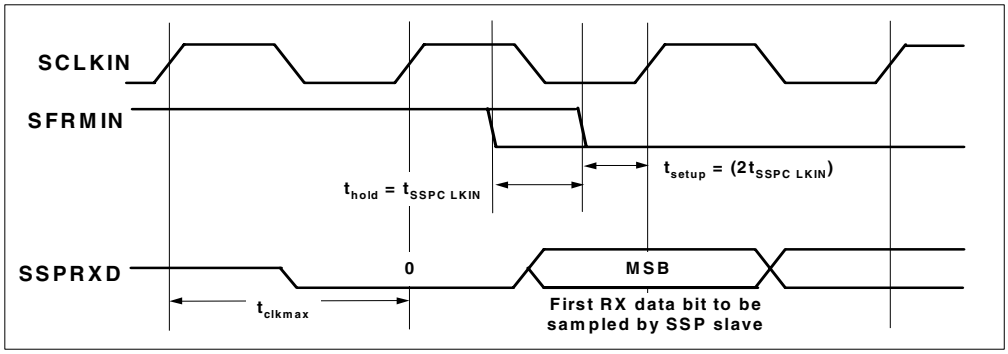
19.5.11.1 Setup and Hold Time Requirements on SFRMIN with Respect to SCLKIN in Microwire Mode

In the Microwire mode, the SSP slave samples the first bit of receive data on the rising edge of **SCLKIN** after **SFRMIN** has gone LOW. Masters that drive a free-running **SCLKIN** must ensure that the **SFRMIN** signal has sufficient setup and hold margins with respect to the rising edge of **SCLKIN**.

Figure 19-11 illustrates these setup and hold time requirements. With respect to the **SCLKIN** rising edge on which the first bit of receive data is to be sampled by the SSP slave, **SFRMIN** must have a setup of at least two times the period of **SCLKIN** on which the SSP operates. With respect to the **SCLKIN** rising edge previous to this edge, **SFRMIN** must have a hold of at least one **SCLKIN** period.

Figure 19-11. Microwire Frame Format, SFRMIN Input Setup and Hold Requirements



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19.6 Registers

The SSP registers are shown in the following table.

Table 19-1: SSP Register Memory Map Description

Address	Type	Width	Reset value	Name	Description
0x808A_0000	Read/write	16	0x0000	SSPCR0	Control register 0.
0x808A_0004	Read/write	8	0x00	SSPCR1	Control register 1.
0x808A_0008	Read/write	16	0x0000	SSPDR	Receive FIFO (Read)/ Transmit FIFO data register (Write).
0x808A_000C	Read	7	0x00	SSPSR	Status register.
0x808A_0010	Read/write	8	0x00	SSPCPSR	Clock prescale register.
0x808A_0014	Read	3	0x0	SSPIIR/ SSPICR	Interrupt identification register (read) Interrupt clear register (write).
0x808A_0018 - 0x808A_003C	-	-	-	-	Reserved
0x808A_0094 - 0x808A_00FF	-	-	-	-	Reserved

Register Descriptions

SSPCR0

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCR								SPH	SPO	FRF		DSS			

Address:

0x808A_0000 - Read/Write

Default:

0x0000_0000

Definition:

SSPCR0 is the control register 0 and contains four different bit fields, which control various functions within the SSP.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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SCR: Serial clock rate. The value SCR is used to generate the transmit and receive bit rate of the SSP. SCR is a value from 0 to 255. This provides the secondary divide of (1+SCR) after a pre divide of CPSDVSR (ranging from 2 to 254)

SPH: SCLKOUT phase (applicable to Motorola SPI frame format only).

SPO: SCLKOUT polarity (applicable to Motorola SPI frame format only).

FRF: Frame format:
00 Motorola SPI frame format
01 - TI synchronous serial frame format
10 - National Semiconductor Microwire frame format
11 - Reserved, undefined operation

DSS: Data Size Select:
0000 - Reserved, undefined operation
0001 - Reserved, undefined operation
0010 - Reserved, undefined operation
0011 - 4-bit data
0100 - 5-bit data
0101 - 6-bit data
0110 - 7-bit data
0111 - 8-bit data
1000 - 9-bit data
1001 - 10-bit data
1010 - 11-bit data
1011 - 12-bit data
1100 - 13-bit data
1101 - 14-bit data
1110 - 15-bit data
1111 - 16-bit data

SSPCR1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD									SOD	MS	SSE	LBM	RORIE	TIE	RIE

Address:

0x808A_0004 - Read/Write

Default:

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0x0000_0000

Definition:

SSPCR1 is the control register 1 and contains six different bit fields, which control various functions within the SSP.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

SOD: Slave-mode output disable. This bit is relevant only in the slave mode (MS=1). In multiple-slave systems, it is possible for an SSPMS master to broadcast a message to all slaves in the system while ensuring that only one slave drives data onto its serial output line. In such systems the RXD lines from multiple slaves can be tied together. To operate in such systems, the SOD may be set if the SSP slave is not supposed to drive the **SSPTXD** line.
0 - SSP may drive the **SSPTXD** output in slave mode.
1 - SSP must not drive the **SSPTXD** output in slave modes.

MS: Master / Slave mode select. This bit can be modified only when the SSP is disabled (SSE=0).
0 - Device configured as master (default).
1 - Device configured as slave.

SSE: Synchronous serial port enable:
0 - SSP operation disabled
1 - SSP operation enabled.

LBM: Loop back mode:
0 - Normal serial port operation enabled.
1 - Output of transmit serial shifter is connected to input of receive serial shifter internally.

RORIE: Receive FIFO overrun interrupt enable:
0 - Overrun detection is disabled. Overrun condition does not generate the **SSPRORINTR** interrupt.
1 - Overrun detection is enabled. Overrun condition generates the **SSPRORINTR** interrupt.

TIE: Transmit FIFO interrupt enable:
0 - Transmit FIFO half-full or less condition does not generate the **SSPTXINTR** interrupt.
1 - Transmit FIFO half-full or less condition generates the **SSPTXINTR** interrupt.

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RIE: Receive FIFO interrupt enable:
0 - Receive FIFO half-full or more condition does not generate the **SSPRXINTR** interrupt.
1 - Receive FIFO half-full or more condition generates the **SSPRXINTR** interrupt.

SSPDR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DATA															

Address:

0x808A_0008 - Read/Write

Default:

0x0000_0000

Definition:

SSPDR is the data register and is 16-bits wide. When SSPDR is read, the entry in the receive FIFO (pointed to by the current FIFO read pointer) is accessed. As data values are removed by the SSPs receive logic from the incoming data frame, they are placed into the entry in the receive FIFO (pointed to by the current FIFO write pointer).

When SSPDR is written, the entry in the transmit FIFO (pointed to by the write pointer), is written. Data values are removed from the transmit FIFO one value at a time by the transmit logic. It is loaded into the transmit serial shifter, then serially shifted out onto the **SSPTXD** pin at the programmed bit rate.

When a data size of less than 16 bits is selected, the user must right-justify data written to the transmit FIFO. The transmit logic ignores the unused bits. Received data less than 16 bits is automatically right justified in the receive buffer.

When the SSP is programmed for National Semiconductor Microwire frame format, the default size for transmit data is eight bits (the most significant byte is ignored). The receive data size is controlled by the programmer. The transmit FIFO and the receive FIFO are not cleared even when SSE is set to zero. This allows the software to fill the transmit FIFO before enabling the SSP.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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DATA: Transmit / Receive FIFO:
Read - Receive FIFO
Write - Transmit FIFO

Note: The user should right-justify data when the SSP is programmed for a data size that is less than 16 bits. Unused bits at the top are ignored by transmit logic. The receive logic automatically right justifies.

SSPSR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD											BSY	RFF	RNE	TNF	TFE

Address:

0x808A_000C - Read Only

Default:

0x0000_0000

Definition:

SSPSR is a read-only status register, which contains bits that indicate the FIFO fill status and the SSP busy status.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

BSY: SSP busy flag (read-only):
0 - SSP is idle.
1 - SSP is currently transmitting and / or receiving a frame or the transmit FIFO is non-empty.

RFF: Receive FIFO full (read-only):
0 - Receive FIFO is not full
1 - Receive FIFO is full

RNE: Receive FIFO not empty (read-only):
0 - Receive FIFO is empty.
1 - Receive FIFO is not empty

TNF: Transmit FIFO not full (read-only):
0 - Transmit FIFO is full.
1 - Transmit FIFO is not full.

TFE: Transmit FIFO empty (read-only):
0 - Transmit FIFO is not empty
1 - Transmit FIFO is empty

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SSPCPSR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								CPSDVSR							

Address:

0x808A_0010 - Read/Write

Default:

0x0000_0000

Definition:

SSPCPSR is the clock prescale register and specifies the division factor by which the input SSPCLK should be internally divided before further use.

The value programmed into this register should be an even number between 2 and 254. The least significant bit of the programmed number is hard-coded to zero. If an odd number is written to this register, data read back from this register will have the least significant bit as zero.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

CPSDVSR: Clock pre-scale divisor. Should be an even number from 2 to 254, depending on the frequency of SSPCLK. The least significant bit CPSDVSR[0] always returns zero on reads since it is hard-coded to 0

SSPIIR / SSPICR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													RORIS	TIS	RIS

Address:

0x808A_0014 - Read Only

Note: A write to this register clears the receive overrun interrupt, regardless of the data value written.

Default:

0x0000_0000

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Definition:

The interrupt status is read from the SSP interrupt identification register (SSPIIR). A write of any value to the SSP interrupt clear register (SSPICR) clears the SSP receive FIFO overrun interrupt. Therefore, clearing the RORIE bit in the SSPCR1 register will also clear the overrun condition if already asserted. All the bits are cleared to zero when reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

RORIS: Read: SSP Receive FIFO overrun interrupt status
0 - **SSPRORINTR** is not asserted.
1 - **SSPRORINTR** is asserted.
This bit is cleared by writing any value to the SSPSR register

TIS: Read: SSP transmit FIFO service request interrupt status
0 - **SSPTXINTR** is not asserted indicating that the transmit FIFO is more than half full.
1 - **SSPTXINTR** is asserted indicating that the transmit FIFO is less than half full (space available for at least four half words).

RIS: Read: SSP receive FIFO service request interrupt status
0 - **SSPRXINTR** is not asserted indicating that the receive FIFO is less than half full.
1 - **SSPRXINTR** is asserted indicating that the receive FIFO is more than half full (4 or more half words present in FIFO)

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Chapter 20

Analog-to-Digital Converter (ADC) Interface

20.1 Introduction

The ADC block consists of a 12-bit Analog-to-Digital converter with an analog input multiplexor. The multiplexor can be set to measure battery voltage or one of the five analog measurement pins. The input voltage measurement range is 0 to 3.3 V.

20.2 ADC Operation

- To enable clocks for the ADC block, set the TSEN bit in the Syscon section (ADCClkDiv register).
- Set the DeviceCfg.ADCEN bit.
- Clear the DeviceCfg.ADCPD bit.
- Select an input. First unlock the software lock by writing 0xAA to the ADCSWLock register. Then write an appropriate value (selected from Table 20-2 on page 520) to the ADCSwitch register.
- To poll, read the ADCResult register repeatedly. Bit 31 of this register is the SDR, or Synchronous Data Ready, bit. This bit is set when a new valid conversion value appears in this register and is cleared when this register is read. So when two consecutive reads show the bit clear and then set, the second read has the new valid value.
- Conversion data may also be processed using interrupts from this module. If bit 11 in the ADCIntEn register (the RINTEN bit) is set, an interrupt occurs whenever the SDR bit in the ADCResult register is set. Therefore, an interrupt handler can read the ADCResult register whenever a new valid sample appears in the register, which both returns a new conversion value and clears the interrupt.

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20.3 Registers

Table 20-1: Register Memory Map

Address	Name	SW locked	Type	Size	Description
0x8090_0000					Reserved
0x8090_0004					Reserved
0x8090_0008	ADCResult	No	Read Only	32 bits	ADC result register.
0x8090_000C					Reserved
0x8090_0010					Reserved
0x8090_0014					Reserved
0x8090_0018	ADCSwitch	Write	Read/Write	28 bits	ADC Switch Matrix control register.
0x8090_001C					Reserved
0x8090_0020	ADCSWLock	NA	Read/Write	1-bit read 8-bit write	ADC software lock register.
0x8090_0024	ADCIntEn	No	Read/Write	9 bits	ADC Interrupt Enable Register

Note: The ADC block decodes APB address bits PADR[6:2] only. If the decode for the PSEL_HATSH APB block select is a larger block size in the APB decoder, the registers will be repeated through memory. ADC registers are intended to be word accessed only. Since the least significant bytes of the address bus are not decoded, byte and half word accesses are not allowed and may have unpredictable results.

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Register Descriptions

ADCResult

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SDR	RSVD														

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				AD											

Address:

0x8090_0008

Default:

0x0000_0000

Definition:

ADC result register.

Bit Descriptions:

RSVD: Reserved. Unknown during read.

SDR: Synchronous Data Ready. This bit is set when new conversion data from the ADC digital filter appears the TSXYResult register. The bit is cleared when the TSXYResult register is read.

AD: Analog-to-digital converter output at 12-bit resolution.

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ADCSwitch

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SCTL															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCTL															

Address:

0x8090_0018

Default:

0x0000_0000

Definition:

Analog switch control Registers.

Bit Descriptions:

SCTL: Analog switch control values. A “1” indicates that the switch is made or closed. A “0” indicates that the switch is open.

Table 20-2 contains the values that must be loaded into the switch registers, depending on the type of input being measured.

Table 20-2: Table of ADCSwitch values

Input to Measure	ADCSwitch Value
ADC4	0x0000_0610
ADC3	0x0000_0620
ADC2	0x0000_0640
ADC1	0x0000_0680
ADC0	0x0000_0608

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ADCSWLock

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								SWLCK							

Address:

0x8090_0020

Default:

0x0000_0000

Definition:

Software lock register.

Bit Descriptions:

RSVD: Reserved. Unknown during read.

SWLCK: Software lock bits.

WRITE: The Unlock value for this feature is 0xAA. Writing 0xAA to this register will unlock all locked registers until the next block access. The ARM lock instruction prefix should be used for the two consecutive write cycles when writing to locked chip registers.

READ: During a read operation SWLCK[0] has the following meaning:
1 = Unlocked for current bus access.
0 = Locked

The Read feature of the SWLOCK register is used for testing the locking function. Since the software lock only remains unlocked for the next block cycle, this test must be performed on two consecutive cycles using the ARM lock instruction prefix. The contents of SWLCK[7:1] are unknown during a read operation.

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ADCIntEn

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD				RINTEN	RSVD										

Address:

0x8090_0024

Default:

0x0000_0000

Definition:

ADC Interrupt Enable Register

Bit Descriptions:

RSVD: Reserved. Unknown during read.

RINTEN: Synchronous Data Ready Interrupt Enable. Setting this bit results in an interrupt whenever the Synchronous Data Ready (SDR) bit in the ADCResult register is set.

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Chapter 21

GPIO Interface

21

21.1 Introduction

The General Purpose Input/Output (GPIO) is an Advanced Peripheral Bus (APB) slave module. The GPIO block is the primary controller for the **EGPIO, RDLED, GRLED, EECLK,** and **EEDAT** pins.

There are two types of GPIOs, standard and enhanced. The enhanced GPIO, called EGPIO, have interrupt generation capability.

The GPIO block has seven ports, named Port A through Port C and Port E through Port H. Ports C, E, G, and H are standard GPIO ports. Ports A, B, and F are enhanced GPIO ports.

GPIO ports control up to eight individual pins. Each port has an 8-bit data register and an 8-bit data direction register. The EGPIO ports each have additional 8-bit registers for interrupt configuration and status. The control of an individual pin is determined in a bit-slice fashion across all registers for that port; only a single bit at a particular index from each register affects or is affected by that pin.

Port sizes are as follows:
Port A - 8 bits
Port B - 8 bits
Port C - 1 bits
Port E - 2 bits
Port F - 3 bits
Port G - 2 bits
Port H - 4 bits.

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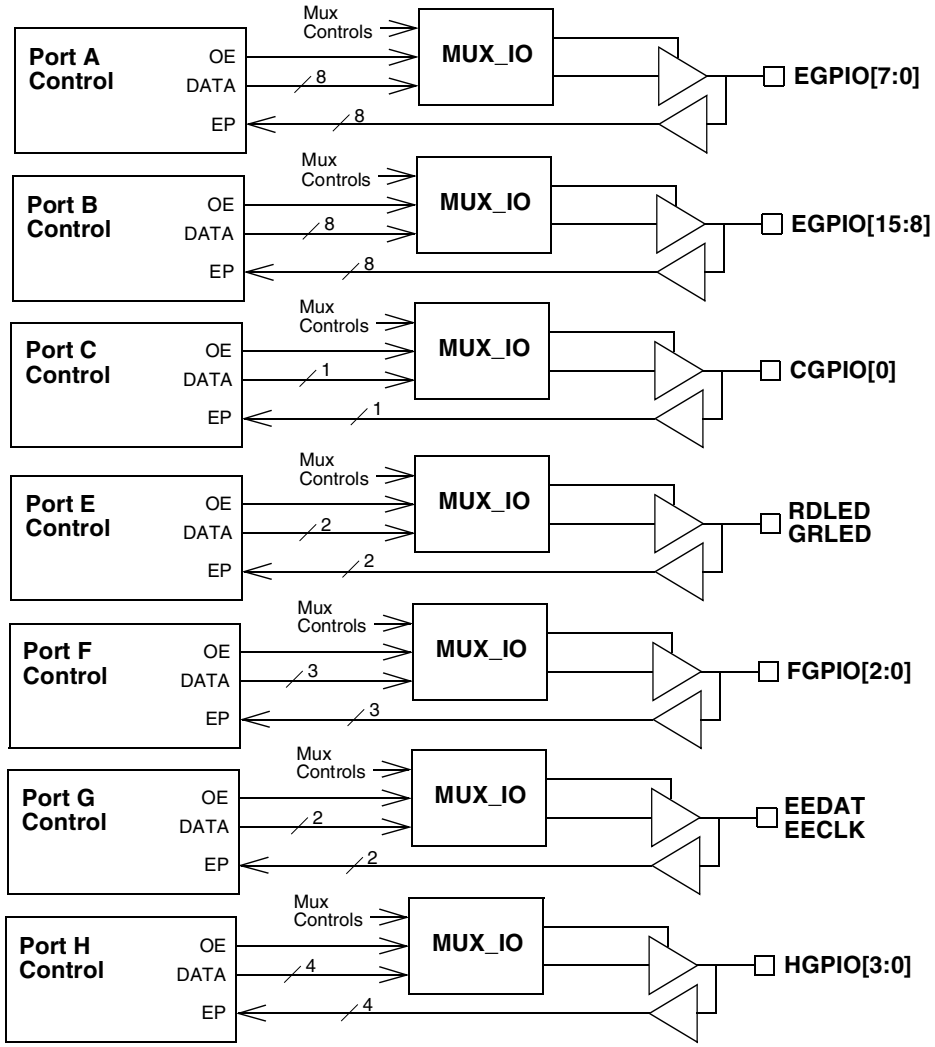
Figure 21-1. System Level GPIO Connectivity



21.1.1 Memory Map

The GPIO base address is 0x8084_0000. All registers are 8 bits wide and are aligned on word boundaries. For all registers, the upper 24 bits are not modified when written and always read zeros.

21.1.2 Functional Description

Each port has an 8-bit data register and an 8-bit direction register. The data direction register controls whether each individual GPIO pin is an input or output. Writing to a data register only affects the pins that are configured as

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outputs. Reading a data register returns the value on the corresponding GPIO pins.

Ports A, B, and F also provide interrupt capability. The 16 interrupt sources from Ports A and B are combined into a single signal **GPIOINTR** which is connected to the system interrupt controller. All three individual interrupt signals on Port F are available to the system interrupt controller as **GPIO0INTR** through **GPIO2INTR**.

The interrupt properties of each of the 19 GPIO pins on ports A, B, and F are individually configurable. Each interrupt can be either high or low level sensitive or either positive or negative edge triggered. It is also possible to enable debouncing on the Port A, B, and F interrupts. Debouncing is implemented using a 2-bit shift register clocked by a 128 Hz clock.

There are seven additional registers for ports A, B and F:

- *GPIO Interrupt Enable* registers (GPIOAIntEn, GPIOBIntEn, GPIOFIntEn) control which bits are to be configured as interrupts. Setting a bit in this register configures the corresponding pin as an interrupt input.
- *GPIO Interrupt Type 1* registers (GPIOAIntType1, GPIOBIntType1, GPIOFIntType1) determines interrupt type. Setting a bit in this register configures the corresponding interrupt as edge sensitive; clearing it makes it level sensitive.
- *GPIO Interrupt Type 2* registers (GPIOAIntType2, GPIOBIntType2, GPIOFIntType2) determines interrupt polarity. Setting a bit in this register configures the corresponding interrupt as rising edge or high level sensitive; clearing it configures the interrupt as falling edge or low level sensitive.
- *GPIO End-Of-Interrupt* registers (GPIOAEOI, GPIOBEOI, GPIOFEOI) are used to clear specific bits in the interrupt Status Register. Writing a one to a bit will clear the corresponding interrupt; writing a zero has no effect.
- *GPIO Debounce* registers (GPIOADB, GPIOBDB, GPIOFDB) enable debouncing of specific interrupts signals.
- *Interrupt Status* registers (IntStsA, IntStsB, IntStsF) provide the status of any pending unmasked interrupt.
- *Raw Interrupt Status* registers (RawIntStsA, RawIntStsB, RawIntStsF) provide the status of any pending interrupt regardless of masking.

In order to stop any spurious interrupts that may occur during the programming of the GPIOxINTTYPEx registers, the following sequence should be observed:

1. Disable interrupt by writing to GPIO Interrupt Enable register.
2. Set interrupt type by writing GPIOxINTTYPE1/2 register.

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3. Clear interrupt by writing to GPIOxEOI register.
4. Enable interrupt by writing to GPIO Interrupt Enable register.

Figure 21-5 and Figure 21-6 illustrate the signal connections for GPIO and EGPIO.

21

Figure 21-2. Signal Connections Within GPIO Port C Control Logic

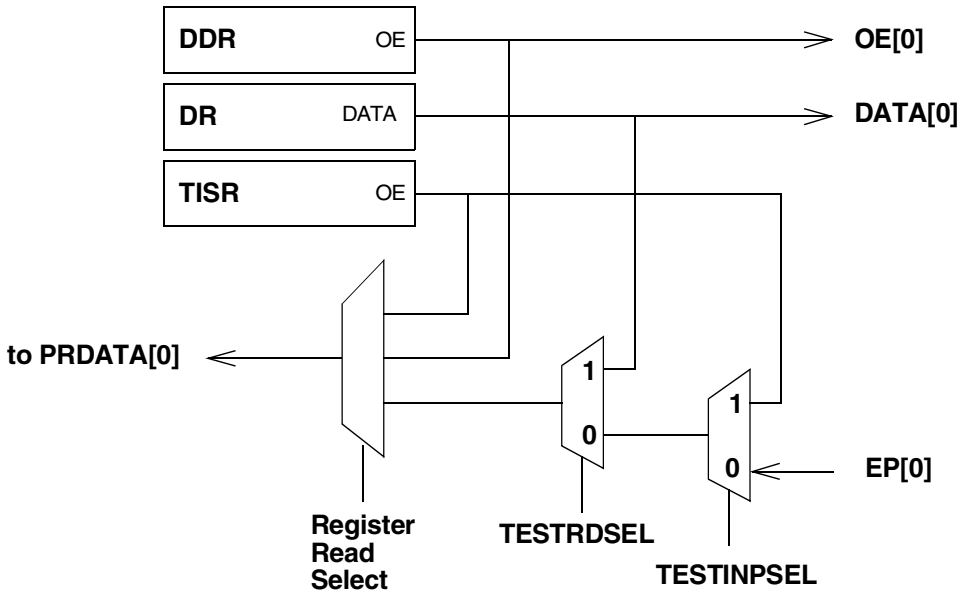

Figure 21-3. Signal Connections Within GPIO Port E Control Logic

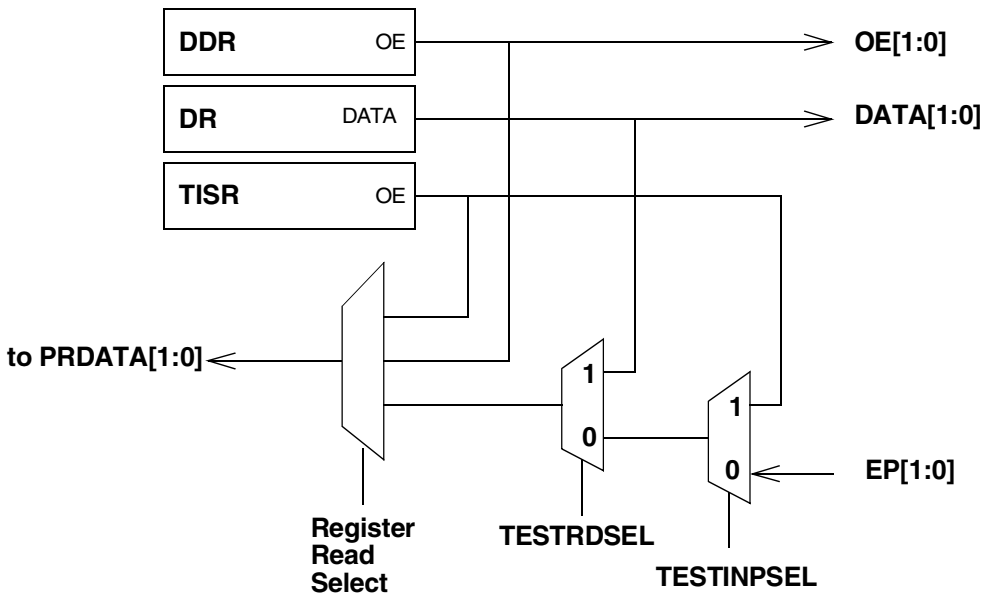

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Figure 21-4. Signal Connections Within GPIO Port G Control Logic

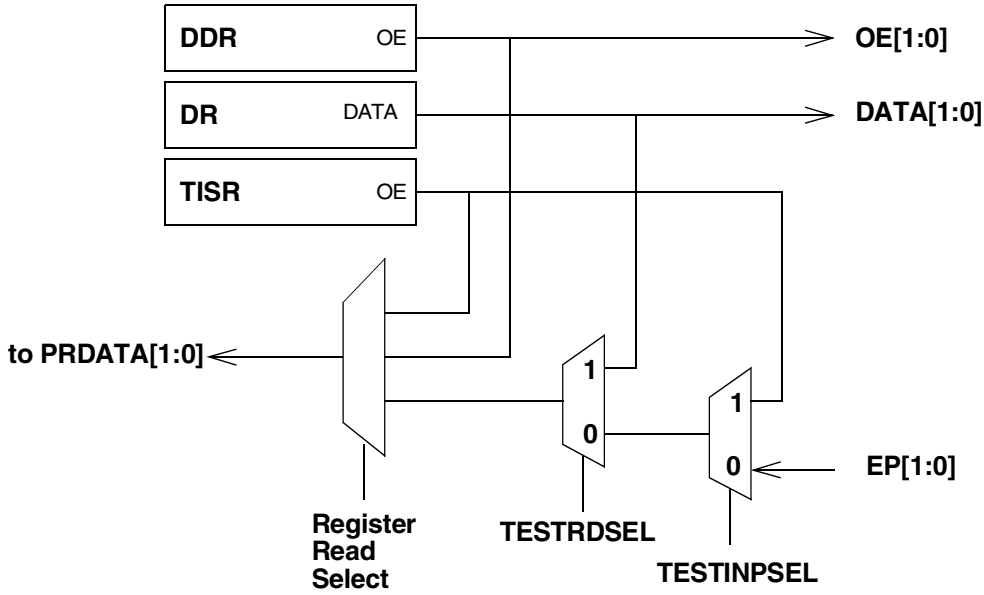

Figure 21-5. Signal Connections Within GPIO Port H Control Logic

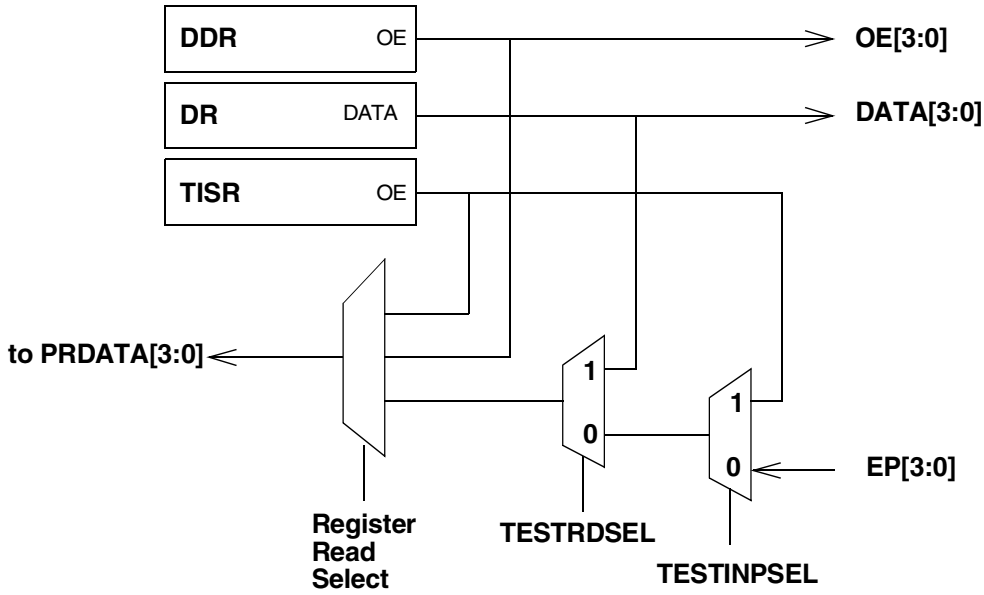

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Figure 21-6. Signal Connections Within the Enhanced GPIO Port A and B Control Logic

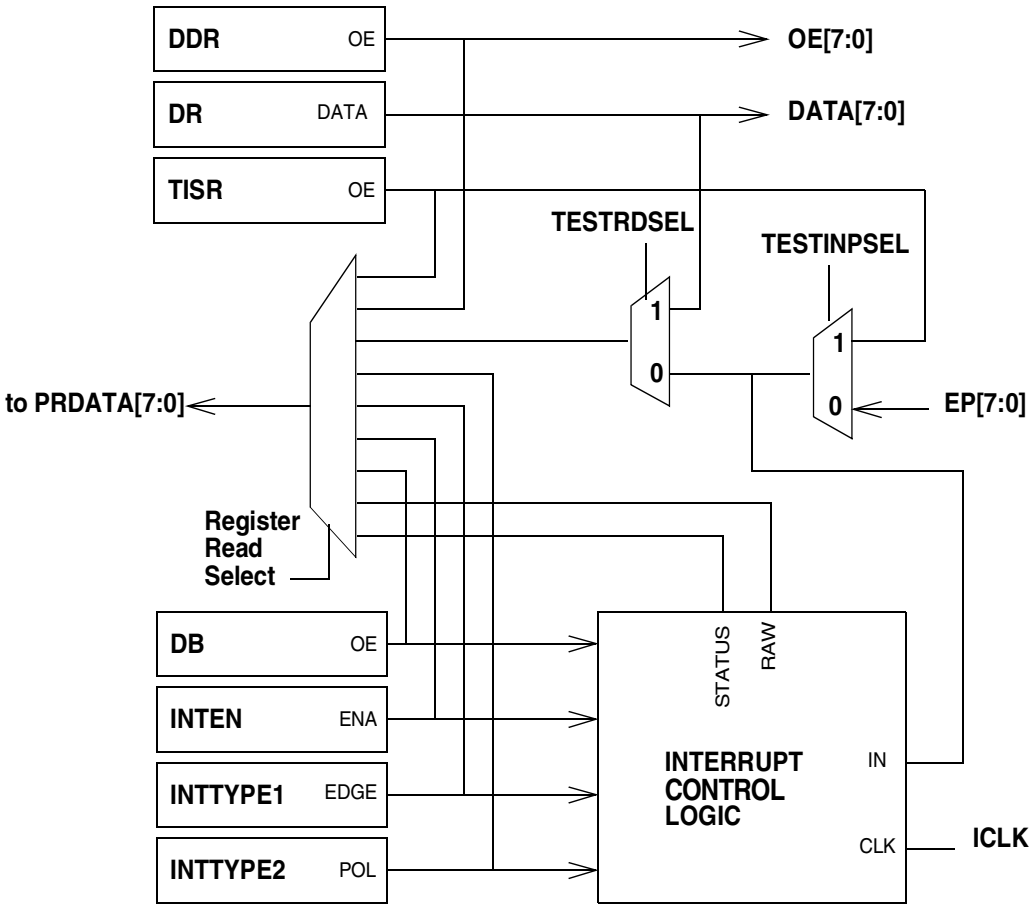

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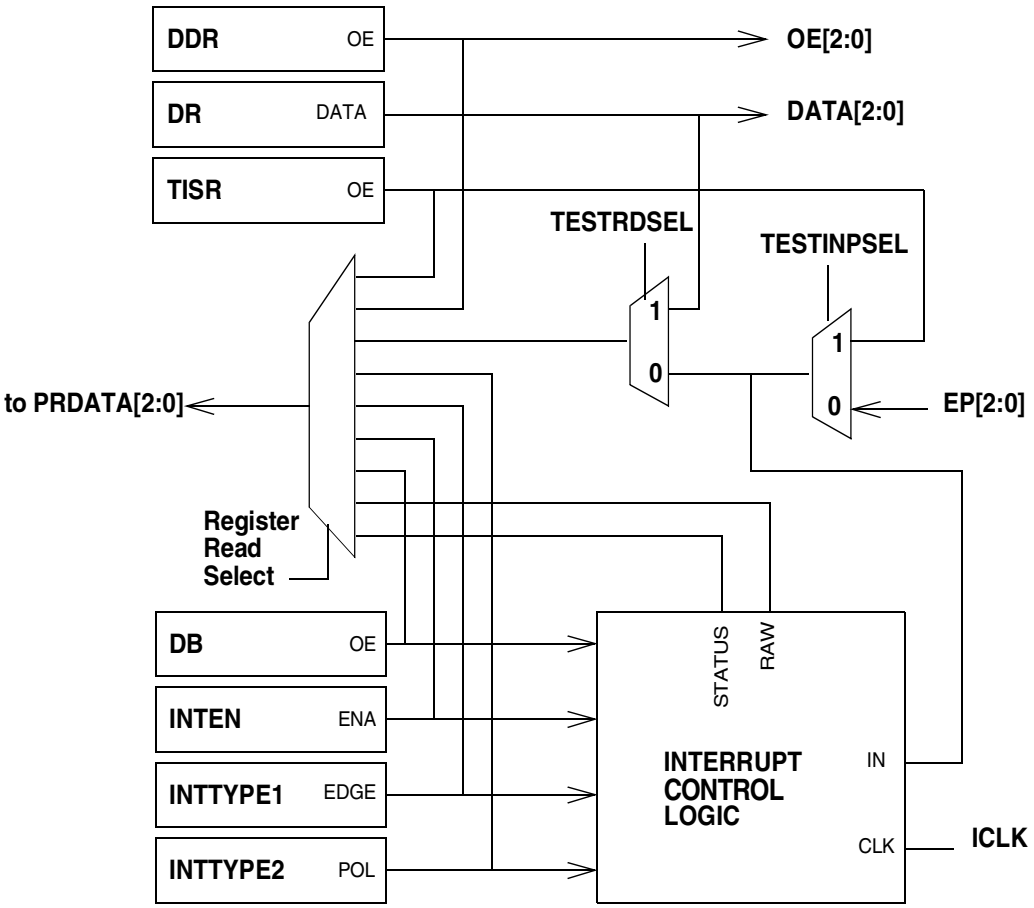
Figure 21-7. Signal Connections Within the Enhanced GPIO Port F Control Logic



21.1.3 Reset

All GPIO registers are initialized on system reset. The data and data direction registers for all ports (except as noted below) are cleared, configuring them as inputs. Port E[1:0] bits are used for the LED outputs **RDLED** and **GRLED** respectively and are set to drive high. Port G[1:0] bits are used for **EEDAT** and **EECLK** respectively and are set up as inputs. All interrupt control and debounce registers are cleared.

21.1.4 GPIO Pin Map

All GPIO signals are mapped to device pins. The following table shows how the GPIO ports map to EP9301 pins.

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Table 21-1: GPIO Port to Pin Map

Pin Name	Default Function
EGPIO[7:0]	Port A
EGPIO[15:8]	Port B
GRLED	Port E[0]
RDLED	Port E[1]
EECLK	PortG[0]
EEDAT	PortG[1]

GRLED is the Green LED pin.
RDLED is the Red LED pin.
EECLK is the EEPROM clock pin.
EEDAT is the EEPROM data pin.

When the GPIO port signals are not explicitly mapped to a device pin, as defined in Table 21-1, the inputs will continue to monitor the pin while outputs are disconnected.

Another level of functional muxing is applied to several EGPIO pins. The Syscon DeviceCfg register bits RonG, MonG, HC1EN, and map different functionality to the EGPIO pins:

- MonG maps **RI** (modem Ring Indicator) onto **EGPIO[0].**
- RonG maps **CLK32K**, the 32 KHz clock monitor output for RTC calibration, onto **EGPIO[1]**.
- HC1EN maps the synchronous HDLC clock onto **EGPIO[3]**.

Some GPIO signals are used as inputs by other functional blocks. **EGPIO[2:1]** are routed to the DMA controller to allow for external DMA requests.

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21.2 Registers

Table 21-2: GPIO Register Address Map

Address	Read Location	Type	Write Location	Reset Value
0x8084_0000	PADR	R/W	PADR	Note 1
0x8084_0004	PBDR	R/W	PBDR	Note 1
0x8084_0008	PCDR	R/W	PCDR	Note 1
0x8084_000C	Reserved	-	Reserved	-
0x8084_0010	PADDR	R/W	PADDR	0x00
0x8084_0014	PBDDR	R/W	PBDDR	0x00
0x8084_0018	PCDDR	R/W	PCDDR	0
0x8084_001C	Reserved	-	Reserved	-
0x8084_0020	PEDR	R/W	PEDR	Note 2
0x8084_0024	PEDDR	R/W	PEDDR	0x03
0x8084_0028	Reserved	-	Reserved	-
0x8084_002C	Reserved	-	Reserved	-
0x8084_0030	PFDR	R/W	PFDR	Note 1
0x8084_0034	PFDDR	R/W	PFDDR	0x00
0x8084_0038	PGDR	R/W	PGDR	Note 1
0x8084_003C	PGDDR	R/W	PGDDR	0x0C
0x8084_0040	PHDR	R/W	PHDR	Note 1
0x8084_0044	PHDDR	R/W	PHDDR	0x00
0x8084_0048	Reserved	-	Reserved	-
0x8084_004C	GPIOFIntType1	R/W	GPIOFIntType1	0x00
0x8084_0050	GPIOFIntType2	R/W	GPIOFIntType2	0x00
0x8084_0054	Reserved, Read undefined	Write Only	GPIOFEOI	0x00
0x8084_0058	GPIOFIntEn	R/W	GPIOFIntEn	0x00
0x8084_005C	IntStsF	Read only	-	0x00
0x8084_0060	RawIntStsF	Read only	-	Note 3
0x8084_0064	GPIOFDB	R/W	GPIOFDB	0x00
0x8084_0090	GPIOAIntType1	R/W	GPIOAIntType1	0x00
0x8084_0094	GPIOAIntType2	R/W	GPIOAIntType2	0x00
0x8084_0098	-	Write Only	GPIOAEOI	-
0x8084_009C	GPIOAIntEn	R/W	GPIOAIntEn	0x00
0x8084_00A0	IntStsA	Read only	-	0x00
0x8084_00A4	RawIntStsA	Read only	-	Note 3
0x8084_00A8	GPIOADB	R/W	GPIOADB	0x00
0x8084_00AC	GPIOBIntType1	R/W	GPIOBIntType1	0x00
0x8084_00B0	GPIOBIntType2	R/W	GPIOBIntType2	0x00
0x8084_00B4	-	Write Only	GPIOBEOI	-
0x8084_00B8	GPIOBIntEn	R/W	GPIOBIntEn	0x00
0x8084_00BC	IntStsB	Read only	-	0x00
0x8084_00C0	RawIntStsB	Read only	-	Note 3
0x8084_00C4	GPIOBDB	R/W	GPIOBDB	0x00
0x8084_00C8	EEDrive	R/W	EEDrive	0x00

Note: 1 - A read from the data register returns the value of the GPIO module input port. These ports have a default pin assignment. The read value default is the pin state based on the default pin map.

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Note: 2 - Port E bits 1 and 0 provide the LED driver function. The Port E[1:0] defaults to drive high. A read from the Port E data register would be expected to return 0x03, if the other pins mapped to Port E inputs are zero.

Note: 3 - The RAWSTATUSx registers have pin dependent default read states. The interrupt control registers default to low level sensitive interrupt on reset. Therefore the external pin state will ripple through the interrupt logic to determine the RAWSTATUSx default.

Register Descriptions

PADR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PADATA							

Address:

PADR: 0x8084_0000 - Read/Write

Definition:

Port A Data Register. Values written to this read/write register will be output on port A pins if the corresponding data direction bits are set HIGH (port output). Values read from this register reflect the external state of Port A inputs. All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PADATA: Port A 8-bit data.

PBDR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PBDATA							

Address:

PBDR: 0x8084_0004 - Read/Write

Definition:

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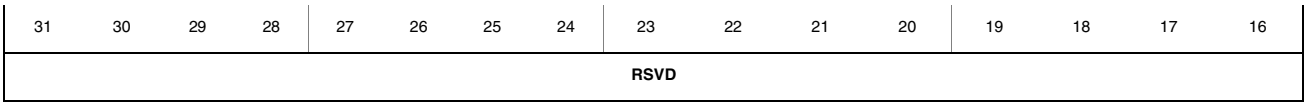
Port B Data Register. Values written to this read/write register will be output on port B pins if the corresponding data direction bits are set HIGH (port output). Values read from this register reflect the external state of Port B inputs. All bits are cleared by a system reset.

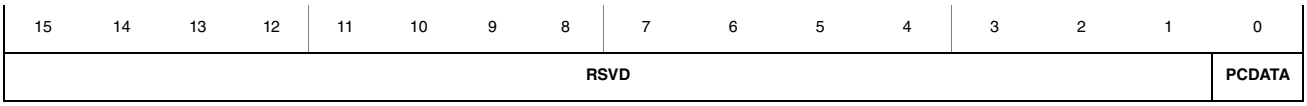
Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PBDATA: Port B 8-bit data.

PCDR





Address:

PCDR: 0x8084_0008 - Read/Write

Definition:

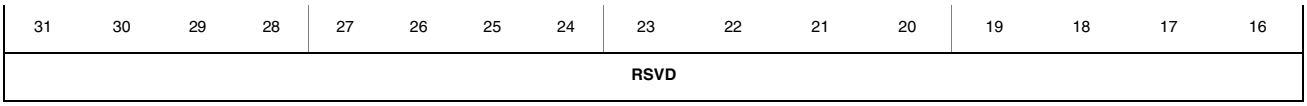
Port C Data Register. Values written to this read/write register will be output on port C pins if the corresponding data direction bits are set HIGH (port output). Values read from this register reflect the external state of Port C inputs. All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PCDATA: Port C 1-bit data.

PEDR



Address:

PEDR: 0x8084_0020 - Read/Write

Definition:

Port E Data Register. Values written to this read/write register will be output on port E pins if the corresponding data direction bits are set HIGH (port output).

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Values read from this register reflect the external state of Port E inputs. All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PEDATA: Port E 2-bit data.

PFDR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														PFDATA	

Address:

PFDR: 0x8084_0030 - Read/Write

Definition:

Port F Data Register. Values written to this read/write register will be output on port F pins if the corresponding data direction bits are set HIGH (port output). Values read from this register reflect the external state of Port F inputs. All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PFDATA: Port F 3-bit data.

PGDR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															PGDATA

Address:

PGDR: 0x8084_0038 - Read/Write

Definition:

Port G Data Register. Values written to this read/write register will be output on port G pins if the corresponding data direction bits are set HIGH (port output). Values read from this register reflect the external state of Port G inputs. All bits are cleared by a system reset.

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Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PGDATA: Port G 2-bit data.

PHDR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												PHDATA			

Address:

PHDR: 0x8084_0040 - Read/Write

Definition:

Port H Data Register. Values written to this read/write register will be output on port H pins if the corresponding data direction bits are set HIGH (port output). Values read from this register reflect the external state of Port H inputs. All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PHDATA: Port H 4-bit data.

PADDR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PADIR							

Address:

PADDR: 0x8084_0010 - Read/Write

Definition:

Port A Data Direction Register. Bits cleared in this read/write register will select the corresponding pin in port A to become an input, setting a bit sets the pin to output. All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

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PADIR: Port A direction bits.

PBDDR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PBDIR							

Address:

PBDDR: 0x8084_0014 - Read/Write

Definition:

Port B Data Direction Register. Bits cleared in this read/write register will select the corresponding pin in port B to become an input, setting a bit sets the pin to output. All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PBDIR: Port B direction bits.

PCDDR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															PCDIR

Address:

PCDDR: 0x8084_0018 - Read/Write

Definition:

Port C Data Direction Register. Bits cleared in this read/write register will select the corresponding pin in port C to become an input, setting a bit sets the pin to output. All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PBDIR: Port B direction bits.

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PEDDR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														PEDIR	

Address:

PEDDR: 0x8084_0024 - Read/Write

Definition:

Port E Data Direction Register. Bits cleared in this read/write register will select the corresponding pin in port E to become an input, setting a bit sets the pin to output. All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PEDIR: Port E direction bits.

PFDDR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														PFDIR	

Address:

PFDDR: 0x8084_0034 - Read/Write

Definition:

Port F Data Direction Register. Bits cleared in this read/write register will select the corresponding pin in port F to become an input, setting a bit sets the pin to output. All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PFDIR: Port F direction bits.

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PGDDR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD															PGDIR

Address:

PGDDR: 0x8084_003C - Read/Write

Definition:

Port G Data Direction Register. Bits cleared in this read/write register will select the corresponding pin in port G to become an input, setting a bit sets the pin to output. All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PGDIR: Port G direction bits.

PHDDR

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD												PHDIR			

Address:

PHDDR: 0x8084_0044 - Read/Write

Definition:

Port H Data Direction Register. Bits cleared in this read/write register will select the corresponding pin in port H to become an input, setting a bit sets the pin to output. All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PHDIR: Port H direction bits.

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GPIOAIntEn

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PAINT							

Address:

GPIOAIntEn: 0x8084_009C - Read/Write

Definition:

The GPIO Interrupt Enable register controls which bits of port A are to be configured as interrupts. A “1” written to a bit in this register will configure the bit on port A to become an interrupt. The user must make sure that the direction of port A is set to input (PADDR defaults to input on reset). Writing a “0” (default on reset) to a bit in the register will configure that bit on port A as a normal GPIO port and the interrupt output corresponding to that bit will be zeroed. The user can read the inputs on port A in either mode via the PADR.

The interrupt type is controlled by the GPIOAINTTYPE1/2 registers described in the following sections.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PAINT: Port A interrupt enables.

GPIOBIntEn

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PBINT							

Address:

GPIOBIntEn: 0x8084_00B8 - Read/Write

Definition:

The GPIO Interrupt Enable register controls which bits of port B are to be configured as interrupts. A “1” written to a bit in this register will configure the bit on port B to become an interrupt. The user must make sure that the direction of port B is set to input (PBDDR defaults to input on reset). Writing a “0” (default on reset) to a bit in the register will configure that bit on port B as a

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normal GPIO port and the interrupt output corresponding to that bit will be zeroed. The user can read the inputs on port B in either mode via the PBDR.

The interrupt type is controlled by the GPIOBINTTYPE1/2 registers described in the following sections.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PBINT: Port B interrupt enables.

GPIOFIntEn

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													PFINT		

Address:

GPIOFIntEn: 0x8084_0058 - Read/Write

Definition:

The GPIO Interrupt Enable register controls which bits of portF are to be configured as interrupts. A “1” written to a bit in this register will configure the bit on port F to become an interrupt. The user must make sure that the direction of port F is set to input (PFDDR defaults to input on reset). Writing a “0” (default on reset) to a bit in the register will configure that bit on port F as a normal GPIO port and the interrupt output corresponding to that bit will be zeroed. The user can read the inputs on port F in either mode via the PFDR.

The interrupt type is controlled by the GPIOFINTTYPE1/2 registers described in the following sections.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PFINT: Port F interrupt enables.

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GPIOAIntType1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PAINTE							

Address:

GPIOAIntType1: 0x8084_0090 - Read/Write

Definition:

The INTTYPE1 register controls what type of INTERRUPT can occur on Port A. Level sensitive when “0” is written to a bit location (“0” default on reset), edge sensitive when “1” is written to a bit location (the type of edge/level is controlled by the INTTYPE2 register). The user must make sure that the direction of port A is set to input and the corresponding bit in the GPIO INTERRUPT ENABLE register is set to allow the interrupt.
All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PAINTE: Determines which type of interrupt may occur.

GPIOBIntType1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PBINTE							

Address:

GPIOBIntType1: 0x8084_00AC - Read/Write

Definition:

The INTTYPE1 register controls what type of INTERRUPT can occur on Port B. Level sensitive when “0” is written to a bit location (“0” default on reset), edge sensitive when “1” is written to a bit location (the type of edge/level is controlled by the INTTYPE2 register). The user must make sure that the direction of port B is set to input and the corresponding bit in the GPIO INTERRUPT ENABLE register is set to allow the interrupt.

All bits are cleared by a system reset.

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Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PBINTE: Determines which type of interrupt may occur.

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GPIOFIntType1

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														PFINTE	

Address:

GPIOFIntType1: 0x8084_004C - Read/Write

Definition:

The INTTYPE1 register controls what type of INTERRUPT can occur on Port F. Level sensitive when “0” is written to a bit location (“0” default on reset), edge sensitive when “1” is written to a bit location (the type of edge/level is controlled by the INTTYPE2 register). The user must make sure that the direction of port F is set to input and the corresponding bit in the GPIO INTERRUPT ENABLE register is set to allow the interrupt.
All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PFINTE: Determines which type of interrupt may occur.

GPIOAIntType2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PAINTR							

Address:

GPIOAIntType2: 0x8084_0094 - Read/Write

Definition:

The GPIOAINTTYPE2 registers controls the type of edge/level sensitive interrupt that can occur on the bits in Ports A.

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The interrupt is rising edge or high level sensitive if a “1” is written to the corresponding bit in GPIOAINTTYPE2 and falling edge or low level sensitive if a “0” is written to the corresponding bit in GPIOAINTTYPE2. The user must make sure that the direction of port A is set to input and the corresponding bits in the GPIO Interrupt Enable register and GPIOAINTTYPE1 are set correctly in order for this register to have any effect. For edge sensitive interrupts the GPIOAINTTYPE1 bit should set high and low for level sensitive interrupts.

All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PAINTR: Determines which type of edge or level sensitive interrupt may occur.

GPIOBIntType2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PBINTR							

Address:

GPIOBIntType2: 0x8084_00B0 - Read/Write

Definition:

The GPIOBINTTYPE2 registers controls the type of edge/level sensitive interrupt that can occur on the bits in Ports B.

The interrupt is rising edge or high level sensitive if a “1” is written to the corresponding bit in GPIOBINTTYPE2 and falling edge or low level sensitive if a “0” is written to the corresponding bit in GPIOBINTTYPE2. The user must make sure that the direction of port B is set to input and the corresponding bits in the GPIO Interrupt Enable register and GPIOBINTTYPE1 are set correctly in order for this register to have any effect. For edge sensitive interrupts the GPIOBINTTYPE1 bit should set high and low for level sensitive interrupts.

All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PBINTR: Determines which type of edge or level sensitive interrupt may occur.

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GPIOFIntType2

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														PFINTR	

Address:

GPIOFIntType2: 0x8084_0050 - Read/Write

Definition:

The GPIOFINTTYPE2 registers controls the type of edge/level sensitive interrupt that can occur on the bits in Ports F.

The interrupt is rising edge or high level sensitive if a “1” is written to the corresponding bit in GPIOFINTTYPE2 and falling edge or low level sensitive if a “0” is written to the corresponding bit in GPIOFINTTYPE2. The user must make sure that the direction of port F is set to input and the corresponding bits in the GPIO Interrupt Enable register and GPIOFINTTYPE1 are set correctly in order for this register to have any effect. For edge sensitive interrupts the GPIOFINTTYPE1 bit should set high and low for level sensitive interrupts.

All bits are cleared by a system reset.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PFINTR: Determines which type of edge or level sensitive interrupt may occur.

GPIOAEOI

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PAINTC							

Address:

GPIOAEOI: 0x8084_0098 - Write Only

Definition:

In order to clear an edge sensitive interrupt that can occur over port A, the user must write a data value of “1” to the corresponding bit in the GPIOAEOI

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register bit. The user must clear an interrupt before changing port A from interrupt mode to GPIO mode as the interrupts are cleared once this change has occurred. Once an interrupt has occurred and the interrupt service routine has started, one of the first instructions should be a write to this location in order to clear the interrupt so that subsequent interrupts on the same line are not missed.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PAINTC: Clears Interrupts

GPIOBEOI

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PBINTC							

Address:

GPIOBEOI: 0x8084_00B4 - Write Only

Definition:

In order to clear an edge sensitive interrupt that can occur over port B, the user must write a data value of “1” to the corresponding bit in the GPIOBEOI register bit. The user must clear an interrupt before changing Port B from interrupt mode to GPIO mode as the interrupts are cleared once this change has occurred. Once an interrupt has occurred and the interrupt service routine has started, one of the first instructions should be a write to this location in order to clear the interrupt so that subsequent interrupts on the same line are not missed.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PBINTC: Clears Interrupts

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GPIOFEOI

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														PFINTC	

Address:

GPIOFEOI: 0x8084_0054 - Write Only

Definition:

In order to clear an edge sensitive interrupt that can occur over port F, the user must write a data value of “1” to the corresponding bit in the GPIOFEOI register bit. The user must clear an interrupt before changing Port F from interrupt mode to GPIO mode as the interrupts are cleared once this change has occurred. Once an interrupt has occurred and the interrupt service routine has started, one of the first instructions should be a write to this location in order to clear the interrupt so that subsequent interrupts on the same line are not missed.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PFINTC: Clears Interrupts

GPIOADB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PAINTDB							

Address:

GPIOADB: 0x8084_00A8 - Read/Write

Definition:

For each port, if interrupts are enabled, it is possible to debounce the input signal. Setting a bit in this register enables debouncing for the corresponding interrupt signal; clearing the bit disables debouncing. Debouncing is implemented by passing the input signal through a 2-bit shift register clocked by a 128 Hz clock.

Bit Descriptions:

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RSVD: Reserved. Unknown During Read.

PAINTDB: Interrupt debounce enable.

GPIOBDB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PBINTDB							

Address:

GPIOBDB: 0x8084_00C4 - Read/Write

Definition:

For each port, if interrupts are enabled, it is possible to debounce the input signal. Setting a bit in this register enables debouncing for the corresponding interrupt signal; clearing the bit disables debouncing. Debouncing is implemented by passing the input signal through a 2-bit shift register clocked by a 128 Hz clock.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PBINTDB: Interrupt debounce enable.

GPIOFDB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													PFINTDB		

Address:

GPIOFDB: 0x8084_0064 - Read/Write

Definition:

For each port, if interrupts are enabled, it is possible to debounce the input signal. Setting a bit in this register enables debouncing for the corresponding interrupt signal; clearing the bit disables debouncing. Debouncing is implemented by passing the input signal through a 2-bit shift register clocked by a 128 Hz clock.

Bit Descriptions:

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RSVD: Reserved. Unknown During Read.

PFINTDB: Interrupt debounce enable.

RawIntStsA

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PAINTRS							

Address:

RawIntStsA: 0x8084_00A4 - Read Only

Definition:

Each bit in the register reports whether an interrupt would be signalled if the interrupt were enabled for the corresponding port; a set bit indicates that an interrupt would be signalled. The value reported is unaffected by whether interrupts are enabled or disabled. How a bit is set depends on the interrupt type. If the interrupt is level sensitive active high, it reflects the pin value. If level sensitive active low, it reflects the inverse of the pin value. If the interrupt is edge triggered, the bit latches a one whenever the proper level change occurs. How a bit is cleared also depends on the interrupt type. When an interrupt is level sensitive, it is cleared when not asserted. When edge triggered, it is cleared by writing the corresponding bit in GPIOAEOI. Note that the value of a bit is a debounced value if debouncing is enabled.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PAINTRS: Raw Interrupt Status.

RawIntStsB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PBINTRS							

Address:

RawIntStsB: 0x8084_00C0 - Read Only

Definition:

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Each bit in the register reports whether an interrupt would be signalled if the interrupt were enabled for the corresponding port; a set bit indicates that an interrupt would be signalled. The value reported is unaffected by whether interrupts are enabled or disabled. How a bit is set depends on the interrupt type. If the interrupt is level sensitive active high, it reflects the pin value. If level sensitive active low, it reflects the inverse of the pin value. If the interrupt is edge triggered, the bit latches a one whenever the proper level change occurs. How a bit is cleared also depends on the interrupt type. When an interrupt is level sensitive, it is cleared when not asserted. When edge triggered, it is cleared by writing the corresponding bit in GPIOBEOI. Note that the value of a bit is a debounced value if debouncing is enabled.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PBINTRS: Raw Interrupt Status.

RawIntStsF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD													PFINTRS		

Address:

RawIntStsF: 0x8084_0060 - Read Only

Definition:

Each bit in the register reports whether an interrupt would be signalled if the interrupt were enabled for the corresponding port; a set bit indicates that an interrupt would be signalled. The value reported is unaffected by whether interrupts are enabled or disabled. How a bit is set depends on the interrupt type. If the interrupt is level sensitive active high, it reflects the pin value. If level sensitive active low, it reflects the inverse of the pin value. If the interrupt is edge triggered, the bit latches a one whenever the proper level change occurs. How a bit is cleared also depends on the interrupt type. When an interrupt is level sensitive, it is cleared when not asserted. When edge triggered, it is cleared by writing the corresponding bit in GPIOFEOI. Note that the value of a bit is a debounced value if debouncing is enabled.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PFINTRS: Raw Interrupt Status.

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IntStsA

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PAINTS							

Address:

IntStsA: 0x8084_00A0 - Read Only

Definition:

For each port, this register reports the same value as the RawIntStsA register for each bit whose corresponding interrupt is enabled. Bits whose corresponding interrupt is not enabled report “0”.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PAINTS: Masked Interrupt Status.

IntStsB

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PBINTS							

Address:

IntStsB: 0x8084_00BC - Read Only

Definition:

For each port, this register reports the same value as the RawIntStsB register for each bit whose corresponding interrupt is enabled. Bits whose corresponding interrupt is not enabled report “0”.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PBINTS: Masked Interrupt Status.

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IntStsF

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														PFINTS	

Address:

IntStsF: 0x8084_005C - Read Only

Definition:

For each port, this register reports the same value as the RawIntStsF register for each bit whose corresponding interrupt is enabled. Bits whose corresponding interrupt is not enabled report “0”.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PFINTS: Masked Interrupt Status.

EEDrive

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD														DATOD	CLKOD

Address:

0x8084_00C8 - Read/Write

Definition:

EEPROM interface pin drive type control. Defines the driver type for the **EECLK** and **EEDAT** pins. When set, the corresponding pin is open drain, so that the pin will require an external pullup. When clear, the corresponding pin is a normal CMOS driver. DATOD controls the **EEDAT** pin. CLKOD controls the **EECLK** pin.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

DATOD: Defines the EEDAT pin output driver.

CLKOD: Defines the EECLK pin output driver.

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Chapter 22

Security

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22.1 Introduction

Security is a generalized architecture consisting of Boot ROM, laser fuses and proprietary circuitry for secure hardware initialization. In the context of this environment, the chip supports multiple digital-rights-management content-protection from several security vendors, (such as Microsoft and InterTrust). It exceeds all the requirements set forth by the Secure Digital Music Initiative and allows for protection of object code as well as content.

22.2 Features

Key features include:

- 256 bits of laser fuse for permanent IDs and passwords.
- Security boot firmware and private passwords are “invisible” except when the IC is “locked”.
- Each instantiation of the system software may be uniquely encoded and protected using the private ID.
- Multiple security vendors can co-exist in the same system.
- JTAG functionality is disabled when security is enabled.
- External boot is disabled when security is enabled.

22.3 Contact Information

Contact Cirrus Logic at *www.cirrus.com* for additional information regarding security features.

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22.4 Registers

This section contains the detailed register descriptions for some registers in the Security block. Table 22-1 shows the address map for the registers in this block, followed by a detailed listing for each register.

Note: Most Security registers are not documented in this Guide. Please contact Cirrus Logic at www.cirrus.com for additional information regarding security features.

Table 22-1: Security Register List

Address	Name	SW Locked	Type	Size	Description
0x8083_2714	ExtensionID	No	R	32	PartID for EP93XX devices

Register Descriptions

ExtensionID

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
RSVD															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
RSVD								PartID							RSVD

Address:

0x8083_2714 - Read Only

Definition:

This register contains the PartID for EP93XX devices.

Bit Descriptions:

RSVD: Reserved. Unknown During Read.

PartID: Identification number for each type of EP93XX device.
0x04 - EP9301

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Chapter 23

Glossary

Term	Definition
AC'97	Serial Audio data transmission standard
ADC	Analog to Digital Converter
AMBA	Advanced Micro-controller Bus Architecture
APB	Advanced Peripheral Bus
ARM920T	ARM9 processor is the main processor in EP9301. A general purpose processor.
ATAPI	AT Advanced Packet Interface
Buffer	A "buffer" refers to the area in system memory that is characterized by a buffer descriptor, that is, a start address and the length of the buffer in bytes.
CODEC	Coder/Decoder
CRC	Cyclic Redundancy Check
DAC	Digital to Analog Converter
DMA	Direct Memory Access
EEPROM	Electronically Erasable Programmable Read Only Memory
FIQ	Fast Interrupt Request
FIR	Fast Infrared
FLASH	FLASH memory
GPIO	General Purpose Input Output
HDLC	High-level Data Link Control
I2C	See I^2S
I^2S	Inter-IC Sound, also known as I2S
ICE	In-circuit Emulator
IDE	Integrated Drive Electronics
Ir or IR	Infrared
IrDA	Infrared Data Association
IRQ	Standard Interrupt Request
ISO	International Standards Organization
JTAG	Joint Test Action Group
LCDDAC	Liquid Crystal Display Digital to Analog Converter
LED	Light Emitting Diode
MAC	Media Access Controller - Ethernet
MII	Media Independent Interface
MIR	Medium Infrared
MMU	Memory Management Unit

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Term	Definition
OHCI	Open Host Controller Interface
PHY	Physical layer
PIO	Programmed I/O
PLL	Phase Locked Loop
PPM	Pulse Position Modulation
RISC	Reduced Instruction Set Computer
RTC	The ARM Real Time Clock
RTL	Register Transfer Level
RTZ	Return-to-zero
RZI	Return-to-zero Inverted
SDLC	Synchronous Data Link Control
SDMI	Secure Digital Music Initiative
SDRAM	Synchronous Dynamic Random Access Memory
SIR	Slow Infrared
SPI	Serial Peripheral Interface. Also known as SSP, Synchronous Serial Peripheral, supporting the Motorola SPI format.
SRAM	Static Random Access Memory
SSP	Synchronous Serial Peripheral. Also known as SPI, Serial Peripheral Interface, supporting the Motorola format.
Syscon	System control registers
TFT	Thin Film Transistor
TLB	Translation Lookaside Buffer
TTB	Translation Table Base
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VIC	Vectored Interrupt Controller
Watchdog	A count down timer designed to restart the processor if the processor hangs.

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