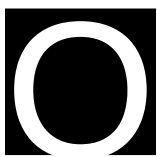


IC Supports Primary-Side Power Monitoring

By Dave Cooper, Application Manager,
Potentia Semiconductor, Ottawa, Canada

In mission-critical applications with isolated dc-dc converters, monitoring conditions on the 48-V power bus can significantly improve system performance by detecting latent faults before they cause system outages.



Over the past few years, many system designs have migrated to a distributed power architecture to support the requirements for high power and very low voltage at the integrated circuits (ICs). A relatively high voltage is distributed through the backplane or motherboard, and each of the cards in the system includes dc-dc converters to reduce the backplane voltage to the low voltages needed by the ICs.

Some systems use 12 V or 5 V as the backplane voltage, but as equipment power levels continue to increase, the high backplane currents become difficult to manage. Consequently, most large systems distribute a higher voltage to reduce current and improve power efficiency. The telecom standard of 48 V has been adopted in a wide range of applications such as compute servers, industrial products and military systems.

One significant consequence of using the higher backplane voltage is that each card must provide isolation between the primary side (the 48-V input) and the sec-

ondary side, both for safety and to avoid unwanted ground current paths. A recently developed control IC allows designers to manage the primary-side power functions while maintaining the required isolation. The circuit design techniques required for the primary-side controller involve a selection of a variety of external components.

Card Power System

Card power systems usually are implemented using standard dc-dc converter modules, available from many suppliers as isolated bricks or nonisolated point-of-load converters (POLs). Fig. 1 shows a simple block diagram for a typical card power system with four low-voltage output rails.

In this example, an isolated brick generates an intermediate voltage, with POL converters producing the low-voltage outputs. This configuration is known as intermediate bus architecture (IBA) and is one of several power architectures widely used today.

Fig. 1 also shows power monitoring and control functions that are not provided by the dc-dc converters themselves. These functions include startup and shutdown sequencing, fault handling and voltage adjustment for margining and trimming. Through a monitoring interface, the system processor is able to read power system status in real time and can initiate margining on demand.

The power management functions described apply only to the secondary side of the power system. Output voltage measurement, trimming and fault handling for the POL converters all can be achieved without any primary-side connections. However, in mission-critical high-availability applications, primary-side monitoring significantly can improve system

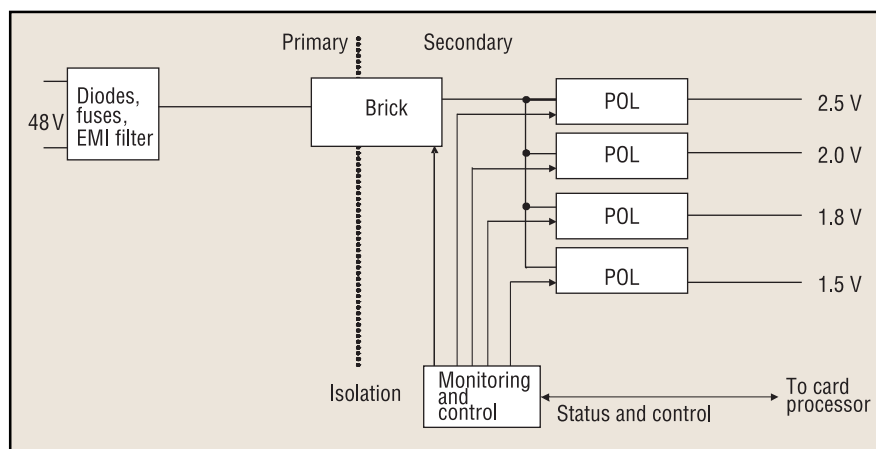


Fig. 1. Card power system.

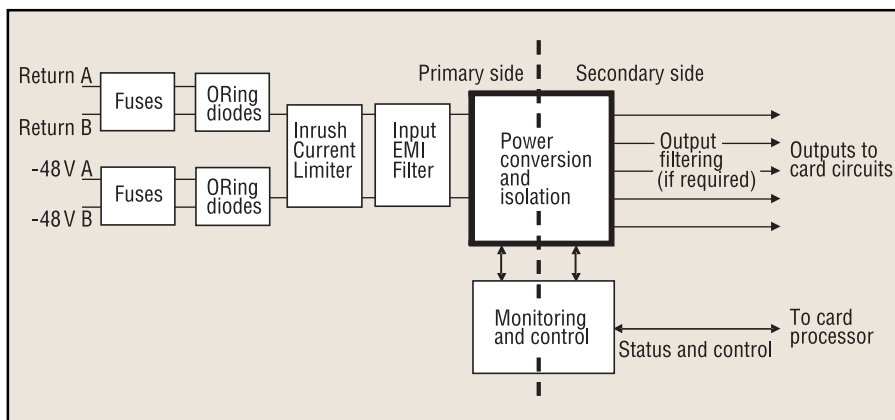


Fig. 2. Primary-side functions.

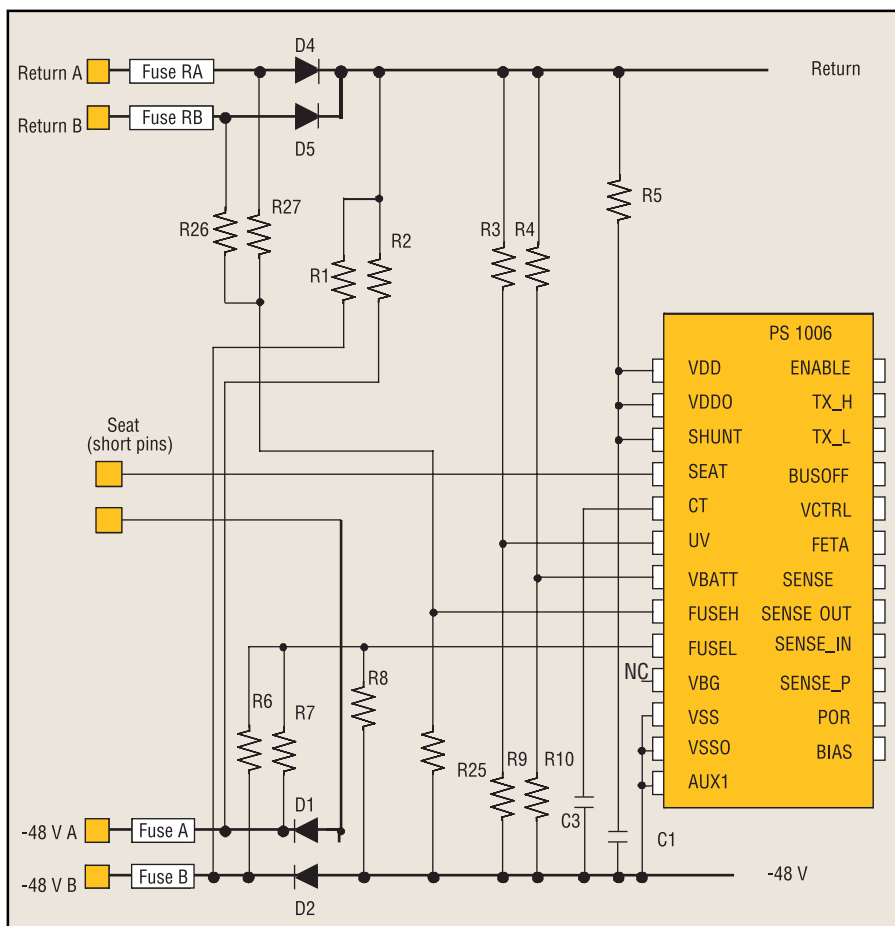


Fig. 3. Primary-side voltage and fuse monitor.

performance by detecting latent faults before they cause system outages.

Fig. 2 shows the primary-side functions of the card power system in more detail for a high-availability application where duplicated 48-V feeds are used to provide redundancy. Fuses are needed at the power input pins to meet safety requirements. Diodes are used to provide an OR function between the redundant power

feeds. The inrush current limiter prevents current surges during hot-swap of the card and also can function as an electronic circuit breaker to provide overcurrent (OC) protection.

Primary-side monitoring functions include card seating detection; measurement of input voltage and input current; detection of overvoltage (OV), undervoltage (UV) or OC conditions; fuse failure detection; and

inrush limiter status. As indicated in Fig. 2, the monitoring and control function must now include isolation to allow reporting of primary-side status information through the secondary-side interface.

While some of the primary monitoring functions can be achieved using discrete components, comprehensive monitoring is best achieved using a dedicated primary monitor IC. Integration allows improved performance, simplifies design and reduces component count. The PS-1006 from Potentia Semiconductor provides full primary-side monitoring and achieves primary-secondary isolation using a small, inexpensive transformer to communicate with the secondary-side controller. The communication uses a proprietary protocol referred to as the PI-Link™ interface.

Fig. 3 shows how the PS-1006 is connected to measure input voltage, detect primary-side OV and UV conditions, and monitor the input fuses. Fig. 4 depicts how the PS-1006 connects to the intermediate bus brick and how it controls inrush current. It also depicts the communication link to the secondary-side controller, in this example using the Potentia PS-2406.

Monitoring Circuit Description

The PS-1006 measures input voltage using an internal 10-bit ADC at the VBATT pin, through the voltage divider R4 and R10 (see Figs. 3 and 4). The measured value is transmitted to the secondary-side controller through the PI-Link interface and is accessible through the I²C interface of the PS-2406.

The voltage at the VBATT pin is compared to an internal 2.38-V reference to provide OV detection. If an OV condition is detected, the information is transmitted to the secondary-side controller via the PI-Link interface.

When selecting R4 and R10, choose values that will give 2.38 V at VBATT at the desired OV threshold. For example, if R10 = 9.42 kΩ and

$R4 = 301 \text{ k}\Omega$, the OV threshold is $2.38 \times 310.42/9.42 = 78.42 \text{ V}$. Remember that the voltage at the card input will be approximately 1.5 V higher because of the drop in the two ORing diodes and the input fuses.

Voltage divider resistors R3 and R9 connect to the UV pin of the PS-1006. The voltage at the UV pin is compared to an internal 1.25-V reference to provide UV detection. An internal 10- μA current source is switched in when UV is detected to provide hysteresis. If a UV condition is detected, the intermediate bus brick is shut down via an optocoupler. The optocoupler is necessary because the brick is on the other side of the EMI filter, and there can be a significant voltage drop across the filter under transient conditions.

The UV pin also is compared to a slightly higher internal reference of 1.31 V. This comparator is used to detect a brownout condition, as a warning that the input voltage is low before the brick shutdown occurs. If a brownout is detected, the information is transmitted to the secondary-side controller via the PI-Link interface.

Choose values for R3 and R9 that will give 1.25 V at the UV pin at the desired UV shutdown threshold. For example, if $R9 = 10.5 \text{ k}\Omega$ and $R3 = 301 \text{ k}\Omega$, the UV shutdown threshold is $1.25 \times 311.5/10.5 = 37.08 \text{ V}$. Also, choose the value of R3 to give the required hysteresis between UV shutdown and recovery.

Because the hysteresis current is 10 μA , the value of 301 $\text{k}\Omega$ results in a hysteresis of 3 V, and the power system will restart at an input voltage of 40.08 V. Again, remember the voltage at the card input will be approximately 1.5 V higher because of the drop in the two ORing diodes and the input fuses.

The PS-1006 has two pins for monitoring the input fuses, FUSEH and FUSEL. Pin FUSEH monitors the high-side fuses (in the battery return input) via resistor network R25, R26 and R27. The voltage at pin FUSEH is compared against the voltage at pin VBATT, and if it is lower than 57% of

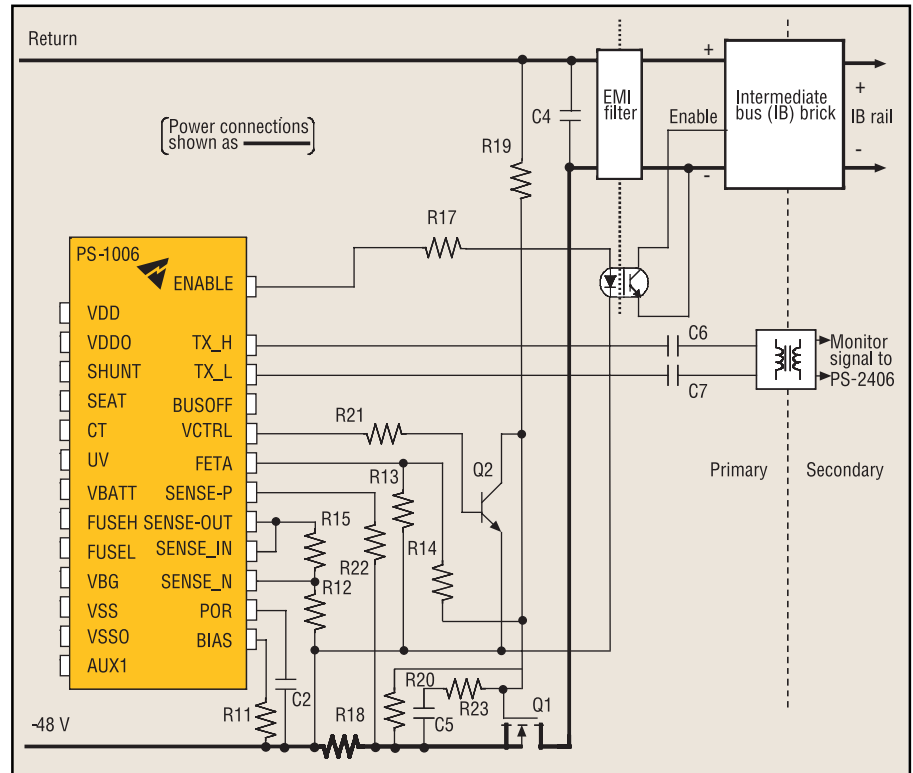


Fig. 4. Inrush limiter, brick control and communication.

VBATT, a fuse failure is detected.

Pin FUSEL monitors the low-side fuses (in the -48-V feeds) via resistor network R1, R2, R6, R7 and R8. The voltage at pin FUSEL is compared against the voltage at pin VBATT, and if it is higher than 57% of VBATT, a fuse failure is detected. When any fuse failure is detected, the information is transmitted to the secondary-side controller via the PI-Link interface.

Resistor values must be chosen to guarantee the circuit correctly detects a fuse failure even when the voltage at the two feeds is not equal. Using the resistor values recommended in the table, the circuit will correctly detect fuse failures even if one feed is at 36 V and the other feed is at 75 V, an extreme worst-case condition.

Note the detection of a fuse failure can be affected if the ORing diodes

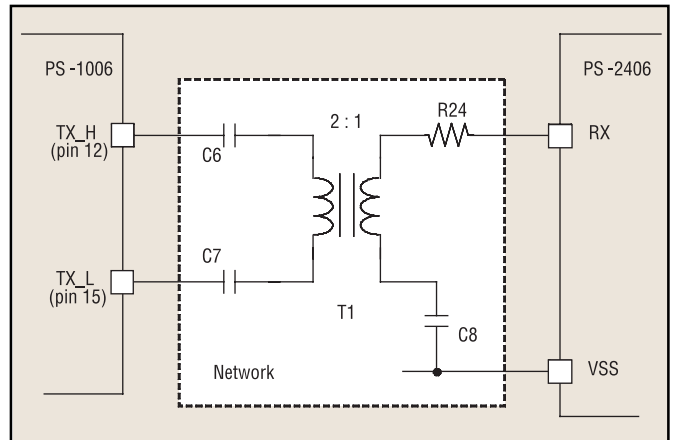


Fig. 5. Communication link components.

Resistor	Recommended Value (k Ω)
R1	100
R2	100
R6	301
R7	301
R8	9.09
R25	3.32
R26	301
R27	301

Table. Recommended fuse monitor resistors.

have a high leakage current. Because the normal current in the fuse-failure detection circuits is about 160 μA for

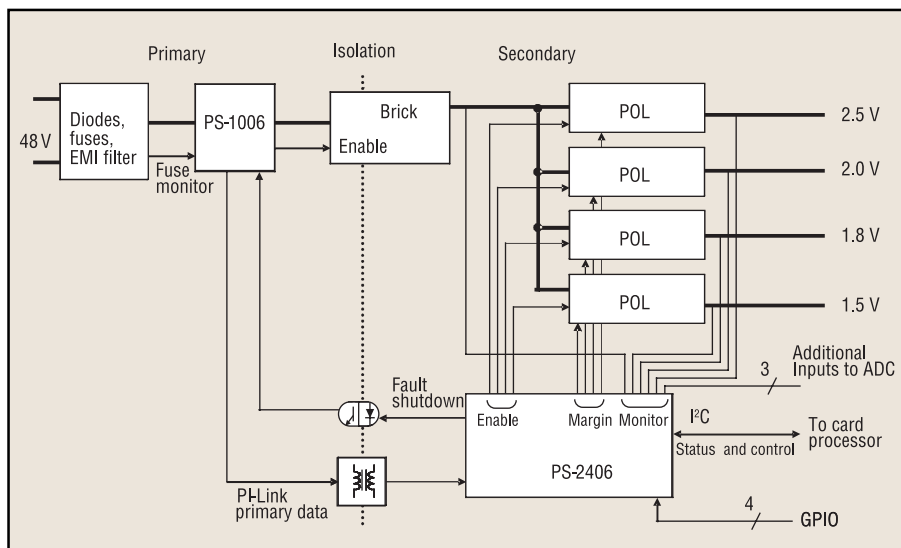


Fig. 6. Primary and secondary power management.

high-side fuses and 125 μ A for low-side fuses, select diodes with a leakage current less than 10 μ A.

Primary current is measured by current-sense resistor R18 (Fig. 4), using a current-sense amplifier in the PS-1006. R12 and R15 are used to set the gain of the amplifier and should be chosen so that the output of the current-sense amplifier is approximately 2 V at full load current. For ex-

ample, for a 200-W card, the maximum card current is 5 A at 40 V. If a value of 20 m Ω is used for R18, the current-sense voltage is 100 mV at 5 A. In this case, choose R15 = 47.5 k Ω and R12 = 2.49 k Ω to give an amplifier gain of 20.

The output of the current-sense amplifier is connected to the SENSE_IN pin of the PS-1006, where it is measured by the ADC. The measured value is transmitted to the secondary-side controller PS-2406 through the PI-Link interface, and is accessible through the I²C interface of the PS-2406.

The voltage at the SENSE_IN pin is compared to an internal 2.38-V reference to provide OC detection. If an OC condition is detected, the information is transmitted to the secondary-side

controller via the PI-Link interface. With the component values discussed in the example above, OC is detected at 5.95 A.

The PS-1006 can provide an electronic circuit breaker function if required. If it detects an OC condition, it turns off the MOSFET used for inrush current limiting. A time delay is included to prevent nuisance tripping.

Communication Link to Secondary

The isolated communication link uses a small transformer together with three capacitors and one resistor, as shown in Fig. 5. The recommended transformer is type ESMIT 4153A from Sumida, or equivalent. This transformer has a 2-to-1 winding ratio and must be connected, as shown in Fig. 5.

Capacitors C6 and C7 (100 nF) provide isolation to fully meet safety requirements of IEC 60950. Capacitor C8 (1 μ F) provides dc blocking and resistor R24 (1 k Ω) acts as a high-frequency filter in conjunction with the input pad input capacitance of the PS-2406.

The transformer itself meets the isolation (creepage and clearance) requirements for basic insulation according to IEC 60950 for input voltages up to 60 V nominal (75 Vdc maximum, 100 V transient).

To ensure the complete card meets these safety requirements, the intermediate bus brick and any optocouplers used for isolation must meet the same requirements. The PCB must maintain adequate spacing between primary and secondary. This is best achieved by using an isolation barrier in the PCB that is free of copper on all layers. The isolation barrier should be a minimum of 0.062 in., or preferably 0.1 in.

The main information transmitted over the PI-Link interface includes:

- DAC voltage measurements (real time)
- Input voltage (10-bit value)
- Input current (8-bit value)

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- Status information bits
- Fuse fault
- Input OV
- Input brownout
- Input OC.

Additional information also is transmitted such as SEAT pin status, input UV, inrush complete and auxiliary voltage measurement. All this information is available through the secondary-side I²C interface on the PS-2406. Along with implementing the primary-side monitoring functions, the PS-1006 controls the primary intermediate bus brick and provides inrush current limiting.

The PS-1006 controls the intermediate bus brick via its enable pin. When the input voltage is below the UV shutdown threshold, the enable pin is turned off. When the input voltage rises above the UV recovery threshold, the enable pin is turned on.

As an option, the PS-2406 can provide an additional shutdown function to protect against catastrophic faults in the secondary-side POLs. Such faults can occur in any power system using nonisolated POLs, because most of these converters use a buck topology in which the output voltage is controlled by varying the duty cycle of an upper and lower switching FET.

If the upper FET fails short-circuit, then the output voltage becomes equal to the input and cannot be controlled except by removing the input voltage. If one of these POLs

has an unrecoverable OV fault, the PS-2406 transmits a primary shutdown signal and the enable pin on the bus brick is immediately turned off.

The PS-1006 provides inrush current limiting for hot-swap applications, to control the surge current into the input capacitors at the instant of plug-in. The inrush limit MOSFET (Q1 in Fig. 4) is slowly turned on by the PS-1006, via the transistor Q2. When the input current rises to the current limit point set by R18, R12 and R15 (refer to the previous discussion of OC detection), the drive to Q2 is reduced to prevent the input current exceeding the limit value.

A time-out and retry capability is included to limit power dissipation in the MOSFET under overload conditions. In this way, the PS-1006 combines the functions of primary-current measurement, inrush current limiting and OC detection during normal operation.

In addition to the I²C and PI-Link interfaces, the PS-2406 provides full management of up to four POL dc-dc converters. Management functions include startup and shutdown sequencing control, output voltage monitoring, OV and UV protection, and voltage margin control. Fig. 6 shows the same power system as Fig. 1, but includes power management functions on both primary and secondary sides. All power system parameters and control functions are available through the secondary-side I²C interface.

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