Synchronization

WHY SYNCHRONIZATION?

In systems where more than one converter is required, synchronization should be used if it is available. It can reduce cost, space and conducted and radiated noise (EMI/RFI). A single low-pass filter will reduce cost and space when all converters operate at the same frequency. This also eliminates multi-frequency harmonics and subharmonics from the power bus (see Figures 6A & 6B for oscillograms of reflected ripple with and without synchronization). The design of the 15W series is based on a current mode PWM in a forward topology configuration. The oscillation frequency is set by a R_T-C_T network as is shown in Figures 1 and 2. The timing capacitor is connected to input power ground through a series resistor R ≈ 100Ω and the common point (node) of R-C_T is used for synchronization of multiple converters of the same input voltage range.

There are three methods to synchronize the 15W series converters:

1) single wire
2) capacitor coupling to external clock
3) direct drive of the SYNC input by an open drain MOSFET

NOTE: For any of the three sync methods to achieve reliable sync, each converter must have the same input voltage range and must have a minimum load of 20%.

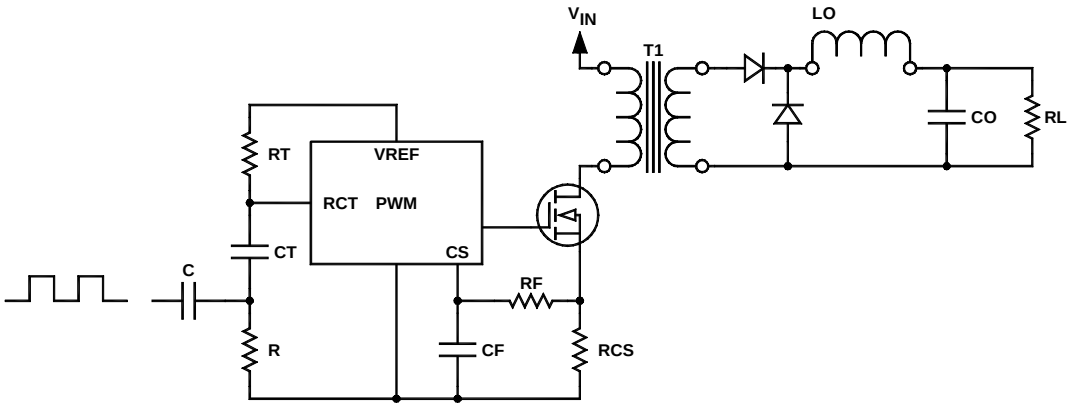


FIGURE 1

SINGLE WIRE SYNCHRONIZATION

Connecting all the SYNC pins by a single wire from unit to unit, the timing capacitors, C_T, of each converter is forced to share the same parallel combination of the series resistor, R (see Figure 1).

The injected current at the R-C_T node (SYNC pin) by any of the converter clocks appears as a voltage spike at the input R_T-C_T terminal of the PWM (see Figure 3). This voltage spike is observed on the timing capacitor C_T waveform and its positive edge triggers the internal circuitry of the PWM thus achieving synchronization. This single wire synchronization is reliable for up to 3 units due to the fact that the series resistor, R, becomes smaller and smaller as more units are connected in parallel, and the current through each C_T is relatively constant.

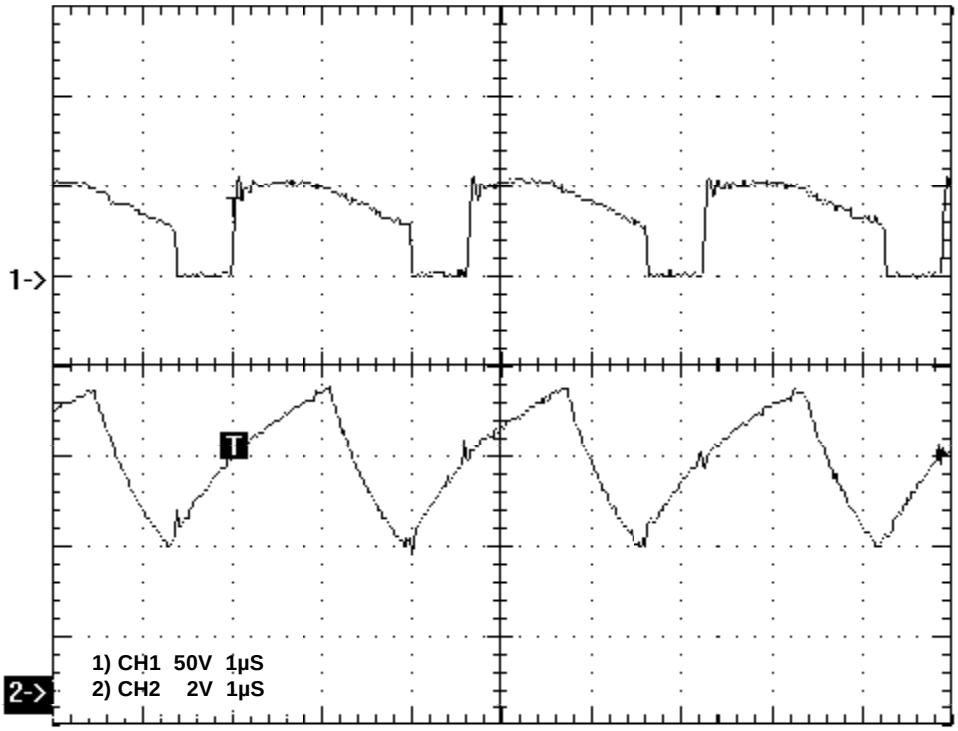


FIGURE 2. Typical V_{DS} and internal PWM clock

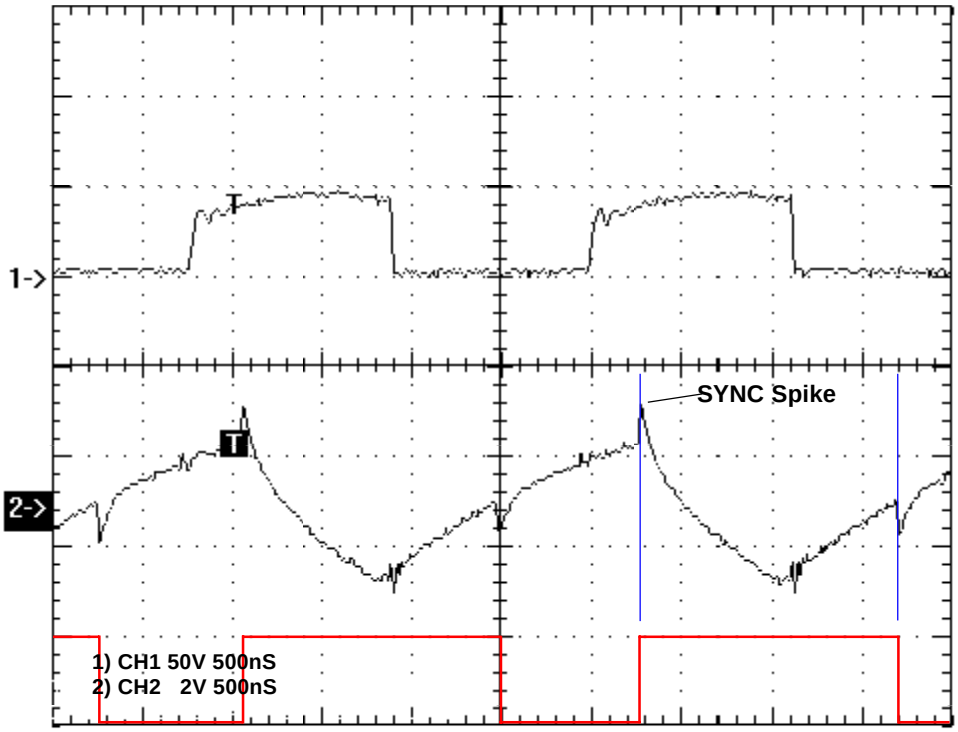
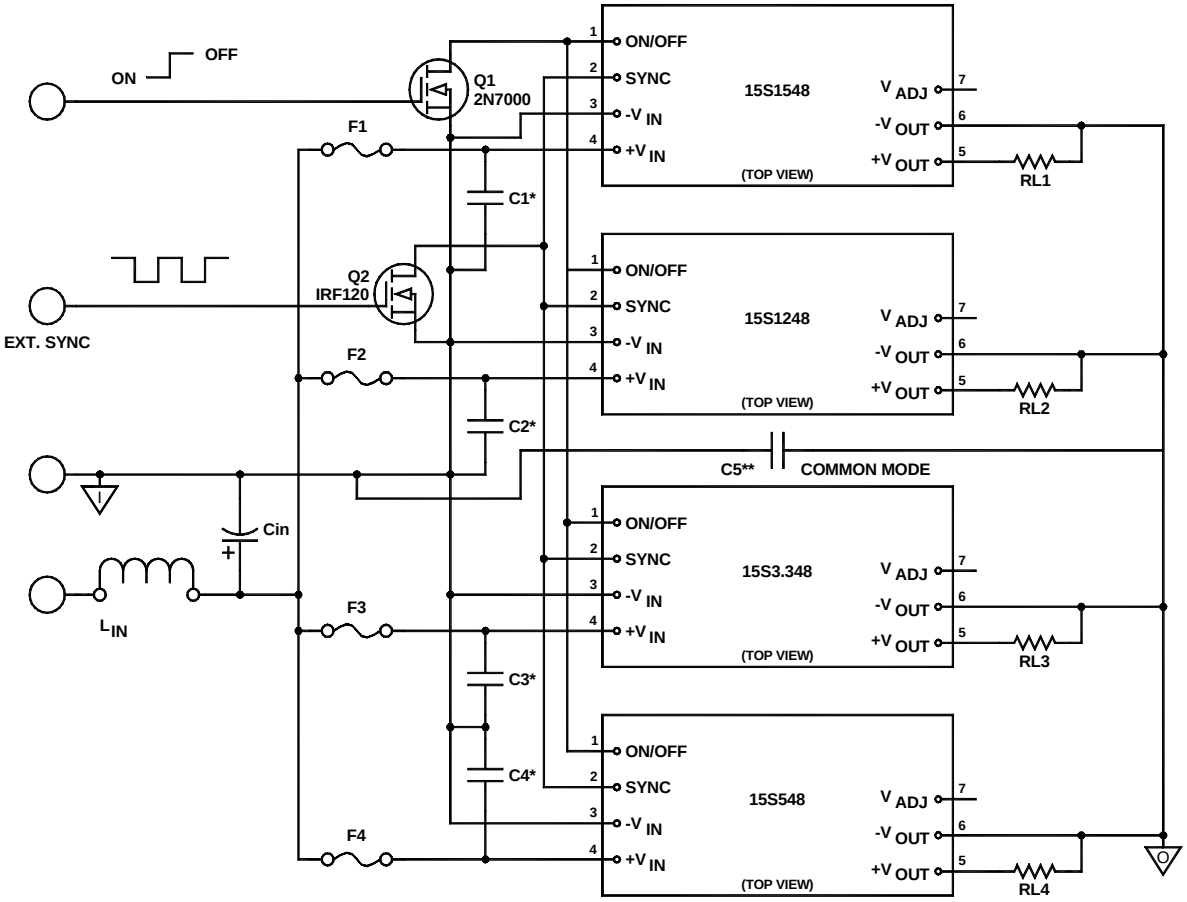


FIGURE 3. 15W V_{DS}, Clock with external sync

EXTERNAL SYNCHRONIZATION

When synchronization of the converters to a system clock is required, there are two methods available to the designer to achieve synchronization. Assuming a -48V bus is used for powering the converters and because the ON/OFF and the SYNC input of the converters are referenced to the -INPUT while the external clock is referenced to system ground, a capacitor can be used for isolation. Depending on the number of units in the system, a capacitor between 470pF and 0.01µF can be used. Again, all the SYNC input pins are connected together and the external clock is connected through the series-selected capacitor as is shown in the connection diagram found on the datasheet. Other isolation components such as small signal isolation transformers or high-speed opto-isolators can also be used, but they require more parts and space.



15W MULTIPLE CONVERTER EXTERNAL SYNCHRONIZATION
***C1, C2, C3 & C4: 1µF/100V CERAMICS TO BE INSTALLED AS CLOSE AS POSSIBLE TO PIN #3 & #4 OF EACH UNIT**
****CS: OPTIONAL COMMON-MODE NOISE FILTER CAPACITOR**

FIGURE 4. 15W multiple converter with external synchronization

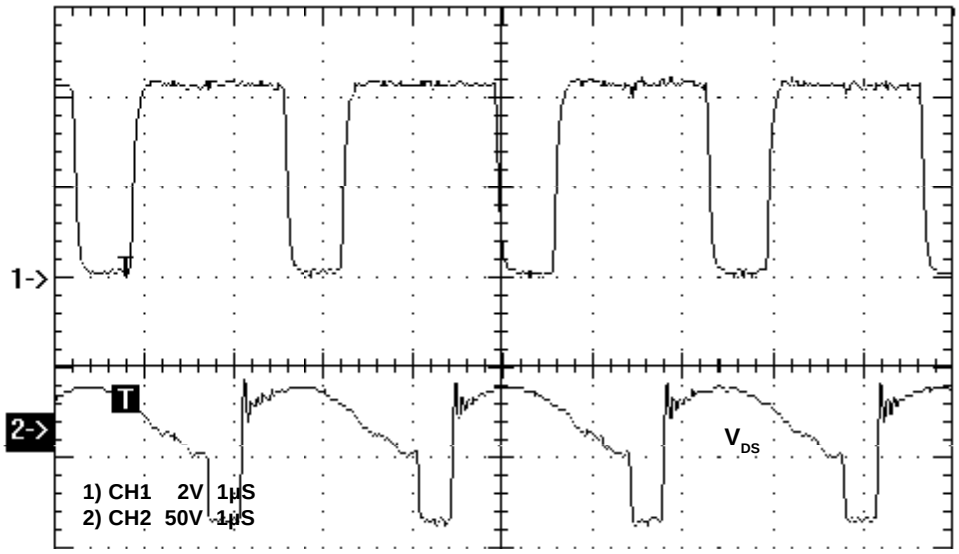
OPEN DRAIN EXTERNAL SYNCHRONIZATION

In Figure 4 a schematic of four different converters powered by a +48Vdc bus is given. All ON/OFF input pins and SYNC pins are connected together. The open drain IRF120 drives the SYNC input of the four converters forcing them to synchronize. Any transistor of RDS_{ON} < 0.5Ω can be used. The oscillograms given in Figure 5 were taken from different units under different loads, without L_{IN}-C_{IN}. Also note the effects synchronization has on the reflected ripple, as is shown in Figures 6A & 6B.

LAYOUT CONSIDERATIONS

For any power device or analog circuitry, the layout of the components is critical. One must avoid ground loops, bouncing ground, common-mode noise or any other noise which may be coupled to any input or output pin of a device. A ground plane and star ground connection will eliminate ground loops and a bouncing ground while bypassing common-mode noise from the input to output or to chassis ground will reduce system noise and improve performance.

The input fuses can be replaced or completely eliminated. But if a component failure occurs—such as a shorted input capacitor or transistor—and the PCB power run is thin, damage to the PCB or meltdown may occur. Even though the MTBF of the 15W series is over 1 million hours and all Beta Dyne converters are burned in for 48 hours, we cannot guarantee zero failures under all conceivable applications or forms of handling.



IRF120 Gate Signal

FIGURE 5A. 15S15/48

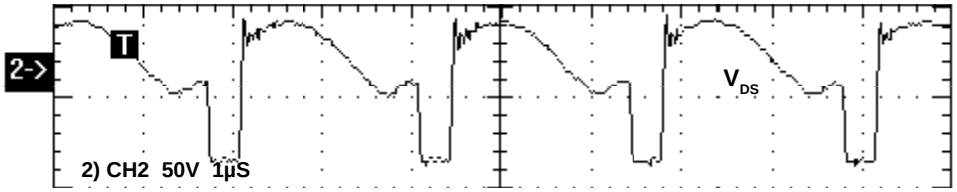


FIGURE 5B. 15S12/48

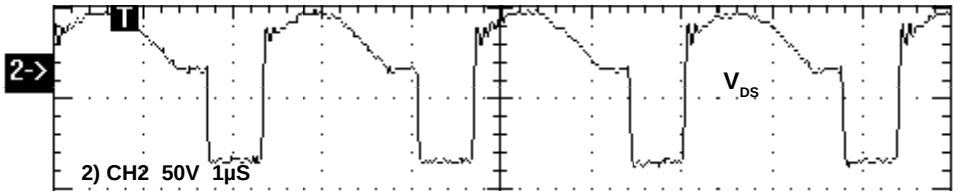


FIGURE 5C. 15S3.3/48

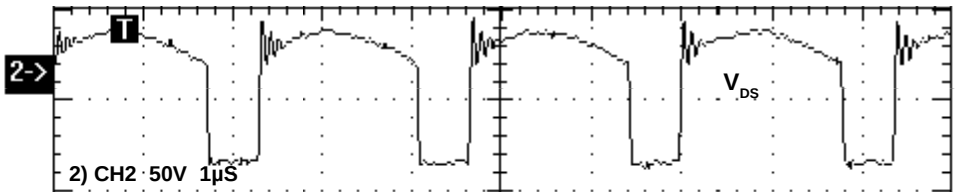
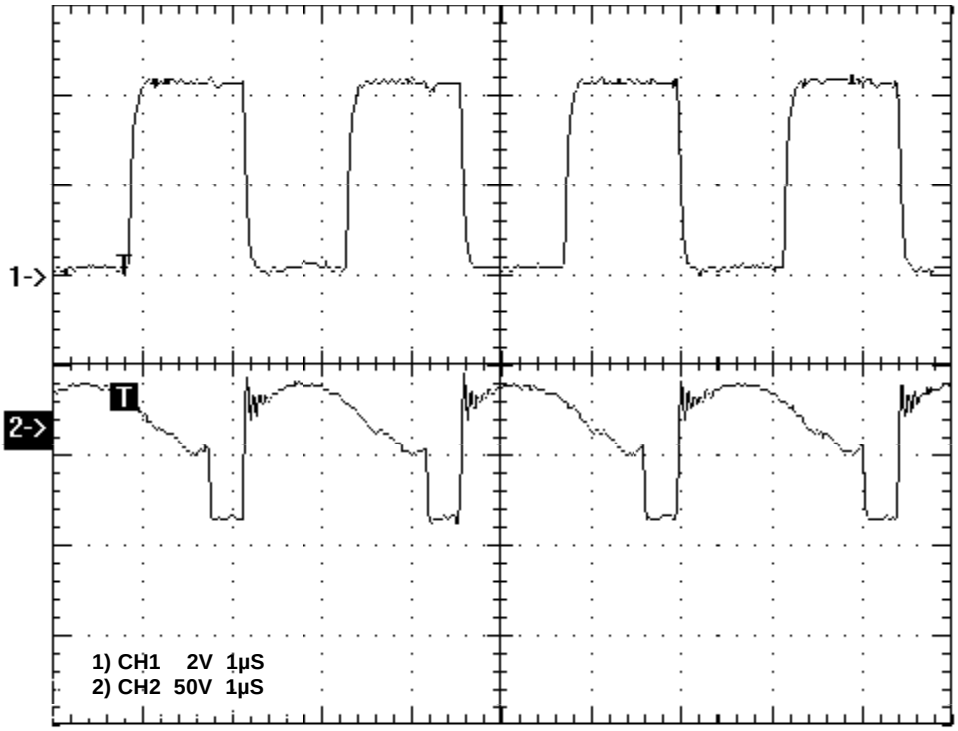


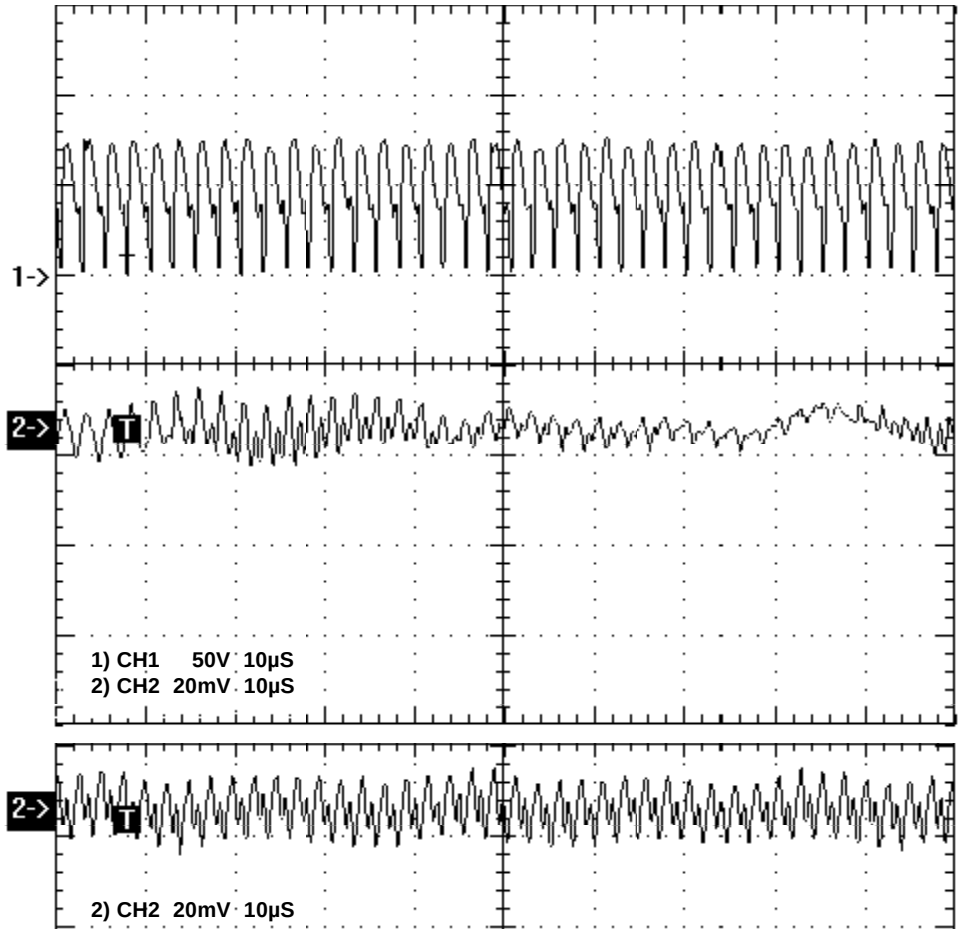
FIGURE 5D. 15S5/48

FIGURES 5A-D. Synchronization of four converters to an external clock from the schematic given in Figure 4



IRF120
Gate Signal

FIGURE 5F. 15S15/48, 15W external synchronization (Note the gate signal has ≈50% duty cycle)



V_{DS}

+48Vdc bus noise without LC filter and without synchronization

+48Vdc bus noise without LC filter and with synchronization

FIGURES 6A & 6B. Reflected ripple