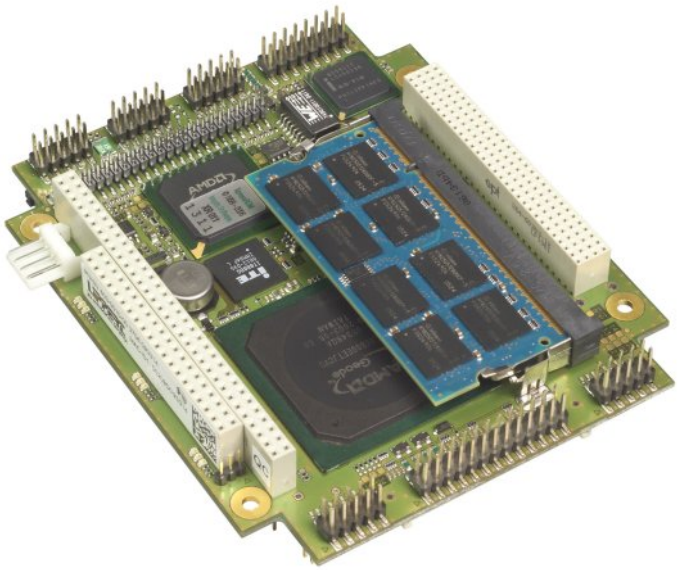
Cool RoadRunner-LX800

PC/104-Plus CPU Board

Technical Manual



TME-104P-CRR_LX800-R1V7.doc
Revision 1.7 / January 08
© LiPPERT Embedded Computers GmbH
Hans-Thoma-Str. 11
D-68163 Mannheim
http://www.lippert-at.com/

Technical Manual Cool RoadRunner-LX800

LiPPERT Document: TME-104P-CRR_LX800-R1V6.doc Revision 1.7

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Table of Contents

1 Overview 1

1.1 Introduction 1
Features 1
Block Diagram 2

1.2 Ordering Information 3
Cool RoadRunner-LX800 Models 3
Cable Sets and Accessories 3

1.3 Specifications 4
Electrical Specifications 4
Environmental Specifications 4
MTBF 4
Mechanical 5

2 Getting Started 6

2.1 Connector Locations 6
Top 6
Bottom 7

2.2 Jumper Locations 8

2.3 LED indicators 9

2.4 Hardware Setup 10

3 Module Description 11

3.1 Processor 11

3.2 Companion 12

3.3 Watchdog 12

3.4 Graphics-Controller 13
SVGA Configuration 13
VGA Connector 14
Flat Panel and LVDS Configuration 14
Flat Panel Connector 15
Flat Panel Backlight Connector 15
LVDS Connector 16
Display Voltage Selector 16

3.5 Compact Flash Connector 16

3.6 Ethernet Controller 17

Ethernet Interface 17

3.7 On Board Power Supply 17

Power Connector 17

3.8 EIDE Port 18

EIDE Connector 18

3.9 PS/2 Keyboard Interface 19

Keyboard Connector 19

3.10 PS/2 Mouse Interface 19

Mouse Connector 19

3.11 USB 2.0 Ports 20

USB 2.0 Connector 20

3.12 Serial Ports 21

COM1/2 Connector 21

RS485-Termination Jumpers 22

3.13 IrDA Interface 22

3.14 Parallel Port LPT1 23

LPT1 Connector X15 23

3.15 Speaker 24

3.16 Audio Interface 24

3.17 External Power-Button 25

3.18 Reset-In Signal 25

3.19 Supervisory Connector 26

3.20 PC/104-Plus Bus Interface 26

3.21 PC/104 Bus Interface 28

PC/104 Bus Connector 28

4 Using the Module 29

4.1 BIOS 29

Configuring the XpressROM BIOS 29

Trouble Shooting BIOS Settings 35

4.2 Drivers 35

4.3 Programming GPIO Signals 36
4.4 Watchdog Programming 37
4.5 Reading Temperatures 38
Handling of PWM Outputs 39
5 Address Maps 40
5.1 Memory Address Map 40
5.2 I/O Address Map 41
5.3 Interrupts 42
5.4 DMA Channels 42
5.5 PC/104 Bus Address Space 43
Appendix A, Contact Information A
Appendix B, Additional Information B
B.1 Additional Reading ..... B
B.2 PC/104 and PC/104-Plus Specifications ..... B
Appendix C, Getting Help C
Appendix D, Revision History D

1 Overview

1.1 Introduction

The Cool RoadRunner-LX800 is a high-performance PC/104-Plus board with AMD's Geode™ LX processor, having very low power requirements. The board comprises all peripherals needed for an embedded PC on a small 3.775" by 4.050" printed circuit board. It is fully plug-in compatible with the Cool RoadRunner 2, which was obsoleted due to end-of-life of the Geode GX1.

The Cool RoadRunner integrates a powerful yet efficient AMD Geode™ LX800 processor together with a CS5536 I/O companion and a Super I/O chip to form a complete PC, with all the standard peripherals already on board. There is graphics controller with VGA, LVDS, and parallel TFT adapters to connect many sorts of display terminals. Backlighting is provided for LCD modules.

A fast 100/10BaseT Ethernet port, RS232/RS42/RS485 serial ports, and four USB 2.0 host ports handle the communication with external devices. There are PS/2 connectors for keyboard and mouse as well as a parallel printer port available. Sound I/O according to AC97 is supported, too. An IDE ATA100 adapter allows connection of hard disk or CD drives. Applications that require non-moving storage can use the integrated Compact Flash socket.

System expansion is easily done using the PC/104 and PC/104-Plus connectors . I2C bus, PWM outputs, and programmable general purpose digital signals are available on a supervisory connector.

The Cool RoadRunner-LX800 is powered by a 5V-only supply and supports ACPI, advanced power management and PCI power management. Security critical applications take advantage of the Geode LX processor, too. It has an on-chip AES 128-bit crypto acceleration block capable of 44 Mbps throughput on either encryption or decryption. The AES block runs asynchronously to the processor core and is DMA based.

The Cool RoadRunner-LX800 runs Windows, Linux and VxWorks operating systems.

Features

CPU

- AMD Geode™ LX 800@1.0W (500MHz)
- Cache Memory with:
- 64 KB/64 KB level 1 I/D caches
- TLB (Translation Look-aside Buffer):
- 128 KB level 2 cache
- Efficient Prefetch

Chipset

- AMD CS5536 companion device

Interfaces

- Ethernet 10/100BaseT
- Compact Flash Type III header
- ATA-6 EIDE (Ultra DMA-100)
- PS/2 Keyboard
- PS/2 Mouse
- 4 x USB 2.0 ports
- 2 x RS232/RS485, software selectable
- 1 x parallel port

Main Memory

- One DDR333 SODIMM Module, up to 1GB
- Recommended: 256MB at minimum

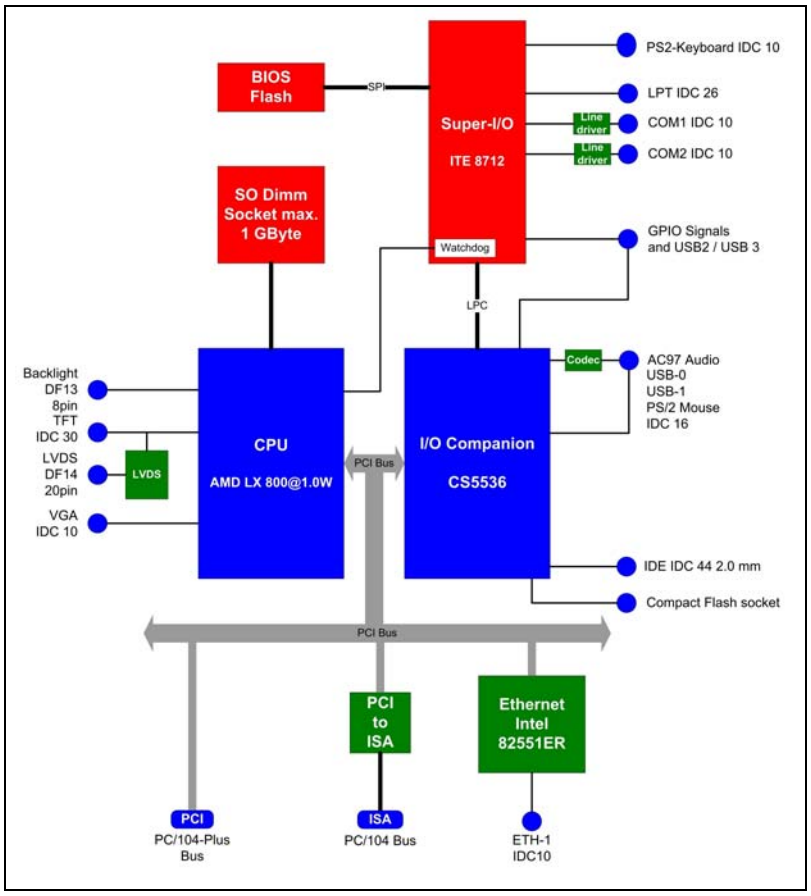
Extension slots

- 1 x 32-bit PC/104-Plus
- 1 x 16-bit PC/104 with full DMA capability

- SVGA monitor
- 18 Bit Flat Panel
- 24 Bit LVDS for displays
- Supervisory port: external power button, live signal, watchdog, hardware monitoring and some general purpose signals
- Power supply

Other configurations are possible at high volumes.

Block Diagram



1.2 Ordering Information

Cool RoadRunner-LX800 Models

Order number	Description
803-0010-10	Cool RoadRunner-LX800 (CRR-LX800) with LCD+VGA-CRT, AMD GEODE LX800@0.9W (500 MHz), low power consumption, up to 1GB DDR SDRAM, 4x USB2.0, IrDA, RTC, GoldCap, EIDE, 3x COM, LPT (EPP/EPC), PS/2 Keyboard, PS/2 Mouse, WDOG, PC/104 bus, PC/104+ bus, VGA controller (TFT Displays supported), bitparallel and LVDS Interface, Fast Ethernet 100/10BaseT, 8Bit GPIO, Compact Flash Type II Socket, Sound I/O AC97 compliant. Operating temp. range: -20°C .. +60°C
903-0010-10	Cool RoadRunner-LX800 (CRR-LX800) with LCD+VGA-CRT, AMD GEODE LX800@0.9W (500 MHz), low power consumption, up to 1GB DDR SDRAM, 4x USB2.0, IrDA, RTC, GoldCap, EIDE, 3x COM, LPT (EPP/EPC), PS/2 Keyboard, PS/2 Mouse, WDOG, PC/104 bus, PC/104+ bus, VGA controller (TFT Displays supported), bitparallel and LVDS Interface, Fast Ethernet 100/10BaseT, 8Bit GPIO, Compact Flash Type II Socket, Sound I/O AC97 compliant. Operating temp. range: -40°C .. +85°C

Cable Sets and Accessories

There are some options available for the Cool RoadRunner-LX800. Please check their availability before ordering.

Order number	Description
863-0011-10	Adapter Cable Set Cable set for Cool Roadrunner LX800, power, keyboard, 2.5" IDE, cable adapter 2.5" > 3.5", adapter 3.5" > 2.5", printer, 2 x serial, floppy adapter, VGA-CRT, Ethernet, 2 x USB, sound I/O, mouse.

1.3 Specifications

Electrical Specifications

Supply voltage	+5 V DC
Rise time	< 5 ms
Supply voltage tolerance	± 5%
Inrush current	2.5 A
Supply current	max. 1.5 A depending on operating system and RAM
	typ. 0.9 A (Windows XP idle mode)
	typ. 0.06 A (running Windows XP Suspend to RAM)

Environmental Specifications

Operating:

Temperature range	-20 … 60 °C (standard version)
	-40 … 85 °C (extended version)
Temperature change	max. 10K / 30 minutes
Humidity (relative)	10 … 90 % (non-condensing)
Pressure	450 … 1100 hPa

Non-Operating / Storage / Transport:

Temperature range	-40 … 85 °C
Temperature change	max. 10K / 30 minutes
Humidity (relative)	5 … 95 % (non-condensing)
Pressure	450 … 1100 hPa

MTBF

MTBF at 25°C	364.293 hours

In order to perform a failure rate assessment, several assumptions have to be made to minimize the complexity of the analysis.

Basis for the calculation was „Parts-Stress" method according to MIL-HDBK-217 F Notice 2. Although this method requires stress values for all components, mean stress values have been used.

Environmental factor „Ground Benign" according to MIL-HDBK-217 has been used as well as an environmental temperature of 25 °C.

Failure rate of mechanical components (screws, chassis, etc) is negligible.

The detailed analysis report is available on request.

Mechanical

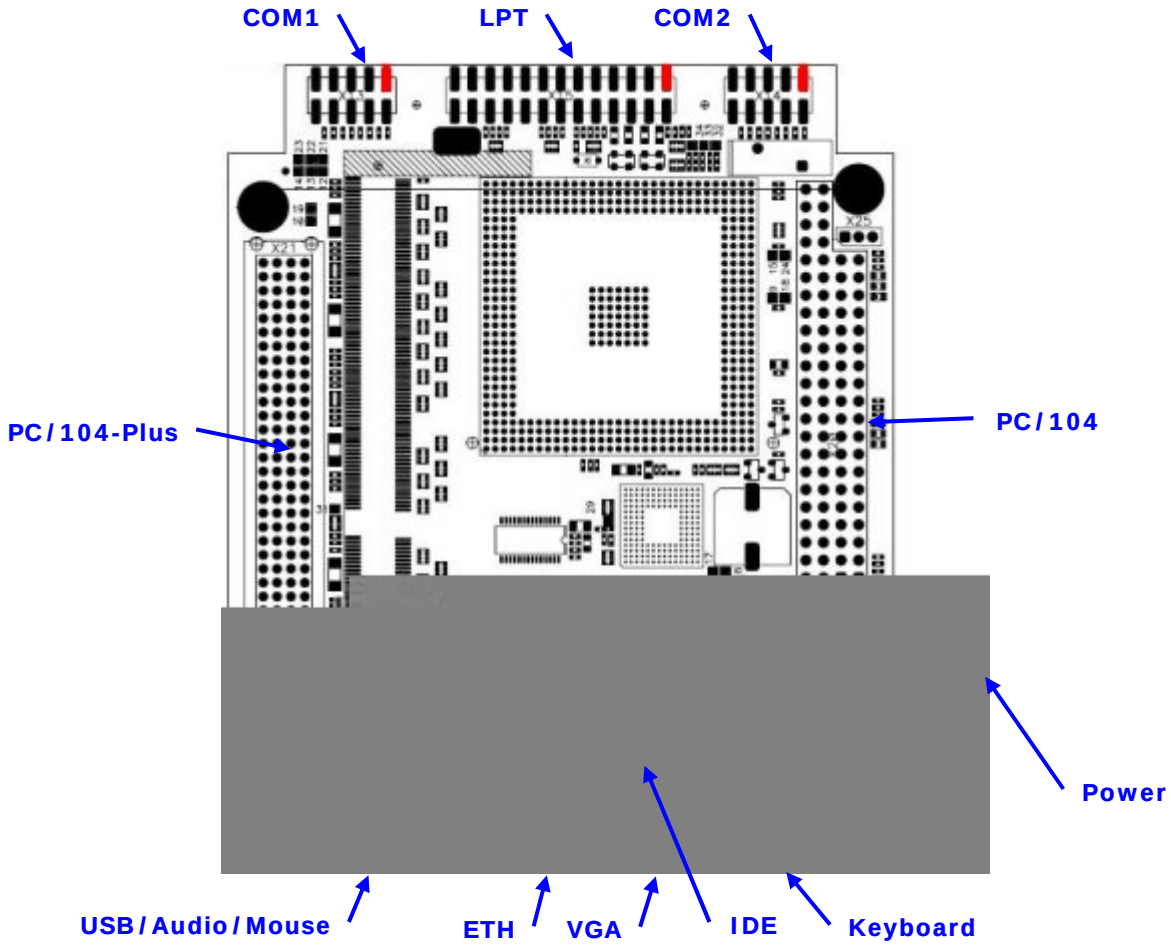
Dimensions (LxW)	95.9 mm x 115.6 mm (including I/O extension)
Height	max. 14 mm on topside above PCB max. 12 mm on bottomside above PCB
Weight	150 g (including RAM)
Mounting	4 mounting holes

Note: *It is strongly recommend using plastic spacers instead of metal spacers to mount the board. With metal spacers, there is a possible danger to create a short circuit with the components located around the mounting holes. This can damage the board!*

2 Getting Started

2.1 Connector Locations

Top



The connectors' pin 1 is marked RED

2.4 Hardware Setup

Caution Be sure to observe the EMC security measures. Make sure you are always at the same potential as the module.

Caution Never connect or disconnect peripherals like HDD's while the board's power supply is connected and switched on!

Use the cable set provided by LiPPERT to connect the Cool RoadRunner-LX800 to a VGA monitor. Connect either PS/2 or USB keyboard and mouse, respectively. Use the 40-wire flat foil cable to connect the harddisk. Make sure that the pins match their counterparts correctly and are not twisted. If you plan to use addtitional other peripherals, now is the time to connect them, too.

Connect a 5 volt, 2 amps power supply to to the power connector and swith the power on.

Note *The 2 amps value is the minimum you should have for the standard periperals mentioned. If you want to use more and/or others, please plan your power budget first! The system will not work if there is not enough supply current for all your devices.*

The display shows the BIOS messages. If you want to change the standard BIOS settings, press the <F1> key to enter the BIOS menu. See chapter 4.1 for BIOS setup details.

If you need to load the BIOS default values, they can be automatically loaded at boot time. See chapter 4.1, "Trouble Shooting BIOS Settings", about how to do it.

The Cool RoadRunner-LX800 boots from CD drives, USB floppy, USB stick, or harddisk. Provided that any of these is connected and contains a valid operating system image, the display then shows the boot screen of your operating system.

The Cool RoadRunner-LX800 does not need any cooling measures, neither at standard environment temperatures from –20 °C … +60 °C nor in the extended range of -40 °C ... +85 °C.

3 Module Description

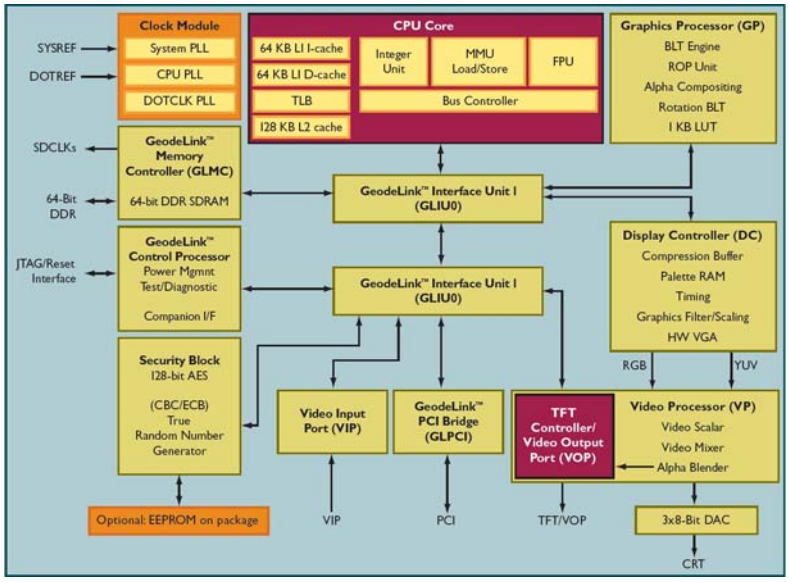
3.1 Processor

The AMD Geode LX 800@0.9W processor delivers the best performance per watt in the industry today, providing X86 power and versatility to embedded products. Its architecture and high level of integration guarantees longer battery life and allows very small designs, while delivering full X86 functionality.

The AMD Geode LX 800 processor consumes a maximum power of 3.9W and 1.8W typical at 500 MHz, enabling systems that only need to be passively cooled.

The x86 compatibility allow designers to focus on developing end products that efficiently meet consumer needs without being concerned with software porting or compatibility issues.

Coupled with the AMD Geode™ CS5536 companion device, the combined chipset, which operates at 1.9W typical at 433MHz and at 2.4W typical at 500MHz, offers a complete set of features that deliver full desktop functionality to embedded and portable devices.



Processor functional blocks are

- CPU Core
- GeodeLink™ Control Processor
- GeodeLink Interface Units
- GeodeLink Memory Controller
- Graphics Processor
- Display Controller
- Video Processor
- Video Input Port
- GeodeLink PCI Bridge
- Security Block

For further information, please refer to the data book of the AMD Geode™ LX 800

3.2 Companion

AMD Geode™ CS5536 companion device

The AMD Geode™ CS5536 companion device is designed to work with an integrated processor North Bridge component such as the AMD Geode™ GX/LX processor. Together, the Geode GX/LX processor and Geode CS5536 companion device provide a system-level solution well suited for the high-performance and low-power needs of a host of embedded devices including digital set-top boxes, mobile computing devices, thin client applications, and single board computers.

The internal architecture uses a single, high-performance modular structure based on GeodeLink™ architecture. This architecture yields high internal speed (over 4 GB/s) data movement and extremely versatile internal power management. The GeodeLink architecture is transparent to application software. Communication with the Geode GX/LX processor is over a 33/66 MHz PCI bus.

The Geode CS5536 companion device incorporates many I/O functions, including some found in typical Super-I/O chips, simplifying many system designs. Since the graphics subsystem is entirely contained in the Geode GX/LX processor, system interconnect is simplified. The device contains state-of-the-art power management that enables systems, especially battery powered systems, to significantly reduce power consumption.

Audio is supported by an internal controller, designed to connect to multiple AC97 compatible codecs. An IR (infrared) port supports all popular IR communication protocols. The IR port is shared with one of two industry-standard serial ports that can reach speeds of 115.2 kbps. An LPC (low pin count) port is provided to facilitate connections to a Super-I/O should additional expansion, such as a floppy drive, be necessary, and/or to an LPC ROM for the system BIOS

The hard disk controller is compatible to the ATA-5 specification. The bus mastering IDE controller includes support for two ATA-compliant devices on one channel. The CS5536 companion device provides four Universal Serial Bus (USB) 2.0 compliant ports, supporting low speed, full speed, and high speed connections. All four ports are individually automatically associated with either the Open Host Controller Interface (OHCI) or the Enhanced Host Controller Interface (EHCI) depending on the attached device type. A real-time clock (RTC) keeps track of time and provides calendar functions.

A suite of 82xx devices provides the legacy PC functionality required by most designs, including two PIC's (programmable interrupt controllers), one PIT (programmable interval timer) with three channels, and DMA (direct memory access) functions. The CS5536 companion device contains eight MFGPT's (multi-function general purpose timers) that can be used for a variety of functions. A number of GPIO's (general purpose input/outputs) are provided, and are assigned to system functions on power-up.

State-of-the-art power management features are attained with the division of the device into two internal power domains. The GPIO's and multi-function timers are distributed into each domain allowing them to act as wakeup sources for the device. The device provides full ACPI (Advanced Configuration Power Interface) compliance and supports industry-standard Wakeup and Sleep modes.

3.3 Watchdog

An internal circuit of the ITE8712 Super I/O implements a watchdog. It is accessible through general-purpose ports of the Super I/O controller.

Please refer to chapter 4.4 for programming watchdog functions.

3.4 Graphics-Controller

The graphics controller is integrated in the Geode LX and does high performance 2D-graphics handling. CRT monitors can be used as well as TFT- or LVDS displays. Therefore, different connectors are on the board. It is possible to switch between CRT and TFT via BIOS or driver settings. It is also possible to use a CRT and a TFT/LVDS display simultaneously (driver setting).

The Cool RoadRunner-LX800 supports 3,3V and 5V TFT displays up to 18bit, and LVDS displays with 18/24bit interfaces with unconventional signal configuration. The display type and resolution can be selected in BIOS setup: **Motherboard Device Configuration → Video and Flat Panel Configuration.**

SVGA Configuration

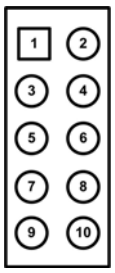
Resolution	Color Depth (bpp)	Refresh Rate (Hz)	Dot Clock (MHz)	Min. GLIU Frequency (MHz)
640 x 480	8, 16, or 24/32	60	25.175	75
	8, 16, or 24/32	70	28.560	75
	8, 16, or 24/32	72	31.500	75
	8, 16, or 24/32	75	31.500	75
	8, 16, or 24/32	85	36.000	75
	8, 16, or 24/32	90	37.889	400
	8, 16, or 24/32	100	43.163	400
800 x 600	8, 16, or 24/32	60	40.000	75
	8, 16, or 24/32	70	45.720	75
	8, 16, or 24/32	72	49.500	75
	8, 16, or 24/32	75	49.500	75
	8, 16, or 24/32	85	56.250	75
	8, 16, or 24/32	90	60.065	400
	8, 16, or 24/32	100	68.179	400
1024 x 768	8, 16 or 24/32	60	65.000	75
	8, 16, or 24/32	70	75.000	100
	8, 16, or 24/32	72	78.750	100
	8, 16, or 24/32	75	78.750	100
	8, 16, or 24/32	85	94.500	100
	8, 16, or 24/32	90	100.187	400
	8, 16, or 24/32	100	113.310	400
1152x864	8, 16, or 24/32	60	81.600	100
	8, 16, or 24/32	70	97.520	100
	8, 16, or 24/32	72	101.420	200
	8, 16, or 24/32	75	108.000	200
	8, 16, or 24/32	85	119.650	200
	8, 16, or 24/32	90	129.600	400
	8, 16, or 24/32	100	144.000	400
1280 x 1024	8, 16, or 24/32	60	108.000	200
	8, 16, or 24/32	70	129.600	200

Resolution	Color Depth (bpp)	Refresh Rate (Hz)	Dot Clock (MHz)	Min. GLIU Frequency (MHz)
	8, 16, or 24/32	72	133.500	200
	8, 16, or 24/32	75	135.000	200
	8, 16, or 24/32	85	157.500	200
	8, 16, or 24/32	90	172.800	400
	8, 16, or 24/32	100	192.000	400
1600 x 1200	8, 16, or 24/32	60	162.000	200
	8, 16, or 24/32	70	189.000	200
	8, 16, or 24/32	72	198.000	233
	8, 16, or 24/32	75	202.500	233
	8, 16, or 24/32	85	229.500	266
	8, 16, or 24/32	90	251.182	400
	8, 16, or 24/32	100	280.640	400
1920x1440	8, 16, or 24/32	60	234.000	266
	8, 16, or 24/32	70	278.400	400
	8, 16, or 24/32	72	288.000	400
	8, 16, or 24/32	75	297.000	400
	8, 16, or 24/32	85	341.349	400

VGA Connector

Connector type: IDC10 pin header 2.00 mm

Pin	Signal	Pin	Signal
1	Red	2	GND
3	Green	4	GND
5	Blue	6	GND
7	HSYNC	8	GND
9	VSYNC	10	n.c.



Flat Panel and LVDS Configuration

Flat panel and LVDS have the same display options as shown in the table:

Setting	Possible Values
Flat Panel Type	Auto, TFT, LVDS
Resolution	320x240, 640x480, 800x600, 1024x768, 1152x864, 1280x1024, 1600x1200
Data Bus Type	9-24 Bits, 1ppc
Refresh Rate	60 Hz
HSYNC Polarity	High, Low

Setting	Possible Values
VSYNC Polarity	High, Low
LP Active Period	Active Only → only active during SYNC Free Running → always active
SHFCLK Active Period	Active Only → only active during SYNC Free Running → always active

To ease usage of these displays it's possible to select the display and backlight supply voltages with the on-board voltage selector jumpers. (Jumper X8, see below)

Flat Panel Connector

Connector type: IDC30 pin header 2.00 mm

Pin	Signal	Pin	Signal
1	GND	2	FPCLK
3	HSYNC	4	VSYNC
5	GND	6	R0
7	R1	8	R2
9	R3	10	R4
11	R5	12	GND
13	G0	14	G1
15	G2	16	G3
17	G4	18	G5
19	GND	20	B0
21	B1	22	B2
23	B3	24	B4
25	B5	26	GND
27	EN	28	VLCD-SW
29	VLCD-SW	30	GND

Flat Panel Backlight Connector

Connector type: Hirose DF13 8 pin

Pin	Signal	Pin	Signal
1	+12 Volts	2	+12 Volts
3	+5 Volts	4	+5 Volts
5	EN	6	NC
7	GND	8	GND

LVDS Connector

Connector type: Hirose DF14 20-pin header

Pin	Signal	Pin	Signal
1	SW-VDD	2	SW-VDD
3	GND	4	GND
5	TX3-	6	TX3+
7	GND	8	TXCLK-
9	TXCLK+	10	GND
11	TX2-	12	TX2+
13	GND	14	TX1-
15	TX1+	16	GND
17	TX0-	18	TX0+
19	DDC Clk	20	DDC Data

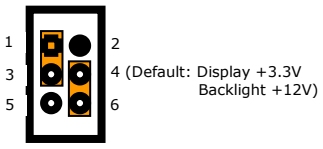
Display Voltage Selector

Jumper X8

Connector type: IDC6 jumper 2.00 mm.

Use a 2 mm jumper between 1-3 or 3-5 to select the backlight voltage.

Use a 2 mm jumper between 2-4 or 4-6 to select the display voltage.



Pin	Signal	Pin	Signal
1	+12 volts	2	+5 volts
3	Backlight voltage	4	Display voltage
5	+ 5 volts	6	+3.3 volts

3.5 Compact Flash Connector

On the bottom side of the board a compact flash connector is located that allows the use of compact flash cards instead of a hard disk. This socket is connected to the chipset's EIDE port. As default it is defined as Master.
Compact flash cards are available as solid-state disks starting at 16 Mbytes up to several Gbytes and also as IBM Micro Drives.

3.6 Ethernet Controller

Intel 82551IT Fast Fast Ethernet Controller

The 82551IT is an evolutionary addition to Intel's family of 8255x controllers. It provides excellent performance by offloading TCP, UDP and IP checksums and supports TCP segmentation off-load for operations such as Large Send. The 82551IT provides an extended operating temperature in addition to all of the same capabilities and features as the 82551ER to address applications requiring a wider operating temperature range.

Its optimized 32-bit interface and efficient scatter-gather bus mastering capabilities enable the 82551IT to perform high speed data transfers over the PCI bus. This capability accelerates the processing of high level commands and operations, which lowers CPU utilization. Its architecture enables data to flow efficiently from the bus interface unit to the 3 KB Transmit and Receive FIFO's, providing the perfect balance between the wire and system bus. In addition, multiple priority queues are provided to prevent data underruns and overruns.

The 82551IT includes both a MAC and PHY. In also has a simple interface to the analog front end, which allows cost effective designs requiring minimal board real estate. The 82551IT is pin compatible with the 82559 family of controllers and is offered with software that provides backwards compatibility with previous 8255xER controllers.

Ethernet Interface

Connector type: IDC10 pin header 2.54 mm

Pin	Signal	Pin	Signal
1	TX+	2	TX-
3	RX+	4	PE
5	PE	6	RX-
7	PE	8	PE
9	nc	10	nc

3.7 On Board Power Supply

The on board power supply generates all necessary voltages from the single supply voltage of 5 volts. The generated 3.3 volts are available on the connectors "Flat Panel" and "LVDS".

Note *This 3.3 V must not be used to supply external electronic devices with high power consumption like other PC/104 boards or displays.*

Power Connector

Connector type: 3.5" FDD Power connector

Pin	Signal	Pin	Signal
1	+5 Volts	2	GND
3	GND	4	+ 12 Volts

3.8 EIDE Port

An EIDE (**E**nhanced **I**ntegrated **D**rive **E**lectronics) port is provided by the chipset to connect one drive. The connected device must be set as slave.
To enhance the performance, this port has a 100 MB/s IDE controller in UDMA mode per the ATA-5 specification The EIDE port is available on a standard 44-pin header (2 mm) for 2.5" hard disks. An adapter cable is available to connect standard EIDE devices with a 40 pin IDC header.

EIDE Connector

Connector type: IDC14 pin header 2.00 mm

Pin	Signal	Pin	Signal
1	/Reset	2	GND
3	Data7	4	Data8
5	Data6	6	Data9
7	Data5	8	Data10
9	Data4	10	Data11
11	Data3	12	Data12
13	Data2	14	Data13
15	Data1	16	Data14
17	Data0	18	Data15
19	GND	20	NC
21	DRQ0	22	GND
23	Write	24	GND
25	Read	26	GND
27	Ready	28	CSEL
29	DACK0	30	GND
31	IRQ	32	IOCS16-
33	Address1	34	PD66
35	Address0	36	Address2
37	CS1	38	CS3
39	NC	40	GND
41	+5 Volts	42	+5 Volts
43	GND	44	GND

3.9 PS/2 Keyboard Interface

The keyboard interface is located on the IDC10 Header "KEYBOARD". An adapter cable is available to use a standard PS/2 keyboard with this connector.

Keyboard Connector

Connector type: IDC10 pin header 2.54 mm

Pin	Signal	Pin	Signal
1	Speaker	2	GND
3	Reset#	4	N.C.
5	KB Data	6	KB Clock
7	GND	8	VCCKB
9	Ext. Battery	10	Reset# (PWRBTN#)

3.10 PS/2 Mouse Interface

The PS/2 mouse signals MCLK and MDAT are located on the IDC16 header "AUDIO". An adapter cable is available to use a standard PS/2 mouse with this connector.

Mouse Connector

Connector type: IDC16 pin header 2.54 mm

Pin	Signal	Pin	Signal
1	IRRX	2	IRTX
3	MS Data	4	MS Clock
5	USBDT0+	6	USBDT0-
7	USBDT1+	8	USBDT1-
9	USBVCC	10	USBGND
11	Line In L	12	Line In R
13	Line Out L	14	Line Out R
15	Microphone	16	GND Audio

3.11 USB 2.0 Ports

4 standard USB 2.0 host ports are provided at the with Cool RoadRunner-LX800. Two are located on the IDC16 header "AUDIO". An adapter cable is available to use a standard USB devices with this connector. The other two are located at the supervisory connector. There is no standard adapter available.

It is possible to use an USB keyboard under MSDOS without special driver software.

Note: *Not all USB keyboard models are supported.*

USB 2.0 Connector

Connector type: IDC16 pin header 2.54 mm

Pin	Signal	Pin	Signal
1	IRRX	2	IRTX
3	MS Data	4	MS Clock
5	USBDT0+	6	USBDT0-
7	USBDT1+	8	USBDT1-
9	USBVCC	10	USBGND
11	Line In L	12	Line In R
13	Line Out L	14	Line Out R
15	Microphone	16	GND Audio

3.12 Serial Ports

The serial ports are located on two IDC headers "COM1" and "COM2". Adapter cables with standard DB9 male connectors are available. The ports either work in RS232 or RS485 mode, selectable in the BIOS. When entering **Motherboard Device Configuration → LPC CARD I/O Device Configuration**, **COM Port 1 Mode** and **COM Port 2 Mode** can be selected. Termination resistors for RS485 Mode can be set with Jumpers on pin headers X12 and X24 as described in chapter 4.15.

To enable transmitters of COM1 and COM2 in RS485 Mode set RTS signal to '1'.

The serial ports are programmable in BIOS setup. When entering **Motherboard Device Configuration → LPC CARD I/O Device Configuration,** configuration of the serial ports is accessible.

The following settings are possible for COM1 and COM2:

- Disabled
- 3F8 / IRQ4 (base address / interrupt channel)
- 2F8 / IRQ3 (base address / interrupt channel)
- 3E8 / IRQ4 (base address / interrupt channel)
- 2E8 / IRQ3 (base address / interrupt channel)

The modes can be switched between RS232 and RS485.

COM1/2 Connector

Connector type: IDC10 pin header 2.54 mm

Pin	RS232	RS485	Pin	RS232	RS485
1	DCD	*Not used*	2	DSR	RXD+
3	RXD	RXD-	4	RTS	TXD+
5	TXD	TXD-	6	CTS	*Not used*
7	DTR	*Not used*	8	*Not used*	*Not used*
9	GND	GND	10	+5 Volts	+5 Volts

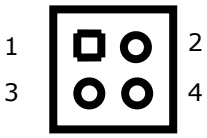
RS485-Termination Jumpers

Connector type: IDC4 pin header 2.00 mm. Use 2 mm jumpers to terminate lines correctly.

There are two jumpers, X12 for COM1, and X24 for COM2, respectively.

The RS485 termination jumpers are located at the bottom of the printed circuit board, see chapter 2.2

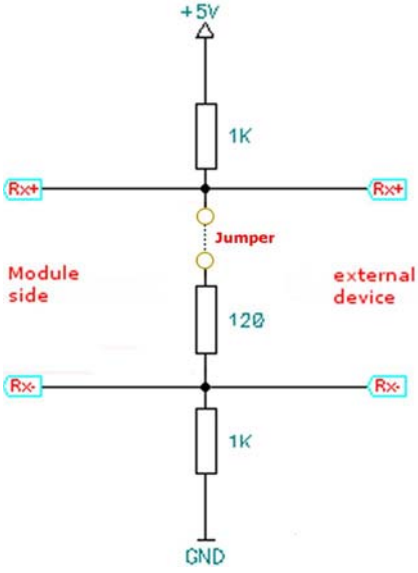
Pin	Signal	Pin	Signal
1	TX+	2	TX-
3	RX+	4	RX-



When the jumper is set, the differential pairs (e.g. RX+ and RX-) are terminated with 120Ω between them.

Additionally, positive/negative receive lines are pulled up/down with 1kΩ to 5V/GND in order to protect the transceivers of the Cool RoadRunner-LX800 from overvoltages.

It is recommended to protect the ports of the external device in the same way!



Caution: Termination Resistors **must not** be used in RS232 Mode. Otherwise, the serial ports will not work.

3.13 IrDA Interface

The IrDA interface signals IRRX and IRTX are located on the USB/JJJJ/LKJL connector.

To use the IrDA interface an external transmitter must be connected to the IrDA signals.

Connector type: IDC16 pin header 2.54 mm

Pin	Signal	Pin	Signal
1	IRRX	2	IRTX
3	MS Data	4	MS Clock
5	USBDT0+	6	USBDT0-
7	USBDT1+	8	USBDT1-
9	USBVCC	10	USBGND
11	Line In L	12	Line In R
13	Line Out L	14	Line Out R
15	Microphone	16	GND Audio

3.14 Parallel Port LPT1

The parallel port is located on an IDC26 header. An adapter cable with a standard DB25 female connector is available.

The parallel port is programmable in BIOS. Entering **Motherboard Device Configuration → LPC CARD I/O Device Configuration**, configuration of LPT1 is accessible.

LPT1 Parameter	Possible Settings
Base Address	Disabled, 0x378 0x3BC and 0x278 are not recommended, because of a possible conflict with the PCI to ISA Bridge
Mode	Compatible, PS/2 Bi-directional, EPP 1.7, EPP 1.9
IRQ	Disabled, IRQ 5, IRQ 7, IRQ 9, IRQ 10, IRQ 11
DMA	None, Channel 1, Channel 3

LPT1 Connector X15

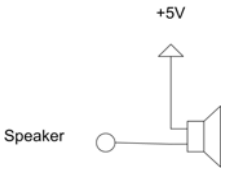
Connector type: IDC26 pin header 2.54 mm

Pin	Signal	Pin	Signal
1	Strobe	2	Auto LF
3	Data0	4	Error
5	Data1	6	Init
7	Data2	8	Select In
9	Data3	10	GND
11	Data4	12	GND
13	Data5	14	GND
15	Data6	16	GND
17	Data7	18	GND
19	ACK	20	GND
21	Busy	22	GND
23	Paper End	24	GND
25	Select	26	+5V_SBY

3.15 Speaker

The speaker signal is located on the IDC10 Header "KEYBOARD". A standard PC Speaker can be connected between the signal SPEAKER and VCCKB.

Connector type: IDC10 pin header 2.54 mm



Pin	Signal	Pin	Signal
1	Speaker	2	GND
3	Reset#	4	N.C.
5	KB Data	6	KB Clock
7	GND	8	VCCKB (+5V)
9	Ext. Battery	10	Reset# (PWRBTN#)

3.16 Audio Interface

The audio signals are located on the IDC16 header "AUDIO". The signals are LINE-IN (left/right), LINE-OUT (left/right) and MICROPHONE-IN of the AC-97audio codec.

There is an adapter cable available with standard audio connectors.

Connector type: IDC16 pin header 2.54 mm

Pin	Signal	Pin	Signal
1	IRRX	2	IRTX
3	MS Data	4	MS Clock
5	USBDT0+	6	USBDT0-
7	USBDT1+	8	USBDT1-
9	USBVCC	10	USBGND
11	Line In L	12	Line In R
13	Line Out L	14	Line Out R
15	Microphone	16	GND Audio

3.17 External Power-Button

The Power-Button signal is located on the IDC10 Header "KEYBOARD". To power up/down the board the signal Power-Button must be pulled to GND. It is not available in standard configuration.

Connector type: IDC10 pin header 2.54 mm

Pin	Signal	Pin	Signal
1	Speaker	2	GND
3	Reset#	4	N.C.
5	KB Data	6	KB Clock
7	GND	8	VCCKB
9	Ext. Battery	10	Reset# (PWRBTN#)

3.18 Reset-In Signal

The RESET-IN signal is located on the IDC10 Header "KEYBOARD". To reset the board, the signal RESET-IN must be pulled to GND.

Connector type: IDC10 pin header 2.54 mm

Pin	Signal	Pin	Signal
1	Speaker	2	GND
3	Reset#	4	N.C.
5	KB Data	6	KB Clock
7	GND	8	VCCKB
9	Ext. Battery	10	Reset# (PWRBTN#)

3.19 Supervisory Connector

The Cool RoadRunner-LX800 provides a 25-pin Supervisory Connector on its bottom side. The table below shows the assignment of the different signals.
(*The secondary functions are available only with customized versions. Please ask for a quotation*)

Connector type: Hirose DF14 30-pin

Pin	Signal		Pin	Signal	
	Primary	Secondary		Primary	Secondary
1	+5 Volts		2	+3.3 Volts	
3	GPIO40[1]	SMB CLK	4	GPIO41[1]	SMB DATA
5	GPIO42[1]	IDE LED[2]	6	GPIO43[1]	SBY LED[2]
7	GPIO44[1]	LIVE LED[2]	8	N.C.	ACT_LED[2]
9	N.C.	LINK LED[2]	10	GPIO47[1]	ETH SPD LED[2]
11	PWM2[4]		12	PWM3[4]	
13	PWM4[4]		14	PWM5[4]	
15	AGND		16	N.C.	
17	N.C.		18	N.C.	
19	N.C.		20	N.C.	
21	N.C.		22	WD ACTIVE	PME#[3]
23	VCCUSB2		24	USB2+	
25	USB2-		26	USBGND	
27	USB3+		28	USB3-	
29	USBVCC3		30	GND	

Notes:

(1) See chapter 4.3 about GPIO programming
(2) Connect cathode of LED to this pin. An external resistor is required
(3) Power Management Signal
(4) See chapter 4.7 about PWM programming
(5) See chapter 4.5 about ADC programming

3.20 PC/104-Plus Bus Interface

The PC/104-Plus bus is a modification of the standard PCI bus. It allows all of the PC/104 features to be used, together with the high speed PCI bus.

The main features are:

- PC/104-Plus Bus slot, fully compatible with PCI version 2.2 specifications.
- Integrated PCI arbitration interface (32 bit wide, 3.3V).
- Translation of PCI cycles to ISA bus.
- Translation of ISA master initiated cycle to PCI.
- Support for burst read/write from PCI master.
- 33 MHz PCI clock.

Pin	A	B	C	D
1	GND	Reserved	+5 Volts	AD00
2	VI/O	AD02	AD01	+5 Volts
3	AD05	GND	AD04	AD03
4	C/BE0	AD07	GND	AD06
5	GND	AD09	AD08	GND
6	AD11	VI/O	AD10	M66EN
7	AD14	AD13	GND	AD12
8	n.c.	C/BE1	AD15	n.c.
9	SERR	GND	SB0	PAR
10	GND	PERR	n.c.	SDONE
11	STOP	n.c.	LOCK	GND
12	n.c.	TRDY	GND	DEVSEL
13	FRAME	GND	IRDY	n.c.
14	GND	AD16	n.c.	C/BE2
15	AD18	n.c.	AD17	GND
16	AD21	AD20	GND	AD19
17	n.c.	AD23	AD22	n.c.
18	IDSEL0	GND	IDSEL	IDSEL2
19	AD24	C/BE3	VI/O	IDSEL3
20	GND	AD26	AD25	GND
21	AD29	+5 Volts	AD28	AD27
22	+5 Volts	AD30	GND	AD31
23	REQ0	GND	REQ1	VI/O
24	GND	REQ2	+5 Volts	GNT0
25	GNT1	VI/O	GNT2	GND
26	+5 Volts	CLK0	GND	CKL1
27	CLK2	+5 Volts	CLK3	GND
28	GND	INTD	+5 Volts	RST
29	+12 Volts	INTA	INTB	INTC
30	-12 Volts	REQ3	GNT3	GND

Note: *All VI/O pins are connected to +3.3V.*
The voltages +5V and +12V are not generated by the onboard power-supply but routed from the Power Supply Connector. This board does not support -12 Volts. The maximum current is limited to 1.0 amp for each voltage.

3.21 PC/104 Bus Interface

The PC/104 bus is a modification of the industry standard (ISA) PC bus specified in IEEE P996. The PC/104 bus has different mechanics than P966 to allow the stacking of modules. The main features are:

- Supports programmable extra wait state for ISA cycles
- Supports I/O recovery time for back-to-back I/O cycles

The following table shows the pin assignment of the PC/104 connector.

Note: -5 V and –12 V on the PC/104 connector are not supported on this board.

PC/104 Bus Connector

Pin	D	C
0	GND	GND
1	MEMCS16	SBHE
2	IOCS16	LA23
3	IRQ	LA22
4	IRQ	LA21
5	IRQ	LA20
6	IRQ	LA19
7	IRQ	LA18
8	DACK	LA17
9	DRQ	MEMR
10	DACK	MEMW
11	DRQ	SD8
12	DACK	SD9
13	DRQ	SD10
14	DACK	SD11
15	DRQ	SD12
16	+5V	SD13
17	MASTER	SD14
18	GND	SD15
19	GND	GND

Pin	A	B
1	IOCHCK	GND
2	D7	RSTDRV
3	D6	+5V see note
4	D5	IRQ9
5	D4	-5V
6	D3	DRQ2
7	D2	-12V see note
8	D1	ENDXFER
9	D0	+12V
10	IOCHRDY	KEY
11	AEN	SMEMW
12	A19	SMEMR
13	A18	IOW
14	A17	IOR
15	A16	DACK3
16	A15	DRQ3
17	A14	DACK1
18	A13	DRQ1
19	A12	REFRESH
20	A11	SYSCLK
21	A10	IRQ7
22	A9	IRQ6
23	A8	IRQ5
24	A7	IRQ4
25	A6	IRQ3
26	A5	DACK2
27	A4	TC
28	A3	BALE
29	A2	+5V
30	A1	OSC
31	A0	GND
32	GND	GND

4 Using the Module

4.1 BIOS

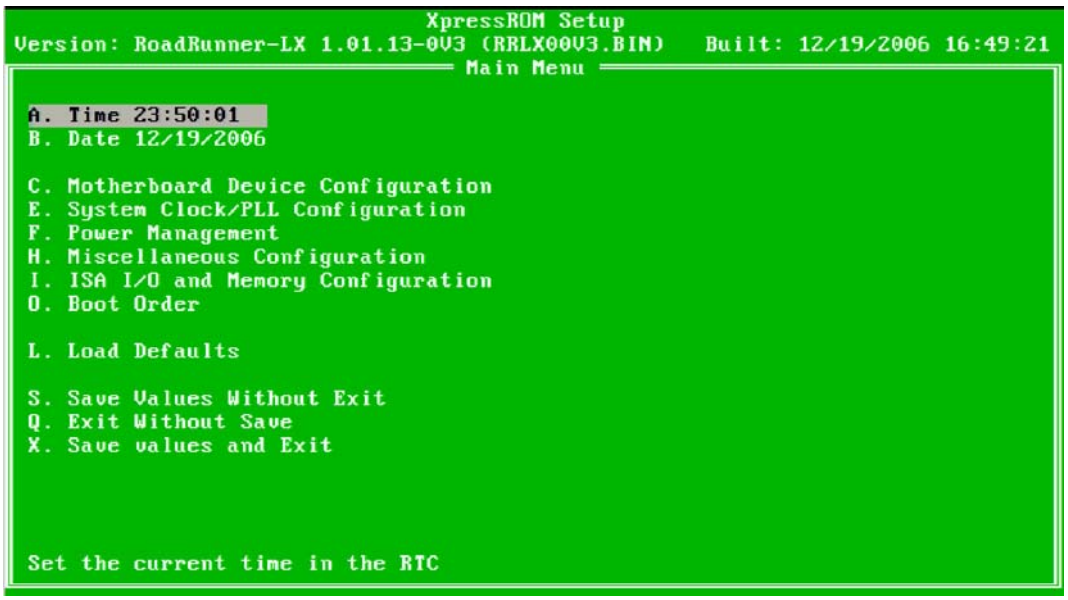
The Cool RoadRunner-LX800 is delivered with a Insyde Technology XpressROM BIOS. The default setting guarantees a "ready to run" system, even without a BIOS setup backup battery.

The BIOS is located in flash memory and can be easily updated on board with software under DOS.

All setup changes of the BIOS are stored in the CMOS RAM of the real time clock. A copy of the CMOS RAM, excluding date and time, is stored in the flash memory. This means that even if the backup battery runs out of power, the BIOS settings are not lost. Only date and time will be reset to their default value. Without an external battery the on board, the GoldCap is able to buffer the date and time information for about 2 days.

Configuring the XpressROM BIOS

Pressing <F1> on power up starts the BIOS setup utility.



Field Selection

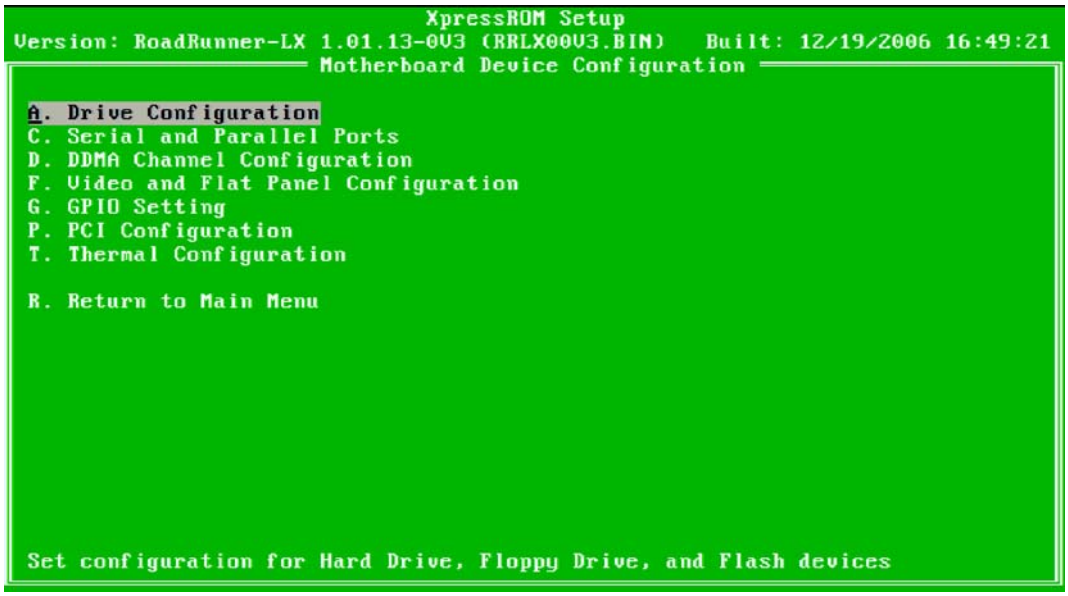
To move between fields in Setup, use the keys listed below:

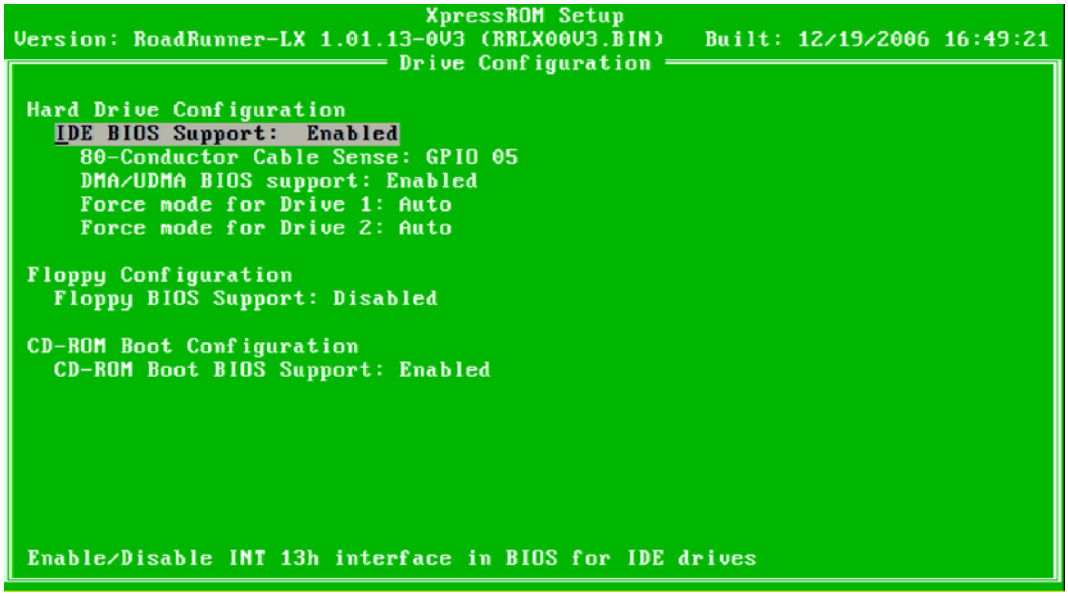
Key	Function
→, ←, ↓, ↑	Move between fields
+, -	Selects next/previous values in fields
Enter	Go to the submenu for the field
Esc	To previous field then to exit menu

In order to save your settings, select ***Save values and Exit*** and confirm with Y. Should you want to discard everything, select ***Exit Without Save***.

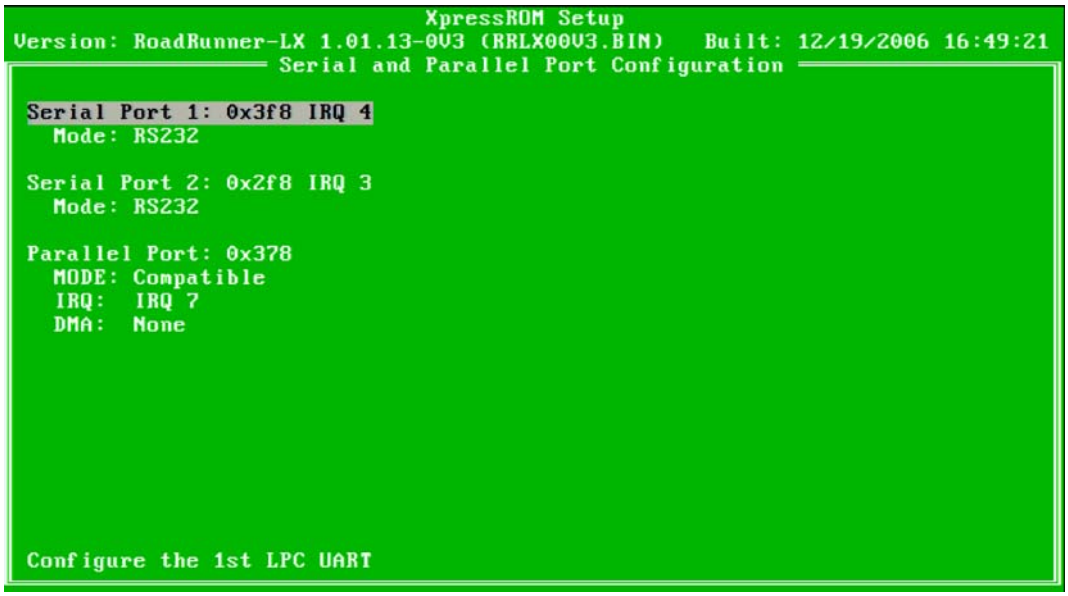
When troubleshooting a system, it is highly recommend to first restore the BIOS's factory settings before any debugging is done. This is achieved with ***Load Defaults*** in the main setup menu.

The ***Motherboard Device Configurations*** menu allows to configure the drives, LPC, DDMA, display, GPIO usage, and PCI configuration. The CPU's temperature can be read here, to.





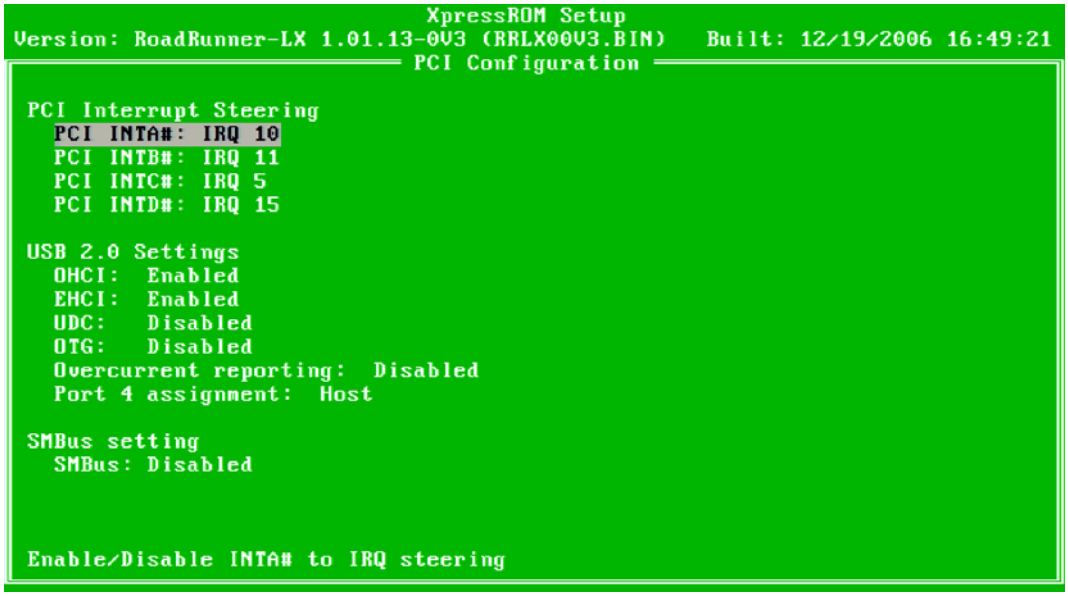
Hard Drive Setting	Choice
80-Conductor Cable Sense	GPIO05, NONE, Force 40, Force 80
Drive Modes	Auto, PIO0, PIO1, PIO2, PIO3, PIO4, MDMA0, MDMA1, MDMA2, UDMA0, UDMA1, UDMA2, UDMA3, UDMA4


XpressROM Setup
Version: RoadRunner-LX 1.01.13-0V3 (RRLX00V3.BIN) Built: 12/19/2006 16:49:21
Serial and Parallel Port Configuration
Serial Port 1: 0x3f8 IRQ 4
Mode: RS232
Serial Port 2: 0x2f8 IRQ 3
Mode: RS232
Parallel Port: 0x378
MODE: Compatible
IRQ: IRQ 7
DMA: None
Configure the 1st LPC UART

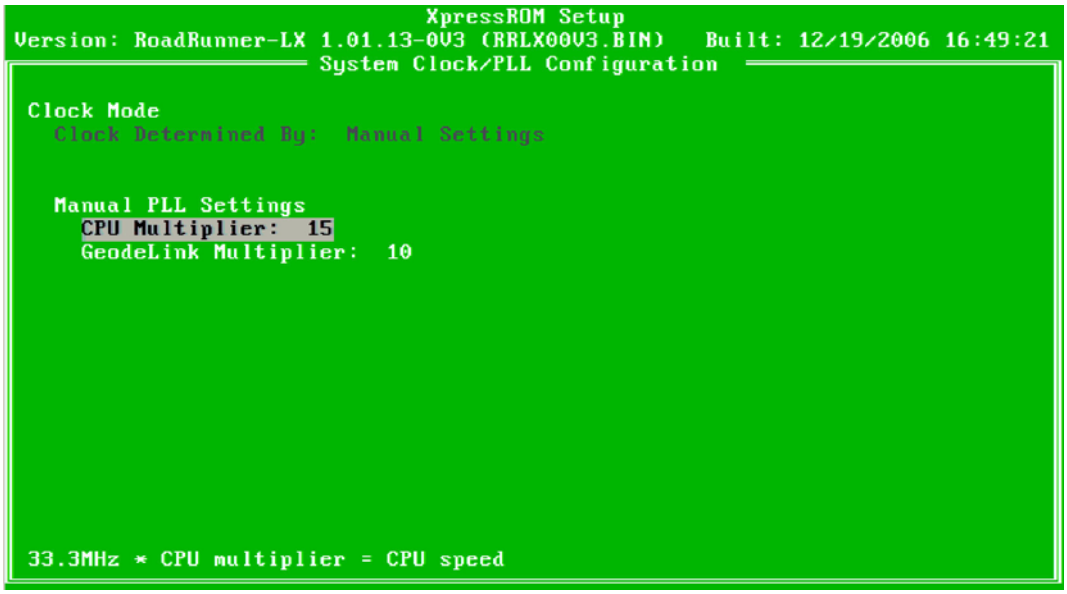
XpressROM Setup
Version: RoadRunner-LX 1.01.13-0V3 (RRLX00V3.BIN) Built: 12/19/2006 16:49:21
DDMA Configuration
DDMA Channels Mapped to ISA
DMA Channel 0 to ISA: Disabled
DMA Channel 1 to ISA: Disabled
DMA Channel 2 to ISA: Disabled
DMA Channel 3 to ISA: Enabled
DMA Channel 5 to ISA: Enabled
DMA Channel 6 to ISA: Disabled
DMA Channel 7 to ISA: Disabled
Enable/Disable mapping of DMA Channel 0 to ISA

XpressROM Setup
Version: RoadRunner-LX 1.01.13-0V3 (RRLX00V3.BIN) Built: 12/19/2006 16:49:21
Graphics Configuration
Internal Adaptor Mode: Disabled
Graphics Memory: 024
Output display: CRT
HSDIP Support: Disabled
HSDIP Memory Size: 004
Driver controls init: Disabled
DOTPLL Bypass: Disabled
Flat Panel Configuration
Type: LVDS
Resolution: 800x600
Data Bus Type: 9-24 bits, 1 ppc
Refresh Rate: 60 Hz
HSYNC Polarity: Active low
VSYNC Polarity: Active low
LP Active Period: Free running
SHFCLK Active Period: Free running
Software Backlight Control
Backlight Enable: Disabled
Initial Brightness: Last Value
Mode for internal controller when an external video device is present.

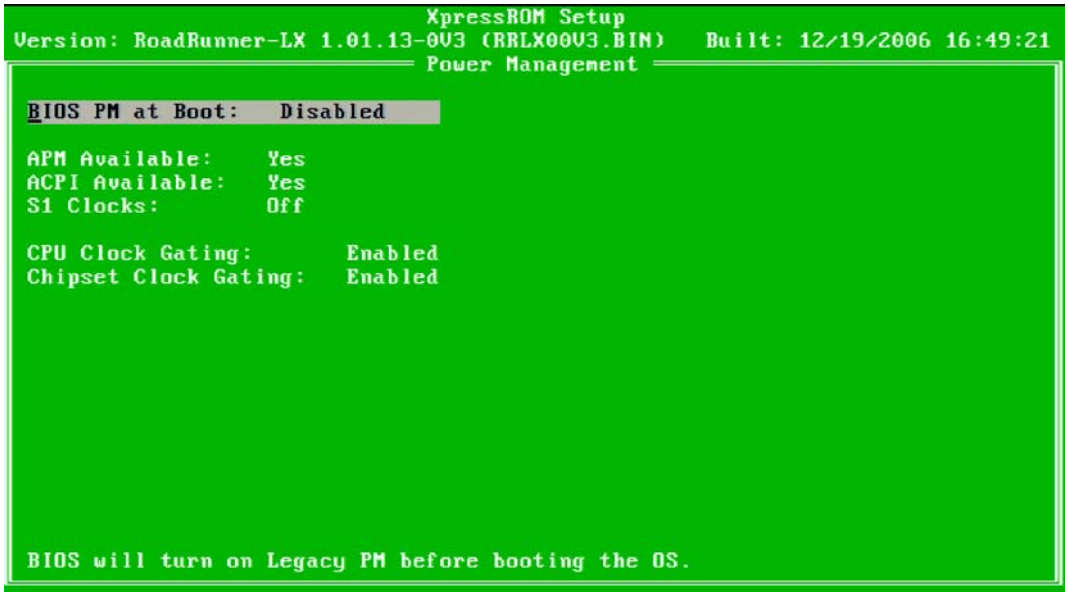
XpressROM Setup
Version: RoadRunner-LX 1.01.13-0V3 (RRLX00V3.BIN) Built: 12/19/2006 16:49:21
PCI Configuration
PCI Interrupt Steering
PCI INTA#: IRQ 10
PCI INTB#: IRQ 11
PCI INTC#: IRQ 5
PCI INTD#: IRQ 15
USB 2.0 Settings
OHCI: Enabled
EHCI: Enabled
UDC: Disabled
OTG: Disabled
Overcurrent reporting: Disabled
Port 4 assignment: Host
SMBus setting
SMBus: Disabled
Enable/Disable INTA# to IRQ steering


XpressROM Setup
Version: RoadRunner-LX 1.01.13-0V3 (RRLX00V3.BIN) Built: 12/19/2006 16:49:21
PCI Configuration
PCI Interrupt Steering
PCI INTA#: IRQ 10
PCI INTB#: IRQ 11
PCI INTC#: IRQ 5
PCI INTD#: IRQ 15
USB 2.0 Settings
OHCI: Enabled
EHCI: Enabled
UDC: Disabled
OTG: Disabled
Overcurrent reporting: Disabled
Port 4 assignment: Host
SMBus setting
SMBus: Disabled
Enable/Disable INTA# to IRQ steering

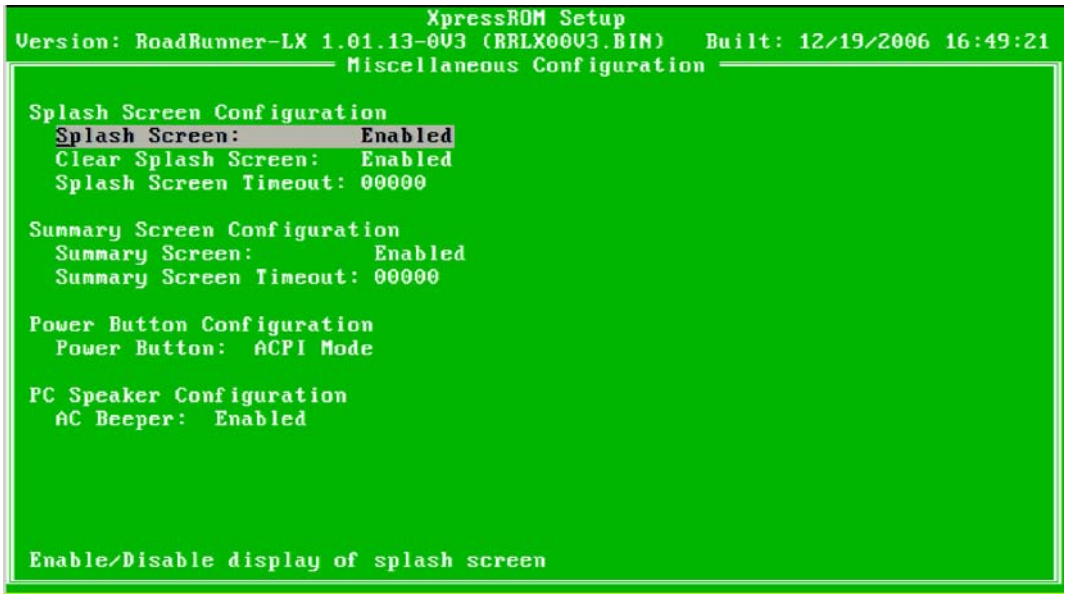
System Clock/PLL Configuration lets you define the CPU and PLL settigs.



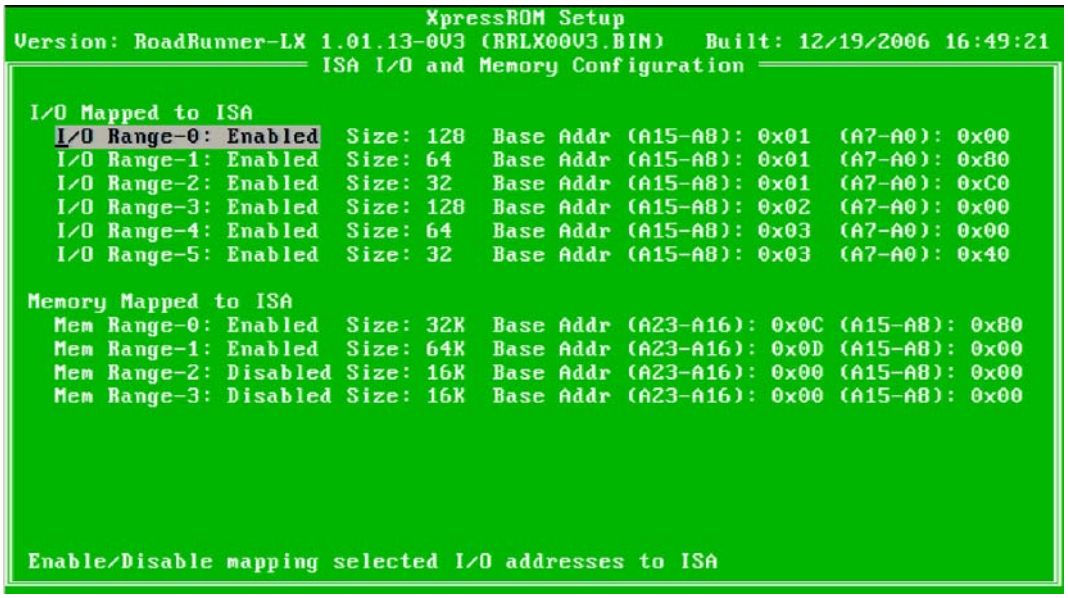
The ***Power Management*** menu gives control over power down modes supported.



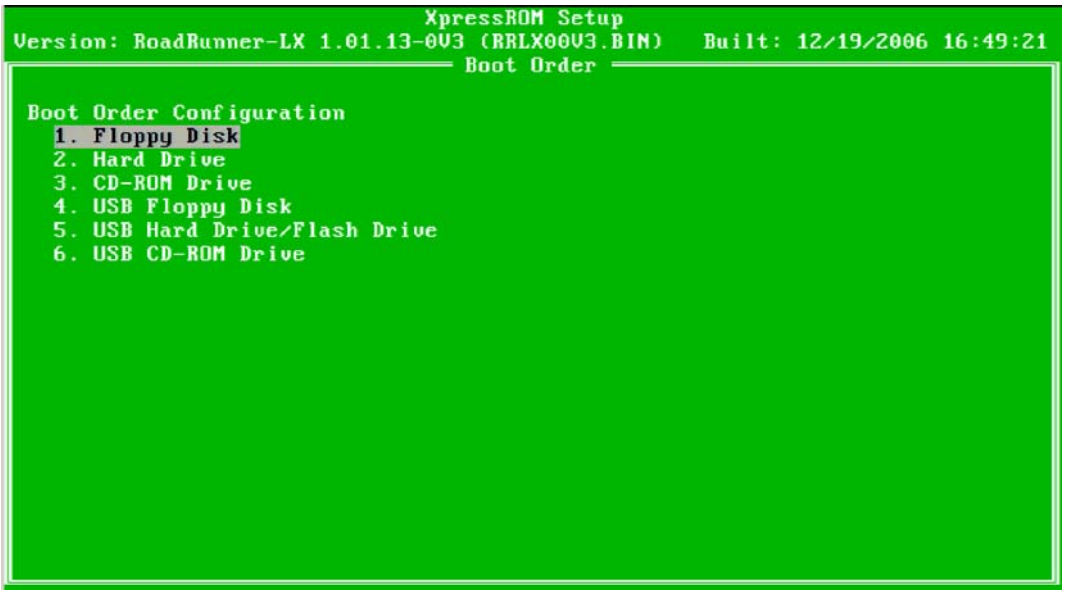
Miscellaneous Configuration controls various other features.



ISA I/O and Memory Configuration allows setting the boards ISA memory and I/O map.

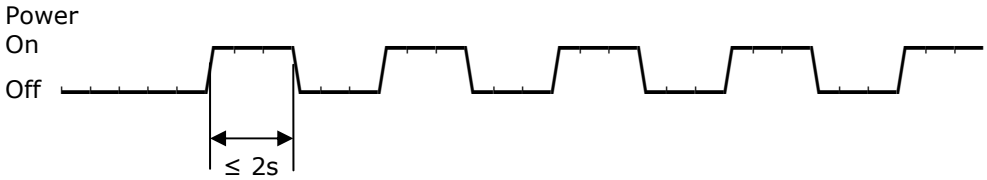


The menu Boot Order specifies the order in which the BIOS tries the various mass memory deices for a bootable operatig system.



Trouble Shooting BIOS Settings

It may happen that the BIOS is so badly configured that the Cool RoadRunner-LX800 does not start at all. To repair this, the default values of the BIOS can be automatically loaded at boot time. To load these, the power must be switched on and off again within 2 seconds. This sequence must be repeated 5 times, then the the default values get loaded by the BIOS.



Pressing the Reset-Button five times while the system is booting achieves the same result.

4.2 Drivers

Software drivers for sound, Ethernet, AES and graphics adapter are available for the Cool RoadRunner-LX800.

These drivers can be downloaded from LiPPERT's website http://www.lippert-at.com.

Follow the installation instructions that come with the drivers.

4.3 Programming GPIO Signals

The Cool RoadRunner-LX800 general purpose I/O signals (GPIO) are part of the ITE8712 SuperIO. They are located in Logical Device 7 of the SuperIO and can be programmed using in/out statements on Index/Data registers 2Eh/2Fh. GPIO's 1x belong to GPIO set #1, GPIO's 2x to set #2 and so on, up to set #5. The following lines show an example how to program GPIO Bank 1.

The code is meant to be compiled using gcc under Linux.

```
#include <sys/io.h>
#include <stdio.h>


#define CONF_ADDR 0x2E
#define CONF_DATA 0x2F
#define GPIO_ADDR 0x0393

//************************************************************
// InitGPIO: initialize GPIO Bank #4
// Parameter: mode: bit=1 -> set to GPIO
//            dir:  bit=1/0 -> set to output/input
//            (char = 8 bit)
// Returns: -
//************************************************************
void InitGPIO(char mode,char dir)
{
  // To set the SuperIO into configuration mode, the sequence
  // 0x87, 0x01, 0x55, 0x55 must be written to the configuration address.
  outb(0x87, CONF_ADDR);
  outb(0x01, CONF_ADDR);
  outb(0x55, CONF_ADDR);
  outb(0x55, CONF_ADDR);
  // Enable Logical Device 7 for programming by writing 07h to
  // register 07h of the SuperIO:
  outb(7, CONF_ADDR);           //Set to logic device
  outb(7, CONF_DATA);          //Number of logic device
  // Set GPIO-Set 4 Multifunction Pin Selection Register 28 to GPIO function
  // and enable the "simple I/O" function
  // Input: mode – each set bit represents a GPIO function
  outb(0x28, CONF_ADDR);      // set bank #4 to GPIO
  outb(mode, CONF_DATA);      // BIT: 1=GPIO , 0=other function
  outb(0xC3, CONF_ADDR);      // set to simple I/O
  outb(mode, CONF_DATA);      // BIT: 1=simple I/O , 0=not simple I/O
  // Define the GPIO's data direction
  // Input: dir – each set bit represents an output
  outb(0xCB, CONF_ADDR);      // set direction: output/input
  outb(dir, CONF_DATA);       // BIT: 1=output, 0=input
  outb(0xBB, CONF_ADDR);      // enable pull-ups if acting as output
  outb(dir, CONF_DATA);       // BIT: 1=pull up, 0=no pull up
  // Set the logical I/O address 0x393 for reading and writing values
  outb(0x62, CONF_ADDR);                        //IO base MSB
  outb((GPIO_ADDR & 0xFF00) >> 8, CONF_DATA);  // -> 0x03
  outb(0x63, CONF_ADDR);                        //IO base LSB
  outb((GPIO_ADDR & 0x00FF), CONF_DATA);       // -> 0x93
  // Reset configuration mode to "wait for Key"
  outb(0x02, CONF_ADDR);
  outb(0x02, CONF_DATA);
}


int main()
{
  char value1=0x55,value2;    //8 bit values
  iopl(3);                    //get all I/O rights
  InitGPIO(0xff,0xff);        //Initialize GPIO:
                              //set all to GPIO and all to output
  outb(value1, GPIO_ADDR);    //write out value1
  printf("Write=%x", value1);
  value2 = inb(GPIO_ADDR);    //read in value2
  printf(", Read=%x\n", value2);
  return 0;
}
```

For a more detailed description about programming the ITE8712 super I/O, please refer to chapter 8 of the datasheet.

4.4 Watchdog Programming

Since the Watchdog is disabled in delivery status, it must be set up for proper use.

The Watchdog is an internal feature of the ITE8712 Super I/O. If the Watchdog is activated and the timer is not set back within a programmed amount of time, the board does a system reset. In order to read back the watchdog event read Bit 0 of Watchdog status register 71h in LDN7.

The following program in C is an example how to test Watchdog function under DOS. Programming the Watchdog is quite similar programming GPIO's.

This routine is meant to be compiled using gcc under Linux.

```
#include <stdio.h>
#include <sys/io.h>
#include <unistd.h>

#define CONF_ADDR 0x2E
#define CONF_DATA 0x2F

int main()
{
  unsigned char i;
  iopl(3);
  outb(0x87, CONF_ADDR); // sets SIO in configuration mode (fix sequence:
                         // 0x87,0x01,x055,0x55)
  outb(0x01, CONF_ADDR);
  outb(0x55, CONF_ADDR);
  outb(0x55, CONF_ADDR);
  outb(0x07, CONF_ADDR); // LDN=0x07
  outb(0x07, CONF_DATA);
  outb(0x72, CONF_ADDR); // set time out value to seconds
  outb(inb(CONF_ADDR)|0x80, CONF_DATA);
  outb(0x73, CONF_ADDR); //set time out:
  outb(0x03, CONF_DATA); //0x03 -> 3 seconds
  printf("Watchdog enabled. Press CTRL+C within 5 seconds to stop resetting.\n");
  for(i=0; i<5; i++)
  {
    outb(0x73, CONF_ADDR); //reset time out
    outb(0x03, CONF_DATA);
    printf(".");
    fflush(stdout);
    sleep(1);
  }
  outb(0x73, CONF_ADDR);
  outb(0x00, CONF_DATA); //deactivate watchdog
  printf("\nWatchdog disabled\n");
  iopl(0);
  return 0;
}
```

4.5 Reading Temperatures

There are temperature sensors available that allow measurement of the CPU's chip temperature as well as the boards ambient temperature. These are shown in in the BIOS setup screens, see above.

This example is meant to be compiled using gcc under Linux.

```
#include <stdio.h>
#include <unistd.h>
#include <sys/io.h>

#define LPC_INDEX 0x295
#define LPC_DATA 0x296

int main()
{
  char cputemp = 0;
  char ambtemp = 0;

  iopl(3);

  //******* needed with BIOS prior version 7 ******
  outb(0x51,LPC_INDEX); //thermal diode mode
  outb(0x03,LPC_DATA);
  outb(0x5C,LPC_INDEX); //unlock offset regs
  outb(0x80,LPC_DATA);
  outb(0x56,LPC_INDEX); //offset adjustment CPU
  outb(0x70,LPC_DATA);
  outb(0x57,LPC_INDEX); //offset adjustment Ambient
  outb(0x3C,LPC_DATA);
  outb(0x5C,LPC_INDEX); //lock offset regs
  outb(0x00,LPC_DATA);
  //***************************************

  printf("Press CTRL+C to cancel!\nCPU AMBIENT\n");
  while(1)
  {
    outb( 0x29,LPC_INDEX); //read out CPU temp
    cputemp = inb(LPC_DATA);
    outb( 0x2A,LPC_INDEX); //read out Ambient temp
    ambtemp = inb(LPC_DATA);
    printf("%3d %3d\r", cputemp, ambtemp); //printout to the screen
    fflush(stdout);
    sleep(1);
  }
  return 0;
}
```

Handling of PWM Outputs

Programming the PWM outputs works the same way as using GPIO's.

Enter configuration mode and switch to logical device 7 (via 2Eh/2Fh).

Enable PWM outputs by setting

- Bit 6 of register 27h to '0' (SIO_PWM2)
- Bit 1 of register 29h to '0' (SIO_PWM3)
- Bits 3 and 4 of register 2Ch to '1' (SIO_PWM4+5)

Enable channels 1-3 by programming the following registers via LPC-Bus (295h/296h):

- Bits 2,1 and 0 of register 13h to '1'
- Bits 2,1 and 0 of register 14h to '1'

Set the global frequency by programming bits 6-4 of register 14h via LPC-Bus (295h/296h):

Bits 6, 5, 4	PWM frequency
000	375.000 KHz
001	187.500 KHz
010	93.750 KHz
011	62.500 KHz
100	46.875 KHz
101	23.430 KHz
110	11.700 KHz
111	5.870 KHz

Set Bit 3 of register 14h to '0' to allow duty cycles between 0...100%. (PWM/128*100%)

Duty cycles can be set different for each PWM channel by programming an 8 Bit value to registers16h for channel 2, 17h for channel 3, 88h for channel 4 and 89h for channel 5.

5 Address Maps

This section describes the layout of the CPU memory and I/O address spaces.

Note *Depending on enabled or disabled functions in the BIOS, other or more resources may be used*

5.1 Memory Address Map

Address Range		Address Range (Hex)			Size	Description
1024K	- 16384K	100000	-	FFFFFF	15360K	Extended Memory
960K	- 1023K	F0000	-	FFFFF	64K	System BIOS
936K	- 959K	EA000	-	EFFFF	24K	Unused
932K	- 935K	E9000	-	E9FFF	4K	ACPI
896K	- 931K	E0000	-	E8FFF	36K	Unused
800K	- 895K	C8000	-	DFFFF	96K	Mapped to ISA bus
768K	- 799K	C0000		C7FFF	32K	Graphics BIOS
736K	- 768K	B8000	-	BFFFF	32K	Color Text Memory
704K	- 736K	B0000	-	B7FFF	32K	Monochrome Text Memory
640K	- 704K	A0000	-	AFFFF	64K	Graphic Memory
0K	- 640K	0	-	9FFFF	640K	Conventional Memory

5.2 I/O Address Map

The system chip set implements a number of registers in I/O address space. These registers occupy the following map in the I/O space.

Address Range	Description
0000 - 000F	DMA-Controller
0020 - 0021	Programmable Interrupt controller
002E - 002F	System
0040 - 0043	System timer
0048 - 004B	System timer
004E - 004F	Super I/O
0060 - 0060	Keyboard
0061 - 0061	System speaker
0064 - 0064	Keyboard
0070 - 0073	System CMOS/Real-time clock
0080 - 008F	DMA-Controller
0092 - 0092	System
00A0 - 00A1	Programmable Interrupt controller
00C0 - 00DF	DDMA-Controller
00F0 - 00FF	Numeric Coprocessor
0100 - 017F	PCI-ISA Bridge Positive Decode Range 1
0180 - 01BF	PCI-ISA Bridge Positive Decode Range 2
01C0 - 01CF	PCI-ISA Bridge Positive Decode Range 3
01F0 – 01FF	IDE Controller
0200 - 027F	PCI-ISA Bridge Positive Decode Range 4
0279 - 0279	ISAPnP-Data port
0295 - 0296	LPC-Bus
02F8 - 02FF	COM2
0300 - 033F	PCI-ISA Bridge Positive Decode Range 5
0340 - 035F	PCI-ISA Bridge Positive Decode Range 6
0378 - 037F	LPT1
03B0 - 03BA	Advanced Micro Devices Win XP Graphics Driver
03C0 - 03DF	Advanced Micro Devices Win XP Graphics Driver
03F0 - 03F7	Standard-Floppy controller
03F8 - 03FF	COM1
0480 - 048F	DMA-Controller
04D0 - 04D1	Programmable Interrupt controller
0A79 - 0A79	ISAPnP-Data port
1200 - 1207	SPI-Flash
1220 - 1227	Simple-I/O (default)
DF80 - DFFF	Geode LX Audio Driver (WDM)
EFF0 - EFFF	Standard-Dual-Channel-PCI-IDE-Controller

5.3 Interrupts

IRQ	System Resource
NMI	Parity error
0	Timer
1	Keyboard
2	Secondary interrupt controller 2
3	Serial port 2
4	Serial port 1
5	Not used
6	FDD controller
7	Parallel port 1
8	Real time clock
9	ACPI controller
10	AMD Win XP graphics driver
10	Geode LX AES crypto driver
11	Geode LX audio driver (WDM)
11	Intel 82551IT PCI Ethernet adapter
11	Standard extended PCI-to-USB universal host controller
11	Standard OpenHCD USB host controller
12	PS/2 mouse
13	Numeric coprocessor
14	Primary IDE channel
15	Not used

Note Depending on the BIOS settings, it's possible to reserve several IRQ's for the PC/104 or Mini PCI bus

5.4 DMA Channels

DMA	Data width	System Resource
0	8 bits	Available
1	8 bits	Available
2	8 bits	Floppy
3	8 bits	Parallel Port
4		Reserved, Cascade Channel
5	16 bits	Available
6	16 bits	Available
7	16 bits	Available

5.5 PC/104 Bus Address Space

The PC/104 bus address space mapping can be changed in the BIOS setup. The table shows the factory default values.

Range	Start Address	End Address	Size	Description
I/O 0	100	17F	128 bytes	IT8712 Positive Decode I/O Range 1
I/O 1	180	1BF	64 bytes	IT8712 Positive Decode I/O Range 2
I/O 2	1C0	1DF	32 bytes	IT8712 Positive Decode I/O Range 3
I/O 3	200	27F	128 bytes	IT8712 Positive Decode I/O Range 4
I/O 4	300	33F	64 bytes	IT8712 Positive Decode I/O Range 5
I/O 5	340	35F	32 bytes	IT8888 Positive Decode I/O Range 6
Mem 0	C8000	CFFFF	32 Kbytes	Memory mapped to ISA
Mem 1	0D000	DFFFF	64 Kbytes	Memory mapped to ISA
Mem 2	-			Disabled
Mem 3	-			Disabled

Appendix A, Contact Information

Headquarters

LiPPERT Embedded Computers GmbH
Hans-Thoma-Straße 11
68163 Mannheim
Germany

Phone	+49 621 4321410
Fax	+49 621 4321430
E-mail	sales@lippert-at.com
	support@lippert-at.com
Website	www.lippert-at.com

US Office

LiPPERT Embedded Computers, Inc.
5555 Glenridge Connector, Suite 200
Atlanta, GA 30342
USA

Phone	+1 (404) 459 2870
Fax	+1 (404) 459 2871
E-mail	ussales@lippert-at.com
	support@lippert-at.com
Website	www.lippert-at.com

Appendix B, Additional Information

B.1 Additional Reading

AMD Geode™ LX Processors Data Book

AMD Geode™ CS5536 Companion Device Data Book

Datasheet LPC interface Winbond 83627HF, available at http://www.winbond.com

B.2 PC/104 and PC/104-Plus Specifications

A copy of the latest PC/104 and PC104-Plus specifications can be obtained from the PC/104 Consortium's website at http://www.pc104.org

Appendix C, Getting Help

Should you have technical questions that are not covered by the respective manuals, please contact our support department at **support@lippert-at.com** .

Please allow one working day for an answer!

Technical manuals as well as other literature for all LiPPERT products can be found in the *Products* section of LiPPERT's website www.lippert-at.com. Simply locate the product in question and follow the link to its manual.

Returning Products for Repair

To return a product to LiPPERT for repair, you need to get a Return Material Authorization (RMA) number first.
Please print the RMA Request Form from http://www.lippert-at.com/index.php?id=rma
fill in the blanks and fax it to +49 621 4321430. We'll return it to you with the RMA number.

Deliveries without a valid RMA number are returned to sender at his own cost!

LiPPERT has a written Warranty and Repair Policy, which can be retrieved from
http://www.lippert-at.com/index.php?id=rwp

It describes how defective products are handled and what the related costs are. Please read this document carefully before returning a product.

Appendix D, Revision History

Filename	Date	Edited by	Change
TME-104P-CRR_LX800-R0V0	2006-10-20	OF	Draft
TME-104P-CRR_LX800-R0V1	2006-11-28	OF	Corrected pinout of LVDS connector, added pinout of KB connector.
TME-104P-CRR_LX800-R0V2	2006-11-20	PK	New document structure and layout
TME-104P-CRR_LX800R1V0	2007-02-27	PK	BIOS screens corrected Super-I/O programming ISA mapping added
TME-104P-CRR_LX800R1V1	2007-06-23	PK	Supervisory connector corrected
TME-104P-CRR_LX800R1V2	2007-10-08	CS	Ch. 3.5: CF description corrected Ch. 3.8: EIDE description corrected
TME-104P-CRR_LX800R1V3	2007-10-17	PK	Ch. 3.17: LED description improved Ch. 1.3: Inrush current specified MTBF specified
TME-104P-CRR_LX800R1V4	2007-10-24	PK	Ch. 3.4: VGA connector added Appendix C inserted
TME-104P-CRR_LX800R1V5	2007-11-30	MS PK	New code examples Chapter "LED indicators" moved
TME-104P-CRR_LX800R1V6	2007-12-07	PK	LPT connector, pin 26 corrected
TME-104P-CRR_LX800R1V7	2008-01-20	PK	BIOS default loading: description streamlined