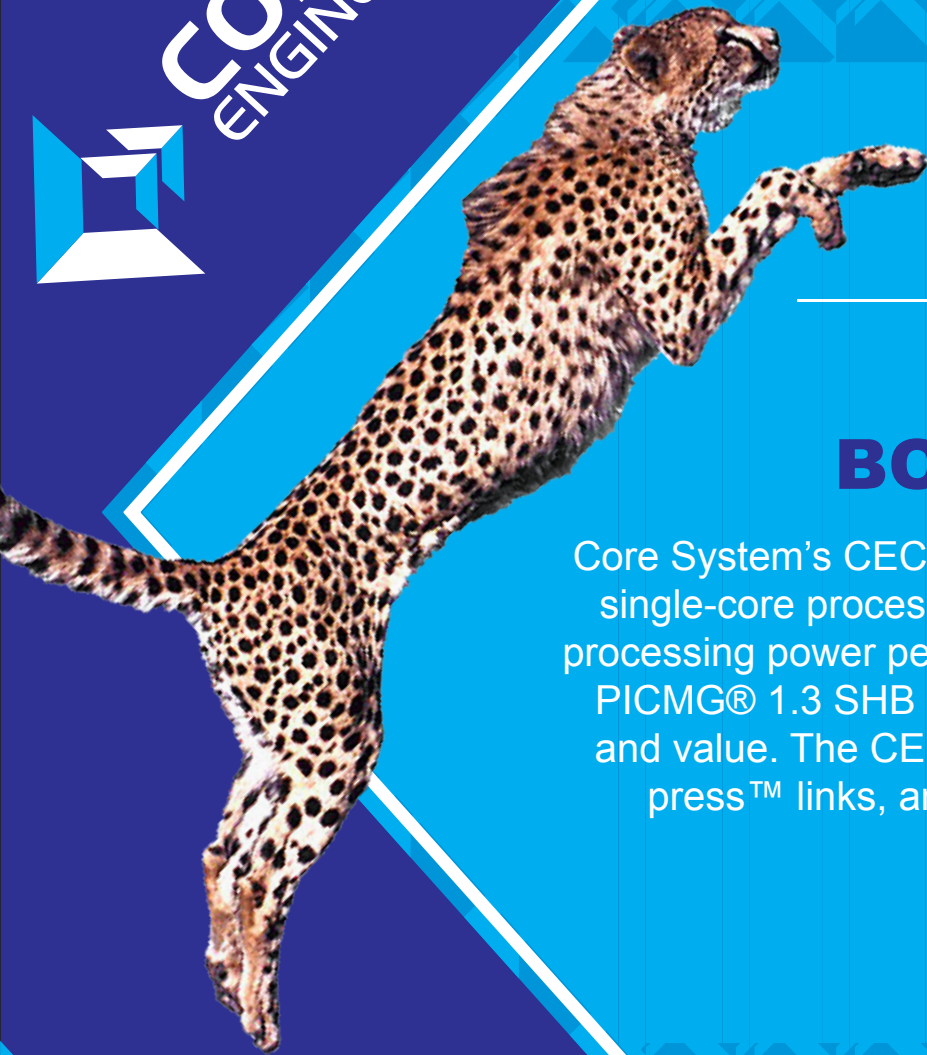




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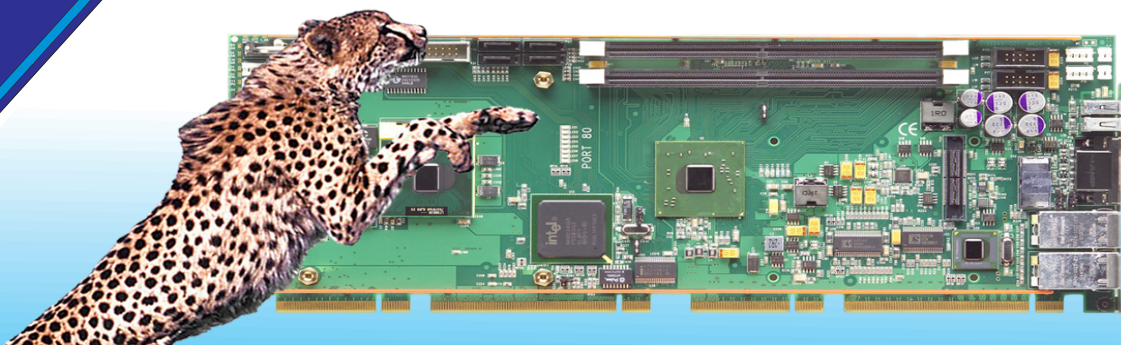
CHEETAH SERIES

CECD SINGLE BOARD COMPUTER

Core System's CECD features low power, dual-core and single-core processor options that maximize the SHB's processing power per watt efficiency. This graphics-class PICMG® 1.3 SHB offers power efficiency, performance and value. The CECD supports x16, x4 and x1 PCI Express™ links, and a 32-bit/33MHz PCI interface to a PICMG 1.3 backplane.

PRODUCT DATA SHEET

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PROCESSOR

Intel® Core™ Duo Processor at 1.66GHz to 2.0GHz*
Intel® Core™ Solo Processor at 1.66GHz to 1.83GHz*
Intel® Celeron® M Processor at 1.6GHz*
Processor Package: FC-PGA6, plugs into a mPGA 478 socket

*Higher speeds as available

CHIPSET

The CECD's Intel® 945G chipset combines advanced video and graphics capabilities with high-bandwidth interfaces such as a dual-channel DDR2-667, PCI Express x16 graphics port and PCI Express x4 and x1 links to a PICMG 1.3 backplane. An Intel® ICH7R I/O Controller Hub provides eight USB 2.0 and four SATA/300 ports. The ICH7R's SATA controller supports independent DMA, Advanced Host Controller Interface (AHCI) and integrated RAID level 0, 1, 5 and 10 functionality. The I/O Controller Hub's LPC interface is routed to the board's controlled impedance connector and supports an optional I/O expansion board (Core's CE-00030) for legacy I/O and serial port communications. A x1 PCI Express (PCIe) link is also routed from the ICH7R to the controlled impedance connector to provide an additional x1 PCIe link to a PICMG 1.3 backplane when using Core's Ce-00031 board. Communications between the Intel® 945G Memory Controller Hub and the Intel® ICH7R I/O Controller Hub occurs over Direct Media Interface (DMI) at a data transfer rate of 10Gb/s in each direction.

ETHERNET INTERFACES

The CECD uses an internal x1 PCI Express link to connect the I/O Controller hub to a dual-port Gigabit Ethernet (Intel® 82571EB) controller chip. This design feature enables dual 10/100/1000Base-T Ethernet interfaces on LAN 1 and LAN2. The LAN ports on the CECD have RJ-45 connectors on the I/O bracket to provide the mechanical interfaces to the Ethernet networks. The ICH7R's internal LAN Interconnect Interface (LCI) connected to the Intel® 82562G1 Ethernet controller chip to provide an additional 10/100Base-T Ethernet interface for use on PICMG® 1.3 backplanes via the SHB's edge connector C.

FOUR SERIAL ATA/300 PORTS

The primary and secondary Serial ATA (SATA) ports on the CECD board support four independent SATA storage devices such as hard disks and CD-RW devices. SATA produces higher performance interfacing by providing data transfer rates up to 300MB per second on each port. The CECD's ICH7R I/O Controller hub features Intel® Matrix Storage Technology, which allows the ICH7R's SATA controller to be configured as a RAID controller supporting RAID 0, 1, 5, and 10 implementations.

CACHE MEMORY (L2 AND L1)

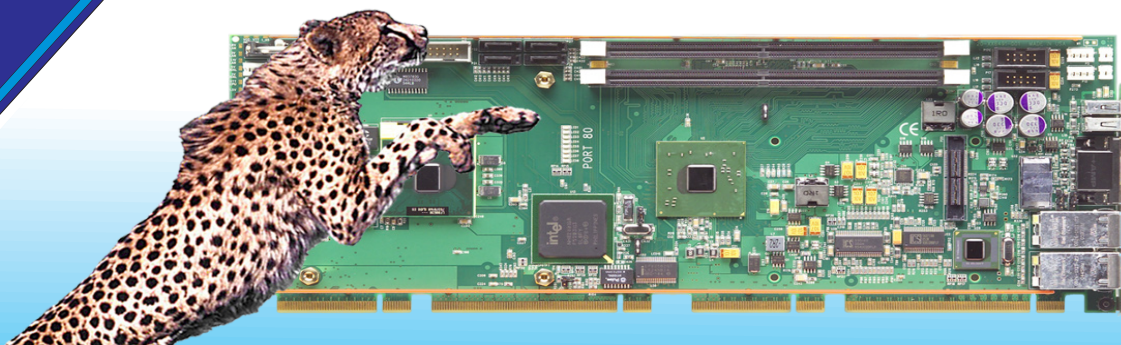
The Intel® Core™ Duo Processor and the Intel® Core™ Solo Processor has a level two (L2) cache memory integrated on-die with Advanced Transfer Cache memory that is 8-way set associative with ECC and runs at the full processor core frequency. The L2 cache memory size on both types of processor is 2MB. The L2 cache is shared between the two cores of the Intel® Core™ Duo Processor.

The Intel® Core™ Duo Processor has two 32KB L1 cache memories and the Intel® Core™ Solo Processor has single 32KB L1 cache.

The Intel® Celeron® M processors feature a 1MB level two (L2) cache memory and a 32KB L1 cache.

All processor options supported on the TML have a 16KB level one (L1) data cache.

CECD SINGLE BOARD COMPUTER



DDR2-667 MEMORY

The DDR2-667 memory interface is a dual-channel interface originating at the Memory Controller Hub, with each channel terminating at a DIMM module socket. The CECD supports system memory transfer rates of either 400, 533 or 667MHz using unbuffered, non-ECC, Pc2-3200, PC2-4200 or PC2-5300 DIMMs. Maximum memory capacity is 4GB. When using a single PC2-5300 DIMM, the memory interface bandwidth is 5.4GB/s and using two DIMMs with equal memory capacities increases the peak memory bandwidth to 10.7GB/s. To maximize system performance and reliability Core recommends using DIMMs that support the Serial Presence Detect (SPD) data structure.

MEMORY DIMM SLOT POPULATION

Core's CECD supports two types of memory operations:

Interleaved Mode - This is the mode of operation that enables the highest memory interface speed and bandwidth throughput capability. Often times this mode of operation is referred to as "dual-channel mode". Interleaved mode occurs when using two DIMM modules with equal memory capacities. The DIMM technology and device width can vary but the installed memory capacity for each channel must be equal. If different speed DIMMs are used in each channel then the slowest DIMM will determine the memory interface speed.

Asymmetric Mode - From a system operational standpoint, asymmetric mode functions as a "single-channel" memory interface. Asymmetric mode occurs when using either a single DIMM module or two DIMM modules with unequal memory capacities. The DIMM technology and device width can vary in each channel and if different speed DIMMs are used in each channel then the slowest DIMM will determine the memory interface speed.

NOTE: Double-sided DIMMS with a x16 organization are not supported.

POWER REQUIREMENTS

Typical Values - System Idling In Windows XP Desktop

CPU	+5V	+12V	+3.3V
2.0GHz*	2.20A	0.75A	2.75A
1.66GHz*	2.10A	0.70A	2.75A

Typical Values - 100% Stressed via MS Windows HCT's System Stress

CPU	+5V	+12V	+3.3V
2.0GHz*	3.50A	2.00A	3.00A
1.66GHz*	3.40A	1.40A	3.00A
-12V @	<100mA		

Tolerance for all voltages is +/- 5% and must be applied by the PICMG 1.3 backplane to edge connector C.

(*)Intel® Core™ Duo T2500, (#) Intel® Core™ Solo T1300

EIGHT USB INTERFACES

A total of eight USB 2.0 interfaces are supported by the CECD. USB ports 0 and 1 are on the I/O bracket and ports 2, 3, 4 and 5 have header connectors on the CECD. USB ports 4 and 5 can be routed to edge connector C for use on a PICMG® 1.3 backplane. The backplane routing for USB 4 and 5 is a factory-build option. Contact Core for ordering details. USB ports 6 and 7 are routed directly to the CECD's edge connector C.

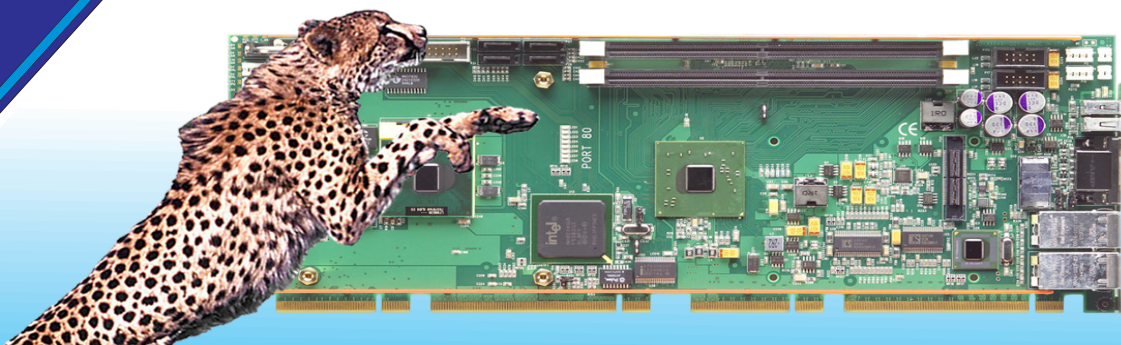
BATTERY

Built-in lithium battery for data retention of CMOS memory.

STANDARDS

- PCI Express Base Specification 1.0a
- SHB Express™ System Host Board PCI Express specification
- PCI Industrial Computer Manufacturers Group (PICMG®) 1.3

CECD SINGLE BOARD COMPUTER



PCI EXPRESS™ INTERFACES

Core's CECD graphics-class system host board provides one x16 PCI Express link on the SHB's edge connectors A and B. This x16 PCIe link is designed to support PCI Express video/graphics cards on an SHB Express™ (PICMG 1.3) backplane. A x4 PCI Express link and five PCI Express reference clocks are also included on edge connectors A and B.

An additional x1 PCI Express link between the CECD and backplane can be provided by Core's optional CE-00031 I/O Expansion Module.

The x4 and x1 PCI Express links are used on SHB Express backplanes to support PCI Express option cards and the bridge chips that provide PCI/PCI-X option card support. During system initialization the CECD automatically negotiates with the PCI Express cards connected to the PCI Express links in order to set up communication between the devices.

The net result is that the CECD system host board supports communication to x1, x4, x8 and x16 PCI Express boards as well as PCI/PCI-X cards via PCI Express-to-PCI/PCI-X bridge chip technology.

The CECD also provides a 32-bit/33MHz PCI bus interface on edge connector D.

PCI EXPRESS™ CONFIGURATION AND BUS SPEED

PCI Express - - One x16 link, one x4 link
Edge Connector A & B - Five reference clocks
PCI Express - (on-board only) - Two x1 links
PCI - 32-bit/33MHz
System or FSB - 667MHz, 533MHz

BIOS (FLASH)

The CECD uses AMIBIOS8®. The flash BIOS resides in the Firmware Hub (FWH). AMIBIOS8 contains features such as: Support for flash devices for BIOS upgrading Integrated support for USB mass storage devices such as USB CD-ROM, CD-RW, etc.

Boot from network, USB mass storage devices, IDE or ATAPI
Serial port console redirection to support headless operation (requires optional CE-00030 or CE-00031)
SATA/ATA/ATAPI support includes 48-bit LBA addressing to support SATA/ATA/IDE hard drive capacities over 137GB

VIDEO INTERFACE

The CECD supports three video connection options: Direct connection via the chipset's Intel® Graphics Media Accelerator 950 with faster graphics and 3D performance A x16 PCI Express graphics port that provides 3.5 times more bandwidth than an AGP 8X interface ADD2 video and graphic cards

CE-00030 EXPANSION BOARD (OPTIONAL)

This optional board provides legacy I/O connections via the Super I/O controller (LPC47B272). The CE-00030's I/O controller connects to the CECD's LPC Bus via the board's controlled impedance connector.

CE-00031 EXPANSION BOARD (OPTIONAL)

The CE-00031 supports all of the same I/O functions as the CE-00030 using cable header connectors. There is no I/O plate on the CE-00031. The CE-00031 also provides a x4 PCI Express edge connector designed to fit into a PCI Express expansion slot on a PICMG 1.3 backplane. When used on the CECD system host board, the CE-00031 provides an extra x1 PCI Express link to the backplane.

The following I/O interfaces are supported by the CECD via either the CE-00030 or CE-00031:

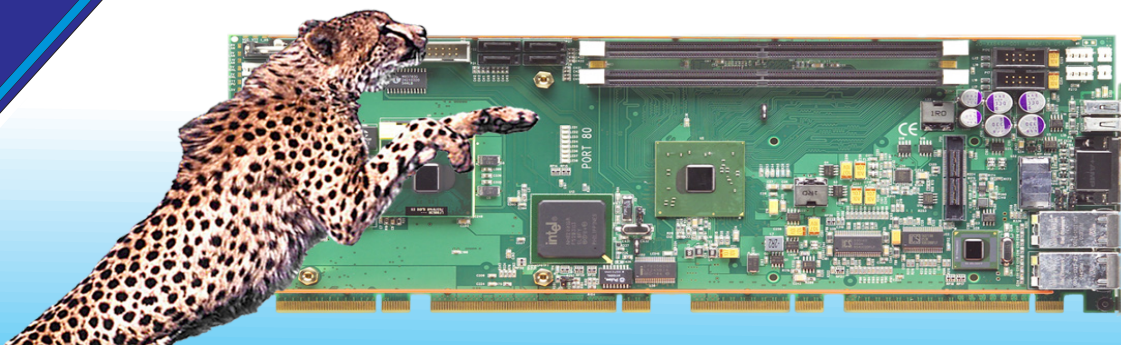
SERIAL INTERFACE

The Super I/O controller supports two full-function serial ports with independently programmable baud rates. The controller has two high-speed, NS16C550 compatible UARTs with Send/Receive 16-byte FIFOs. The IRQ for each serial port has BIOS selectable addressing.

FLOPPY DRIVE INTERFACE

The CE-00030 supports up to two floppy disk drives in combinations of 360K to 2.88MB

CECD SINGLE BOARD COMPUTER



KB AND PS/2 MOUSE INTERFACES

The mini DIN connector located on the I/O bracket provides an external interface for a PS/2 mouse and keyboard. A "Y" adapter plugged into the mini DIN connector allows the PS/2 mouse and keyboard to share the same port. Internal PS/2 mouse and keyboard headers are also available. A self-resetting fuse protects the +5V line of the keyboard and the mouse

PARALLEL INTERFACE

The parallel port interface is compatible with IBM PC/XT®, PC/AT®, PS/2™, Enhanced Parallel Port (EPP1.7, EPP1.9) and Extended Capabilities Port (ECP) modes of operation. Both the EPP and ECP modes are IEEE 1284 compliant. The parallel port has BIOS selectable addressing.

Operating systems exhibit certain boot-up behaviors in regards to the handling of keyboard controller functions that may necessitate the addition of the CE-00030 or CE-00031 to the CECD.

The operating systems that Core has tested that do not require the CE-00030 or CE-00031 are:

- Microsoft® Windows® 2000
- Microsoft® Windows® XP
- Microsoft® Windows® 2003 Server
- Microsoft® Windows® NT 4.0
- RedHat Linux 9.0
- Fedora Core 2.0
- SUSE Linux 9.0

The operating systems that Core has tested that require the CE-00030 or CE-00031 in order to provide required PS/2 keyboard functions are:

- Unixware® 7.11
- Sun® Solaris™ 9.0
- SCO ODT 5.05

MEAN TIME BETWEEN FAILURES (MTBF)

198,407 POH (Power-On Hours) at 40 °C., per Bellcore

TEMPERATURE/ENVIRONMENT

Operating Temperature: 0° to 60° C.
Airflow Requirement: 200LFM continuous airflow when using the passive heat sink
Storage Temperature: -40° to 70° C.
Humidity: 5% to 90% non-condensing

PASSIVE COOLING SOLUTION: The CECD has a board stack-up height of .76" (1.93cm) with the SHB's passive heat sink cooling solution. There are no cooling fans needed on the CECD system host board to achieve the 0° to 60° C operating temperature range. However, adequate airflow of at least 200LFM must always be present across the SHB's passive heat sink. Failure to provide adequate airflow will cause unexpected SHB shut downs that may eventually result in damaging the processor.

ACTIVE COOLING SOLUTION: The CECD's optional active cooling solution has a cooling fan mounted on the passive heat sink resulting in a board stack-up height of 1.16" (2.95cm). Order the CECD's active cooling option when 200LFM or more of continuous airflow is not available for the processor. Chassis designs that provide airflow and adequate venting are recommended.

MECHANICAL

In a typical backplane, the CECD's passive cooling solution enables placement of option cards approximately .78" (1.98cm) away from the top component side of the SHB. The optional active cooling solution requires the placement of option cards more than 1.18" (3.00cm) away from the SHB. The CECD's overall dimensions are 13.330" (33.858cm) L x 4.976" (12.639cm) H. The relative PICMG 1.3 SHB height off the backplane is the same as a PICMG 1.0 SBC due to the shorter PCI Express backplane connectors.

AGENCY APPROVALS & INDUSTRY COMPLIANCE

Designed for UL60950, CAN/CSA C22.2 No. 60950-00, EN55022:1998 Class B, EN61000-4-2:1995, EN61000-4-3:1997, EN61000-4-4:1995, EN61000-4-5:1995, EN61000-4-6:1996, EN61000-4-11:1994

