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Rev. A

SA.45s Chip-Scale Atomic Clock User's Guide

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Notices

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1 INTRODUCTION

The Symmetricom Model SA.45s Chip-Scale Atomic Clock (CSAC) is the world's smallest, lowest power atomic clock technology. The low power consumption of the CSAC, less than 125 mW, enables atomic timing accuracy in portable, battery-powered applications.

This manual provides technical guidance to facilitate mechanical, electrical, and functional integration of the CSAC into Users' systems and applications. Please contact Symmetricom's Applications Support group for further assistance or support for non-standard applications.

This manual also describes the CSAC **Developer's Kit** (Part # 990-00123-000), which includes an evaluation board, cabling, and the **CSACdemo** software interface. Installation and use of the **Developer's Kit** is presented in **Section 4** of this User's Guide. The descriptions of CSAC functionality in **Section 5** include examples from the **Developer's Kit**. **Section 6** contains detailed programming information for systems' integrators.

2 REFERENCE DOCUMENTS

For additional documentation, please contact your Symmetricom sales representative or visit us online at www.symmetricom.com.

3 CSAC OVERVIEW

3.1 PRECAUTIONS



Caution: To avoid electrostatic discharge (ESD) damage, proper ESD handling procedures must be observed in unpacking, assembling, and testing the CSAC.

The CSAC is delivered in ESD-safe packaging. The CSAC should only be removed from the ESD-protective bag in an ESD-safe environment. Once installed on the test fixture, the ESD sensitivity is considerably reduced. However, it is recommended that the entire assembly be treated as ESD-sensitive insofar as possible.

3.2 PACKAGING

Please retain the original CSAC ESD-safe packaging material in the event that the device needs to be returned to Symmetricom for service.

3.3 ABSOLUTE MAXIMUM RATINGS

Table 1 indicates the absolute maximum ratings to which the CSAC can be subjected without permanent unrecoverable damage. Note that the CSAC cannot be expected to operate normally when operated outside of the **Recommended Operating Conditions** (see **Table 3**). All ratings apply at 25°C, unless otherwise noted.

Parameter	Rating
Supply Voltage (Vcc)	4.1 V
Analog Tuning Voltage	Vcc
Maximum current draw	1 PPS in, RS232, BITE: +/- 2 mA 1 PPS out, 10 MHz out: +/- 20 mA
Storage Temperature	-40°C to +90°C

Table 1: Absolute Maximum ratings

3.4 MECHANICAL INTERFACE AND MOUNTING CONSIDERATIONS

The physical dimensions of the SA.45s CSAC are 1.6" x 1.4" x 0.45" H. Detailed dimensions are shown in **Figure 1**.

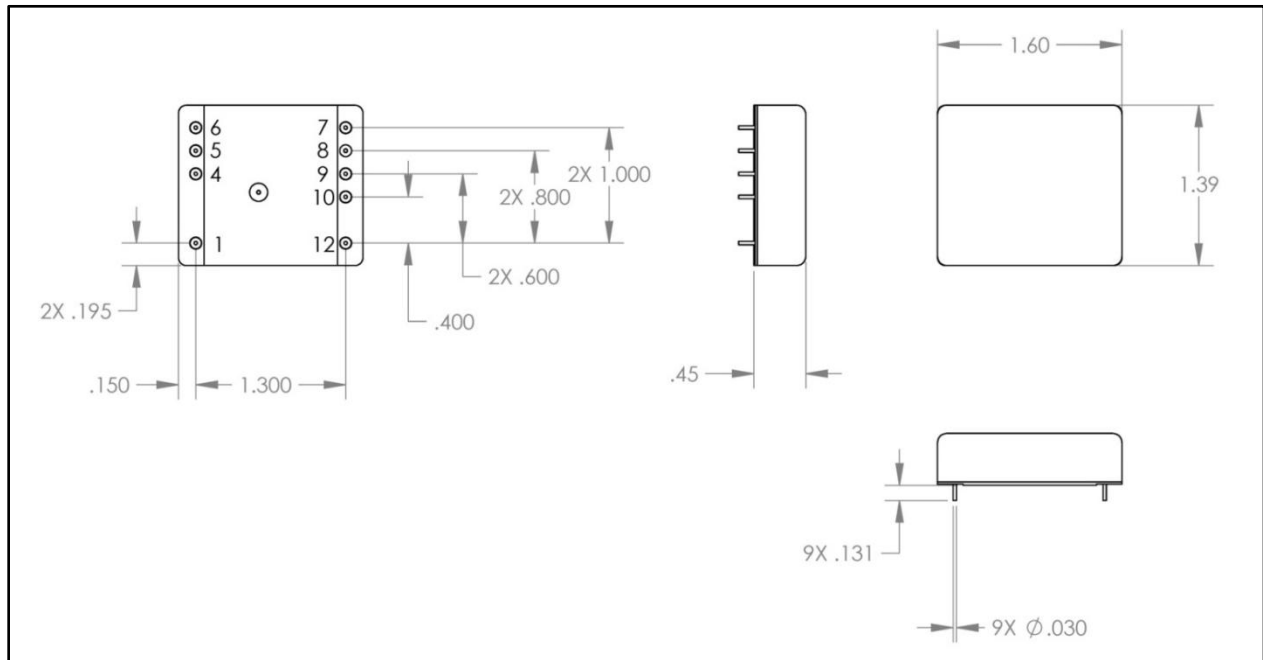


Figure 1: CSAC Mechanical drawing

The pinout of the SA.45s CSAC is shown below.

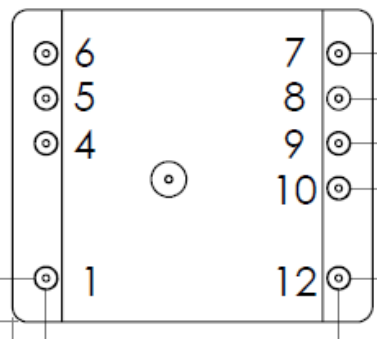
PIN	I.D.	 Bottom View
1	Tune	
2	N/A	
3	N/A	
4	BITE	
5	Tx	
6	Rx	
7	V _{CC}	
8	GND	
9	1 PPS IN	
10	1 PPS OUT	
11	N/A	
12	10 MHz OUT	

Table 2: SA.45s CSAC Pinout

Pins labeled “N/A” are not present in the SA.45s.

For initial testing and evaluation it is recommended that the pins should not be modified or soldered to a PCB. The recommended socket for PCB attachment is **Tyco P/N 4-5332070-4**.

3.5 RECOMMENDED OPERATING CHARACTERISTICS

The SA.45s pinout is defined in **Table 2**. The electrical function of each pin is defined in this section. Refer to the **Reference Section** describing each pin for a more complete definition of functionality.

Pin	Function		Notes	Reference Section
1	Analog Tuning Input	0-2.5V	1	5.10
4	$\overline{\text{Lock}}$ (BITE)	Logic H > 2.5 V Logic L < 0.5 V	2	5.2
5/6	RS232	2.5 V < Logic H < Vcc 0 V < Logic L < 0.5		6.1
7	VCC	3.3 VDC +/- 0.1 VDC		
8	Ground			
9	1 PPS in	2.5 V < Logic H < Vcc 0 V < Logic L < 0.5	3	5.7
10	1 PPS out	2.5 V < Logic H < Vcc-0.2 V 0 V < Logic L < 0.5	4, 5	5.6
12	10 MHz out	2.5 V < Logic H < Vcc-0.2 V 0 V < Logic L < 0.5	5	5.3

Table 3: Recommended Operating Characteristics

Notes:

- 1: Analog Tuning Input sensitivity is $\frac{\Delta f}{f} = (V_{\text{TUNE}} - 1250 \text{ mV}) \times 1.77 \times 10^{-11} / \text{mV}$.
- 2: Built-in Test Equipment (BITE) output:
0: Normal Operation
1: Unlock Condition
- 3: Timing reference is *rising edge* of input pulse
- 4: Output 1 PPS is 400 μ s in duration. Timing reference is the *rising edge* of Pin 10. Risetime < 5 ns.
- 5: Measured with Iout < 20 μ A

4 DEVELOPER'S KIT

The CSAC Developer's Kit includes all of the necessary hardware, software, and cabling to facilitate validation of performance, brassboard demonstrations, and software interface development.

4.1 PACKAGE CONTENTS:

The Developer's Kit (Part # 990-00123-000) includes:

Item	Symmetricom Part Number	Notes
Evaluation Board	054-00279-000	
Power Adapter	140-00041-000	5 VDC 5mm center positive
RS232 Cable	060-00322-000	
CD-ROM	066-00258-000	

Table 4: Contents of the CSAC Developer's Kit (part # 990-00123-000)

Please contact Symmetricom if any of these items are missing.

4.2 INSTALLING THE CSAC ON THE TEST FIXTURE



Caution: To avoid electrostatic discharge (ESD) damage, proper ESD handling procedures must be observed in unpacking, assembling, and testing the CSAC Prototype.

Remove the CSAC and evaluation board from their ESD protective bags only in an ESD-safe environment. Note that the SA.45s pinout is “keyed” (see **Table 2**) so the CSAC can only be inserted in the proper orientation. Gently insert the CSAC into the socket on the evaluation board as shown in **Figure 2** below.



Figure 2: CSAC on evaluation board

4.3 INSTALLING THE CSACdemo SOFTWARE

The Symmetricom **CSACdemo** software (Part # 084-00365-000) provides a convenient graphical user interface for monitoring and controlling the SA.45s CSAC. **CSACdemo** also is used for collecting and archiving monitor data from the CSAC. It will install and run on any PC running Microsoft Windows® XP or Windows® 7 and having at least one available RS232 (COM) port. Note that multiple CSACs can be monitored from a single PC, provided additional COM ports are available.

To install the **CSACdemo** software, insert the provided CD-ROM into the CD drive of the PC. If installation does not start automatically, browse to the CD-ROM drive in Windows Explorer and double-click on **setup.exe** in the root directory of the CD-ROM or click on **Run...** on the Windows **Start** menu and type “**x:\setup.exe**” where “**x**” is the drive letter (typically “d” or “e”) of your CD drive.

Upon accepting all of the default installation options (recommended), the **CSACdemo** software will be installed in **c:\Program Files\Symmetricom\CSAC**, a startup icon will be added to the **Start→All Programs→Symmetricom→Symmetricom** menu, and a **CSACdemo** icon will be placed on the desktop.

4.4 CABLING

Connect the provided RS-232 cable between the evaluation board and the COM port on the PC. On laptops without an available COM port, a USB-to-RS232 adapter might work. We have tested many of these. Most of them work, some do not.

Make sure the power switch on the evaluation board is in the off position as shown in **Figure 3**. Connect the 5V power adapter between the 5V power input and a 120 VAC wall outlet.

CSAC signal outputs are available from the evaluation board on connectors **J3** (10 MHz) and **J5** (1 PPS). Connect either (or both) of these to your test equipment (frequency counter, spectrum analyzer, etc.)

4.5 EVALUATION BOARD OVERVIEW

Detailed schematics of the evaluation board are provided in A. **Figure 3**, below, shows the connections to the evaluation board.

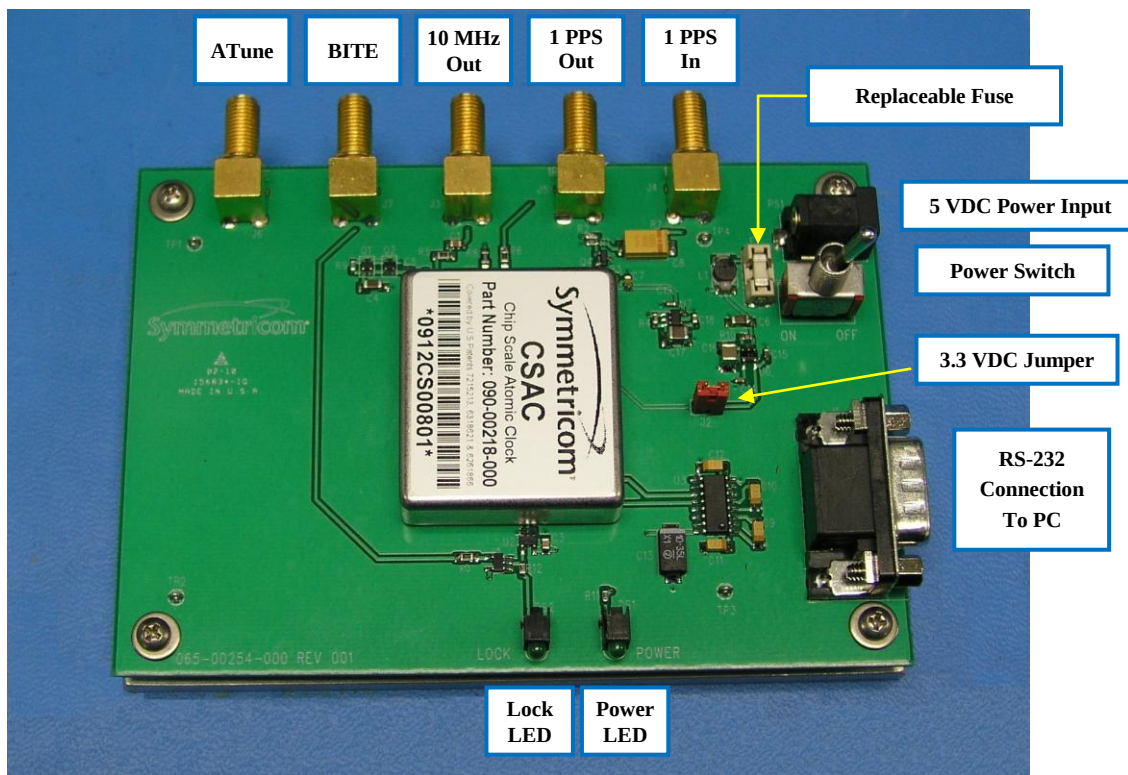


Figure 3: Test Fixture Connections

10 MHz Output (SMA) – The CSAC output is a 10 MHz, CMOS 0-3.3VDC waveform. A high-speed buffer (U1) on the evaluation board converts the CMOS output to an AC-coupled output capable of delivering 10 dBm to a 50Ω load.

3.3 VDC Jumper – The evaluation board provides regulated 3.3 VDC to the CSAC. In order to allow convenient measurement of the CSAC power consumption, a jumper is provided in the Vcc connection to the CSAC. To measure the CSAC current draw, turn off the evaluation board and install a low-impedance current meter in place of the jumper. Observe proper ESD protocols in making this measurement.

Replaceable Fuse – Replacement fuse: Littelfuse Part No. 0453 01.5

5 VDC Input – Input power to the evaluation board is provided on a 5 mm (center positive) coaxial connector (PS1). To avoid damage to the test fixture, it is highly recommended to use only the power adapter which provided by Symmetricom with the **Developer's Kit**.

RS232 Connection (DB9M) –The evaluation board provides a level shifter (U3), which converts the CSAC 0-3.3 VDC serial interface to the RS232 standard +/- 12 V for direct interface with a PC COM port. Connect the test fixture (J1) to a PC with a standard (non-Null) DB9F-DB9F RS232 cable. To avoid complication, please use the proper cable which is provided by Symmetricom with the **Developer's Kit**.

Lock Indicator LED – Indicates normal operation following initial acquisition of the clock signal. Note that this is the logical complement of the BITE output (CSAC PIN 4).

BITE (SMA) – This is a buffered output from PIN 4 of the CSAC.

Power Switch – Controls power to the evaluation board and to the CSAC.

Power LED – Indicates the state of the **Power Switch**.

Analog Tuning Input (SMA) – This input is directly connected to Pin 1 of the CSAC.

1 PPS Input (SMA) – The 1 PPS input connection to the evaluation board accepts a 1 PPS reference of arbitrary amplitude (logic high: $2V < V_{in} < 20V$) and generates a 0-3.3 V CMOS pulse to the CSAC. Note that this input is capacitively coupled to the level-shifting circuit on the evaluation board (see schematic in **A**) and therefore the applied pulse width must be < 10 ms in duration.

1 PPS Output (SMA) – The 1 PPS output is buffered by a CMOS 0-3.3 V logic gate on the evaluation board.

4.6 INITIAL START UP

4.6.1 Initial Power-On

Connect power and RS232 to the Evaluation Board as described in **Section 4.4**, above.

Turn on the power switch on the Evaluation Board.

Double-click the **CSACdemo** icon on the connected PC.

4.6.2 Establishing Communications

When communications are successfully established, the **CSACdemo** main window appears as shown in **Figure 4**.

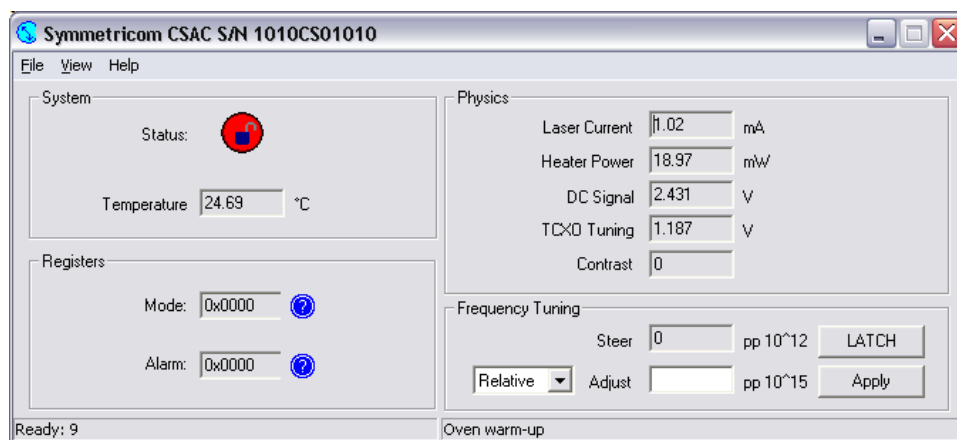


Figure 4: CSACdemo communicating with CSAC during warm-up

The title bar of the window indicates the Unit Serial Number (here “1010CS01010”). The main body of the window shows most of telemetry values from the unit (see **6.4.1** for telemetry descriptions). Initially, upon power-up, the status indicator (“”) reflects the CSAC’s unlocked condition (**BITE**=1). The left field of the bottom status bar indicates the number of seconds until the next poll (here “9”) and the right field indicates the unit status (here “Oven Warm-up”).

In the event of communication failure, the Status indicator appears as “”. In this case, check the cabling, power supply, etc. The bottom left status bar may also indicate the source of the communication failure. If the COM port is in use by another application, the status bar will report “RS232 open failed,” otherwise, it will likely indicate “Instrument not responding”. If you are using a PC serial port other than “COM1,” you may need to select **Options...** from the **File...** menu and select a different **Com Port** as shown below in **Figure 5**. Select the correct COM port from the pull-down menu and click on “**Apply Changes**” to re-attempt communications.

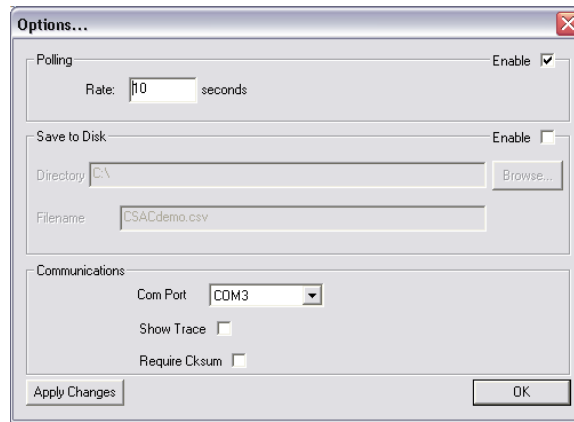


Figure 5: CSACdemo Options... panel

Eventually, through some combination of checking your cable connections and setting the **COM Port** correctly, you should be able to achieve communications similar to the appearance of **Figure 4**.

4.6.3 Monitoring Communications

For development of application-specific embedded firmware for CSAC, it is helpful to observe the communications between the **CSACdemo** program and the CSAC. Enable the **Show Trace** checkbox in the **Communications** section of the **Options...** panel and **Apply Changes** to view the bi-directional protocol.

With the trace visible, the **CSACdemo** main panel appears like:

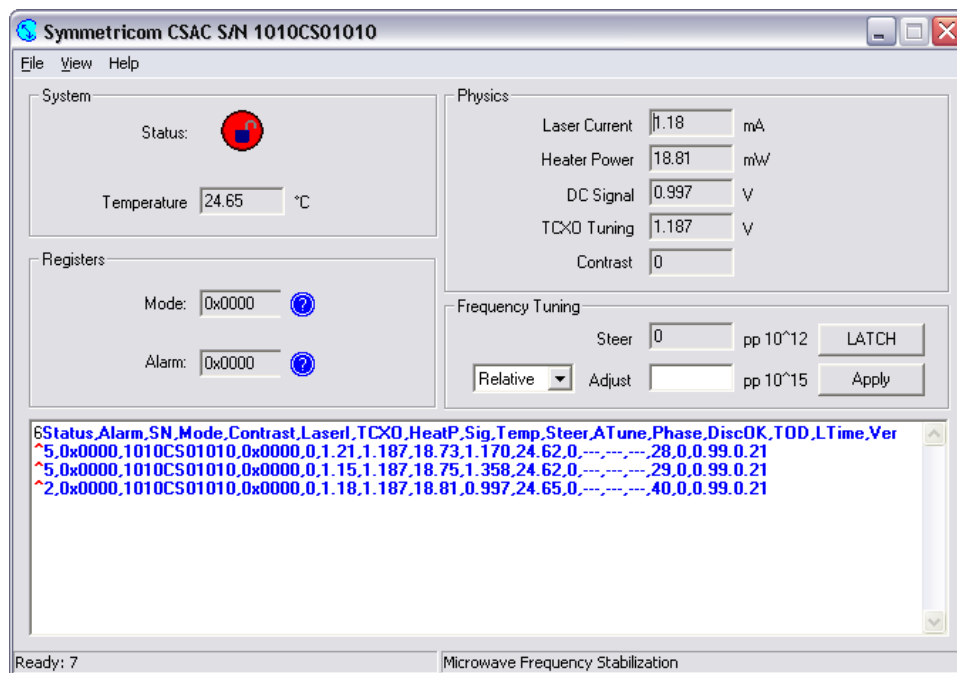


Figure 6: CSACdemo main panel with communications trace visible

Note that communications from the host PC to the CSAC are shown in **RED** and communications from the CSAC to the host are shown in **BLUE**.

4.6.4 Observing Acquisition

Initially, when the CSAC is powered up, the lock LED on the evaluation board will be off. During acquisition the **Unit Status** field in the lower right corner of **CSACdemo** will proceed through the stages corresponding to the values of the **Status** register (see **Table 7**).

Acquisition takes < 2 minutes in a 25°C ambient (up to a maximum of 5 minutes at -40°C). When acquisition is complete, the lock LED on the evaluation board will illuminate, the **CSACdemo** right hand status bar will indicate “Locked,” and the status indicator will change from “” to “.

Once locked, the main panel of **CSACdemo** appears similar to **Figure 7**.

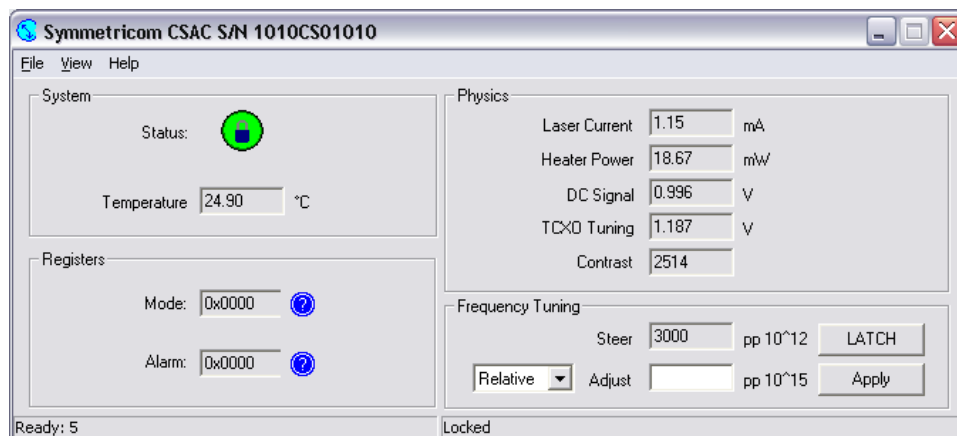


Figure 7: CSACdemo in locked condition

Figure 7 shows typical values for a normally operating CSAC. In this case, the internal case temperature of the CSAC is 24.86°C, the operating mode is 0x0000 (see 6.4.3) and there are no alarms. The physics package parameters in **Figure 7** are fairly typical as well: The laser current is about 1.15 mA, the physics package heaters are drawing less than 25 mW, and the DC signal level is about 1 V. The TCXO tuning is mid-range on 0-2.5V and the contrast is comfortably above 1000.

4.7 DATA ACQUISITION WITH CSACDEMO

For long-term monitoring of the CSAC, select the **Options...** panel from the **File** menu (see **Figure 5**).

Choose a polling rate in seconds. For short-term (1-2 day) measurements, a polling rate of 10 seconds is optimal, and will accumulate data onto disk at a rate of about 1 MB/day. For longer term measurements (30-100 days), a longer polling rate, such as 60 seconds, will reduce the growth of the data file to 150 KB/day. In any case, the files are relatively small by modern standards.

Enable **Save to Disk** with the checkbox in the top right of the panel.

Use the **Browse...** button to select an existing **Directory** in which to archive the CSAC data. Note that you must have write permission to the selected directory. Type in a **Filename** for the Data.

When you are finished, the panel might look something like:

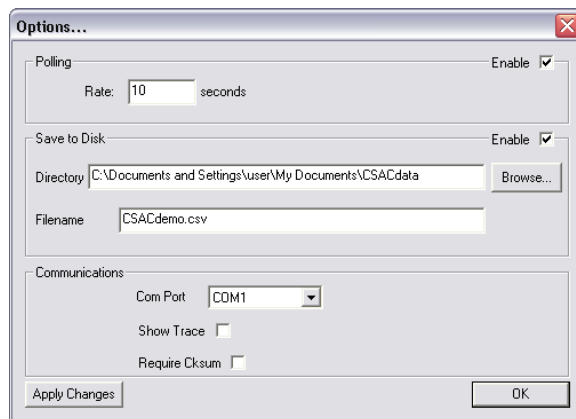


Figure 8: CSACdemo options for datalogging to disk

Click **Apply Changes** to implement the new options or **OK** to discard changes and exit the panel.

The data is stored in ascii comma-separated-values (CSV) format, which allows for convenient import into most popular spreadsheet and analysis software. The first line in the file contains the column headers (see 6.4.1, “!6” command). Subsequent lines contain the corresponding periodically-pollled data (see 6.4.1, “!^” command). The first column in the file contains time stamps, derived from the host computer’s clock, in mean-Julian day (MJD) format, referenced to universal coordinated time (UTC).

5 FUNCTIONAL DESCRIPTION

5.1 PRINCIPLE OF OPERATION

The CSAC is a passive atomic clock, incorporating the interrogation technique of Coherent Population Trapping (CPT) and operating on the D1 optical resonance of atomic cesium. A complete description of passive atomic clocks, CPT, and the CSAC architecture is beyond the scope of this **Users’ Guide**. The following description should be adequate for users and systems integrators.

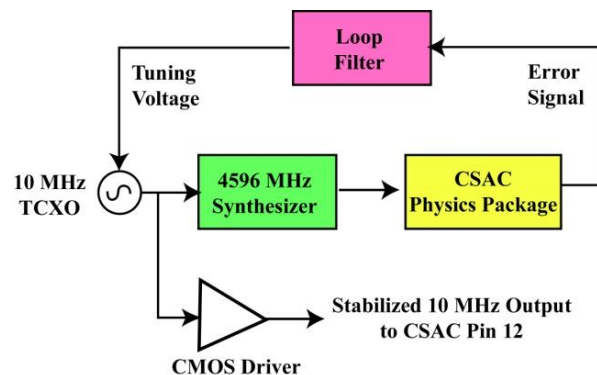


Figure 9: Simplified CSAC block diagram

Figure 9 shows a simplified block diagram of the CSAC. The principal output from the CSAC is provided by a 10 MHz temperature-compensated crystal oscillator (“TCXO”) which is buffered by a CMOS logic gate and provided on the CSAC output pin 12. In normal operation the frequency of the TCXO is continuously compared and corrected to ground state hyperfine frequency of the cesium atoms, contained in the “physics package,” which thereby improves the stability and environmental sensitivity of the TCXO by 4-5 orders of magnitude. In addition to the TCXO and the physics package, which is described in detail in [1], the essential components of the CSAC are the microwave synthesizer and the microprocessor (see [2]). The microwave synthesizer generates 4596.3x MHz with microprocessor-controlled tuning resolution of approximately 1 part in 10¹². The microprocessor serves multiple functions, including implementation of the frequency-lock loop filter for the TCXO, optimization of physics package operation, state-of-health monitoring, and command and control via RS232.

When the CSAC is initially powered on, it performs an acquisition sequence which includes stabilizing the temperature of the physics package, optimizing physics package operating parameters, and acquiring frequency lock to the atomic resonance. The acquisition process may be monitored via the **status** field of the telemetry (see 6.4.1). On power-up, the **status** begins at 8 (oven warm-up). The **status** value decrements numerically through the acquisition until normal operation (**status**=0) is achieved.

5.2 BUILT-IN TEST EQUIPMENT (BITE)

CSAC state-of-health can be monitored electronically on Pin 4 (**BITE**) of the SA.45s CSAC. Frequency lock is indicated both by **status**=0 in the status field of telemetry and by the electrical state of the **BITE** (**LOCK**) output

[1] R. Lutwak, et. al., “The Chip-Scale Atomic Clock – Low-Power Physics Package”, *Proceedings of the 36th Annual Precise Time and Time Interval (PTTI) Systems and Applications Meeting*, December 7-9, 2004, Washington, DC.

[2] R. Lutwak, et. al., “The MAC – A Miniature Atomic Clock”, *Proceedings of the 2005 Joint IEEE International Frequency Control Symposium and Precise Time & Time Interval Systems & Applications Meeting*, August 29-31, 2005, Vancouver, BC.

pin, which is high (logic 1) upon initial power-on and whenever **status** $\neq$ 0. The **BITE** pin is a high-impedance CMOS logic output.

At the conclusion of the acquisition sequence, **BITE** remains high for 5 seconds after **status**=0 in order to avoid false indication in the event of acquisition failure. Subsequently, **BITE** provides an immediate (within 1 second) indication of lock failure or alarm.

The behavior of **BITE** is identical when operating in ULP mode (see 5.11), i.e. it indicates the state of the atomic frequency lock. In ULP, **BITE**=1 during “sleep” periods and reacquisition, and transitions to **BITE**=0 when the CSAC is “awake,” beginning 5 seconds after **status**=0.

5.3 10 MHz OUTPUT CHARACTERISTICS

The buffered CMOS clock output at 10.0 MHz is provided on Pin 12 of the SA.45s CSAC. The output series impedance is 200 Ω . For reference, the output driver circuit of the SA.45s is shown below in **Figure 10**.

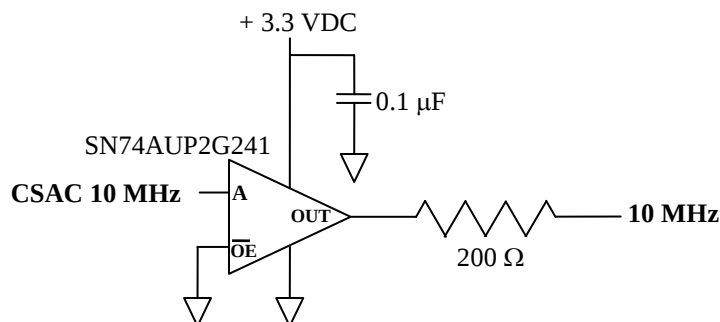


Figure 10: CSAC 10 MHz output driver circuit. 1 PPS is similar

The SA.45s is designed for embedded low-power applications, i.e. it is expected to drive a high impedance input, not a 50 Ω measurement instrument or transmission line. Note that driving a 50 Ω line at 13 dBm consumes nearly as much power as the CSAC itself! If a high-level (high-power) output driver is required, a driver circuit must be implemented external to the CSAC, such as the one implemented on the **Evaluation Board** (see reference schematic in **A**).

The 10MHz output appears on Pin 12 as soon as the CSAC is powered on and is always present, regardless of the lock status. When the CSAC is out of lock (**BITE**=1, **status** $\neq$ 0), the output frequency is provided by the free-running TCXO, which has frequency accuracy specification of $\pm$ 20 ppm and temperature sensitivity of $\approx$ $\pm$ 30 ppb/ $^{\circ}$ C. Typically, the unlocked frequency accuracy during acquisition is significantly better than this (<1 part in 10^8) as the CSAC memorizes its last-known-good tuning voltage and restores this voltage upon power-up and/or subsequent recovery from loss-of-lock.

5.4 FREQUENCY STEERING

For external steering and/or calibration, the CSAC internal microwave synthesizer may be adjusted by the user via the RS232 “**!F**” command (see 6.4.2). Steering values are entered in (integer) units of parts in 10^{15} , though the resolution realized by the CSAC hardware is approximately 1 part in 10^{12} . Steering commands may be entered as either *Absolute* steers (“**!FA**”) or as *Relative* steers (“**!FD**”). In the case of an absolute steer, the contents of the steer register are replaced with the new value. In the case of a relative steer, the new value is summed with the existing value in the steer register. In either case, the maximum steer that can be entered in a single “**!F**” command is $\pm$ 2 parts in 10^8 ($\pm$ 20000000 pp 10^{15}). If a larger correction is sent to the CSAC, the maximum allowed steer will be applied. The maximum total steering (including cumulative relative steering commands) is also limited at $\pm$ 2 parts in 10^8 , i.e. if a number of relative steers are applied such that the total steering exceeds $\pm$ 2 parts in 10^8 the total steering will be clamped to the maximum correction.

Note that steering commands may be entered during acquisition (**Status** $\neq$ 0) but will not take effect until lock is achieved.

Frequency steering is volatile. Upon reboot, the CSAC returns to its nominal (calibrated) frequency setting. To update the non-volatile calibration, use the frequency **Latch** command (see 5.5).

The current steering value appear in the telemetry string as “**Steer**”. Note that **Steer** reports the actual hardware steering, in units of $\text{pp } 10^{12}$, even though the software registers maintain resolution of $\text{pp } 10^{15}$, so that many small relative corrections may be applied. As a result, the reported value may appear to disagree with the applied correction by one unit or so due to roundoff error. An example is provided in 6.4.2.

To apply a frequency correction from the main panel of **CSACdemo**, select **Relative** or **Absolute** from the pulldown menu and enter the desired steering into the **Adjust** field in $\text{pp } 10^{15}$.

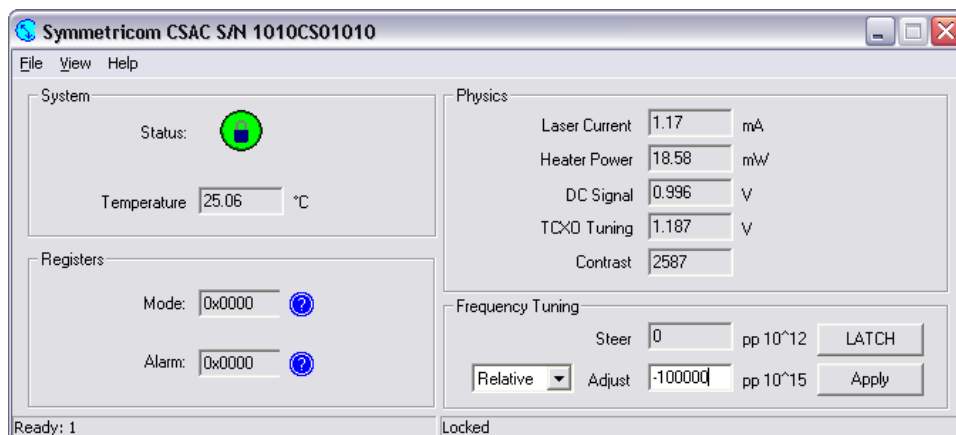


Figure 11: Frequency Offset Adjust

Figure 11 shows an example where an absolute correction of -1×10^{-10} has been entered (as $-100000 \text{ pp } 10^{15}$). The correction is applied to the CSAC when you then click on the **Apply** button.

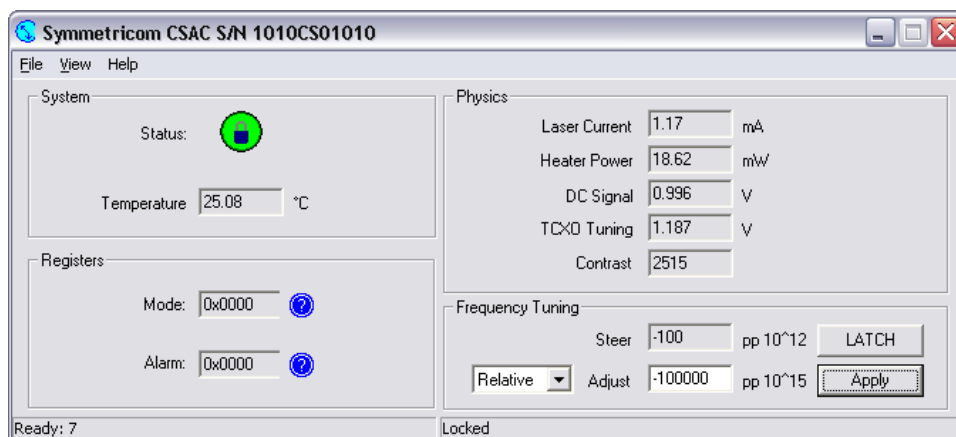


Figure 12: Absolute frequency offset of -1 part in 10^{10} after Apply

As shown in **Figure 12**, after the **Apply** button has been pressed, the correction is applied to the CSAC and the value of **Steer** changes (on the next polling update) to indicate the internal correction of -1×10^{10} (as $-100 \text{ pp } 10^{12}$).

Figure 13 below shows an example of relative frequency tuning. In this example, each time the **Apply** button is clicked, an additional correction of -1×10^{-10} ($-100000 \text{ pp } 10^{15}$) is applied to the CSAC. In the screenshot of **Figure 13** the **Apply** button has been clicked a total of four times.

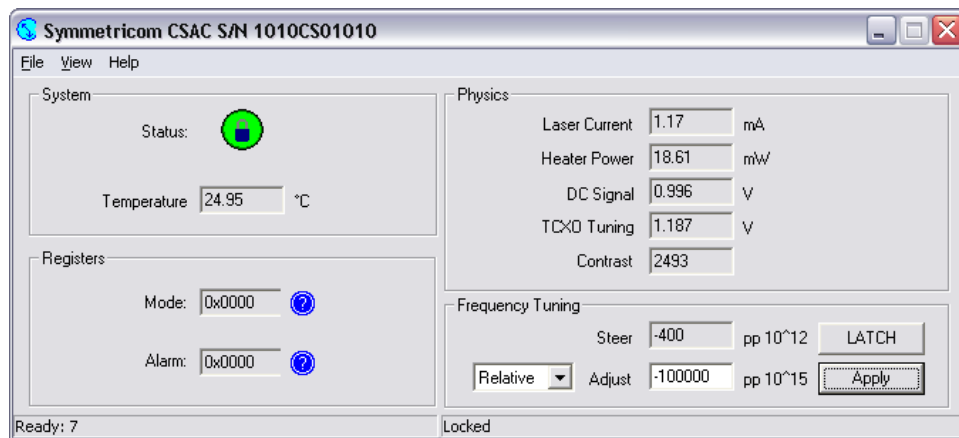


Figure 13: Frequency offset after Applying four relative corrections of -1 part in 10^{10}

5.5 FREQUENCY CALIBRATION

The internal frequency calibration of the CSAC is set prior to shipment. It is often desirable (and likely) that the calibration will need to be updated from time to time to remove cumulative frequency aging offsets.

Calibration of the CSAC is a two-step process. First, the CSAC is **Steered** onto frequency, either via an external “**IF**” command (see 5.4), through 1 PPS disciplining (see 5.8), or with analog tuning (see 5.10). Second, the present value of **Steer** is summed into the non-volatile calibration register via the RS232 frequency **Latch** command (“**IFL**” see 6.4.2). Following a **Latch** command, the value of **Steer** is reset to zero. Note that the **Latch** command is only valid when the CSAC is locked (**Status** = 0).

To **Latch** the current steer value to non-volatile storage from **CSACdemo**, press the **LATCH** button.

Warning: It may be tempting, particularly in disciplining applications, to frequently **Latch** the steering value into calibration, in the event of unforeseen power outage. This is **HIGHLY DISCOURAGED** and **BAD** for the following reason. There is a physical limit on the number of times the non-volatile memory may be written before **DAMAGE** (10,000). If the non-volatile memory of the CSAC is updated more than 10,000 times, the CSAC may become **INOPERABLE**.

5.6 1 PPS OUTPUT

A CMOS level 1 pulse-per-second (1 PPS) output is available on Pin 10 immediately upon power up. The output series impedance is 200Ω. The output driver circuit is similar to that of the 10 MHz output (see **Figure 10**). Nominal levels are 0-3.3 VDC. For synchronization purposes, the “on-time” point is the RISING edge of Pin 10.

The 1 PPS output is derived by digital division of the 10 MHz reference frequency by a factor of 10^7 . The frequency stability and accuracy of the 1 PPS output therefore reflects that of the 10 MHz. Consequently, when unlocked (**BITE**=1, **status** ≠ 0) the 1 PPS stability reflects that of the free-running TCXO.

5.7 1 PPS SYNCHRONIZATION

The 1 PPS output is synchronous with one rising edge of the 10 MHz output (Pin 12). The 1 PPS output may be synchronized with a *particular* cycle of the 10MHz by applying a synchronization pulse to Pin 9. When synchronized, the counters are reset such that the 1 PPS output occurs on the 10 MHz rising edge which is nearest to the externally-applied rising edge. In this fashion, the CSAC 1 PPS can be synchronized to within one clock cycle (+/- 100 ns) of the external reference.

The CSAC provides two modes for 1 PPS synchronization, “**Manual**” and “**Automatic**”, which are selected via a bit in the **Mode Register** (see **Section 6.4.3**). Note that the configuration of the **Mode Register** is non-volatile, i.e. preserved across power cycles.

5.7.1 Manual Synchronization

In **Manual Synchronization** mode (default), the CSAC ignores any signal present on the 1 PPS input line (Pin 9) until commanded via RS232. When a synchronization command, “!S” (see 6.4.4), is received, the CSAC 1 PPS is synchronized to the next rising edge to appear on Pin 9.

This mode is applicable to configurations where the CSAC is embedded in a system where a 1 PPS signal is always present, but not always reliably accurate or stable (such as a GPS receiver). The host microprocessor may command the CSAC to synchronize after it has verified the state-of-health of the 1 PPS reference source (e.g. after querying lock state of the GPS receiver).

To perform manual synchronization from **CSACdemo**, open the **1 PPS...** panel from the **View** menu. The **1 PPS** panel is shown below in **Figure 14**.

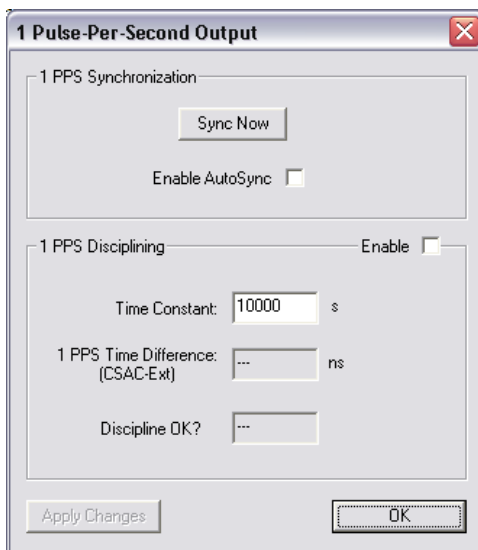


Figure 14: CSACdemo 1 Pulse-per-second Output panel

To manually synchronize the CSAC from **CSACdemo**, make sure that a valid 1 PPS reference is connected to the 1 PPS reference input and click on the **Sync Now** button on the **1 PPS** panel. The CSAC will synchronize to the next rising edge detected on the 1 PPS reference input.

5.7.2 Automatic Synchronization

In **Automatic Synchronization** mode, the CSAC will synchronize its 1 PPS output to *every* rising edge which appears on Pin 9. In this mode, synchronization may be performed by connecting a reference 1 PPS signal to Pin 9 without needing to issue the RS232 synchronization command. Automatic synchronization may be enabled/disabled bit 3 (0x0008) in the **Mode Register** (see 6.4.3).

This mode may be useful, for example, in cases where the host system does not communicate with the CSAC or in which the host system has no method or need to determine the state-of-health of the reference source.

Note that **Automatic Synchronization** mode and **Disciplining** mode (see 5.8) are mutually exclusive. Enabling either in the **Mode** register will disable the other.

To enable **Automatic Synchronization** from **CSACdemo**, check the **Enable Autosync** checkbox on the **1 PPS** panel and **Apply Changes** (see **Figure 14**).

5.8 1 PPS DISCIPLINING

A high-resolution phase meter is implemented within the CSAC for improved synchronization (< 100 ns) as well as for frequency calibration of the CSAC. The phase meter measures the time difference between the internal CSAC 1 PPS (Pin 10) and the externally applied reference 1 PPS (Pin 9). The phase meter measures the relative phase between the CSAC and the reference once per second with a resolution of 450 ps.

Based on the measurements of the phase meter, internal steering algorithms adjust the frequency of the CSAC's microwave synthesizer so as to simultaneously steer both the phase and frequency to that of the external reference, ultimately achieving accuracies of < 5 ns and 5×10^{-13} , respectively.

Disciplining may be enabled/disabled via bit 4 (0x0010) in the **Mode Register** (see 6.4.3). The time constant of the steering algorithm is user selectable via the “!D” command (see 6.4.5). Note that both the mode setting and the time constant are non-volatile, i.e. preserved across power cycles.

Prior to the onset of steering, the disciplining algorithms first perform an initialization sequence in which the variables of the steering algorithm are reset to defaults and a 1 PPS synchronization operation (see 5.7) is executed to bring the 1 PPS output within 100 ns of the reference, thereby avoiding large frequency excursions. Initialization is performed when **Disciplining** is first enabled in the **Mode Register** and, in the case where **Disciplining** is already enabled, immediately after the CSAC achieves frequency lock (**BITE**=0, **status**=0).

In the event that the 1 PPS reference is removed from Pin 9 while **Disciplining**, the CSAC remains in “holdover” and preserves the most recent steering value. If the 1 PPS reference subsequently reappears, **Disciplining** will continue where it left off, without reinitializing. The notable exception to this is the case in which the CSAC 1 PPS has drifted significantly in phase (> 1 μ s) from the reference 1 PPS during the outage, in which case a synchronization is performed, though the **Disciplining** variables are *not* reinitialized.

If it is necessary to force reinitialization of the disciplining variables, perhaps because the reference source is subsequently deemed untrustworthy and subsequently recovers, this may be accomplished by disabling and re-enabling **Disciplining** in the **Mode Register** (see 6.4.3).

When **Disciplining** is enabled, the most recent phase meter measurement, rounded to the nearest nanosecond, is reported in the standard telemetry (see 6.4.1). The sign of the reported value reflects the measurement of (1PPS_CSAC – 1PPS_EXT), i.e. if the CSAC 1PPS rising edge occurs prior to the external 1PPS rising edge, then the sign is negative.

The status of **Disciplining** is indicated by the **DiscOK** parameter in the telemetry (see 6.4.1). **DiscOK**=0 upon startup. **DiscOK**=1 when the magnitude of the phase measurement is < 20 ns for two time constants of duration. **DiscOK**=2 when in holdover (disciplining enabled but no 1 PPS present).

Note that **Automatic Synchronization** (see 5.7.2) mode and **Disciplining** mode are mutually exclusive. Enabling either in the **Mode** register will disable the other.

In **CSACdemo**, enabling/disabling **Disciplining** and setting the discipline time constant are both accomplished on the **1 PPS** panel, accessible from the **View** menu (See **Figure 14**). To modify the discipline time constant, enter the new value in the field (10-10000) and **Apply Changes**.

5.8.1 Cable length Compensation

The “zero point” of disciplining may be adjusted to accommodate cable and other instrumentation delays (or advances) which impact the arrival time of the 1 PPS at the CSAC 1 PPS input pin. The compensation value may optionally be stored in the CSAC non-volatile RAM for one-time calibration.

The maximum compensation adjustment is ± 100 ns, with resolution of 100 ps. The compensation value is entered into the CSAC as a signed integer in units of 100 ps, where positive sign indicates phase advancement of the input 1 PPS. For example, if there is 45 ns of delay between the on-time point and the CSAC 1 PPS input (approximately 33 feet of RG-58 coaxial cable) then the compensation value would be +450.

Note that cable length compensation can also be employed to correct for dynamic *known* errors in the 1 PPS reference provided, for example, from an external measurement system. For this reason, upon application the compensation is subsequently applied to the *previous* 1 PPS measurement.

Note that compensation is implemented in the disciplining algorithm, not in the phase measurement itself. The phase measurement, as reported via telemetry, reports the actual phase measurement, i.e. if the CSAC is disciplined with +50 ns of compensation, the phase meter will report -50 ns of phase error.

Compensation is set with the “!DC” command (see 6.4.6).

5.8.2 The “Art” of Disciplining

Implemented correctly, disciplining can be utilized to calibrate the CSAC frequency in the field, even if a reference source is only occasionally or sporadically available, thereby improving the long-term performance (phase and frequency drift) of the CSAC. At the same time, the disciplined CSAC may be used to “clean-up” the short-term stability of an accurate, but noisy, reference source, such as GPS.

Implemented incorrectly, however, disciplining may degrade the performance of the CSAC if, for example, the CSAC is disciplined with a short time constant to a source which is itself noisier than the CSAC, such as GPS.

Implementing a successful disciplining strategy involves understanding the noise properties of the CSAC, the reference source, and the phase meter itself, and selecting the appropriate time constant that makes the best use of the available timing information.

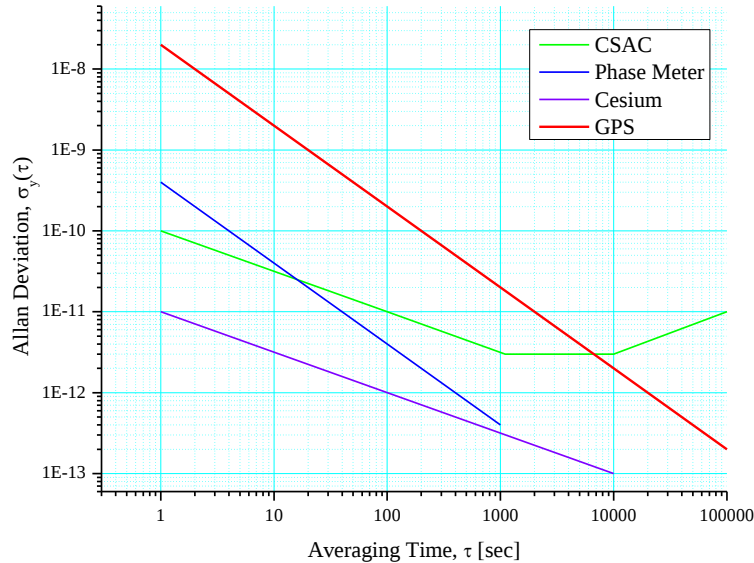


Figure 15: Typical instability (Allan Deviation) of CSAC, Phase meter, GPS, and cesium beam frequency standard

Figure 15 shows typical instability (Allan Deviation) of the CSAC (in green), along with the noise floor of the phase meter (in blue). Also shown are the instabilities of typical reference sources, GPS (in red) and a high-performance cesium beam frequency standard (in purple). When disciplining, the stability of the output of the CSAC (“combined clock”) at any averaging time, reflects the noise properties of the dominant (most noisy) source. For example, if disciplining the CSAC to a GPS source, which is noisier than the CSAC for averaging times < 5000 seconds, the disciplining time constant should be set to $\tau > 5000$ seconds so that the (superior) CSAC stability dominates for $\tau < 5000$ seconds and the (superior) GPS stability dominates for $\tau > 5000$ seconds. On the other hand, consider the case where the CSAC is disciplined to a high-performance cesium clock, which is more stable than the CSAC on all time scales. The noise is dominated by the phase meter for $\tau < 20$ seconds and by the CSAC for $\tau > 20$ seconds. In this case, the disciplining time constant could be set to $\tau = 20$ seconds for optimal performance.

Figure 16 shows an example of a CSAC, which is disciplined to a superior reference (in this case a hydrogen maser) with a time constant of 20 seconds. For this measurement, the CSAC was deliberately mistuned in both frequency and phase prior to the measurement, by $\bar{y} = +1 \times 10^9$ and $\phi = +50$ ns, respectively.

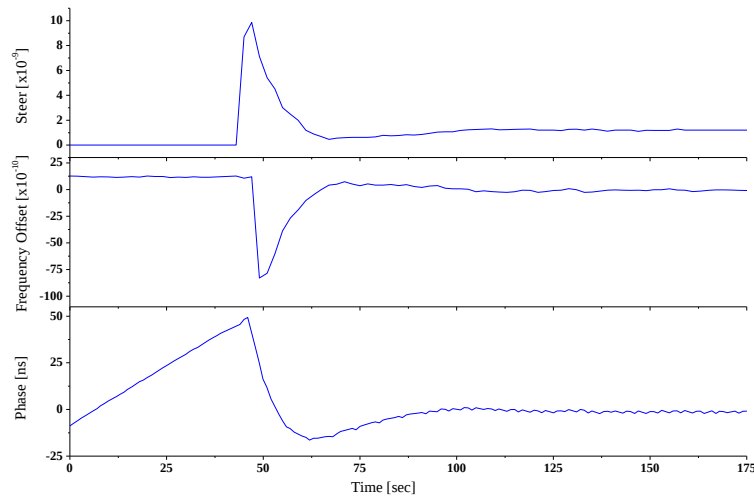


Figure 16: Disciplining CSAC to a superior reference. Time constant is set to 50 seconds

In **Figure 16**, when disciplining was enabled, at $T = 10$ seconds, the steering algorithm immediately inserted a frequency offset of -2.5×10^{-9} , in order to steer out the 50 ns phase error with 20 second time constant. The steering gradually reduces as the phase approaches zero such that both frequency and phase are corrected to within $1/e$ of their initial values at one time constant (20 s) and $1/e^2$ within two time constants (40s). After five-six time constants (≈ 100 s) frequency and phase are corrected to within $\pm 5 \times 10^{-13}$ and ± 5 ns, respectively.

5.9 TIME-OF-DAY

The CSAC maintains time-of-day (TOD) as a 32-bit unsigned integer which is incremented synchronously with the rising edge of the 1 PPS output. Until set otherwise, TOD begins counting from zero when the CSAC is powered on.

TOD is retrieved from the CSAC over RS232 with the “!T” command (see **6.4.8**). When the “!T” command is received, the CSAC waits for the next rising edge of 1 PPS before replying with the TOD of the current epoch, i.e. if the command is received during epoch N , then the reply “ $N+1$ ” appears immediately following the next 1 PPS. This strategy provides the host system with minimum ambiguity in interpreting the response.

TOD may be set with the “!T” command via the RS232 interface (see **6.4.8**). The “!T” command includes provision both for setting an absolute number or for a differential (+/-) adjustment of the present TOD. An example is provided in **6.4.8**. In order to avoid ambiguity in *setting* the TOD, it is recommended that the host system wait for 1 PPS and transmit the setting/adjustment immediately thereafter.

The **CSACdemo** program shows TOD on the **Time-Of-Day...** panel, accessed from the **View** menu and shown below in **Figure 17**.

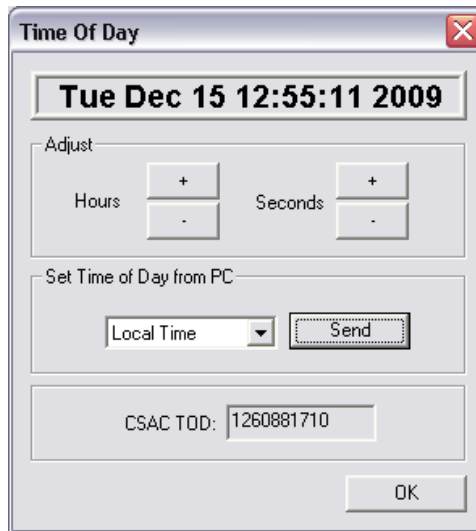


Figure 17: CSACdemo Time-Of-Day panel

The “raw” CSAC TOD value is shown in the lower field of the panel (here 1260881710). The upper display of the TOD panel realizes the time-keeping convention of the C Programming language (as well as in UNIX and Microsoft Windows®) which counts time in seconds from midnight on January 1, 1970. If you click on the **Send** button, it will set the CSAC time according to the host PC’s TOD counter (either local time or UTC depending on the setting of the pull-down menu to the left of the **Send** button). The + and – Hours and Seconds buttons increment or decrement the CSAC TOD by +/- 3600 or +/-1 second respectively.

5.10 ANALOG TUNING

To enable analog frequency tuning for implementation in legacy (quartz crystal) applications, the frequency of the CSAC may be tuned with an external voltage applied to Pin 1. This functionality may be enabled/disabled via a bit in the **Mode Register** (see 6.4.3). The applied voltage is digitized by an internal analog-to-digital converter and the correction is applied to the microwave synthesizer at a rate of once per second, i.e. the maximum tuning rate is 1 Hz.

When analog tuning is enabled, the voltage applied at Pin 1 and the resultant **Steering** are reported in the standard telemetry stream (see 6.4.1)

The tuning voltage input range is 0-2.5 VDC, which corresponds to a full scale tuning range of 4.4×10^{-8} . Nominal “zero-correction” tuning occurs at a tuning input voltage of 1250 mV. The fractional frequency correction, for a given applied voltage, is given by:

$$\frac{\Delta f}{f} = (V_{\text{TUNE}} - 1250 \text{ mV}) \times 1.77 \times 10^{-11} / \text{mV}$$

Note that this formula is accurate for the standard (-001 and -002) SA.45s CSAC, operating at 10.0 MHz output frequency. Consult the datasheet for tuning curves for CSACs at alternate frequencies.

The tuning input pin is nominally biased at ≈ 1250 mV, i.e. approximately zero correction. Note, however, that this bias voltage may vary somewhat due to component variations and/or exhibit temperature sensitivity. Therefore, analog tuning should NOT be enabled unless the functionality is necessary and the analog tuning input pin is connected to a low noise, low impedance voltage source. For non-legacy applications, it is recommended that this feature remain disabled, and that corrections be applied via the digital communications interface (see 5.4) in order to avoid degradation of the CSAC short-term stability due to voltage noise applied to the tuning pin.

Analog tuning can be enabled/disabled and monitored from the **CSACdemo** application from the **Analog Tuning...** panel (accessible from the **View** menu).

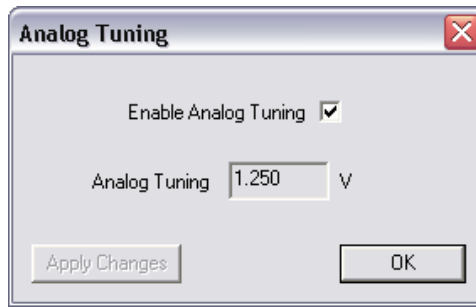


Figure 18: CSACdemo Analog Tuning panel

When analog tuning is enabled, the voltage present on Pin 1 is displayed in the **Analog Tuning** field and also reflected in the current reported value of **Steer** on the main panel. To enable or disable analog tuning, click the **Enable Analog Tuning** checkbox and **Apply Changes**.

5.11 ULTRA-LOW POWER OPERATING MODE

The majority of the power in the CSAC is consumed by the physics package and microwave synthesizer. In ultra-low power (**ULP**) mode, the physics package and synthesizer may be disabled for a user-specified length of time, during which the CSAC operates as a free-running TCXO. Periodically, the “atomic clock” portion of the CSAC is powered on (again for a user-specified amount of time) and the TCXO is “re-calibrated” to the atomic frequency. Operating in this mode, the CSAC exhibits the short-term performance of a TCXO with the long-term stability of an atomic clock at significantly lower power. For example, if the atomic clock portion is only powered on for 5 minutes out of every hour (2 minutes for lock acquisition + 3 minutes of run time), then the time-averaged power of the CSAC may be < 20 mW.

Between calibration cycles, the CSAC in **ULP** mode exhibits the performance characteristics of a free-running TCXO and therefore exhibits significantly higher short-term frequency drift and environmental (temperature, vibration, etc.) sensitivity than a normally-operating CSAC. For this reason, **ULP** mode is principally recommended only for applications which:

- (a) require long-term timing performance, rather than short-term frequency or time stability
- and
- (b) have a very stable environment (temperature, vibration, etc.).

Please consult Symmetricom for additional assistance in evaluating and optimizing **ULP** for your application.

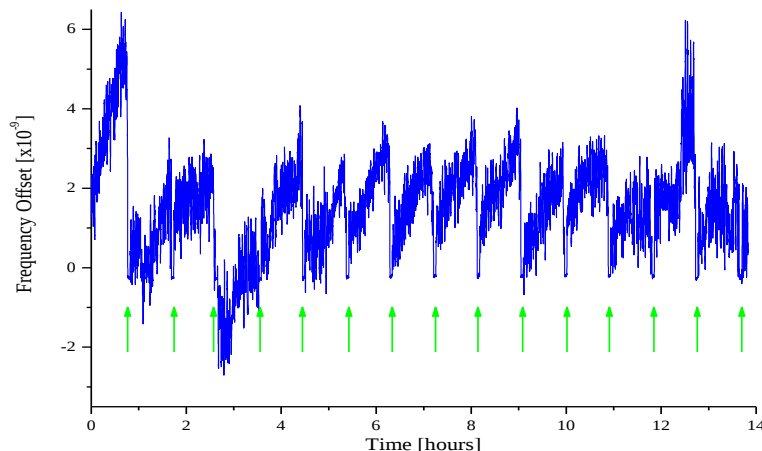


Figure 19: Frequency record of CSAC in ULP mode. Green arrows indicate recalibration periods

Figure 19 shows an example of a CSAC operating in ULP mode, with wake-time = 300 s (5 min) and sleep-time = 3300 s (55 min). The green arrows indicate the “on” time calibrations. Note the relatively poor TCXO drift and temperature behavior between calibrations.

ULP is a very unusual operating mode for an atomic clock and it's important for the user to understand exactly how the clock is behaving in order to effectively implement this feature in a system. In particular, please note the following:

- 1) When operating in ULP mode, the **Status Register** will indicate **Status** = 9 (“asleep”) when the atomic clock portion of the CSAC is asleep. Each wake cycle is indicated by the usual lock process (**Status** = 8, 7, 6, ...) followed by “wake-time” seconds of operation at **Status** = 0 before the cycle repeats. This cycle is also reflected on the **BITE** pin, which is 1 (high) whenever the CSAC is unlocked (or asleep) and only 0 (low) during the locked periods.
- 2) When using **Disciplining** (see 5.8) in conjunction with **ULP**, disciplining functionality is disabled during sleep and unlocked cycles, though steering information is preserved and updated across wake cycles.
- 3) Frequency **Steering** commands may be entered when the CSAC is asleep or unlocked but do not affect the output frequency until lock is achieved, typically on the next wake cycle (see 5.4). Also, the **Latch** command is only valid when the CSAC is locked (**Status** = 0).
- 4) If enabled, **Analog Tuning** (see 5.10) is only active during wake cycles.

ULP is enabled via bit 5 (0x0020) in the **Mode Register** (see 6.4.3) and the “sleep-time” and “wake-time” are set via the “**!U**” command (see 6.4.7). These values are non-volatile, i.e. they persist across power cycles. Note that the wake-time begins counting *after* the CSAC achieves lock, so the actual time that the atomic clock portion of the CSAC is powered on is the sum of the time to lock and the user-configured wake-time. The minimum allowed values of wake-time and sleep-time are 10 seconds and 1800 seconds, respectively

To configure ULP parameters via **CSACdemo**, select **Ultra-Low Power Mode** from the **View** menu to access the panel shown in **Figure 20**.

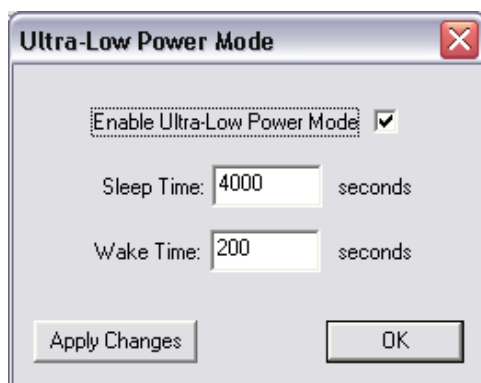


Figure 20: CSACdemo Ultra-Low Power Mode Configuration Panel

Enter the desired settings for the **Enable** checkbox and values for **Sleep Time** and **Wake Time** and click **Apply Changes** to upload new settings to the CSAC.

6 PROGRAMMER'S REFERENCE

6.1 RS232 HARDWARE INTERFACE

Pins 5 and 6 provide a serial interface for communication with the CSAC. The protocol is fundamentally similar to RS232, with the exception that the voltage levels are CMOS (0-3.3 V), rather than +/- 12 V. The serial interface operates at 57600 Baud, 8 data bits, No Parity, and 1 Stop Bit (8-N-1) with no flow control. For interfacing with a standard RS232 controller interface, which requires +/- 12 V logic levels, an external level shifter must be employed, such as the **Maxim MAX202** employed on the **Evaluation Board** (see **A**).

6.2 OVERVIEW OF TELEMETRY INTERFACE

The CSAC communicates exclusively with printable (non-binary) ascii characters.

In general, commands are preceded by an exclamation point ("!") and followed by a carriage-return/linefeed [**CRLF**] pair (ascii 0x0D 0x0A). For convenience and efficiency, each command also provides a single-character shortcut, which is executed immediately, i.e. without bracketing by '!' and [**CRLF**]. For example, the single character shortcut '^' is functionally identical to "!^[**CRLF**]".

After transmitting '!' but prior to sending [**CRLF**], a command may be aborted by sending the escape character (ascii 0x1B).

All commands produce a response from the CSAC which are human readable, with individual lines ending in [**CRLF**]. If an unsupported or improperly formatted command is received, the CSAC responds with "?[**CRLF**]".

6.2.1 Checksum

For improved communications reliability, an NMEA-style checksum may be enabled via bit 6 (0x0040) of the **Mode Register** (see 6.4.3). When enabled, the checksum is required for all input commands and is present on all replies from the CSAC.

The checksum is a two-byte Ascii representation (in hexadecimal) of the XOR of all characters in the command between – but not including – the ! and the [**CRLF**] characters. The checksum is preceded by a '*' character and appended to the command immediately prior to the [**CRLF**]. Because commands including checksum are inherently multi-character, single-character shortcuts are not available when checksum is enabled.

Example (Enable analog tuning via **Mode** register):

<i>Command:</i>	!MA*0C[CRLF]
<i>Unit Response:</i>	0x0041*4D[CRLF]

Example (Disable checksum via **Mode** register):

<i>Command:</i>	!Mc*2E[CRLF]
<i>Unit Response:</i>	0x0000[CRLF]

If the checksum is not present or if the checksum value is invalid, then the command is not executed and the CSAC responds with "*[**CRLF**]".

Example (Malformed checksum):

<i>Command:</i>	!Mc*2D[CRLF]
<i>Unit Response:</i>	*[CRLF]

To experiment with checksum in **CSACdemo** and observe the calculated checksums in the **Trace** window, enable the **Require Cksum** checkbox on the **Options...** panel (see **Figure 5**).

6.3 COMMAND SUMMARY

Table 5, below, summarizes the CSAC commands. The single-character shortcut equivalents are defined in Column “**shortcut**”. Column “**Ref. Section**” refers to detailed descriptions in sections **6.4.x** below.

Cmd	Description	Shortcut	Ref. Section
6	Return telemetry headers as comma-delimited string	!6[CRLF]	6.4.1
^	Return telemetry as comma-delimited string	!^ [CRLF]	6.4.1
F	Adjust frequency	!F?[CRLF]	6.4.2
M	Set operating mode register bits	!M?[CRLF]	6.4.3
S	Sync CSAC 1 PPS to external 1 PPS	!S[CRLF]	6.4.4
D	Set 1 PPS disciplining time constant	!D?[CRLF]	6.4.5
U	Set ultra-low power mode parameters	!M?[CRLF]	6.4.7
T	Set/report time-of-day	!T?[CRLF]	6.4.8
?	Help	!?[CRLF]	6.4.9

Table 5: CSAC command summary

6.4 DETAILED COMMAND DESCRIPTIONS

6.4.1 Telemetry (6 and ^)

CSAC supports two commands, “**!6**” and “**!^**” to retrieve the telemetry headers and values, respectively. Both responses are comma-delimited strings, suitable for importing into spreadsheet programs.

Telemetry headers command: **!6[CRLF]**

Unit Response: Comma-delimited string of identifiers ending in carriage return/linefeed

Example Response:

Status, Alarm, SN, Mode, Contrast, LaserI, TCXO, HeatP, Sig, Temp, Steer, ATune, Phase, DiscOK, TOD, LTime, Ver[CRLF]

Telemetry data command: **!^[CRLF]**

Unit Response: Comma-delimited string of telemetry data ending in carriage return/linefeed

Example Response:

0,0x0000,1209CS00909,0x0010,4381,0.86,1.573,17.62,0.996,28.26,-24,---,-1,1,1268126502,586969,1.0[CRLF]

Note that the single-characters ‘**6**’ and ‘**^**’ are shortcuts for “**!6[CRLF]**” and “**!^[CRLF]**”, respectively.

Table 6, below, lists the telemetry parameters and their associated header identifiers.

Identifier	Description	Notes
Status	Unit Status	See Note 1
Alarm	Pending Unit Alarms	See Note 2
SN	Unit serial number	See Note 3
Mode	Mode of operation	see 6.4.3 for bit definitions.
Contrast	Indication of signal level	Typically > 2000 when locked, and ≈ 0 when unlocked.
LaserI	Laser current (mA)	Typically 0.8 – 1.3 mA
TCXO	Tuning Voltage (V)	0-2.5 VDC tuning range $\approx \pm 10$ ppm
HeatP	Physics package Heater Power (mW)	Typical 15-25 mW under NOC at 25°C ambient
Sig	DC Signal Level (V)	Typical 1.0 V under NOC
Temp	Unit temperature (°C)	Absolute accuracy is $\pm 2^\circ\text{C}$
Steer	Frequency adjust	In pp10 ¹²
ATune	Analog tuning voltage input	“---“ when analog tuning is disabled, 0-2.5V when enabled
Phase	1PPS_CSAC-1PPS_EXT (ns)	Only present when disciplining enabled, otherwise “---“
DiscOK	Discipline status (0-2)	‘0’=acquiring, ‘1’=locked, ‘2’=holdover when disciplining enabled, otherwise “---“
TOD	Time (seconds)	Starts at 0 upon powerup unless set by command
LockT	Time since lock (seconds)	Starts at 0 upon lock
FWver	Firmware version	Two digit number “ <i>M.m</i> ” where ‘ <i>M</i> ’ is major revision and ‘ <i>m</i> ’ is minor revision.

Table 6: Telemetry parameters

Note 1: **Status** reflects the steps of the clock initialization process. It starts at 8 on boot and decreases to 0 as acquisition proceeds. When **Status** $\neq 0$, **BITE**=1. When **Status** =0, **BITE** =0.

Status	Acquisition stage
0	Locked
1	Microwave Frequency Steering
2	Microwave Frequency Stabilization
3	Microwave Frequency Acquisition
4	Laser Power Acquisition
5	Laser Current Acquisition
6	Microwave Power Acquisition
7	Heater equilibration
8	Initial warm-up
9	Asleep (ULP mode only)

Table 7: Status register and acquisition stages

Note 2: Alarms indicate detection of anomalous operating conditions. **Alarm** is the logical OR of all pending alarms (see **Table 8**). If any alarm is tripped (**Alarm** $\neq 0x000$), the CSAC will return to **Status** = 8.

Alarm	Definition	Alarm Limit
0x0001	Signal Contrast Low	Contrast < 1000
0x0002	Synthesizer tuning at limit	Synthesizer detuned from calibration by > +30 kHz or < -15 kHz
0x0004	Temperature Bridge Unbalanced	Bridge – Setpoint > +/- 2 mV
0x0010	DC Light level Low	< 200 mV
0x0020	DC Light level High	> 2.48 V
0x0040	Heater Power Low	< 50 mW
0x0080	Heater Power High	> 40.5 mW
0x0100	uW Power control Low	< 2 mV
0x0200	uW Power control High	> 2.48 V
0x0400	TCXO control voltage Low	< 0.1 V
0x0800	TCXO control voltage High	> 2.4 V
0x1000	Laser current Low	< 0.5 mA
0x2000	Laser current High	> 2.3 mA
0x4000	Stack overflow (firmware error)	

Table 8: Alarm definitions

Note 3: CSAC serial numbers are of the form YYMMCSNNNNN where YYMM is the year and month of production and NNNNN is the serialized production unit number.

6.4.2 Frequency Adjustment (F)

The output frequency of the CSAC may be adjusted (steered) via RS232. The internal resolution of the fractional frequency correction is approximately 1 part in 10^{12} . The correction is entered as integer parts in 10^{15} . The maximum allowed correction, in a single command, is ± 20000000 (2 parts in 10^8). Corrections may be applied as either **Absolute** or **Relative**, depending on the first character following the “!F”, i.e. “!FA” or “!FD” for absolute or relative (“delta”) respectively. In the case of absolute steering, the value of the **Steer** register is replaced with the new value. In the case of relative (delta) steering, the new value is summed with the existing value in the **Steer** register, i.e. two relative corrections of -10000 result in a total offset of -2×10^{-11} . The current steering value is reported in the **Steer** field of the telemetry in units of $\text{pp}10^{12}$.

*Adjust frequency command: !FYXXXXX[CRLF] where Y is either ‘A’ or ‘D’
and XXXXX is the new correction in parts in 10^{15} .*

Example (Apply absolute tuning correction of -1.23×10^{-10}):

Command: **!FA-123000[CRLF]**

Unit Response: **Steer = -123[CRLF]**

Example (Apply delta tuning correction of -1.23×10^{-10}):

Command: **!FD-123000[CRLF]**

Unit Response: **Steer = -246[CRLF]**

Example (Report current value of **steer**):

Command: **!F?[CRLF]**

Unit Response: **Steer = -246[CRLF]**

Note that the single-character ‘F’ is a shortcut for “!F?[CRLF]”.

The contents of the **Steer** register are volatile, i.e. the **Steer** is reset to 0 when power is cycled to the CSAC. In many cases it is desirable to preserve the steer upon power-down, e.g. for calibration of the CSAC. This is accomplished by sending a **Frequency Latch** command to the CSAC, which updates the internal calibration

(stored in non-volatile memory) according to the current value of the **Steer** register and resets **Steer** to zero. Note that the **Latch** command is only valid when the CSAC is locked (**Status** = 0).

Latch calibration value: **!FL[CRLF]**

Example:

Command: **!FL[CRLF]**

Unit Response: **Steer Latched [CRLF]**
 Steer = 0[CRLF]

WARNING: The frequency steering command (**!F**) is recommended for real-time disciplining of CSACs, but the value should NOT be latched (**!FL**) on every steer due to the physical limit on the number of times the non-volatile memory may be written before damage (10,000). For example, if an **!FL** command was applied to the CSAC, accompanying a steer (**!F**), at a rate of 1/sec, the CSAC is expected to fail within 4 hours.

6.4.3 Set/clear Operating Modes (M)

Operating modes of the CSAC are enabled/disabled via individual bits in the **Mode** register. The **!M** command provides access to set/clear each of the bits independently. The **Mode** register is non-volatile, i.e. settings persist across power cycles.

The unit responds by reporting the current value of the mode register in hexadecimal. Each bit in the mode register is associated with enabling/disabling a particular operating mode. The bit assignments are:

0x0001	Analog tuning enable
0x0002	Reserved
0x0004	Reserved
0x0008	1 PPS auto-sync enable
0x0010	Discipline enable
0x0020	Ultra-low power mode enable
0x0040	Require checksum on ! command
0x0080	Reserved

The arguments to the **!M** command include:

A/a	Enable/disable analog tuning input
S/s	Enable/disable 1 PPS auto-sync
D/d	Enable/disable 1 PPS disciplining
U/u	Enable/disable ultra-low power mode
C/c	Enable/disable NMEA-style checksum
?	Report current settings

Example (Enable and then Disable analog tuning):

Command: **!MA[CRLF]**

Unit Response: **0x0001[CRLF]**

Command: **!Ma[CRLF]**

Unit Response: **0x0000[CRLF]**

The current value of the mode register is returned in the standard telemetry query (see 6.4.1) or may be queried independently with the “**!M?**” command.

Example (query Mode register):

Command: **!M?[CRLF]**

Response: **0x0001[CRLF]**

Note that the single-character ‘**M**’ is a shortcut for “**!M?[CRLF]**”.

Autosync mode and Discipline mode are mutually exclusive. Setting one will automatically disable the other.

6.4.4 1 PPS Synchronization (S)

In order to synchronize the 1 PPS output (Pin 10) to an externally applied 1 PPS synchronization input (Pin 9), connect the 1 PPS input to Pin 9 and send the “IS” command. The rising edge of the 1 PPS output will be synchronized to within +/- 100 ns of the next rising edge of the 1 PPS input. If a valid 1 PPS input does not appear at the 1 PPS input within 3 seconds, the operation is aborted and an error is returned.

Synchronize 1PPS: **IS[CRLF]**

Unit Response: **S[CRLF] or E[CRLF]**

The unit response (**S** or **E**) occurs *after* either successful synchronization or 3-second timeout. This permits the host system to verify successful synchronization.

Note that the single-character ‘S’ is a shortcut for “IS[CRLF]”.

6.4.5 Set 1 PPS Disciplining Time Constant (D)

The time constant for disciplining to an externally-supplied 1 PPS reference source may be selected to provide optimal performance in a given application (see 5.8.2). The time constant can lie in the range of 10 to 10000 seconds.

The 1 PPS disciplining time constant is set with the **ID** command:

Set Time Constant command: **IDX[CRLF]** where **X** is the new time constant in seconds.

Example (set disciplining time constant to 80 seconds):

Command: **ID80[CRLF]**

Response: **80[CRLF]**

To query the current time constant setting, without modifying the value, use the command “ID?”

Example (query current disciplining time constant):

Command: **ID?[CRLF]**

Response: **80[CRLF]**

Note that the single-character ‘D’ is a shortcut for “ID?[CRLF]”.

6.4.6 Set 1 PPS Disciplining Cable Length Compensation (DC)

Cable length compensation can be applied to allow for known delay (or advance) in the arrival time of the reference 1 PPS at the CSAC (see 5.8.1).

Cable length compensation is represented as a signed integer in units of 100 ps, with a maximum value of +/- 1000 (100 ns). The sign of the compensation is such that a positive value reflects known *DELAY* in the arrival time of the 1 PPS, i.e. 33 feet of RG-58 cable requires compensation of +50 ns.

The cable length compensation value is set with the **IDC** command:

Set Time Constant command: **IDCX[CRLF]** where **X** is the new compensation value

Example (set cable length compensation to +15 nanoseconds):

Command: **IDC150[CRLF]**

Response: **150[CRLF]**

To query the current compensation setting, without modifying the value, use the command “IDC?”

Example (query current compensation setting):

Command: **IDC?[CRLF]**

Response: **150[CRLF]**

To store the current compensation setting in non-volatile RAM, use the command “**!DCL**”

Example (Latch current value of compensation to power-up default):

Command: **!DCL[CRLF]**

Response: **Phase comp latched[CRLF]**

6.4.7 Set Ultra-low Power Mode Parameters (U)

The ultra-low power operating mode is defined by two parameters, “**Sleep-Time**” and “**Wake-Time**”, which may be set with the **!U** command.

Set ULP parameters command: **!USSS,WWW[CRLF]**

*where **SSS** is the sleep time in seconds and **WWW** is the wake-time in seconds.*

Example (set sleep-time=55 minutes, wake-time=5 minutes):

Command: **!U3300,300[CRLF]**

Response: **3300,300[CRLF]**

The allowed ranges of **Sleep-Time** and **Wake-Time** are 1800-65535 seconds and 10-65535 seconds, respectively.

To query the ULP settings, without modifying their values, use the command “**!U?**”

Example (query current ULP settings):

Command: **!U?[CRLF]**

Response: **3300,300[CRLF]**

Note that the single-character ‘**U**’ is a shortcut for “**!U?[CRLF]**”.

6.4.8 Time-of Day (T)

Time-of-day (TOD) is maintained internally within the CSAC, represented by a single unsigned long integer value, which begins counting up from 0 when the CSAC achieves lock. The TOD is synchronized with the 1 PPS output. TOD is routinely transmitted in the telemetry string (see **Table 6**).

TOD may be set externally with the **!T** command:

Set TOD command: **!TYXXXX[CRLF]**

*where **Y** is either ‘**A**’ for absolute setting or ‘**D**’ for a delta adjustment of TOD*

*and **XXXX** is either the unsigned integer TOD (typically either UNIX/Windows time or GPS time) or a signed integer adjustment to the TOD.*

Example (Absolute setting TOD to 1221578499):

Command: **!TA1221578499[CRLF]**

Unit Response: **TimeOfDay = 1221578499[CRLF]**

Example (retard TOD by 3600 seconds = 1 hour):

Command: **!TD-3600[CRLF]**

Unit Response: **TimeOfDay = 1221574902[CRLF]**

Example (advance TOD by 3600 seconds = 1 hour):

Command: **!TD3600[CRLF]**

Unit Response: **TimeOfDay = 1221574902[CRLF]**

The TOD may be reported synchronous with the 1 PPS output in order to enable unambiguous external time syntonization:

Retrieve TOD command: !T?[CRLF]

Unit Response: XXXX[CRLF] where XXXX is the current TOD.

Note that this response does not occur until immediately following the next 1PPS output pulse.

When queried with the ‘!T?’ command, the first character of TOD will appear on RS232 within 20 ms of the rising edge of the next 1 PPS output pulse. Because this necessarily creates a delay of up to a second between sending the ‘!T?’ command and receiving a response from the CSAC, the host system must allow for an RS232 receive timeout of at least 1000 ms when anticipating a response to the ‘!T?’ command. For less critical timing applications, the TOD can be somewhat ambiguously parsed from the standard telemetry string (see **6.4.1**).

Note that the single-character ‘T’ is a shortcut for “!T?[CRLF]”.

6.4.9 Help (?)

A list of all available commands is displayed in response to the ? command.

Display all commands: ?

<i>Unit Response:</i>	F	Adjust Frequency[CRLF]
	^	Telemetry[CRLF]
	6	Telemetry Headers[CRLF]
	D	Set 1PPS Discipline Tau[CRLF]
	S	Sync 1PPS [CRLF]
	U	Set parameters for ultra-low power mode [CRLF]
	M	Change Mode register [CRLF]
	T	Change/Report Time of Day[CRLF]
	?	Show this list[CRLF]

Note that the single-character ‘?’ is a shortcut for “!?[CRLF]”.

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