PXA166 800 MHz - PXA168 1066 MHz

Rev.A Notes:

D6 and TVS6 not pop ?

R113 pop ? (PS_MODE)

R78 not pop for PXA166

FB16 and FB17 not pop

No stencil change !!

Changes from Rev.P2

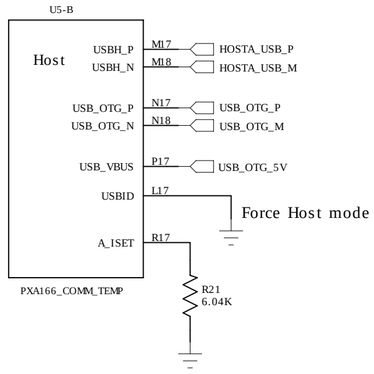
Change FB22 to 0 ohm (R69)

Added PD on EN_SINK_1.2V

U13 EN pin connected to 5V

Model = TS-7250-V2 Rev.A

USB Ports

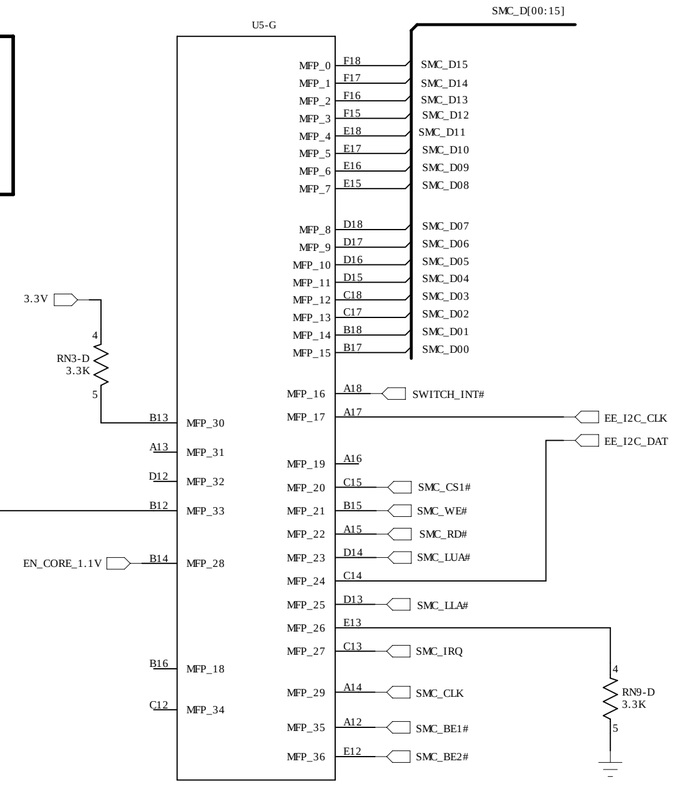


Board ID

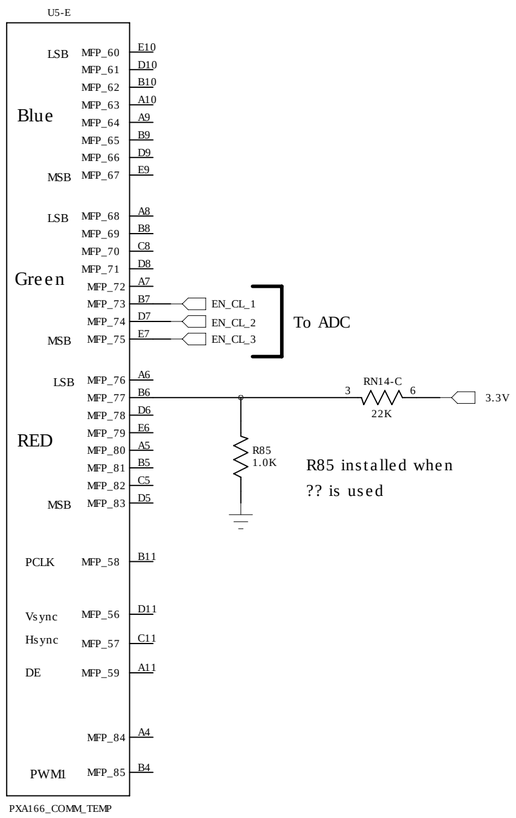
	MFP_26	MFP_30	MFP_33
TS-7250_V2	0	1	0
TS-7800_V2	1	1	1
TS-xxxx	0	0	0

Requires MFP to be Inputs

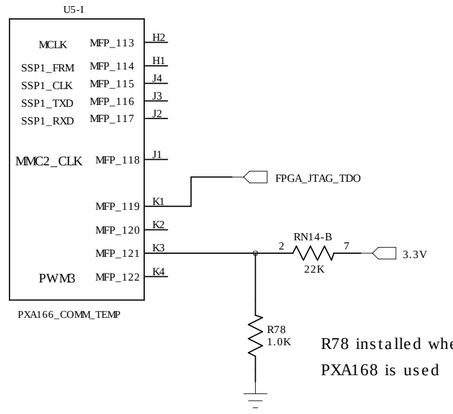
SMC Bus



LCD

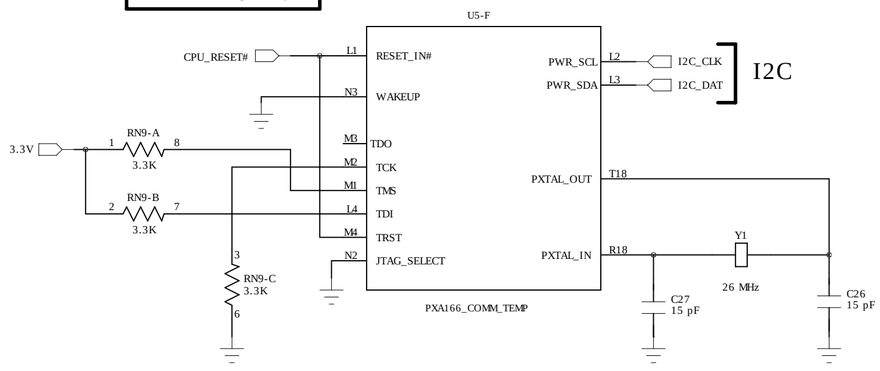


I2S

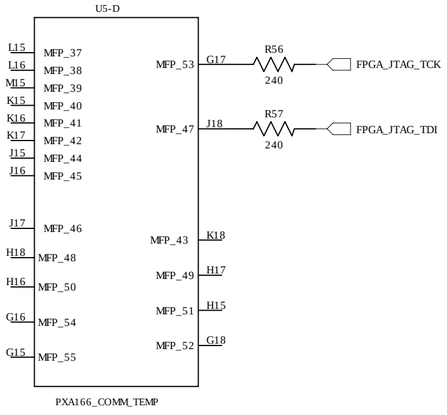


Control

RESET_IN# is Input only



Camera



U2 = PXA166 Commercial Temp

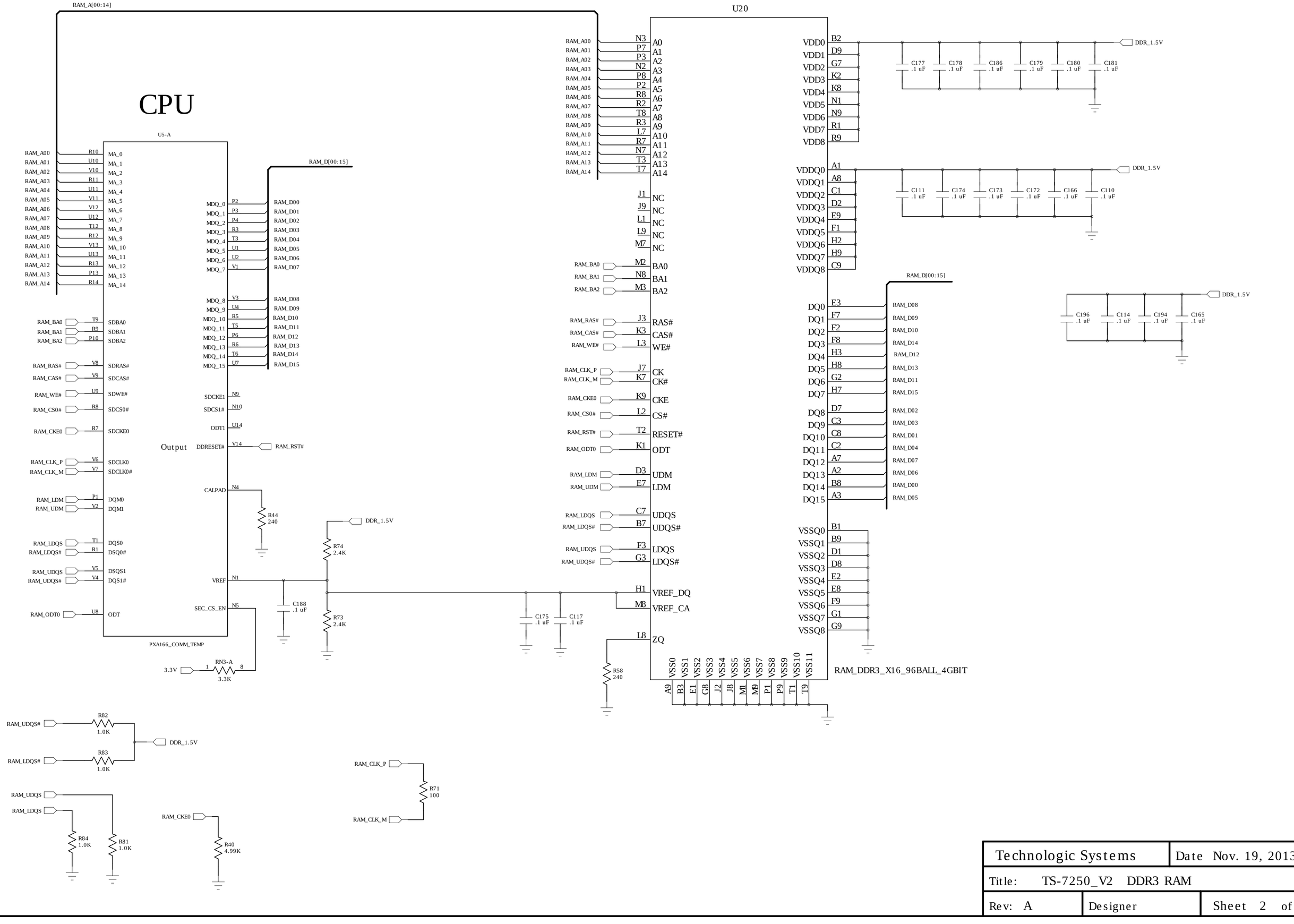
or = PXA168 Industrial Temp

Technologic Systems	Date Nov. 19, 2013	
Title: TS-7250_V2 Marvell PXA166 or PXA168		
Rev: A	Designer	Sheet 1 of 16

DDR3 256Mx16 RAM

4 Gbit RAM chip

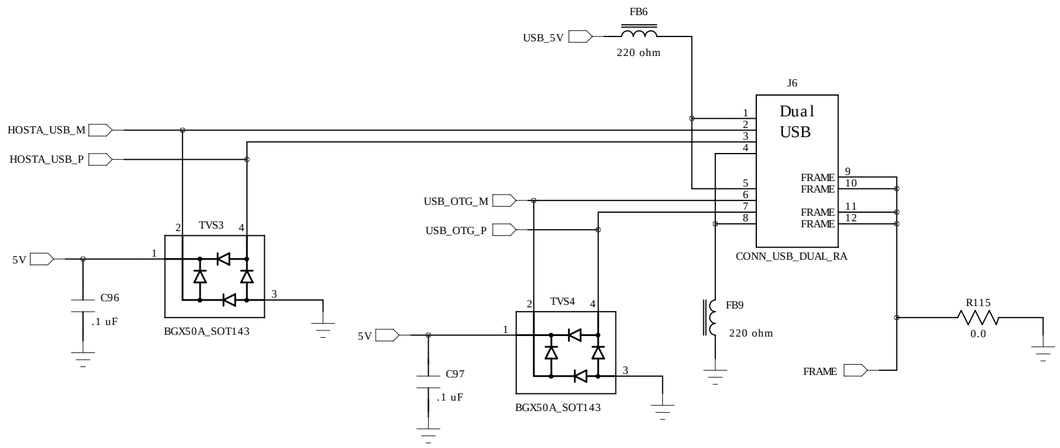
512 MB RAM



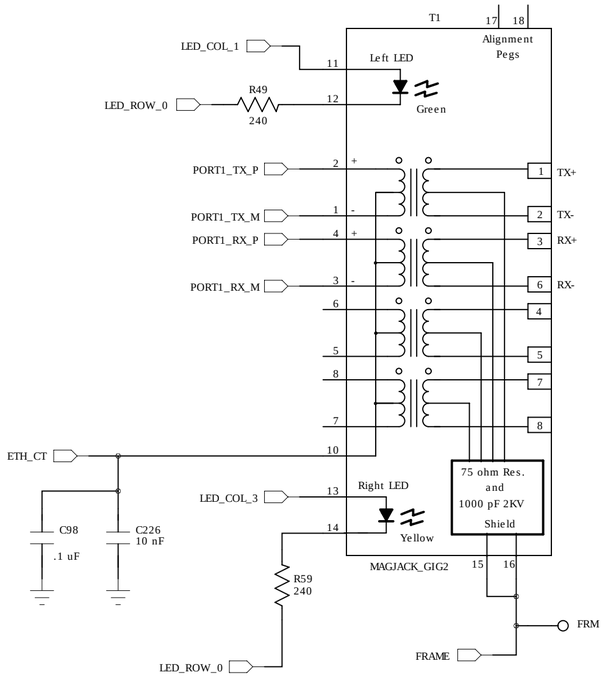
Technologic Systems	Date Nov. 19, 2013	
Title: TS-7250_V2 DDR3 RAM		
Rev: A	Designer	Sheet 2 of 16

Off-Board Connectors

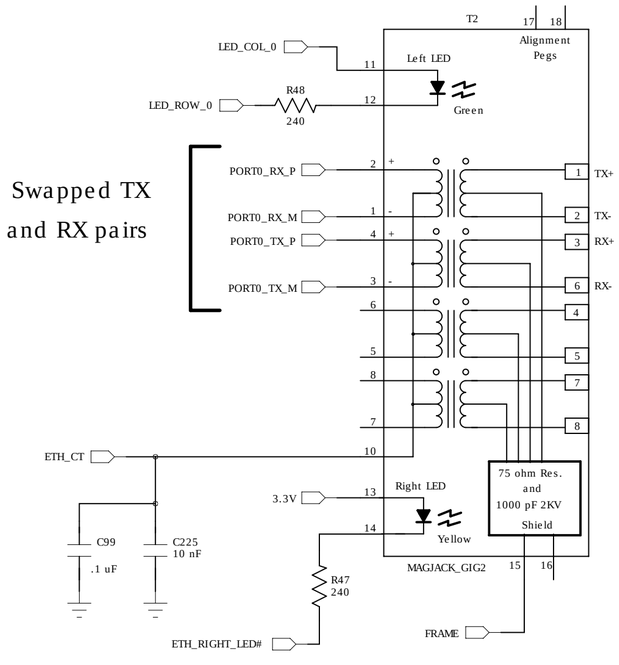
Dual Host USB Ports



Primary MagJack



Second MagJack



Technologic Systems		Date Nov. 19, 2013
Title: TS-7250_V2 Ethernet Magjacks		
Rev: A	Designer	Sheet 3 of 16

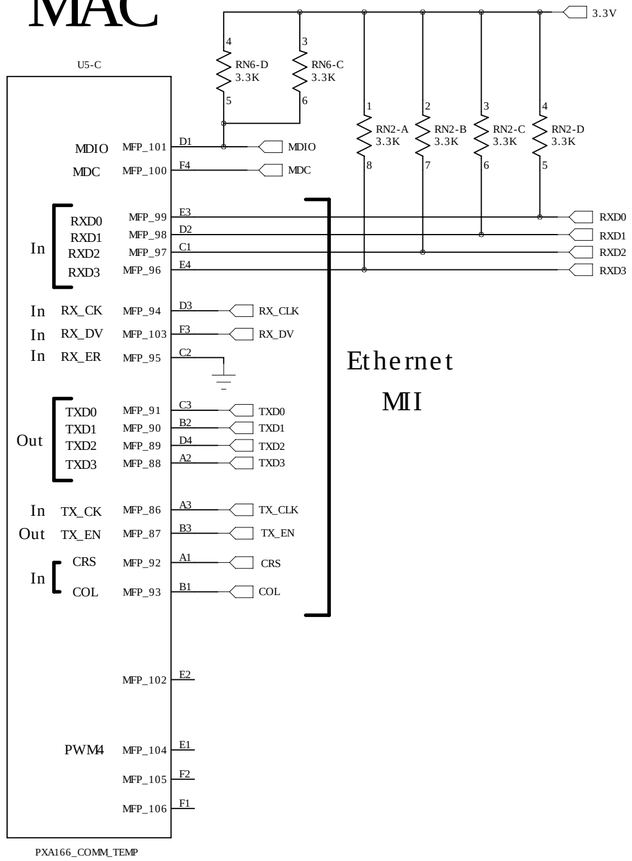
10/100 Ethernet 4-Port Switch

Total 88E6020
Current Drain includes
2 Ports with Mag CT

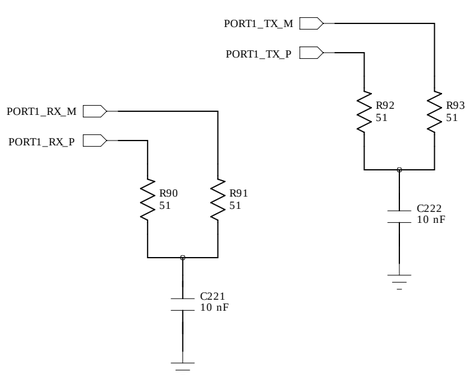
3.3V Rail = 20 mA
1.8V Rail = 80 mA
1.2V Rail = 62 mA

Pull-downs default P6
to port disabled mode

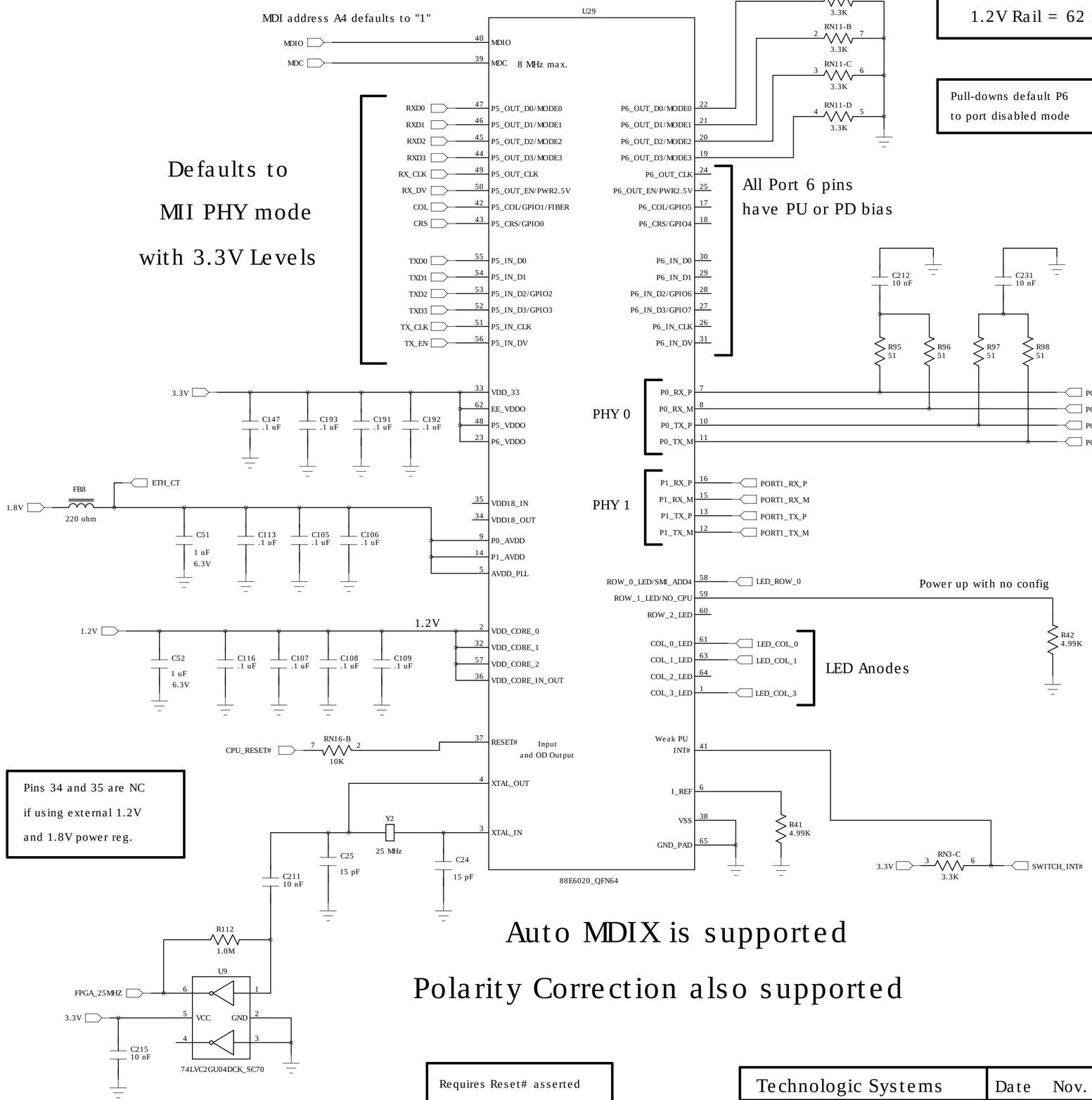
CPU
MAC



Ethernet
MII



Defaults to
MII PHY mode
with 3.3V Levels



Pins 34 and 35 are NC
if using external 1.2V
and 1.8V power reg.

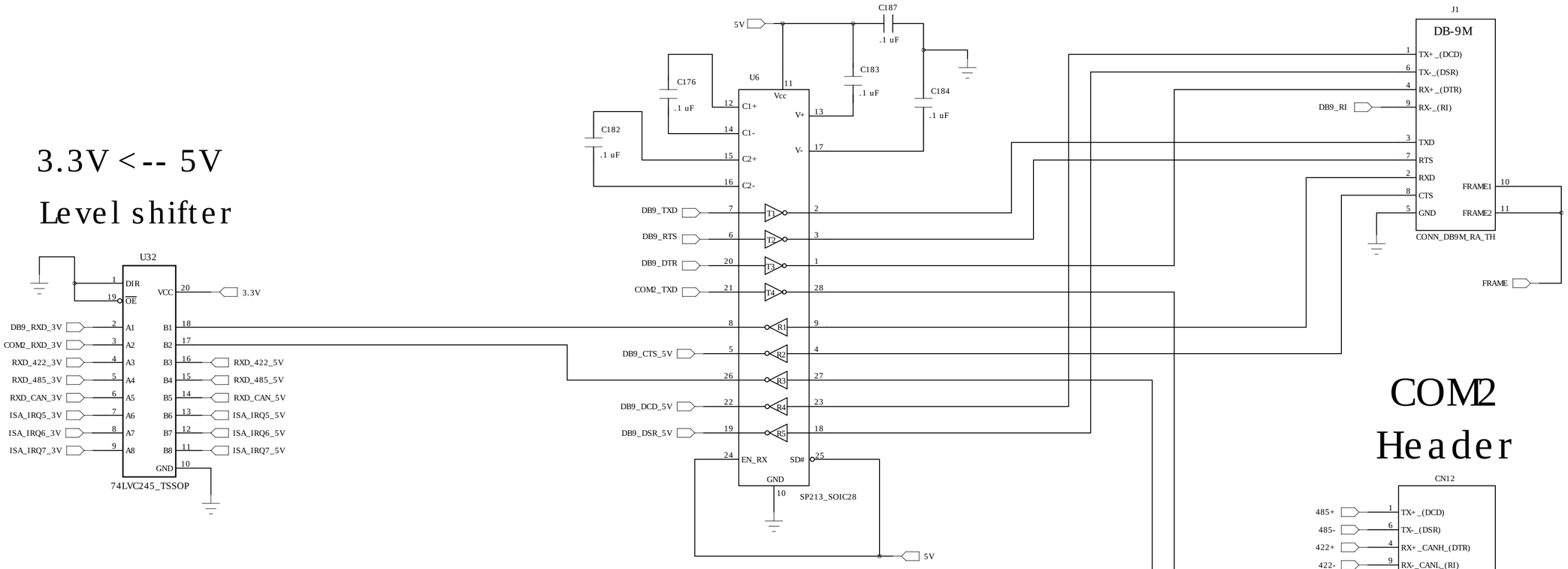
Auto MDIX is supported

Polarity Correction also supported

Requires Reset# asserted
for 10 ms after power

Technologic Systems	Date Nov. 19, 2013	
Title: TS-7250_V2 Ethernet Switch		
Rev: A	Designer RLM	Sheet 4 of 16

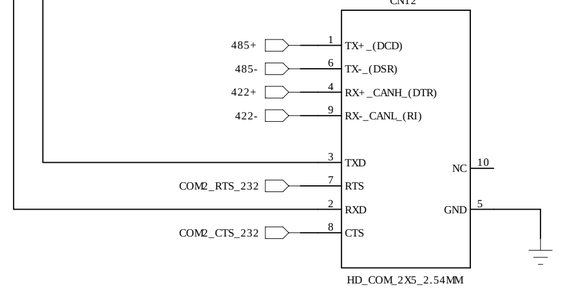
RS-232 Transceiver



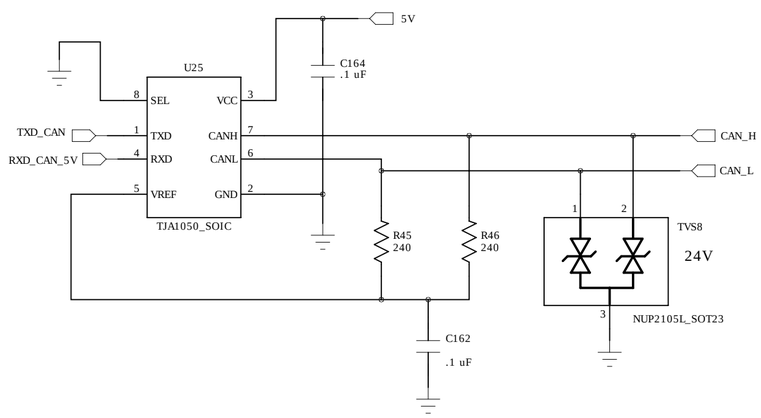
DB-9M

3.3V <-- 5V Level shifter

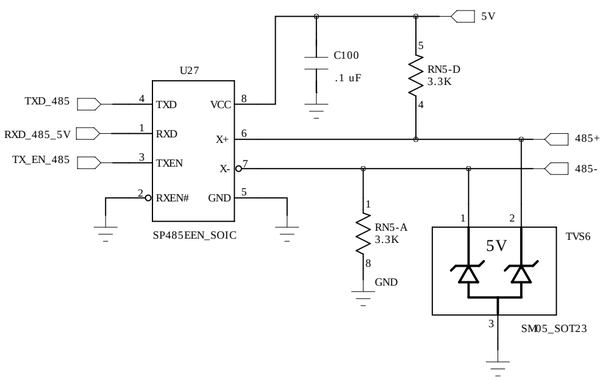
COM2 Header



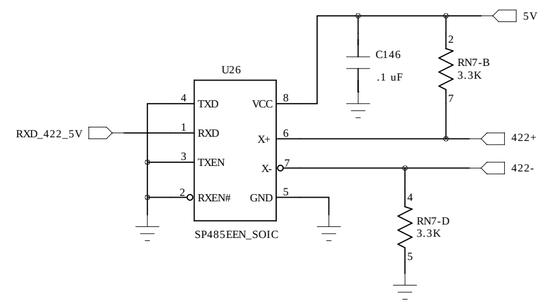
CAN Tranceiver



RS-485 Transceiver



RS-422 Receiver



Technologic Systems		Date Nov. 19, 2013
Title: TS-7250_V2 COM Ports, CAN, RS-485		
Rev: A	Designer	Sheet 5 of 16

FPGA with 8K LUTs

SMC_D[00:15]
SMC_D00 A15 PR3B_2
SMC_D01 B14 PR2B_2
SMC_D02 A14 PR3A_2
SMC_D03 B13 PT32A_1
SMC_D04 D15 PR10A_2
SMC_D05 F12 PR16A_2_CLK
SMC_D06 A13 PT32B_1
SMC_D07 A12 PT30B_1
SMC_D08 F13 PR14A_2
SMC_D09 E13 PR11B_2
SMC_D10 D14 PR6B_2
SMC_D11 C14 PR6A_2
SMC_D12 D13 PR11A_2
SMC_D13 D12 PT31B_1
SMC_D14 B11 PT26B_1
SMC_D15 A11 PT26A_1

SMC Bus from CPU
SMC_CLK T8 PB19A_5_CLK
SMC_RDY B8 PT20A_1_CLK
SMC_CS1# F15 PR13A_2
SMC_LLA# G14 PR16B_2_CLK
SMC_LUA# E16 PR12A_2
SMC_BE1# B16 PR7B_2
SMC_BE2# E12 PT31A_1
SMC_WE# H13 PR19B_3
SMC_RD#
SMC_IRQ B15 PR7A_2
F16 PR16A_2

Serial Ports
DB9_TXD D10 PT25B_1
DB9_RTS F9 PT23B_1
DB9_DTR F11 PR14B_2
DB9_RXD_3V N3 PL31A_6
DB9_CTS_3V R2 PL30A_6
DB9_DSR_3V C16 PR9B_2
DB9_DCD_3V H16 PR18B_3_CLK
COM2_TXD D11 PT27B_1
COM2_RTS N12 PB31A_4
COM2_RXD_3V J6 PL14B_7
COM2_CTS_3V P1 PL27A_6
COM3_TXD R13 PB26B_4
COM3_RTS L12 PR27B_3
COM3_RXD_3V R1 PL29A_6
COM3_CTS_3V N1 PL24B_6
TXD_485 T10 PB20A_4_CLK
TX_EN_485 T9 PB18B_5
RXD_485_3V J5 PL16B_7_CLK
RXD_422_3V N2 PL27B_6
TXD_CAN T11 PB22A_4
RXD_CAN_3V L4 PL23A_6
DEBUG_TXD C11 PT30A_1
DEBUG_RXD C13 PR2A_2
M0_TXD
M0_RXD E6 PT13A_0
L9 PB4A_5
JP2 N13 PR30A_3
JP3# J12 PR21B_3
I2C_CLK A7 PT18B_0
I2C_DAT K6 PL15B_7
FPGA_25MHZ H15 PR18A_3_CLK
CPU_RESET# B7 PT18A_0
3.3V RN4-A 8 1 3.3K
L6 TOE
L7 CFG0
FPGA_JTAG_TDO H12 JTAG_TDO
FPGA_JTAG_TDI G13 JTAG_TDI PU
FPGA_JTAG_TMS G11 JTAG_TMS PU
FPGA_JTAG_TCK H11 JTAG_TCK
3.3V RN4-C 3 6 3.3K
RN4-B 2 7 3.3K
3.3V

ISA_DAT_[00:15]
PT3A_0 B1 ISA_DAT_00
PT3B_0 A2 ISA_DAT_01
PT10B_0 A3 ISA_DAT_02
PT12A_0 B4 ISA_DAT_03
PT12B_0 A4 ISA_DAT_04
PT14B_0 A5 ISA_DAT_05
PT16A_0 B6 ISA_DAT_06
PT16B_0 A6 ISA_DAT_07
PB15A_5 M8 ISA_DAT_08
PB15B_5 N8 ISA_DAT_09
PB13B_5 P7 ISA_DAT_10
PB17A_5 P8 ISA_DAT_11
PB21A_4 M9 ISA_DAT_12
PB17B_5 N9 ISA_DAT_13
PB27A_4 M11 ISA_DAT_14
PB23B_4 N10 ISA_DAT_15
PB20B_4_CLK R10 ISA_ADD_00
PB18A_5 R8 ISA_ADD_01
PB16B_5 T7 ISA_ADD_02
PB14B_5 T6 ISA_ADD_03
PB12B_5 T5 ISA_ADD_04
PB11B_5 N6 ISA_ADD_05
PL25A_6 M5 ISA_ADD_06
PL21A_6 L5 ISA_ADD_07
PB2A_5 P4 ISA_ADD_08
PL32B_6 P3 ISA_ADD_09
PL24A_6 M1 ISA_ADD_10
PL23B_6 L3 ISA_ADD_11
PL18B_6_CLK J1 ISA_ADD_12
PB25A_4 L11 ISA_ADD_13
PT11B_0 G6 ISA_ADD_14
PT17B_0 F7 ISA_ADD_15
PL12B_7 G3 ISA_ADD_16
PL12A_7 F3 ISA_ADD_17
PT17A_0 D7 ISA_ADD_18
PR8B_2 F10 ISA_ADD_19
ISA_ADD_[00:19]
PR9A_2 C15
PL10B_7 G4 ISA_IOR#
PT4A_0 F4 ISA_IOW#
PT9B_0 D5 ISA_MEMW#
ISA_MEMR#
PT4B_0 D4
PT22A_1 D8 ISA_RESET
PB19B_5_CLK R9 ISA_14.3MHZ
PL2B_7 E4 ISA_ENDX
PT25A_1 D9 ISA_AEN
PL18A_6_CLK J2 ISA_REFRESH
PT15B_0 C7 ISA_IOCHK
PT14A_0 C6 ISA_IORDY
PT13B_0 F6 ISA_DRQ3
PT10A_0 C4 ISA_DRQ2
PL13B_7 H3 ISA_DACK3
PL21B_6 K3 ISA_IRQ5_3V
PL19B_6 K4 ISA_IRQ6_3V
PL19A_6 J4 ISA_IRQ7_3V
PL25A_6 M4
PT2A_0 B2 ISA_DATA_EN#
ISA_DIR
Data Buffer
PT2B_0 B3 ISA_IRQ9
PL16A_7_CLK H4 ISA_DACK1
PR22A_3 J11 ISA_DRQ1
PB11A_5 P6 ISA_IRQ3
PL22A_6 L1 ISA_BCLK
PB13A_5 N7 ISA_DACK2
PB14A_5 R6 ISA_TC
PB16A_5 R7 ISA_BALE
D8
D15
ISA
ISA
U8

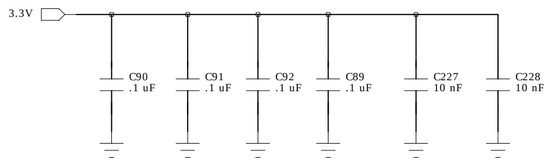
3.3V G8 VCC_AUX
H10 VCC_AUX
J7 VCC_AUX
K9 VCC_AUX
K7 VCC_JTAG
E3 VCCIO7
G5 VCCIO7
K5 VCCIO6
M3 VCCIO6
M7 VCCIO5
P5 VCCIO5
M10 VCCIO4
P12 VCCIO4
K12 VCCIO3
M14 VCCIO3
E14 VCCIO2
G12 VCCIO2
C12 VCCIO1
E10 VCCIO1
C5 VCCIO0
E7 VCCIO0
1.2V G7 V_CORE
G9 V_CORE
H7 V_CORE
J10 V_CORE
K8 V_CORE
K10 V_CORE
G10 NC
T15 NC
ISA_CN_D[01:15]
ISA_CN_D01 C9 PT23A_1
ISA_CN_D02 D6 PT15A_0
ISA_CN_D03 F5 PT11A_0
ISA_CN_D04 E5 PT9A_0
ISA_CN_D05 M13 PB32B_4
ISA_CN_D06 E9 PT22B_1
ISA_CN_D07 F8 PT19B_0_CLK
ISA_CN_D08 H5 PL15A_7
ISA_CN_D09 H6 PL14A_7
ISA_CN_D10 K11 PR22B_3
ISA_CN_D11 K2 PL20A_6
ISA_CN_D12 L2 PL22B_6
ISA_CN_D13 P2 PL29B_6
ISA_CN_D14 N4 PL28B_6
ISA_CN_D15 N5 PB2B_5
E8 PT19A_0_CLK
L10 PB21B_4
M0_SPARE_1 M6 PL28A_6

PB22B_4 R11 SD_D0
PB27B_4 N11 SD_D1
PB24B_4 P11 SD_D2
PB25B_4 M12 SD_D3
PB24A_4 T12 SD_CMD
PB26A_4 T13 SD_CLK_MIC
PL30B_6 T2 SD_CLK_FS
PL32A_6 R3 SD_POWER#
PB3B_5 T4 SD_FLT_LED#
PB12A_5 R4 ACT_LED#
SD_WP
SD Card
PB28A_4 T14
PR21A_3 J15 SPI_MOSI
PR19A_3 J14 SPI_MISO
PR27A_3 L13 SPI_CLK
PR30B_3 N14 SPI_CS#
SPI Bus
PB4B_5 L8 M0_12MHZ_CLK
PR8A_2 E11 M0_SPARE_0
PR23A_3 K15 ADC_DAT
PR24A_3 K14 ADC_CLK
PR29B_3 N16 ADC_A0
PR29A_3 N15 ADC_A1
PR28A_3 L16 ADC_A2
ADC
PL11B_7 H1 MMC_FLT_LED#
PL6B_7 C2 EMMC_D0
PL13A_7 H2 EMMC_D1
PL7A_7 C1 EMMC_D2
PL11A_7 G1 EMMC_D3
PL8B_7 E1 EMMC_D4
PL7B_7 D1 EMMC_D5
PL9A_7 F2 EMMC_D6
PL8A_7 D2 EMMC_D7
PL10A_7 G2 EMMC_CLK
PB23A_4 P10 EMMC_CMD
PL9B_7 F1 EMMC_RESET#
eMMC Flash Drive
PT21B_1 A9 DIO_PIN1
PR21A_3 J13 DIO_PIN3
PT24B_1 A10 DIO_PIN5
PR12B_2 F14 DIO_PIN7
PT20B_1_CLK A8 DIO_PIN8
PT21A_1 B9 DIO_PIN9
PR24B_3 K13 DIO_PIN11
PT24A_1 B10 DIO_PIN13
DIO_PIN15
PR15A_2 G15 EN_DIO_FET
PB3A_5 T3
DIO Header
PB30A_4 R16 LCD_EN
PB29B_4 P15 LCD_WR#
PB31B_4 P14 LCD_RS
PB29A_4 R15 LCD_BIAS
PR25B_3 L14 LCD_PIN7
PT27A_1 C10 LCD_PIN8
LCD_PIN9
PR15B_2 G16 LCD_PIN10
PR20B_3 J16 LCD_PIN11
PR28B_3 M16 LCD_PIN12
PR23B_3 K16 LCD_PIN13
PR10B_2 D16 LCD_PIN14
PR25A_3 L15
LCD Header
PL2A_7 D3
PL6A_7 C3 RED_LED#
FPGA_EN_GRN_LED
ETH_RIGHT_LED#
PB30B_4 P16
PB32A_4 P13 EN_USB_5V
PL20B_6 K1 REBOOT
PB28B_4 R14 BOOT_FLAG

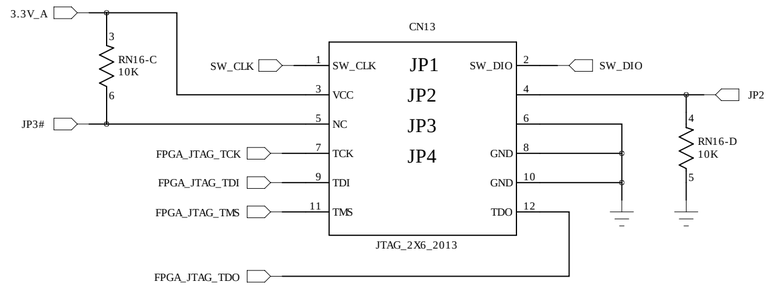
LATTICE_XP2_8K_LUT_256_BALL
GND1 A1
GND2 A16
GND3 B12
GND4 B5
GND5 C8
GND6 E2
GND7 E15
GND8 H8
GND9 H9
GND10 H14
GND11 J3
GND12 J8
GND13 J9
GND14 M2
GND15 M15
GND16 P9
GND17 R5
GND18 R12
GND19 T1
GND20 T16

Technologic Systems	Date Nov. 19, 2013	
Title: TS-7250_V2 FPGA		
Rev: A	Designer	Sheet 6 of 16

FPGA Caps



JTAG Header



Jumpers:

JP1 = ??

JP2 = SD Boot

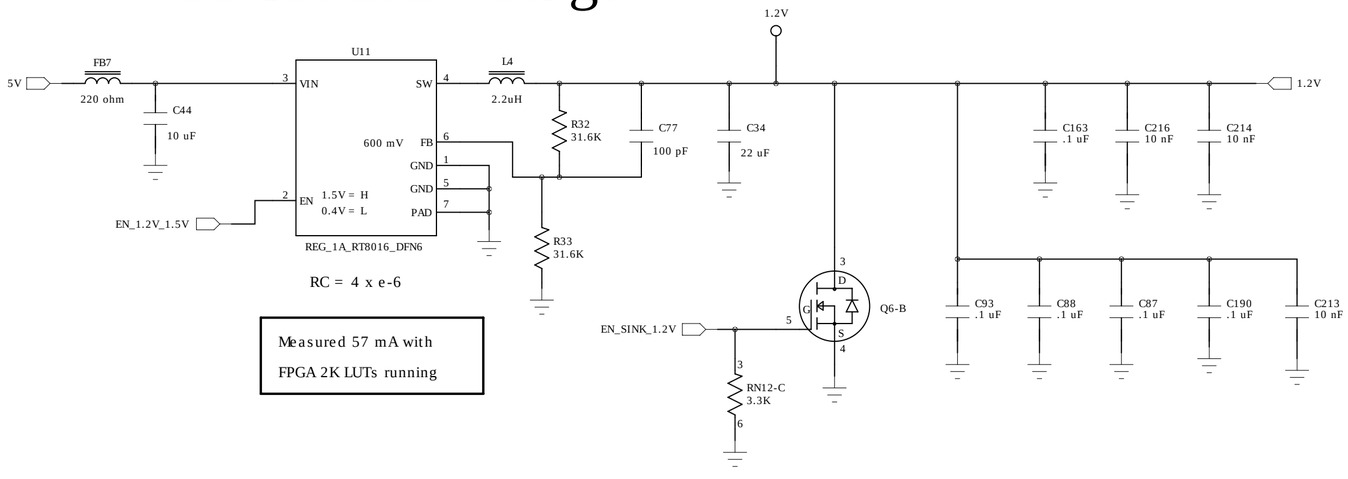
JP3 = Console --> DB9

JP4 = User

If JP4 installed

CPU can not reload FPGA

#4 FPGA 1.2V Reg.



RC = 4 x e-6

Measured 57 mA with

FPGA 2K LUTs running

Page 37 of Data Sheet (Hot Socketing)

FPGA Power Supplies can be sequenced in

any order but must be monotonic

All I/O lines are tri-stated during power cycling

TS-7250

Jumpers:

JP1 = Boot Serial

JP2 = Console Enable

JP3 = Write Enable Flash

JP4 = Stop @ Redboot

JP5 = TS_Test

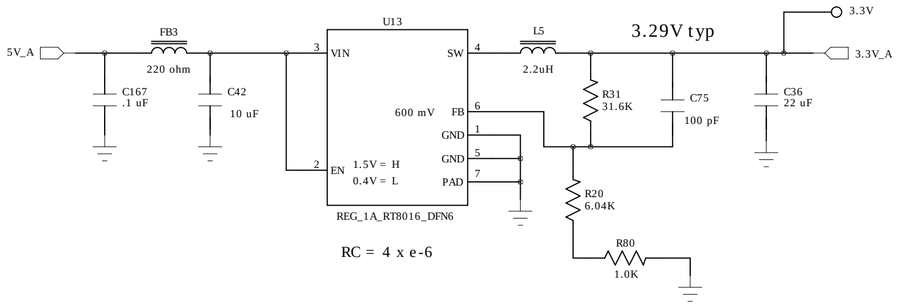
JP6 = Reserved

Technologic Systems		Date Nov. 19, 2013
Title: TS-7250_V2 FPGA PS, JTAG		
Rev: A	Designer	Sheet 7 of 16

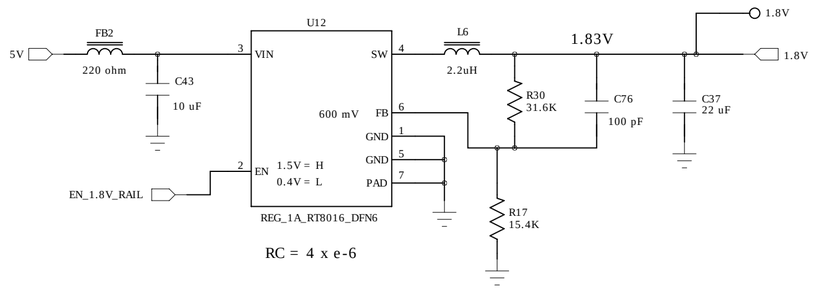
Power Supplies

#1 3.3V Power Supply

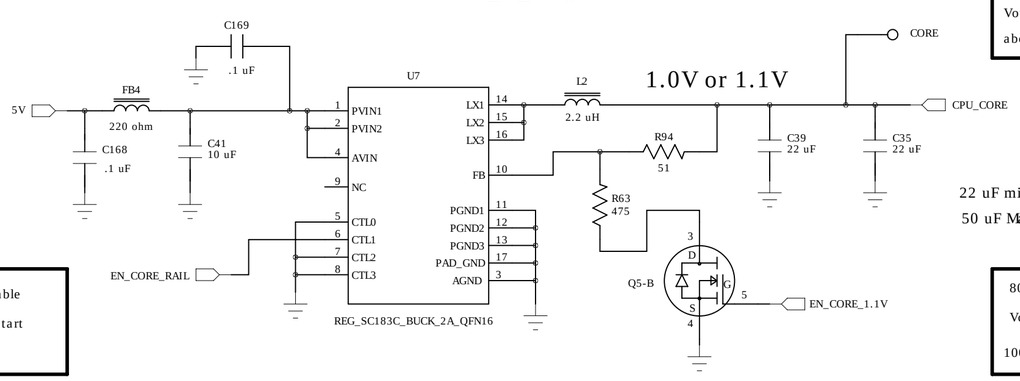
up to 1000 mA



#2 1.8V Regulator



#3 CPU Core Supply



Vout rise time
about 130 us

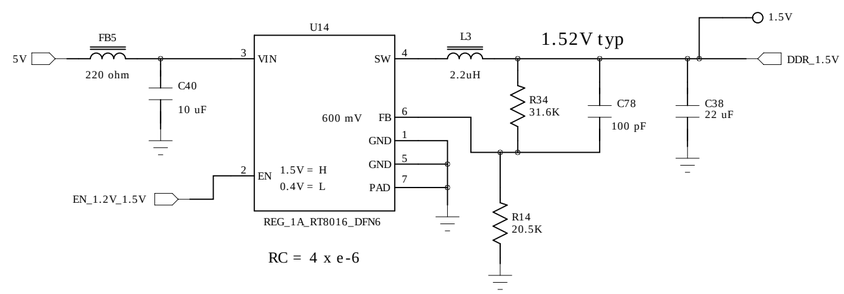
22 uF minimum
50 uF Max.

Delay from Enable
to Vout ramp start
is typ. 50 us

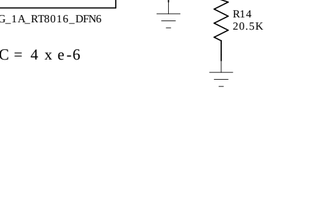
800 MHz CPU needs
Vcore = 1.00V

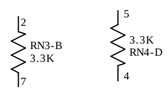
1000 MHz needs 1.10V

#4 DDR3 1.5V Reg.



#5 CPU USB Power





Technologic Systems	Date Nov. 19, 2013	
Title: TS-7250_V2 Power Supplies		
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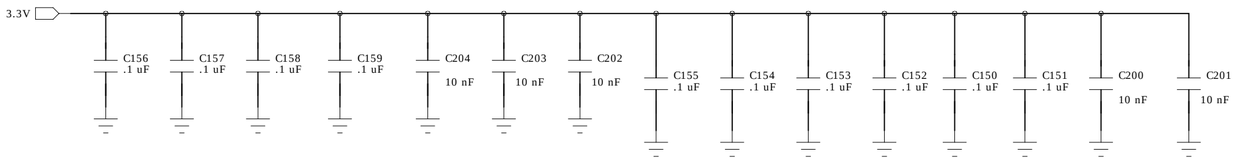
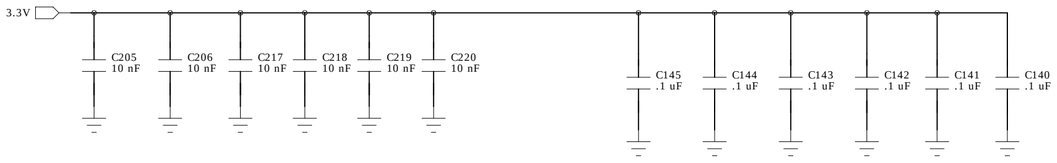
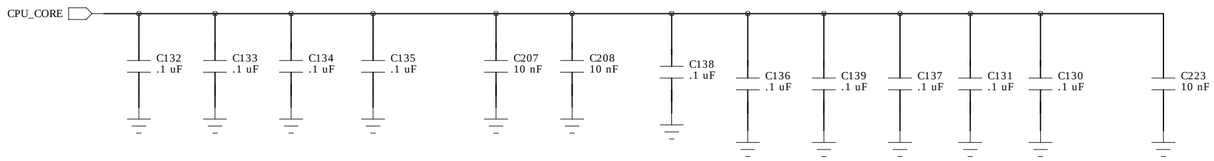
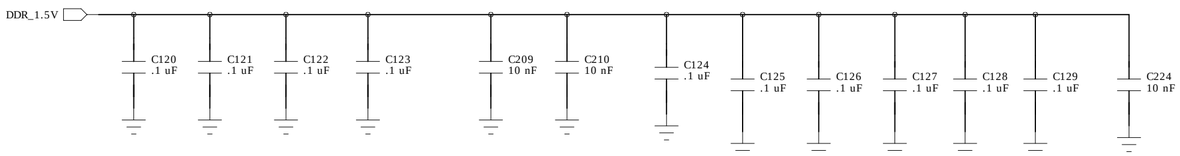
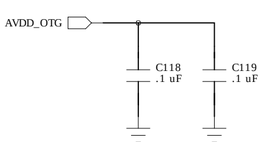
CPU Power





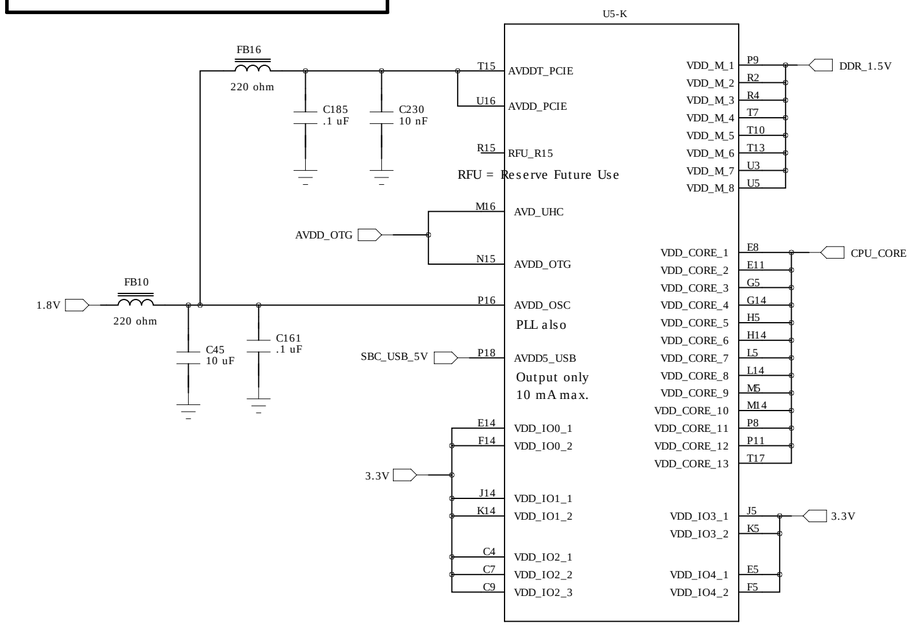




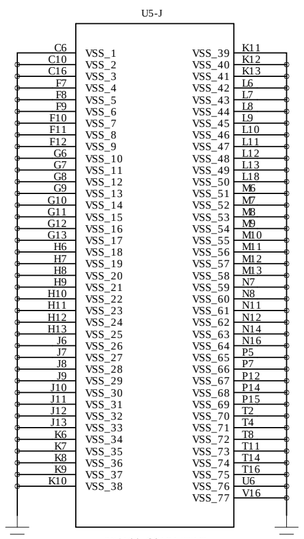


CPU

PXA168 PCIE rails must be connected to AN_1.8V



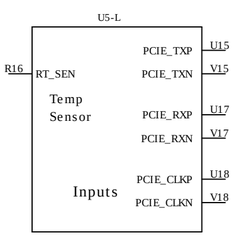
CPU



CPU PCIe

Not used

PCIe not supported on PXA166



Technologic Systems	Date Nov. 19, 2013	
Title: TS-7250_V2 CPU Power, Bypass caps		
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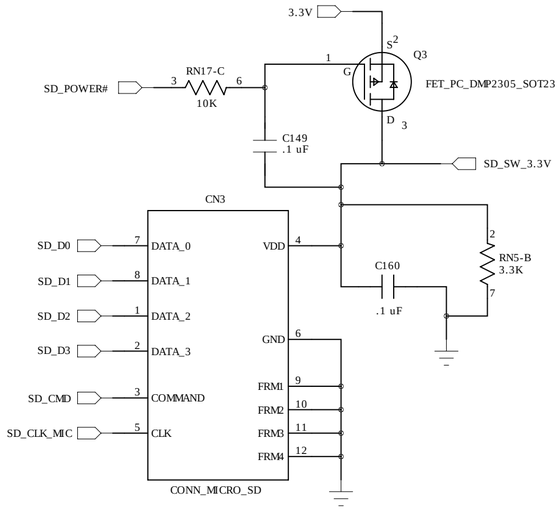
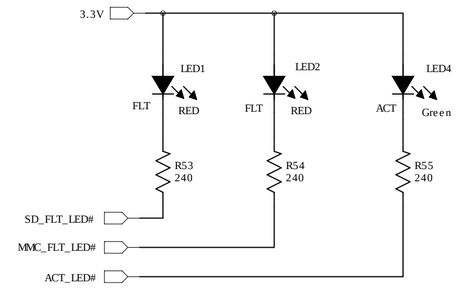
Flash Storage

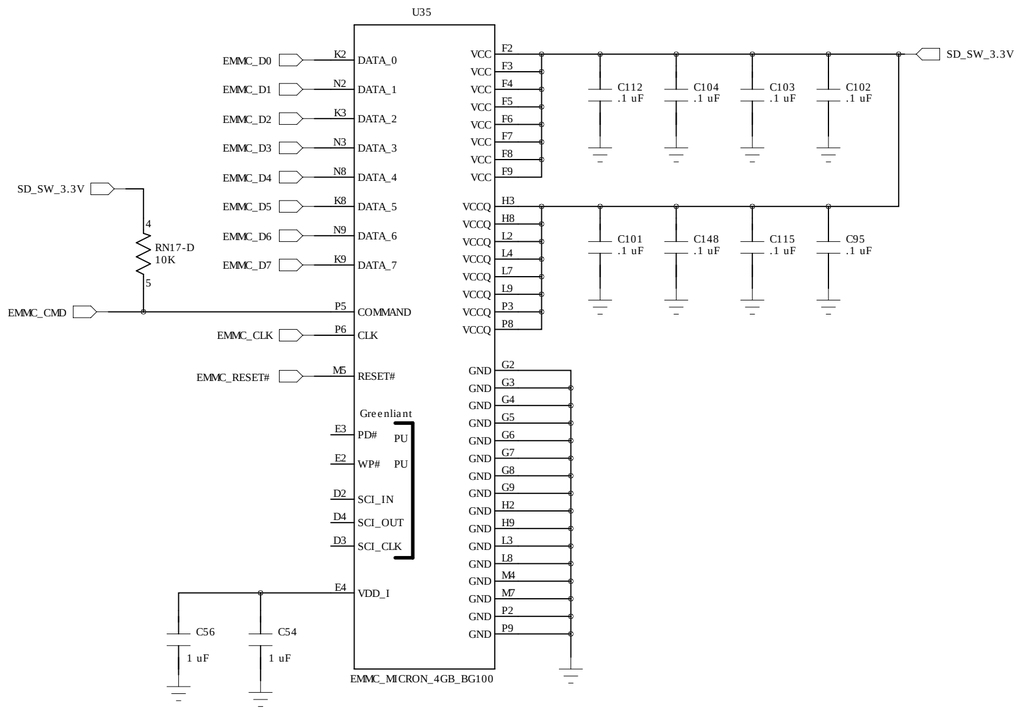
Micro SD Card Socket



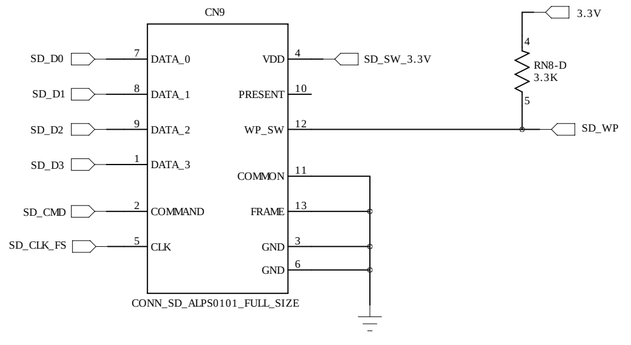
SD Card LEDs



eMMC 4GB



Full Size SD Socket



Technologic Systems	Date Nov. 19, 2013	
Title: TS-7250_V2 SD card, eMMC		
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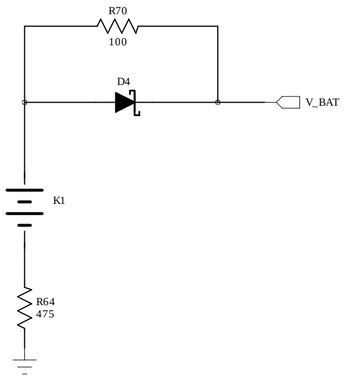
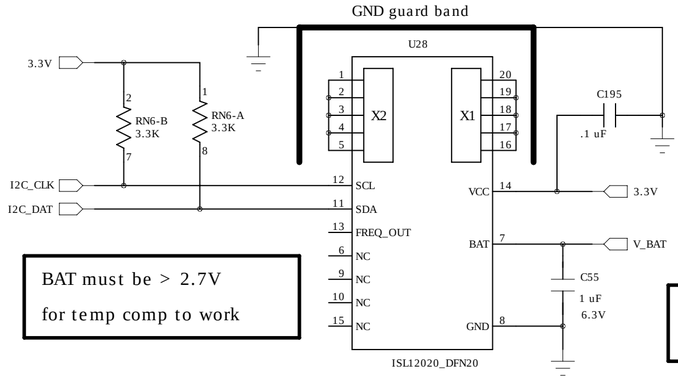
RTC Battery



RTC and Temp. Sensor

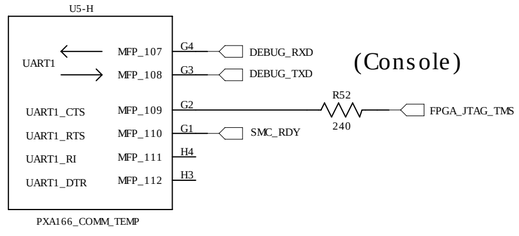


BAT must be > 2.7V
for temp comp to work

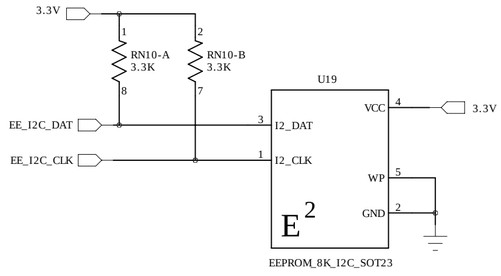
Temp takes 68 uA for 22 ms
Once every 1 or 10 min.

CPU

Debug UART



EEPROM 1 Kbyte



Technologic Systems	Date Nov. 19, 2013	
Title: TS-7250_V2 RTC, Battery, Boot Flag		
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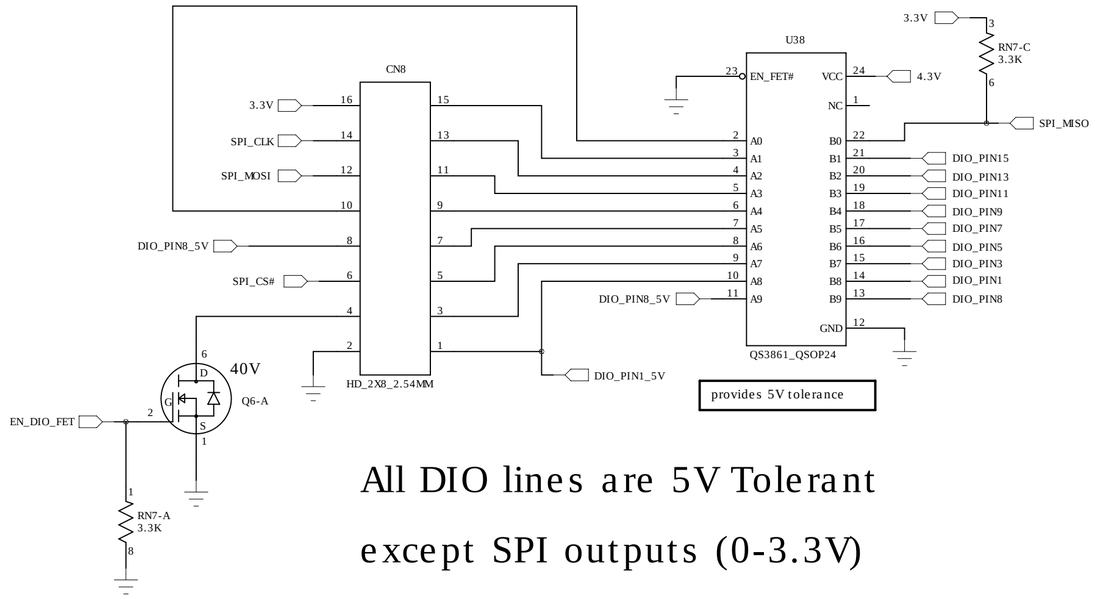
DIO and LCD Headers

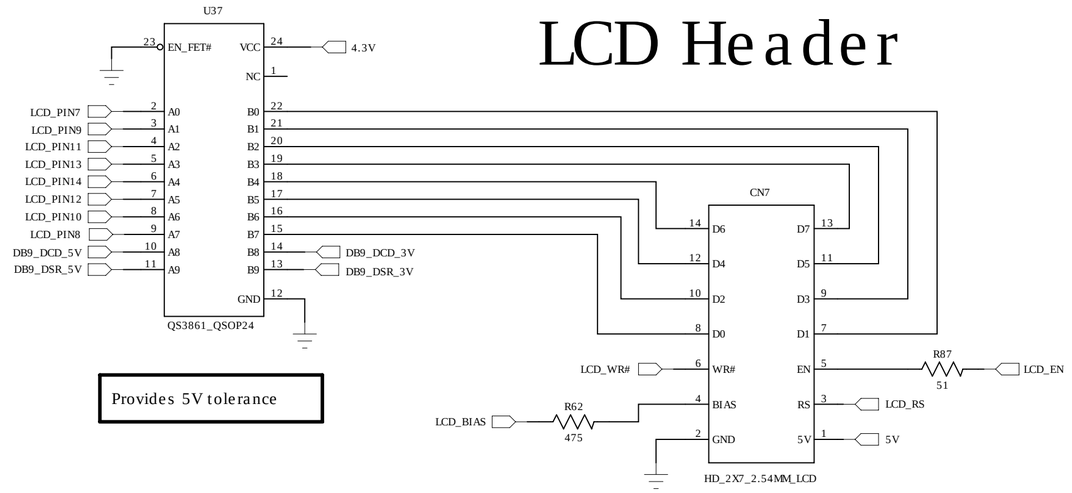
DIO Header



All DIO lines are 5V Tolerant

except SPI outputs (0-3.3V)

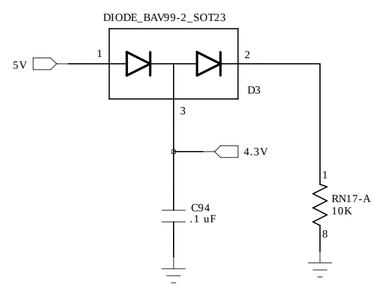
LCD Header



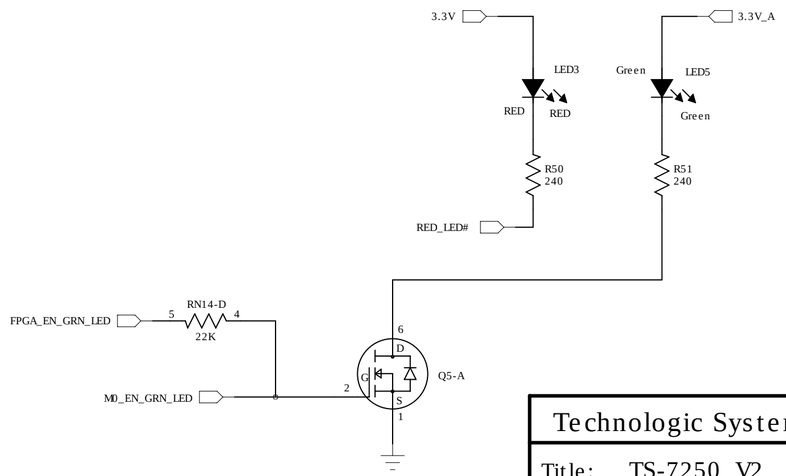
LCD Data lines are 5V tolerant

All LCD pins are bi-directional DIO

4.3V Supply



Red and Green LEDs

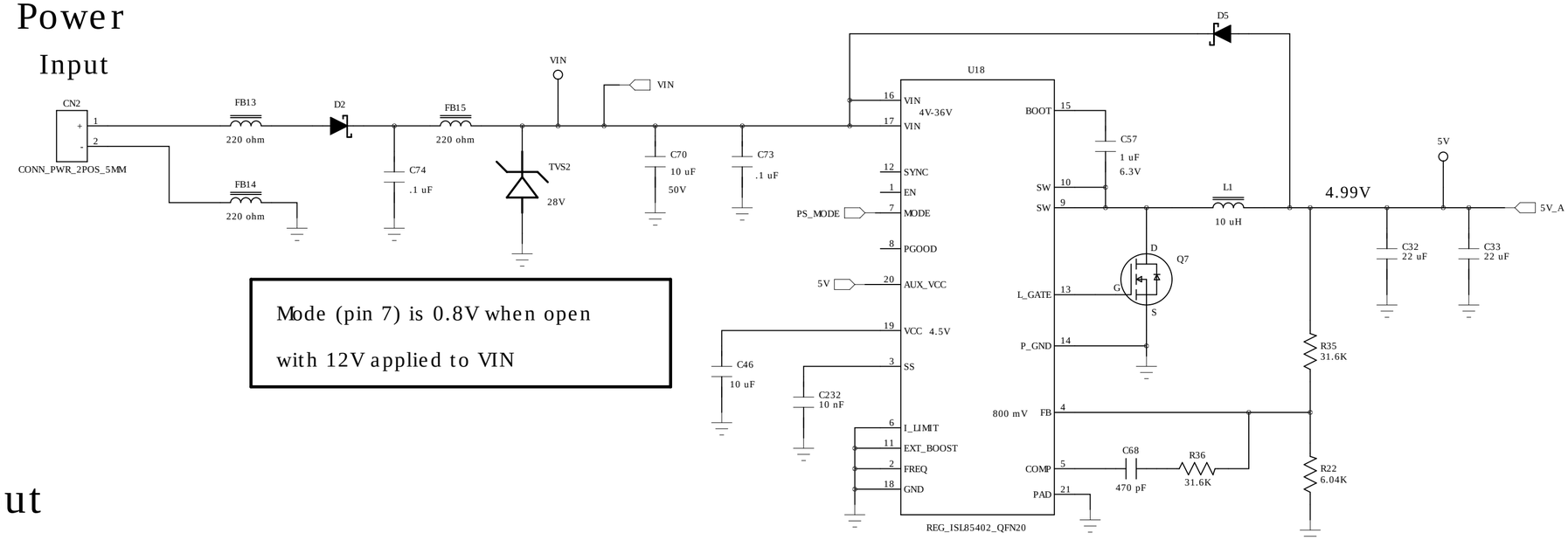


Technologic Systems		Date Nov. 19, 2013
Title: TS-7250_V2 DIO and LCD Headers		
Rev: A	Designer	Sheet 12 of 16

5V Power Supply (2000 mA)

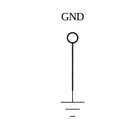
8V-28V

Power Input

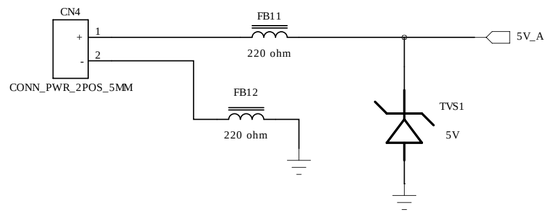


Mode (pin 7) is 0.8V when open with 12V applied to VIN

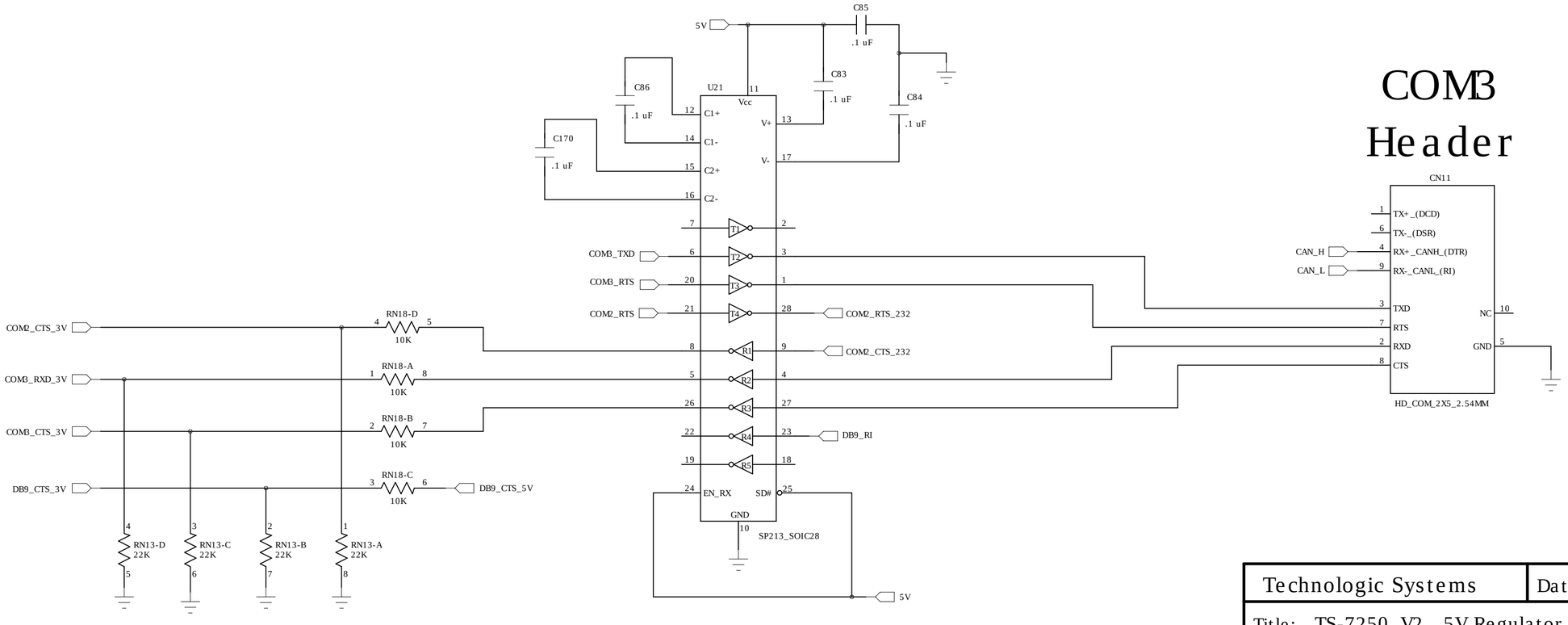
.063 hole



5V Input



RS-232 Transceiver



COM3 Header

Technologic Systems		Date Nov. 19, 2013
Title: TS-7250_V2 5V Regulator		
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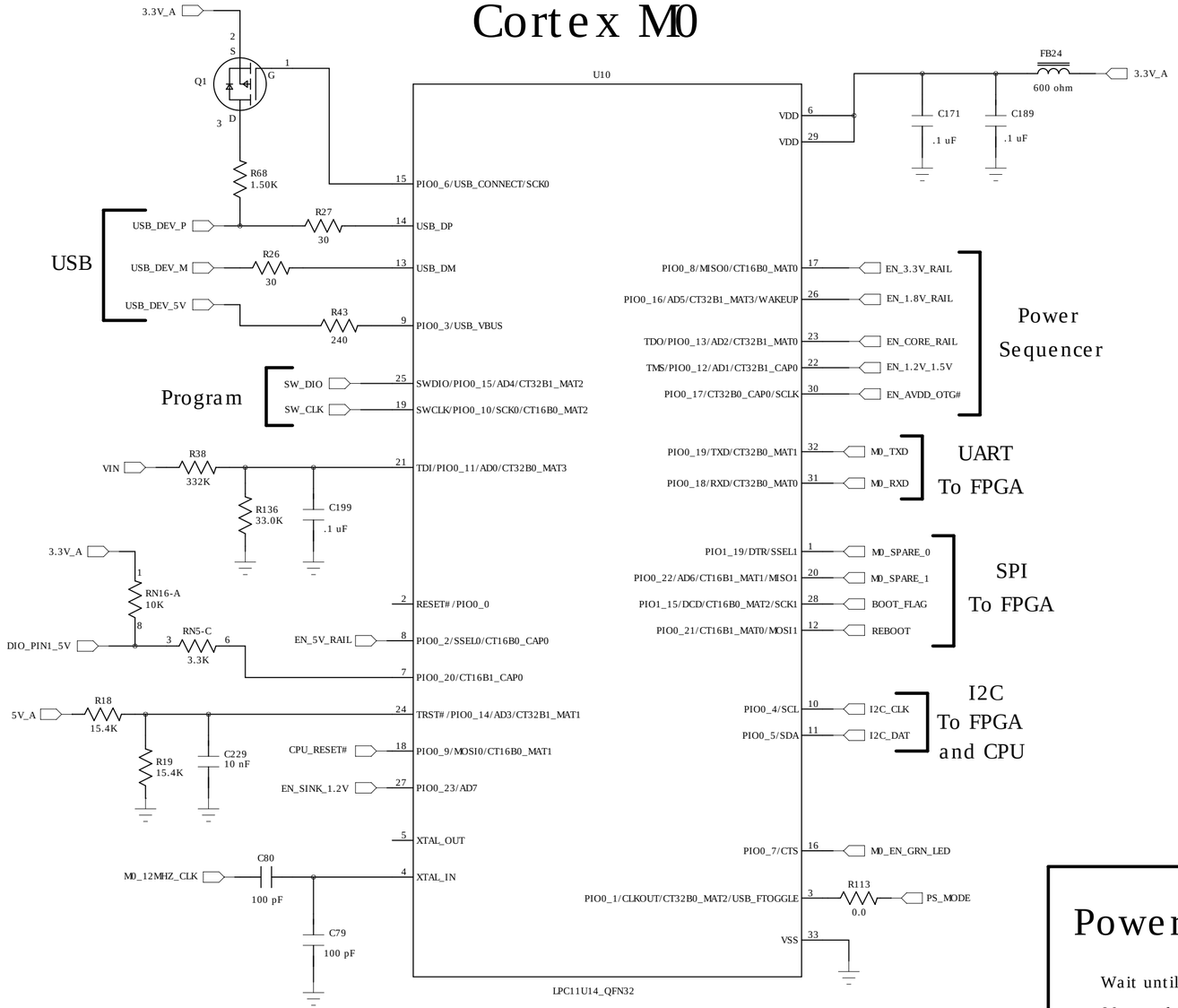
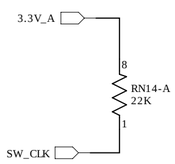
USB Device Port and Cortex M0

Cortex M0



Pins 2 and 3 must be high at Pwr up

DIO pin 1, SW_CLK, or SW_DIO can be used for M0 "Wake up"



To test JP1, set SW_DIO low for 2 us
read SW_CLK, then tri-state SW_DIO

Power Sequencer

Wait until 5V_A rail > 4.2V for 80 ms, then start sequencing

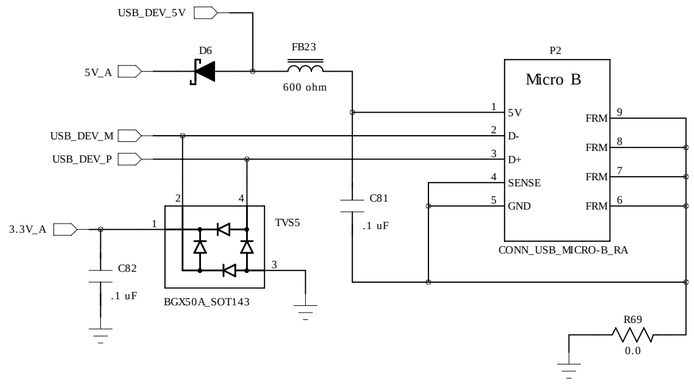
Delay:

	1 - Enable 5V Rail
5 ms	2 - Enable 3.3V Rail
5 ms	3 - Enable 1.8V Rail
5 ms	4 - Enable Core Rail
5 ms	5 - Enable 1.2V and 1.5V
5 ms	6 - Enable AVDD_OTG Rail
80 ms	7 - Deassert CPU_RESET#

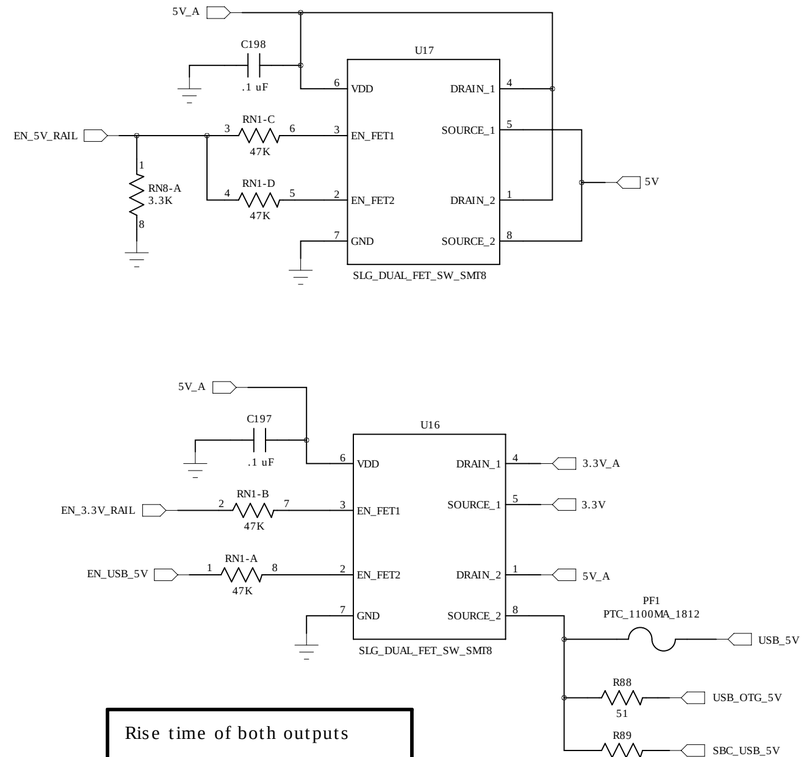
EN_SINK_1.2V is always complement of EN_1.2V_1.5V

If 5V_A < 4.0V, Deassert all Enables

USB Device Port



Switched Power



Rise time of both outputs measured at ~1V/ms

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Title: TS-7250_V2 Cortex M0		
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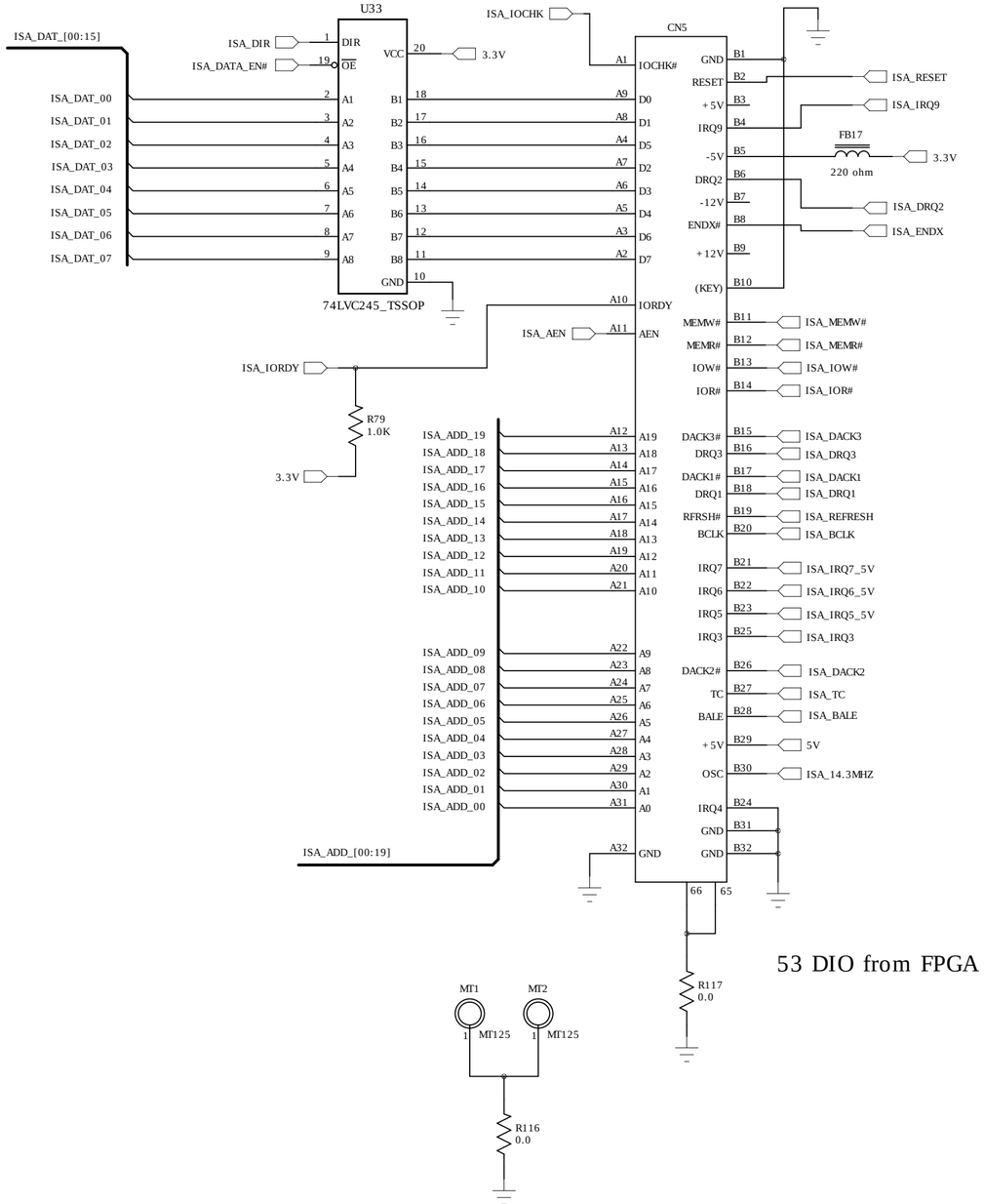
PC/104 Bus

PC/104

64-pin Connector

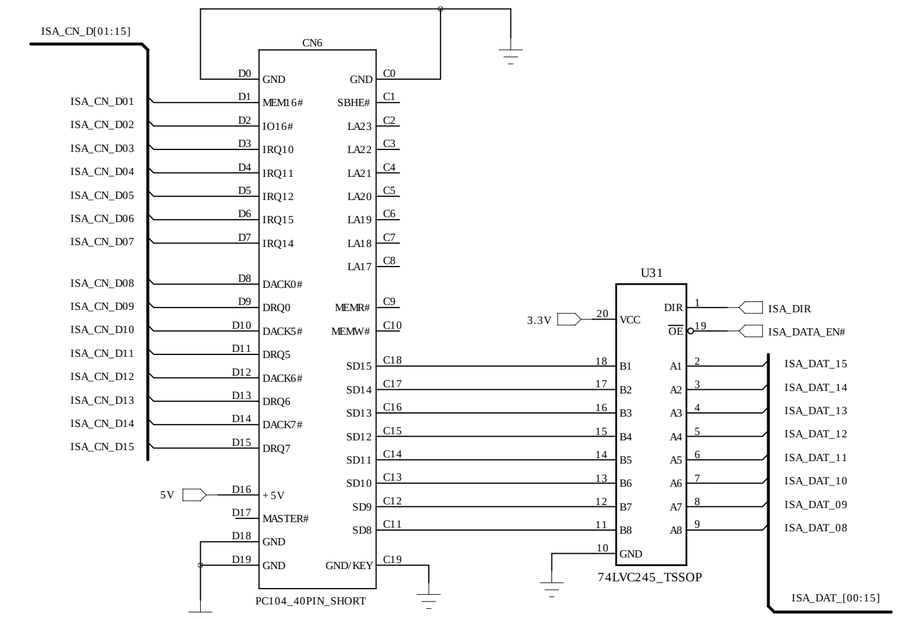


53 DIO from FPGA

Data lines and IRQ5-7
are all 5V tolerant

PC/104

40-pin Connector



23 DIO from FPGA

Technologic Systems		Date Nov. 19, 2013
Title: TS-7250_V2 PC/104 Bus		
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0 to +30V Input range

or

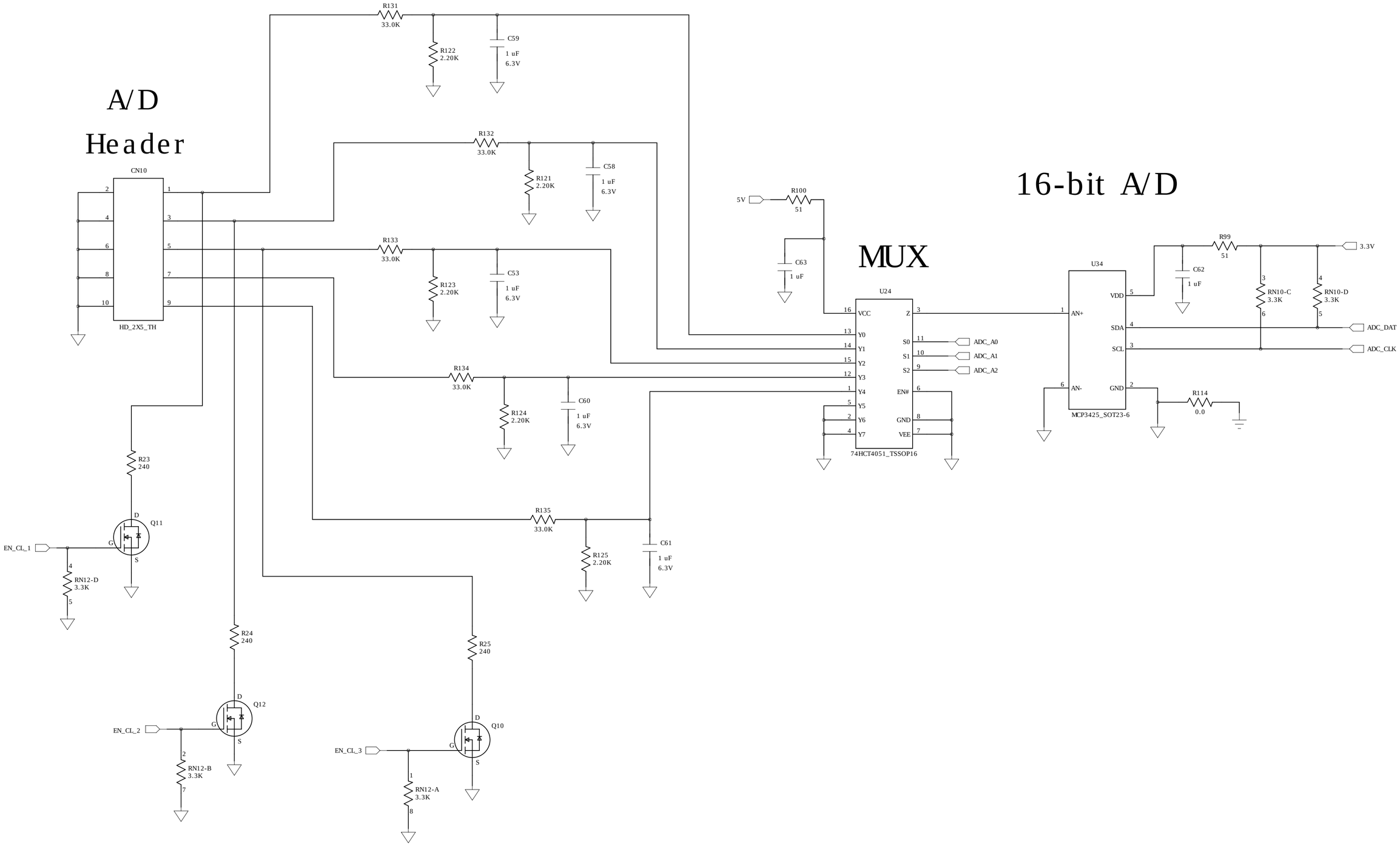
4-20 mA (3 channels)

Analog Inputs

A/D Header

16-bit A/D

MUX



Technologic Systems	Date Nov. 19, 2013	
Title: TS-7250_V2 PC/104 Bus		
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