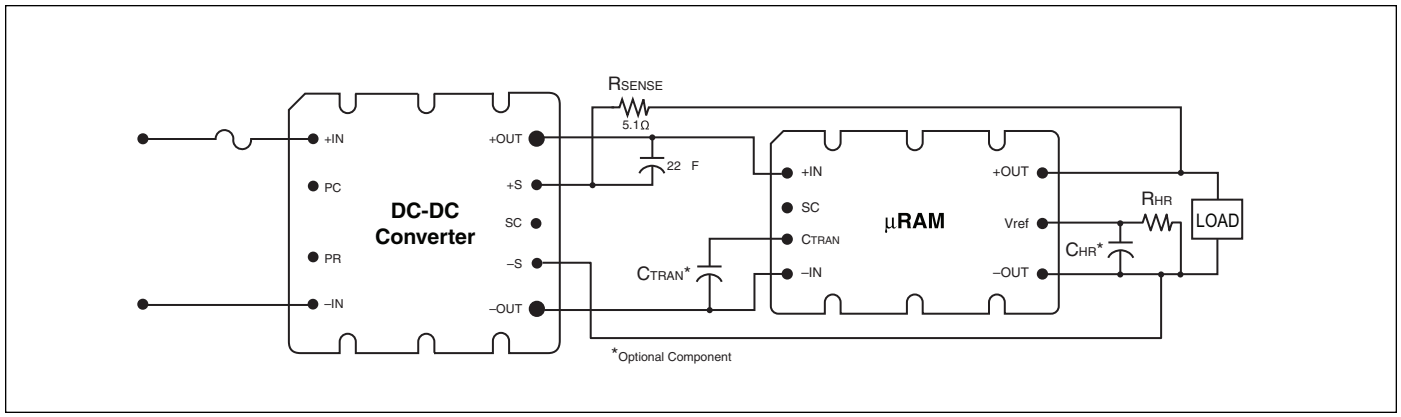

Figure 12–1a *— Typical configuration using remote sense*

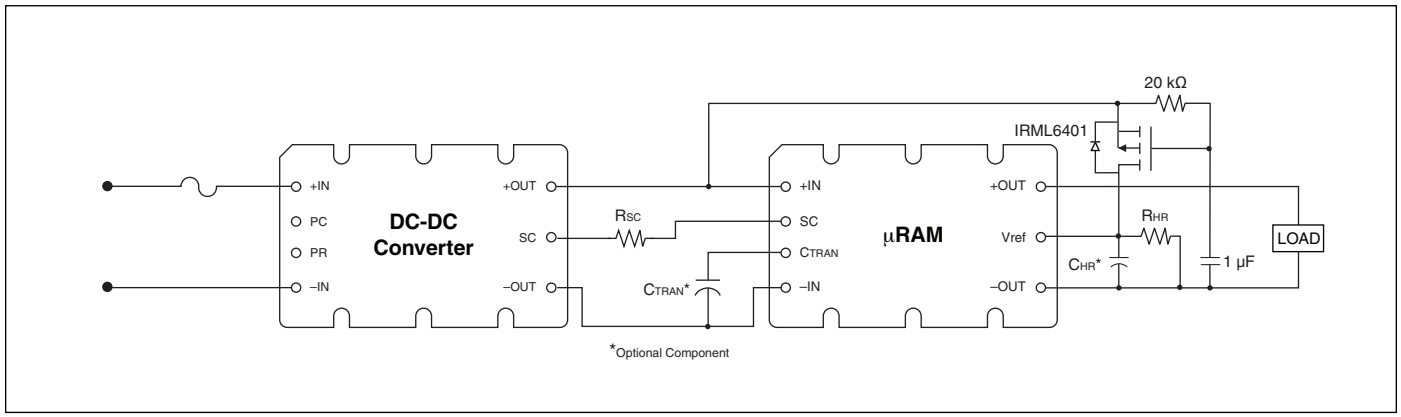

Figure 12–1b *— Typical configuration using SC control (Optional CHR, 25 µF maximum in SC configuration.)*

FUNCTIONAL DESCRIPTION

The MicroRAM has an internal passive filter, (Figure 12–2) that effectively attenuates ripple in the 50 kHz to 1 MHz range. An active filter provides attenuation from low frequency up to the 1 MHz range. The user must set the headroom voltage of the active block with the external RHR resistor to optimize performance. The MicroRAM must be connected as shown in Figures 12–1a or 12–1b depending on the load-sensing method. The transient load current performance can be increased by the addition of optional CTRAN capacitance to the CTRAN pin. The low-frequency ripple attenuation can be increased by addition of optional CHR capacitance to the VREF pin as shown in Figures 12–3a and 12–3b.

Transient load current is supplied by the internal CTRAN capacitance, plus optional external capacitance, during the time it takes the converter loop to respond to the increase in load. The MicroRAM's active loop responds in roughly one microsecond to output voltage perturbations. There are limitations to the magnitude and the rate of change of the transient current that the MicroRAM can sustain while the converter responds. See Figures 12–8 through 12–16 for examples of dynamic performance. A larger headroom voltage setting will provide increased transient performance, ripple attenuation, and power dissipation while reducing overall efficiency. (Figures 12–4a, 12–4b, 12–4c, and 12–4d)

The active loop senses the output current and reduces the headroom voltage in a linear fashion to approximate constant power dissipation of MicroRAM with increasing loads. (Figures 12–7, 12–8 and 12–9) The headroom setting can be reduced to decrease power dissipation where the transient requirement is low and efficient ripple attenuation is the primary performance concern.

The active dynamic headroom range is limited on the low end by the initial headroom setting and the maximum expected load. If the maximum load in the application is 10 A, for example, the 1 A headroom can be set 75 mV lower to conserve power and still have active headroom at the maximum load current of 10 A. The high end or maximum headroom range is limited by the internal ORing diode function.

The SC or trim-up function can be used when remote sensing is not available on the source converter or is not desirable. It is specifically designed for converters with a 1.23 V reference and a 1 kΩ input impedance like Vicor Maxi, Mini, Micro converters. In comparison to remote sensing, the SC configuration will have an error in the load voltage versus load current. It will be proportional to the output current and the resistance of the load path from the output of the MicroRAM to the load.

The ORing feature prevents current flowing from the output of the MicroRAM back through its input terminal in a redundant system configuration in the event that a converter output fails. When the converter output supplying the MicroRAM droops below the ORed output voltage potential of the redundant system, the input of the MicroRAM is isolated from it's output. Less than 50 mA will flow out of the input terminal of the MicroRAM over the full range of input voltage under this condition.

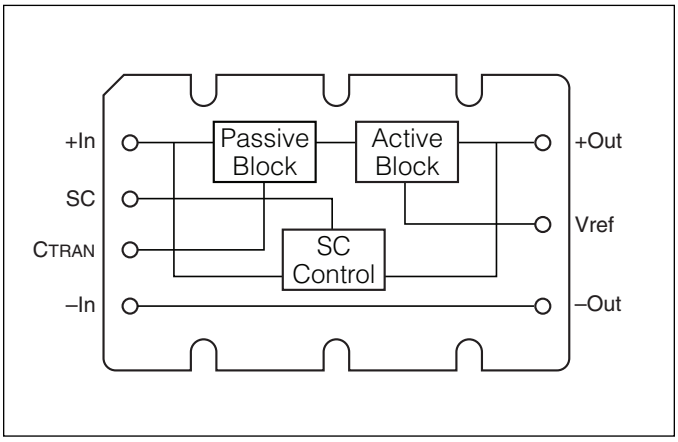

Figure 12-2 *— MicroRAM block diagram*

Load capacitance can affect the overall phase margin of the MicroRAM active loop as well as the phase margin of the converter loop. The distributed variables such as inductance of the load path, the capacitor type and value as well as its ESR and ESL also affect transient capability at the load. The following guidelines should be considered when point-of-load capacitance is used with the MicroRAM in order to maintain a minimum of 30 degrees of phase margin.

1. Using ceramic load capacitance with <1 mΩ ESR and <1 nH ESL:
   a. 20 µF to 200 µF requires 20 nH of trace / wire load path inductance
   b. 200 µF to 1,000 µF requires 60 nH of trace / wire load path inductance
2. For the case where load capacitance is connected directly to the output of the MicroRAM, i.e. no trace inductance, and the ESR is >1 mΩ:
   a. 20 µF to 200 µF load capacitance needs an ESL of >50 nH
   b. 200 µF to 1,000 µF load capacitance needs an ESL of >5 nH
3. Adding low ESR capacitance directly at the output terminals of MicroRAM is not recommended and may cause stability problems.
4. In practice, the distributed board or wire inductance at a load or on a load board will be sufficient to isolate the output of the MicroRAM from any load capacitance and minimize any appreciable effect on phase margin.

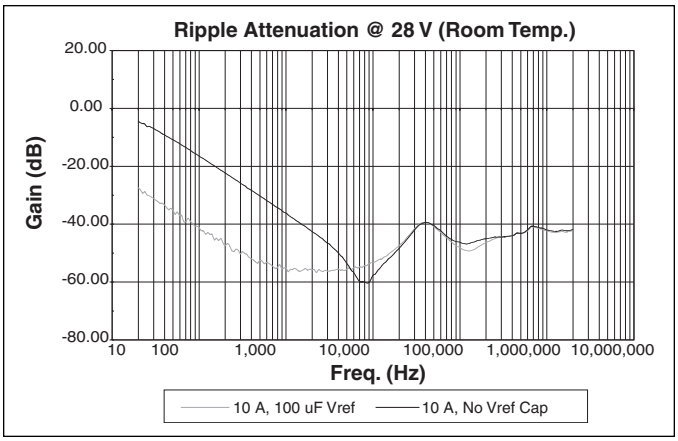

Figure 12–3a *— The small signal attenuation performance as measured on a network analyzer with a typical module at 28 V and 10 A output. The low frequency attenuation can be enhanced by connecting a 100 µF capacitor, CHR, to the VREF pin as shown in Figures 12–1 and 12–2.*

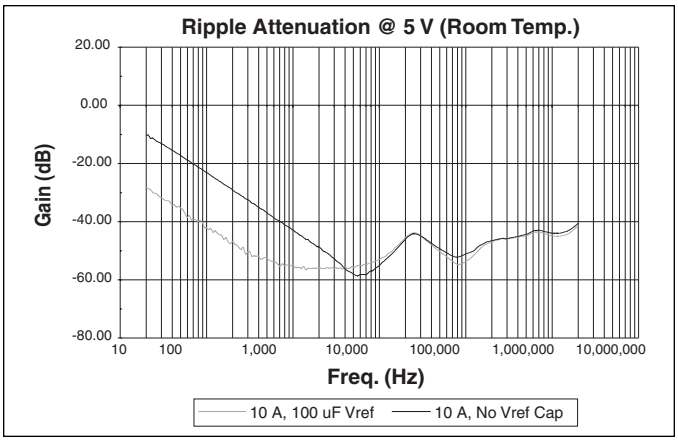

Figure 12–3b *— The small signal attenuation performance as measured on a network analyzer with a typical module at 5 V and 10 A. The low frequency attenuation can be enhanced by connecting a 100 µF capacitor, CHR, to the VREF pin as shown in Figures 12–1 and 12–2.*

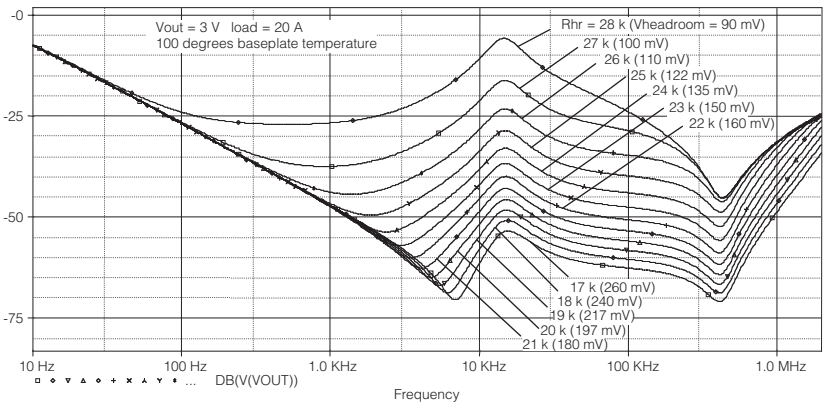

Figure 12–4a *— Graph of simulated results demonstrating the tradeoff of attenuation vs. headroom setting at 20 A and a equivalent 100°C baseplate temperature at 3 V.*

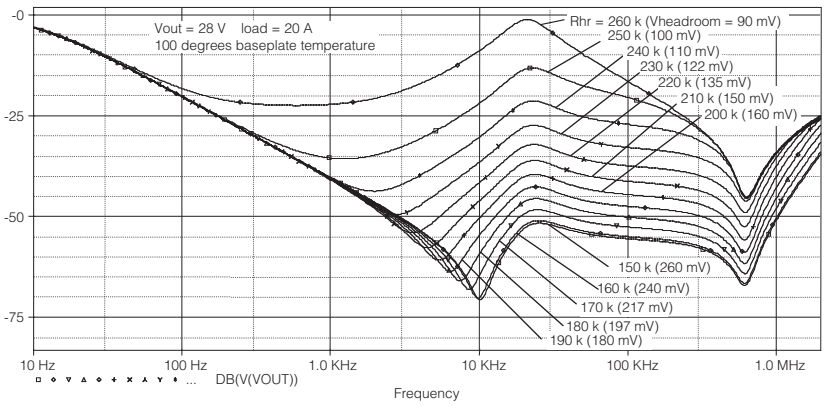

Figure 12–4b *— Graph of simulated results demonstrating the tradeoff of attenuation vs. headroom setting at 20 A and a equivalent 100°C baseplate temperature at 28 V.*

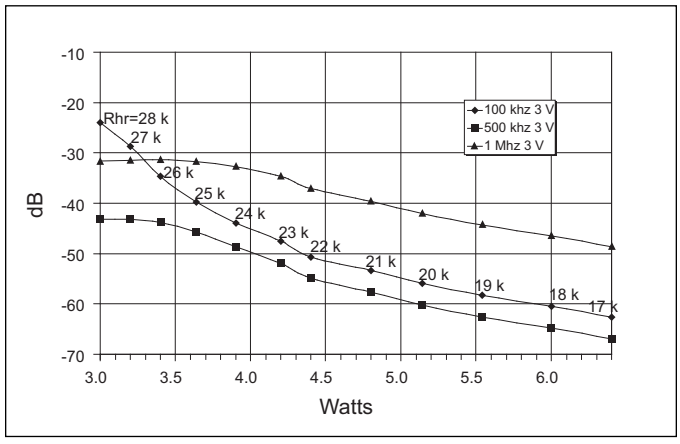

Figure 12–4c *— MicroRAM attenuation vs. power dissipation at 3 V, 20 A*

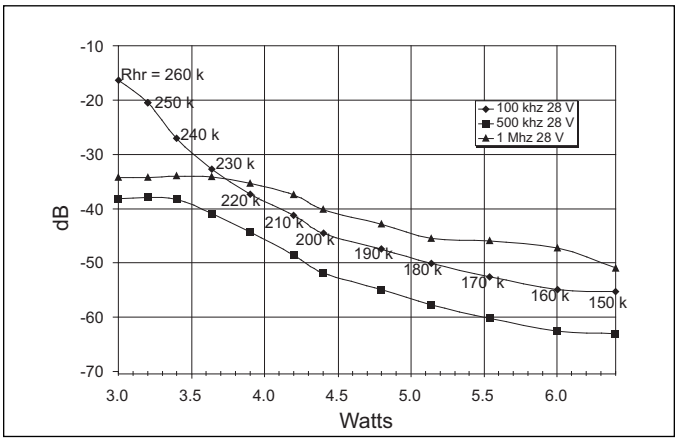

Figure 12–4d *— MicroRAM attenuation vs. power dissipation at 28 V, 20 A*

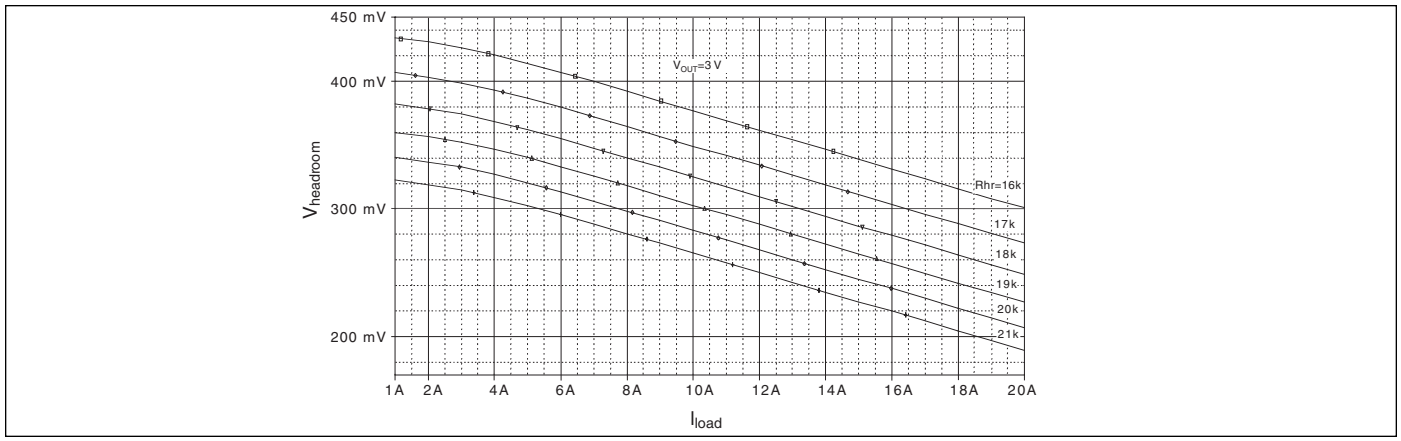

Figure 12–5 *— Headroom vs. load current at 3 V output*

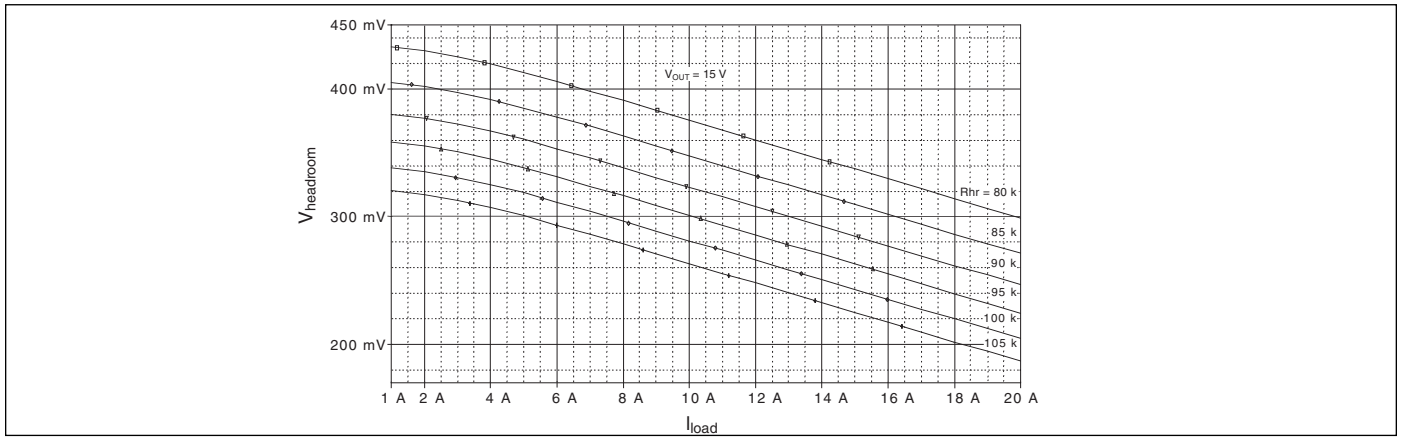

Figure 12–6 *— Headroom vs. load current at 15 V output*

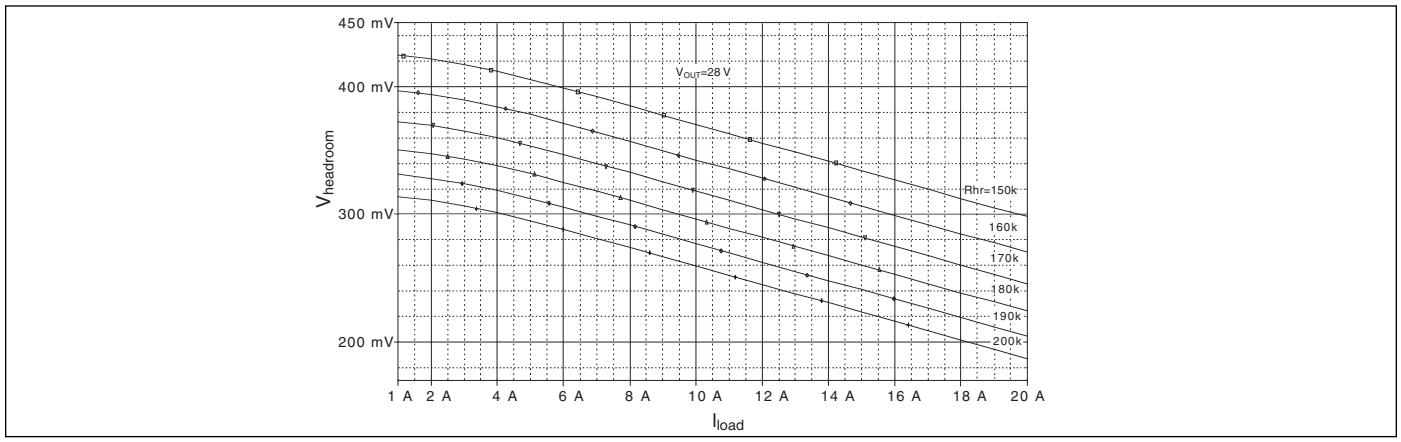

Figure 12–7 *— Headroom vs. load current at 28 V output*

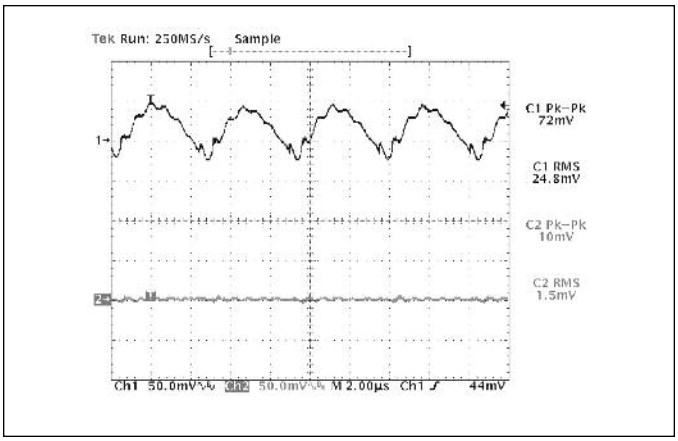

Figure 12–8 *— V375A28C600B and µRAM: Input and output ripple @ 50% (10 A) load CH1 = Vi; CH2 = Vo; Vi – Vo = 332 mV; R_{HR} = 178 k*

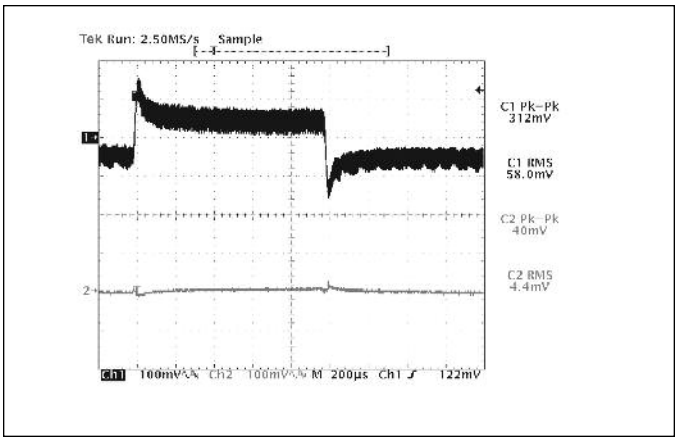

Figure 12–9 *— V375A28C600B and µRAM; Input and output dynamic response no added C_{TRAN}; 20% of 20 A rating load step of 4 A (10 A – 14 A); R_{HR} = 178 k (Configured as in Figures 14–1a and 14–1b)*

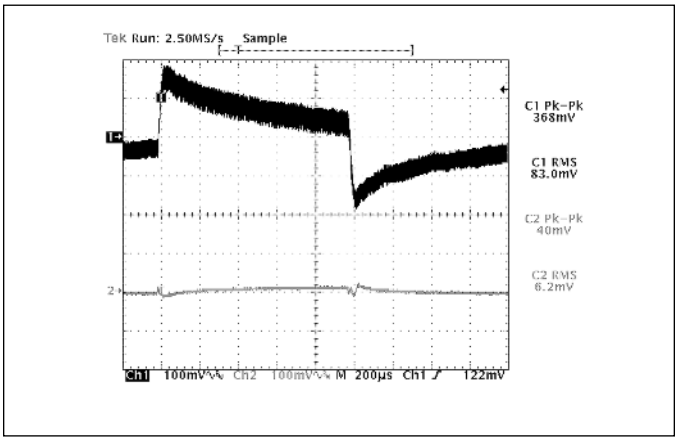

Figure 12–10 *— V375A28C600B and µRAM; Input and output dynamic response C_{TRAN} = 820 µF Electrolytic; 33% of load step of 6.5 A (10 A–16.5 A); R_{HR} = 178 k (Configured as in Figures 14–1a and 14–1b)*

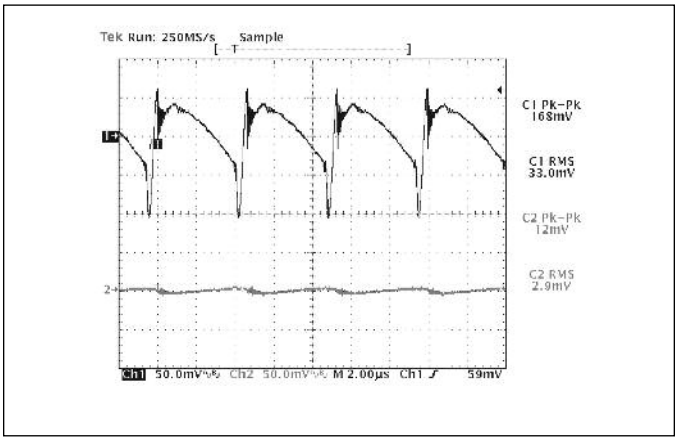

Figure 12–11 *— V375B12C250B and µRAM; Input and output ripple @50% (10 A) load CH1 = Vi; CH2 = Vo; Vi – Vo = 305 mV; R_{HR} = 80 k (Configured as in Figures 14–1a and 14–1b)*

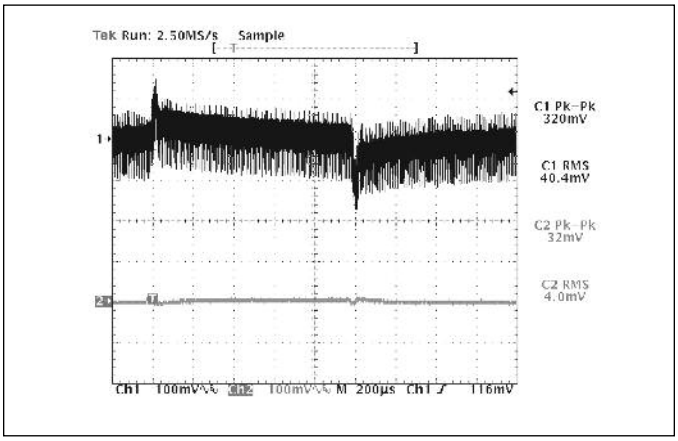

Figure 12–12 *— V300B12C250B and µRAM; Input and output dynamic response no added C_{TRAN}; 18% of 20 A rating load step of 3.5 A (10 A – 13.5 A); R_{HR} = 80 k (Configured as in Figures 14–1a and 14–1b)*

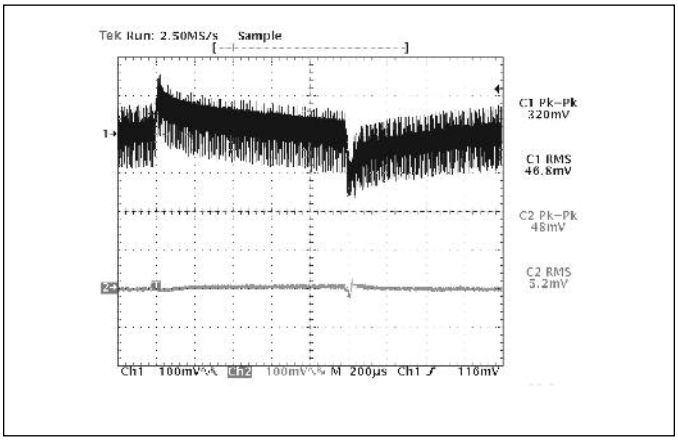

Figure 12–13 *— V300B12C250B and µRAM; Input and output dynamic response C_{TRAN} = 820 µF Electrolytic; 30% of load step of 6 A (10 A – 16 A); R_{HR} = 80 k (Configured as in Figures14–1a and 14–1b)*

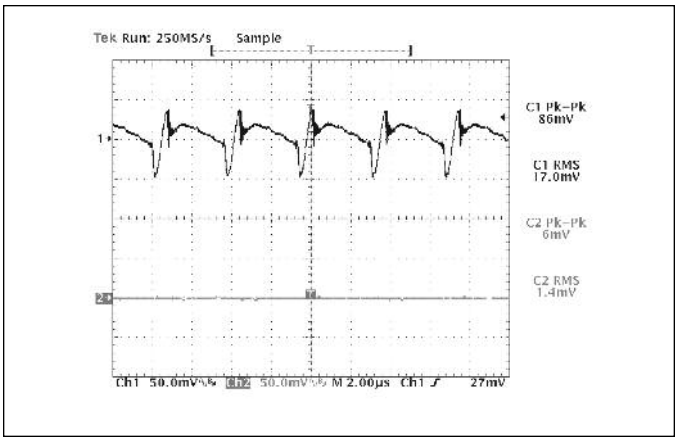

Figure 12–14 *— V48C5C100B and µRAM; Input and output ripple @ 50% (10 A) load CH1 = Vi; CH2 = Vo; Vi – Vo = 327 mV; RHR = 31 k (Configured as in Figures 12–1a and 12–1b)*

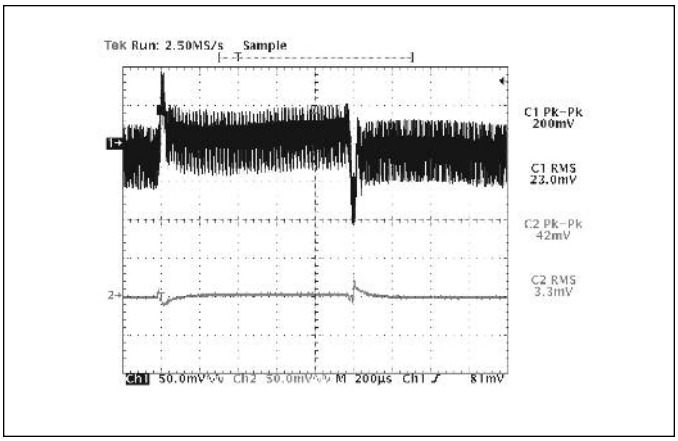

Figure 12–15 *— V48C5C100B and µRAM; Input and output dynamic response no added CTRAN; 23% of 20 A rating load step of 4.5 A (10 A – 14.5 A); RHR = 31 k (Configured as in Figures 12–1a and 12–1b)*

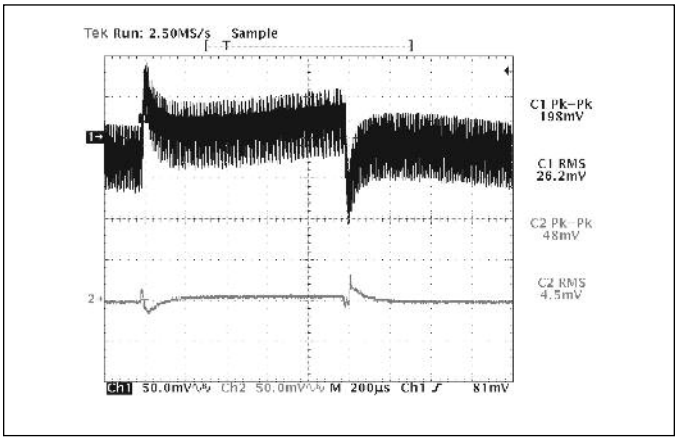

Figure 12–16 *— V48C5C100B and µRAM; Input and output dynamic response CTRAN = 820 µF Electrolytic; 35% of load step of 7 A (10 A – 17 A); RHR = 31 k (Configured as in Figures 12–1a and 12–1b)*

NOTES: The measurements in Figures 12–8 through 12–16 were taken with a µRAM2C21 and standard scope probes set at 20 MHz bandwidth scope setting.

The criteria for transient current capability was as follows: The transient load current step was incremented from 10 A to the peak value indicated, then stepped back to 10 A until the resulting output peak to peak measured ~ 40 mV.