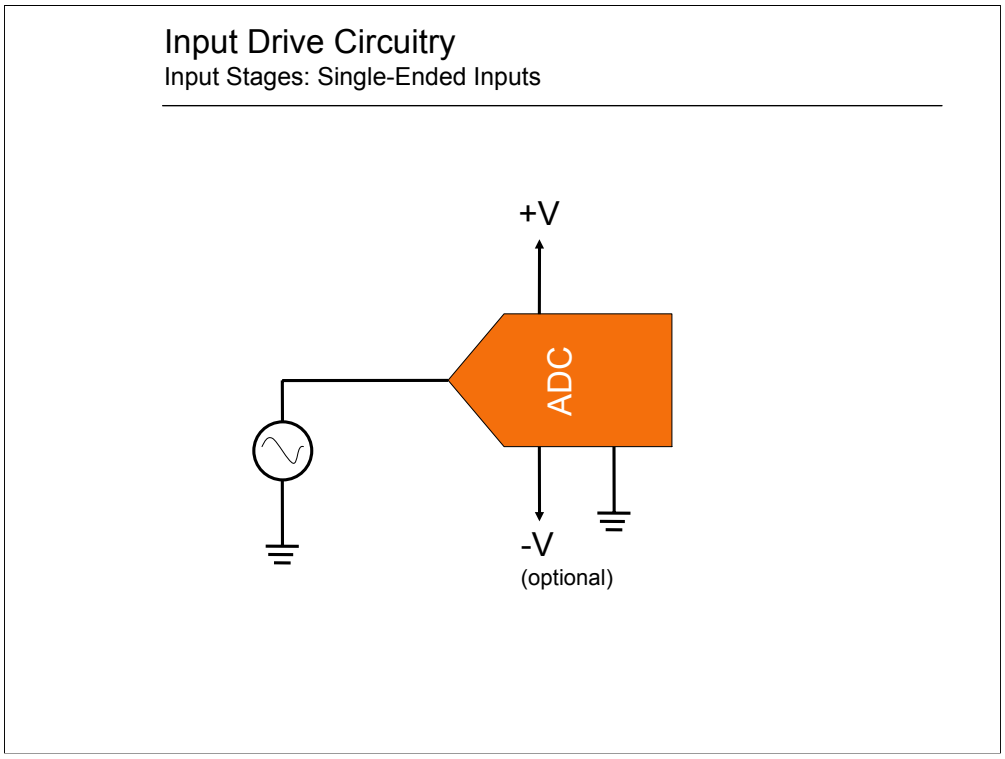
Input Drive Circuitry for SAR ADCs

Section 8

SAR ADCs in particular have input stages that have a very dynamic behavior. Designing circuitry to drive these loads is an interesting challenge. We've been looking at this for some time now, and are making progress toward a better understanding of all of the factors at play in the op amp to ADC interface.

Input Drive Circuitry
Outline

- Input Types
  - Single ended
  - Pseudo-differential
  - Differential
- Buffer Op Amp
  - Rail-to-Rail Considerations
- RC Circuit
  - Establishing starting criteria
- Modeling the ADC Input Interface

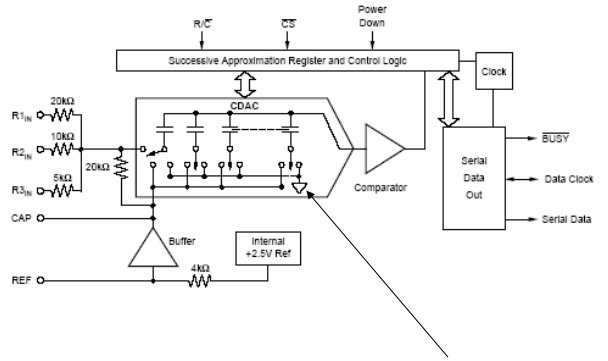


Before we look at the op amp closely, its important to know what type of ADC input you have – many options are available.

Shown above is a single-ended input. These inputs reference the input signal to ground. Depending upon the converter, the actual input voltage may be allowed to swing above and below the converter's ground reference, or may be required to stay only above ground.

Input Drive Circuitry
Input Stages: Single-Ended Inputs

- A single input pin for a particular channel.
- Input signals are referred to ground.



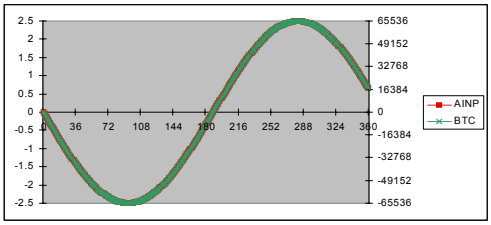
Note: input is referred to GROUND!

Single-ended inputs are easy to spot: there's only one input pin for an input signal! The other reference point is the converter's ground pin.

Input Drive Circuitry

Input Stages: Single-Ended Inputs

Single-Ended parts which handle a bipolar signal with no external circuitry:



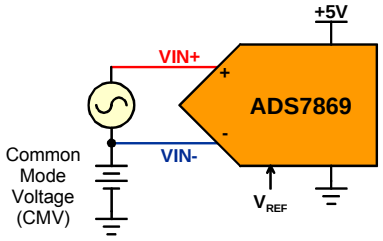
- ADS7810
- ADS7811
- ADS7812
- ADS7813
- ADS7815
- ADS7824
- ADS7825
- ADS8505
- ADS8509
- ADS574
- ADS774
- ADS7800
- ADS7804
- ADS7805
- ADS7806
- ADS7807
- ADS7808
- ADS7809

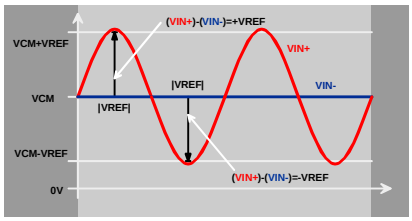
Parts which handle a signal that moves both above and below ground are said to have a *bipolar* input; the input signal may take one of two polarities, above and below ground. Texas Instruments offers a broad line of bipolar input converters.

Input Drive Circuitry

Input Stages: Pseudo-Differential

- More like a single-ended input than differential, but with some advantages.
- IN- pin can move, but in a limited range (typically -0.2V to 0.2V, sometimes up to a volt or two).
- Good for removing common-mode voltages, offsets, etc.
- Provides a “clean” signal reference point.



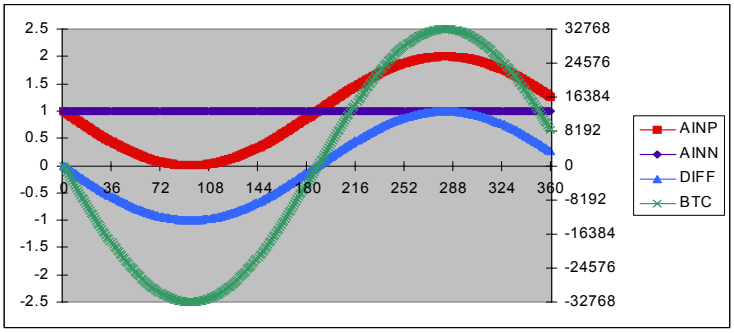


Some of our converters offer what is called a *pseudo-differential* input. In this type of input, the signal is referenced to a second input pin. This input pin can only accept a small range of voltages, perhaps a few hundred millivolts. This can be very helpful in situations where the signal has a slight common-mode offset, as this offset gets removed because the converter sees only the difference between the positive input pin and the negative input pin.

Input Drive Circuitry

Input Stages: Pseudo-Differential

- Example: 0V to 2V sine wave; 1V common mode voltage
- ADC sees the difference between the two inputs (“differential”)
- Output code may be unipolar or bipolar (bipolar shown here)
- This would be called “pseudo-bipolar” as well – ONLY because of the output coding!

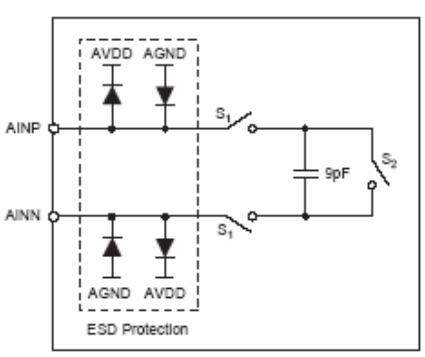


Here’s an example of a pseudo-differential input at work: a sine wave that swings from 0V to 2V is connected to the positive input, while the 1V common-mode signal is connected to the negative input. The ADC only sees the difference between the two pins, so it effectively sees a ±1V input. With an output coding that takes on positive and negative values, the unipolar 0V to 2V signal could be interpreted by the system as the ±1V sine wave - without needing bipolar power supplies!

Input Drive Circuitry
Input Stages: Differential

- Sometimes called “fully differential”.
- ADC sees AINP-AINN as input.
- Both inputs can swing from 0V to the full scale – but NOT below ground! (in most cases).
- Typically move in a “balanced” fashion.

Example: ADS1271

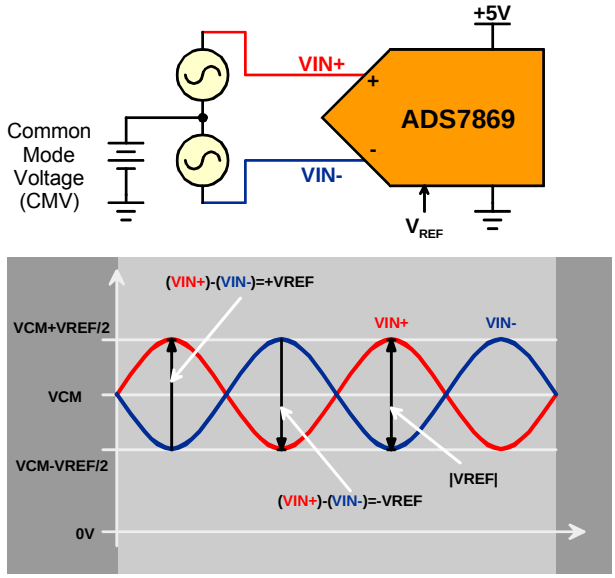


While the previous input circuit was a differential input, since it took the difference signal between the two input pins, it was considered “pseudo-differential” because one input was limited in range. In a truly differential input stage, both input pins can swing the full range, and typically move in a balanced fashion – as one input goes up, the other goes down in a corresponding way.

These types of inputs are commonly found on single-supply converters, such as delta-sigma or pipeline converters. The differential input offers the advantages of common-mode rejection, as well as limiting the input voltage swing required on each pin while preserving a high dynamic range.

Input Drive Circuitry

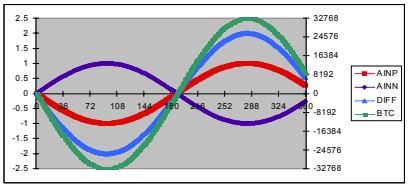
Input Stages: Differential



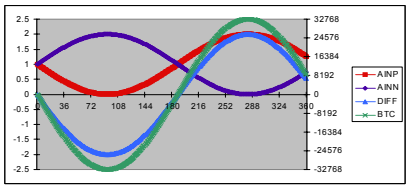
This slide illustrates the balanced fashion that differential inputs are typically used with.

Input Drive Circuitry
Input Stages: Differential

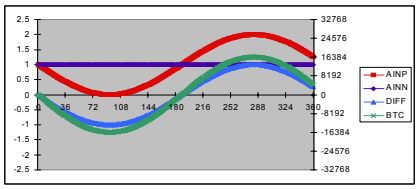
- Balanced Input, 0V offset:



- Balanced Input, 1V offset:

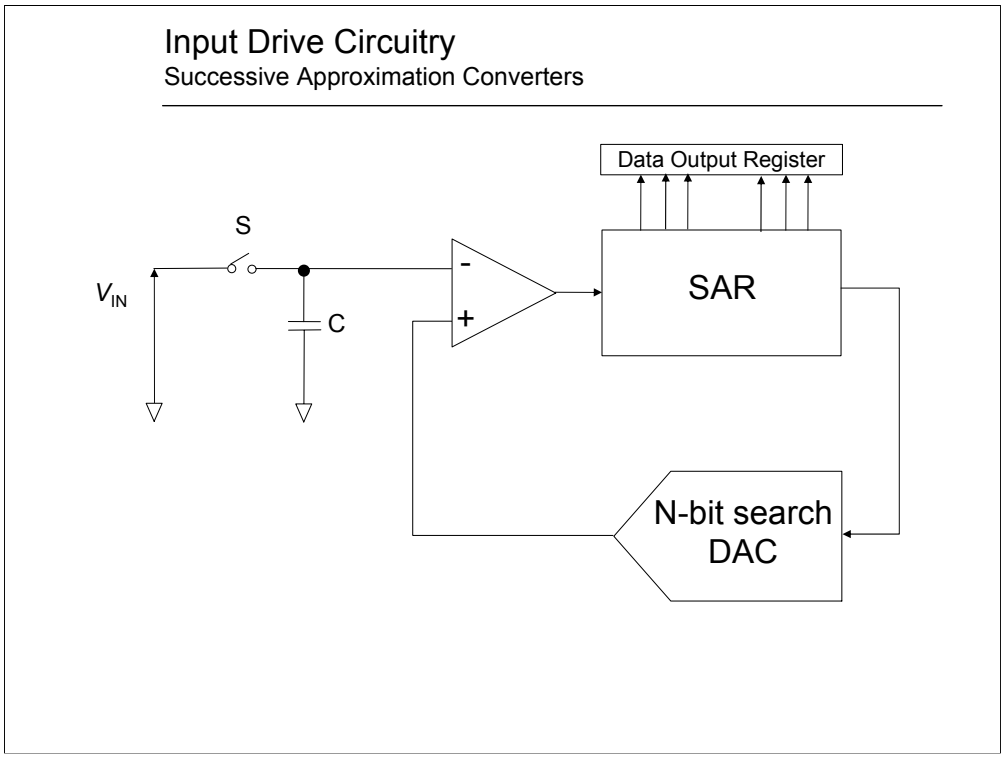


- Unbalanced Input, 1V offset: (note reduced range)



This slide shows the power of the differential input: with or without an input common-mode voltage, the converter sees the difference of the two pins. Each pin needs to swing only 1V, yet the converter sees a 2V swing in each direction.

However, it is important to recognize that using such a converter in a single-ended mode, by grounding or fixing one input at a fixed voltage, (not using it in a balanced fashion) results in a loss of dynamic range.



The most popular and versatile converter is the Successive Approximation Register (SAR) type. These converters work by comparing the analog signal voltage to known fractions of the full scale voltage and setting or clearing bits in a data register as a consequence.

Modern SARs use a C-DAC to successively compare bit combinations, set or clear the corresponding bits in a data register, and they also tend to have an integrated sample/hold function.

A typical SAR conversion cycle has two phases; a sampling phase and a conversion phase.

During the sampling phase, the analog input signal is allowed to charge the ADC's Sample-and-Hold (S/H) capacitor to a level proportional to the analog input.

Conversion begins immediately following the sampling phase. Conversion successively compares the unknown value of the charge stored in the S/H capacitor to known fractions of charge. After each comparison, logic on the ADC determines if the unknown charge is greater or smaller than the known fractional charge. The process will be like this

x >1/2 FS ? - Y - set the corresponding bit

x >3/4 FS ? - N - clear the corresponding bit

x >5/8 FS ? - Y - set the corresponding bit

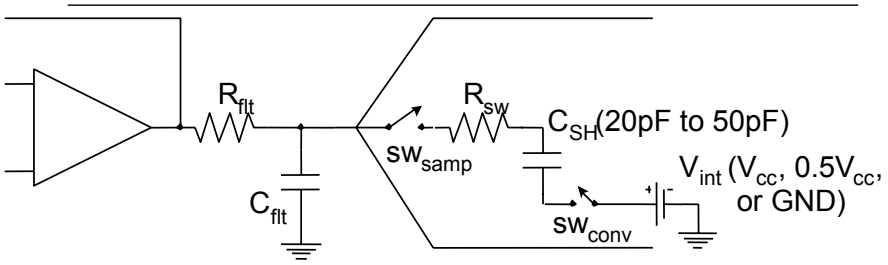
etc

At the end of the process the data register will contain a binary value proportional to the value initially placed on the S/H capacitor. The user reads this value out as converted data.

As shown in the diagram above, these converters rarely provide any type of built-in input buffer amplifier. So choosing an amplifier to match up to these converters is what we will examine next.

Input Drive Circuitry

The Interface Circuit



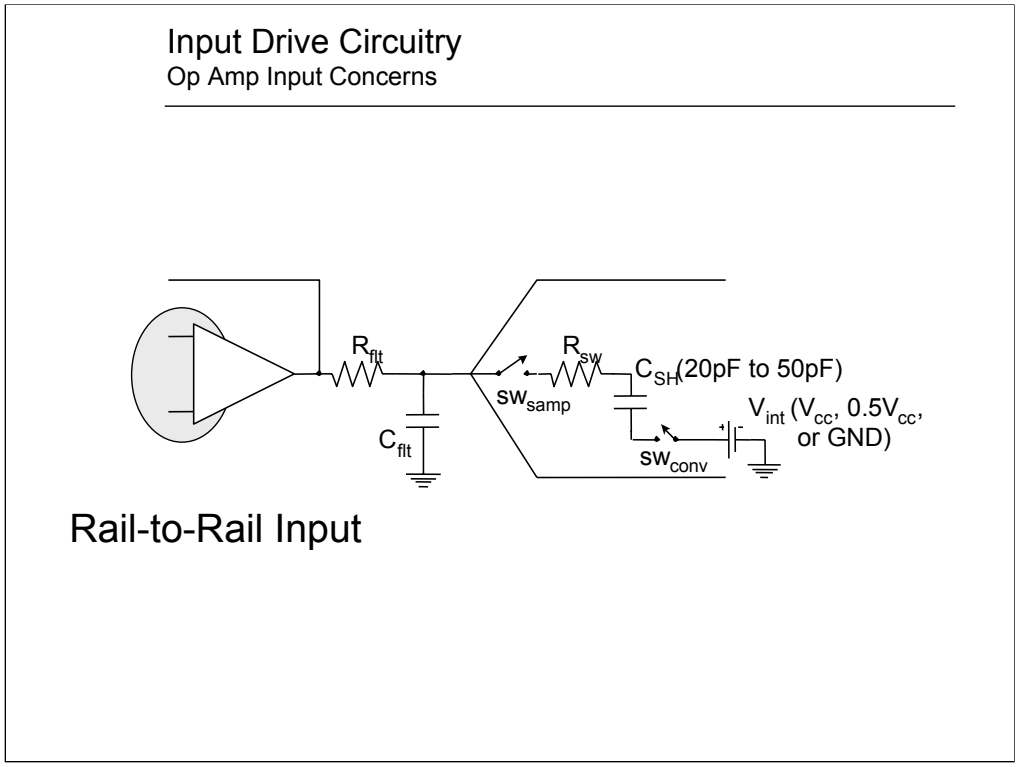
Op Amp	**Filter**	**A/D**
CMV Range, V_{OS} vs CMV	Charge Bucket	Acquisition Time
RR Out-Swing to the rail	Filtering,	Input Circuit Parameters
Slew Rate, Signal BW,	C_{load} Isolation,	Initial Voltage on C_{SH}
Load Transient, Settling Time,		
Output Impedance,		

A closer look at the SAR ADC input and drive circuit is shown here. Many considerations come into play in choosing the optimum external R and C values, and choosing the best op amp to drive this circuit. We'll examine these in more detail in the following slides.

Input Drive Circuitry
Interface Design Check List

- Op Amp Common Mode Voltage
- Op Amp Output Swing to Rail
- Op Amp Settling Time
- Filter Capacitor Type
- Filter Component Values
- Op Amp Specifications

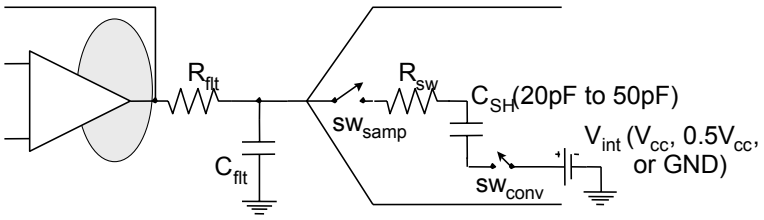
Some of the main factors we need to concentrate on are listed here.



At the op amp input, one of the first considerations, especially with single-supply op amps, is how close to the power supply rail the input signals can swing. Note that many “rail-to-rail” input op amps really mean that the input can swing only within a few hundred millivolts of the rail.

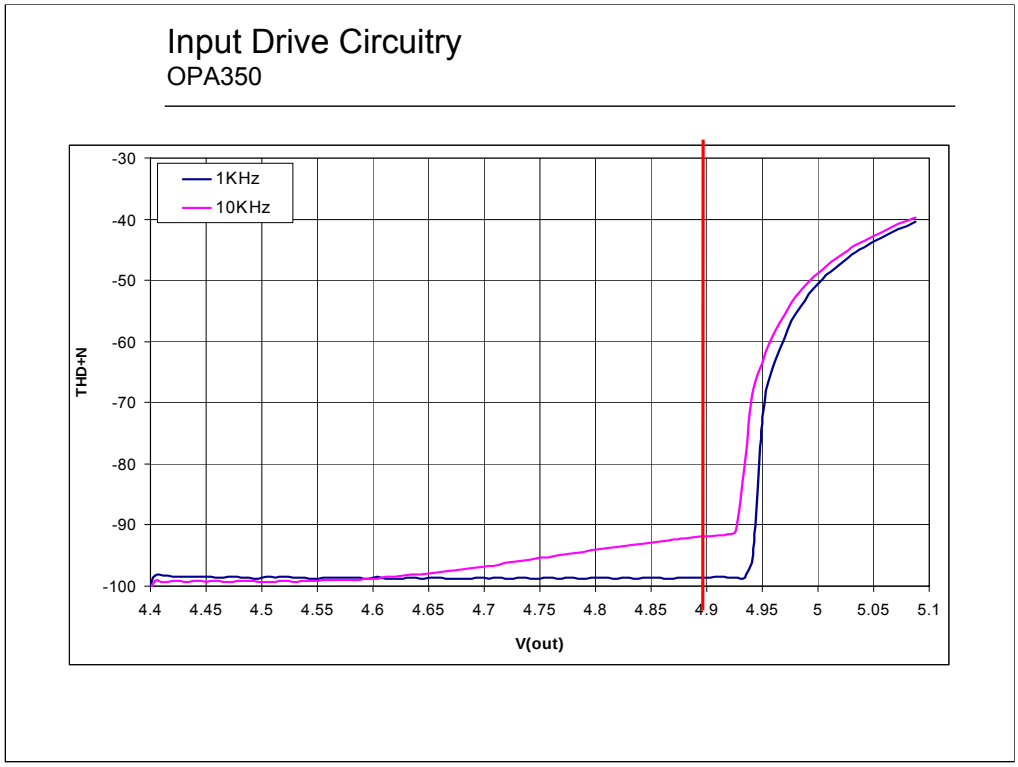
Beware too of rail-to-rail op amps which use two different input stages to handle the rail-to-rail swing. See the Analog e-Lab (September 2004:” Avoiding the Pitfalls with Single Supply Op Amps”, http://www.eetimes.com/netseminar.html) to see how using these devices in a noninverting configuration can lead to significant distortion and errors. If faced with using one of these op amps, consider using them only in an inverting amplifier configuration.

Input Drive Circuitry
Output Stage Concerns

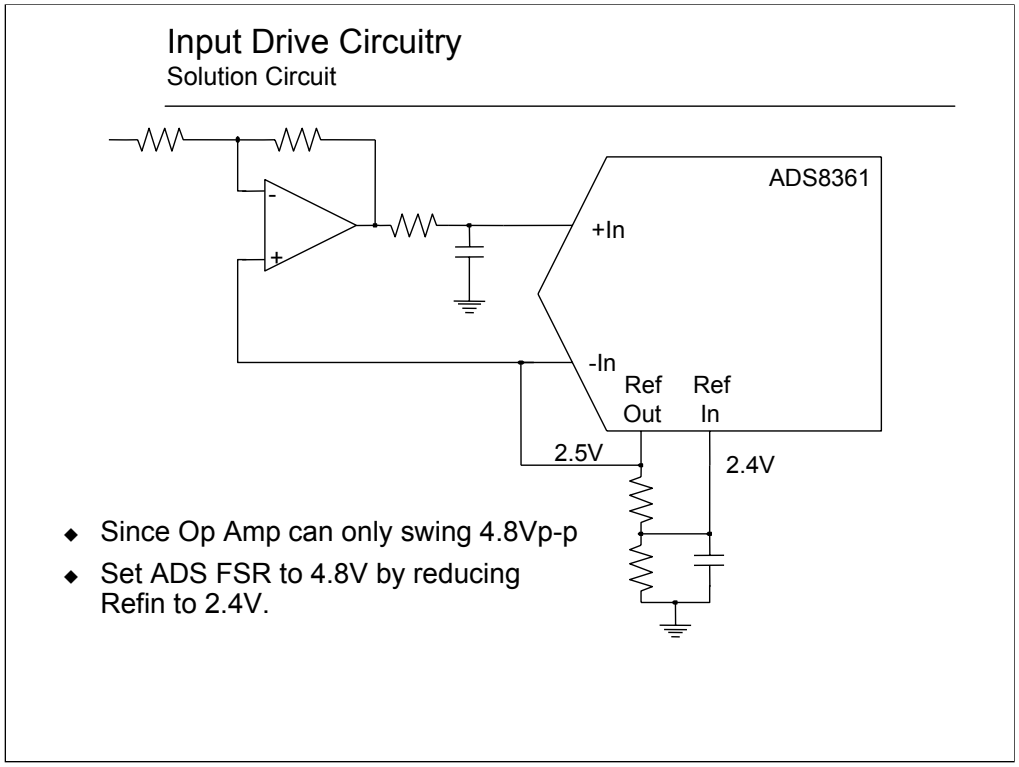


Rail-to-Rail Output

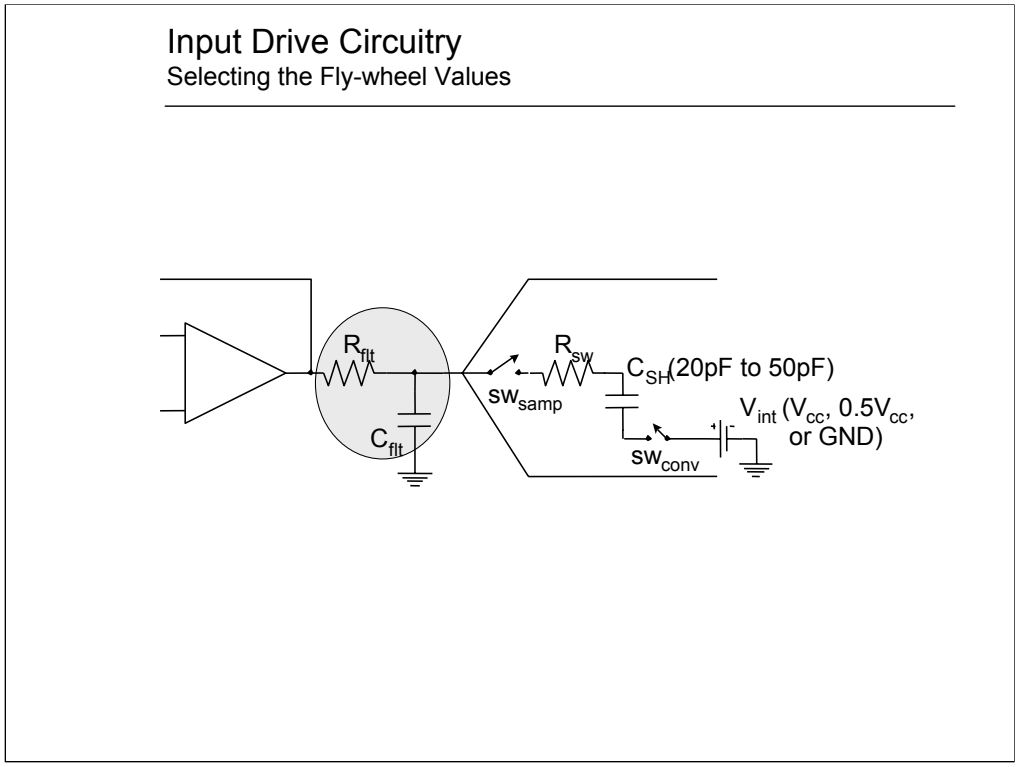
Similarly, the output stage of a “rail-to-rail” amplifier may not actually swing all the way to the supply rail. This can impact the dynamic range that can be used by the SAR ADC, many of which feature a true rail-to-rail input.



The plot above shows distortion versus output voltage swing of an OPA350, a popular rail-to-rail op amp. With a +5V power supply, you can see that noticeable distortion begins to appear when you get within 400mV of the rail. This is in spite of the fact that the OPA350 is rated to swing within 100mV of the rail (red line on this graph)! While the output can indeed swing that close to the rail, the signal fidelity there may not be optimal.

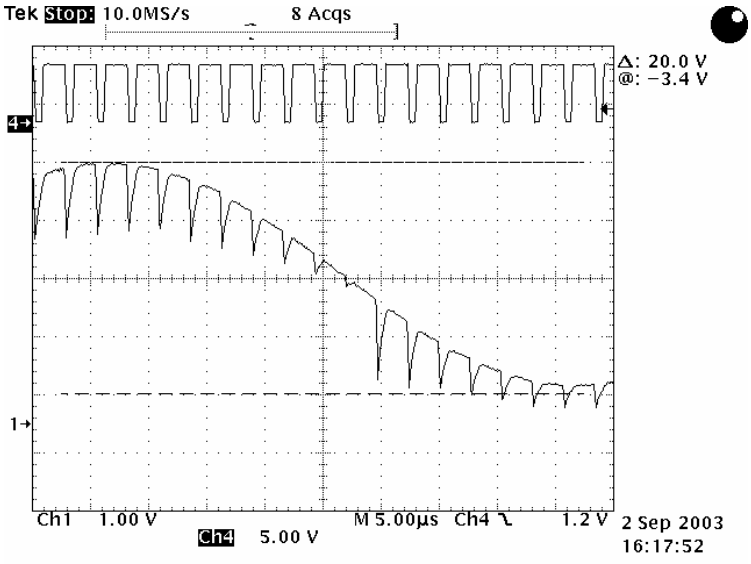


Here's a solution for dealing with the limitations of rail-to-rail op amps. To prevent the input stage from distorting the signal, the buffer amplifier is configured to be inverting, and the noninverting input is fixed at mid-rail (2.5V). However, because of the limitations in the output stage, the output of this op amp shouldn't swing more than ±2.4V around this 2.5V - a 4.8Vp-p swing. If we used the 2.5V reference as the reference for the ADC, then we would be giving up 200mV of dynamic range! By setting the ADC reference to 2.4V, the ADC then has a full-scale range of 4.8V, exactly matching what our op amp is capable of - and preserving dynamic range.



Now that we've handled some of the issues we're concerned with about the driving op amp, we need to examine the RC circuit we use in front of the SAR ADC – what's come to be called the "flywheel" circuit. It is so named because one of the functions of this circuit is for it to act as a charge-storage reservoir-storing energy, like a flywheel in a mechanical system, to charge the internal sampling capacitor of the SAR input stage.

Input Drive Circuitry
Charge Transients



The input sampling capacitor of a SAR ADC is connected to the input signal during the sampling or acquisition phase. The input signal is captured on this capacitor, then the sampling switch opens, disconnecting the input from the rest of the ADC. The conversion process then takes place, acting on this stored voltage, usually by redistributing charge from the capacitor to other capacitors in the internal DAC made up of capacitors.

When the ADC is ready to take another sample, the sampling switch closes again, reconnecting the input to the sampling capacitor. Any residual charge on this capacitor will have only one place to go – back out the input pin of the ADC!

The scope photo above shows these charge injection transients. This was generated by placing a 10KΩ resistor between the buffer op amp and the SAR ADC input, so we could clearly see the spikes. In general, the input impedance presented to a SAR converter should never be that high. Even with lower impedances, you may see spikes at the input of your SAR ADC. The spikes themselves are not bad for the converter, but if they do not settle back to the correct input value within the acquisition time of the converter, then this may result in a measurement error. These spikes also present a very demanding load to the driving op amp.

This is the second function of the RC filter we place in front of the SAR – to provide a path for this charge injection to go, and to do some minimal isolation of the op amp output to these transients.

Input Drive Circuitry
Fly Wheel Component Selection

- Pick C_{flt} =20*C_{SH}
- R_{flt} Calculation
  - $t_{flt\_settle} = t_{ACQ} = 12\ \tau_{FLT}$
  - Theoretical Minimum
  - Practical results
    - Use t =18τ_{FLT} Margin for:
      - Op Amp Output Load Transient
      - Op Amp Output Small Signal Settling Time
  - $R_{flt} = t_{ACQ}/18\ C_{flt}$

In our 2004 seminar, we showed a detailed analysis of how to arrive at good starting values for the external RC components. A summary of the results is shown here.

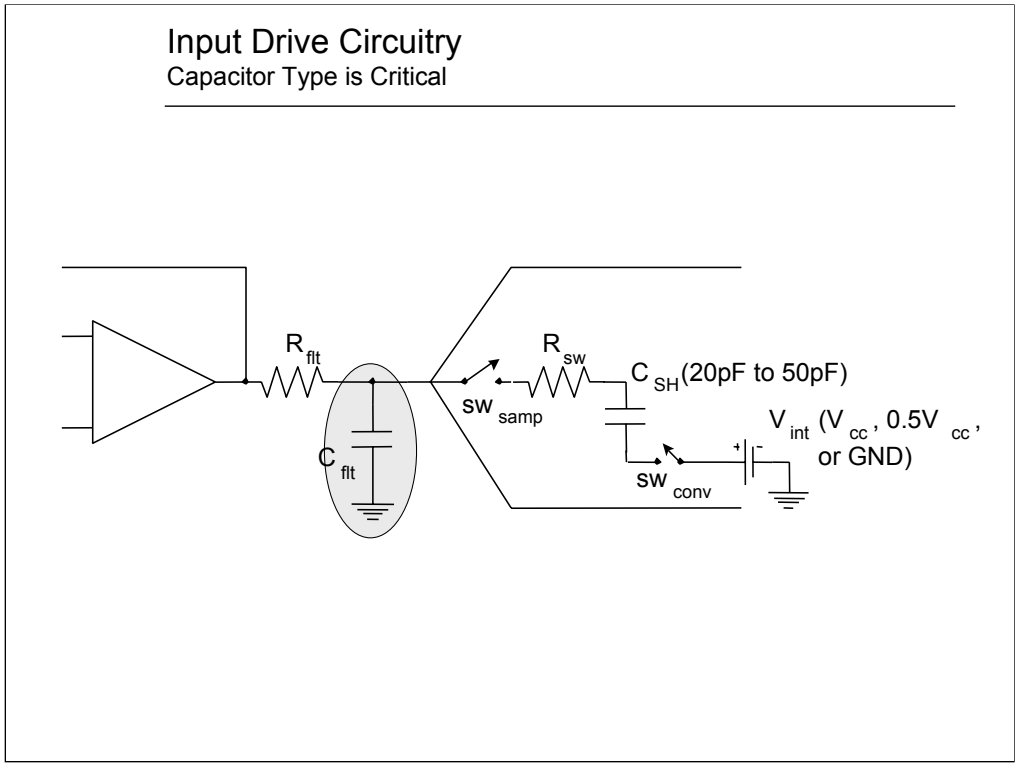
To minimize the effects of nonlinearities in the internal sampling capacitor, as well as minimize the charge injection's effect on the input voltage, we choose the external capacitor value to be at minimum twenty times the size of the internal sampling capacitor.

Once the C value is chosen, the R value can be found by noting that this RC filter must fully settle to the desired accuracy within the acquisition time of the converter. For example, to achieve 16-bit settling accuracy, 12 time constants of that RC must be allowed. That is a theoretical minimum; practical experience tells us that you need even more time, so we add a 50% margin. Thus, for our example 16-bit case, 18 time constants must be able to go by within the acquisition time of our converter.

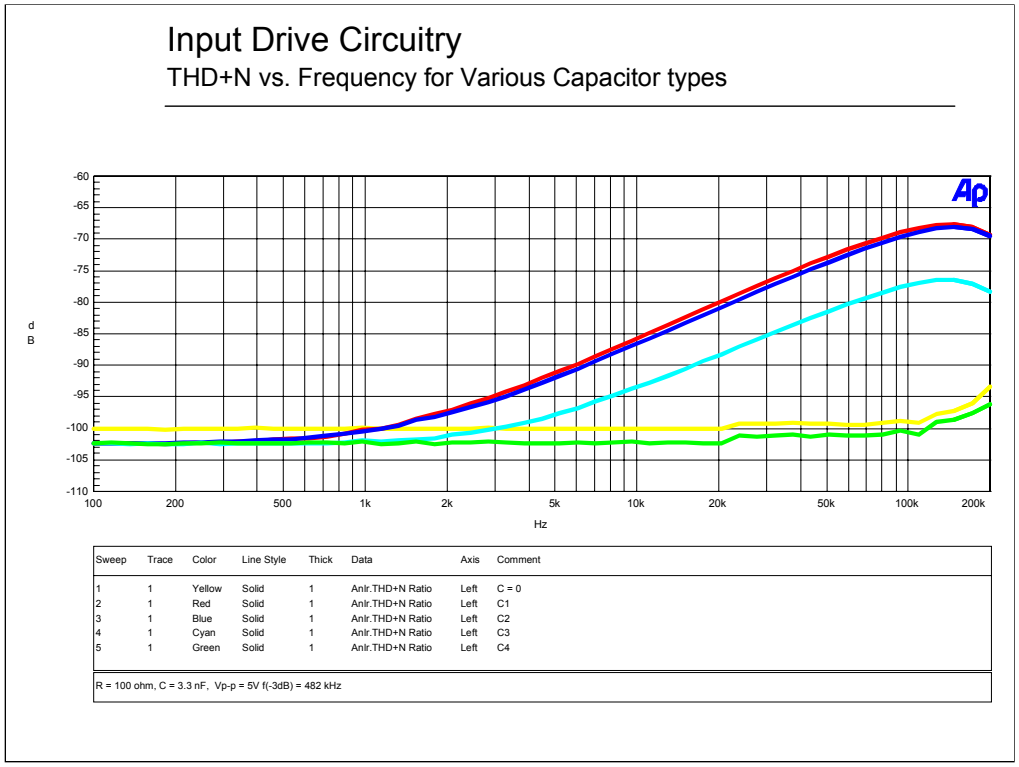
Input Drive Circuitry
Required Settling Time

Number of bits	0.5LSB	Time Constants
10	0.0488281%	8
12	0.0122070%	9
14	0.0030518%	11
16	0.0007629%	12
18	0.0001907%	13
20	0.0000477%	15
22	0.0000119%	17
24	0.0000030%	18

This chart details the number of time constants that must be allowed to achieve a certain accuracy in settling for different resolutions.

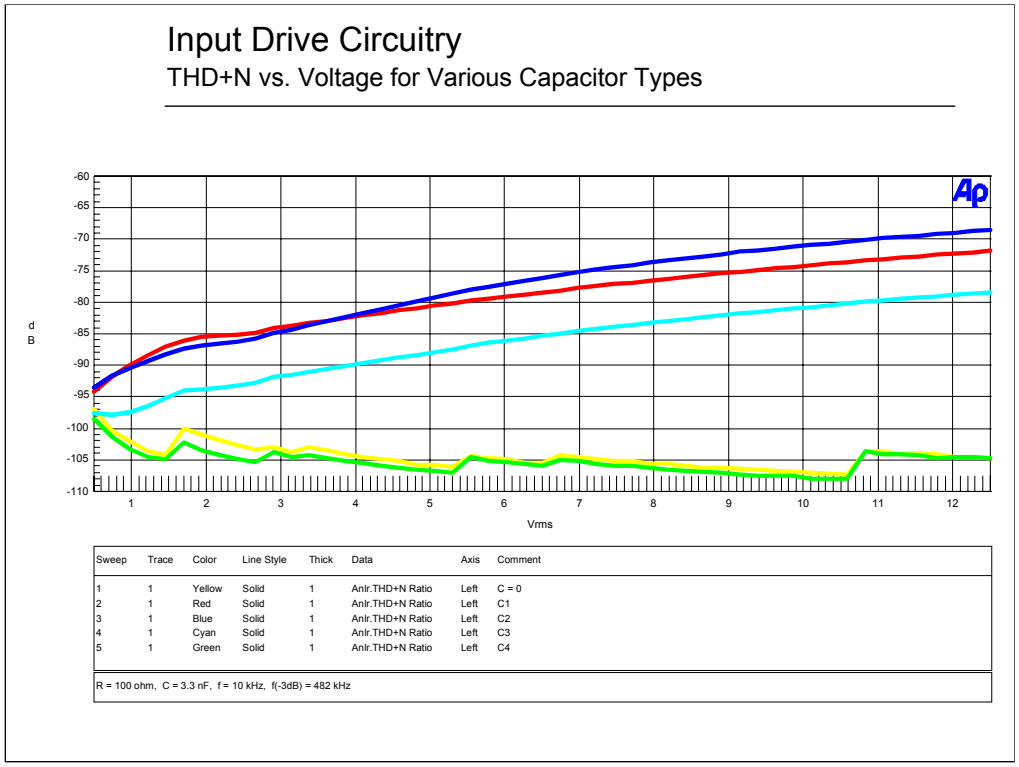


Now that we've determined some starting values for the R and the C, let's consider what type of capacitor dielectric should be used for the external capacitor.



Capacitors have a voltage coefficient, which means that the capacitance changes with applied voltage. This also tends to be nonlinear, and thus introduces distortion which changes with frequency. Here is a look at several capacitor types and their distortion versus frequency characteristics. The lowest line on this chart is the system measurement limit - and the line right next to that is a silver-mica capacitor. The other lines on this chart are from ceramic caps with different dielectrics — Z5U, Y5V, and X7R. Note that these types introduce significant distortion into the signal.

One ceramic dielectric, the C0G type, closely matches the silver mica performance (but is not shown on this chart).

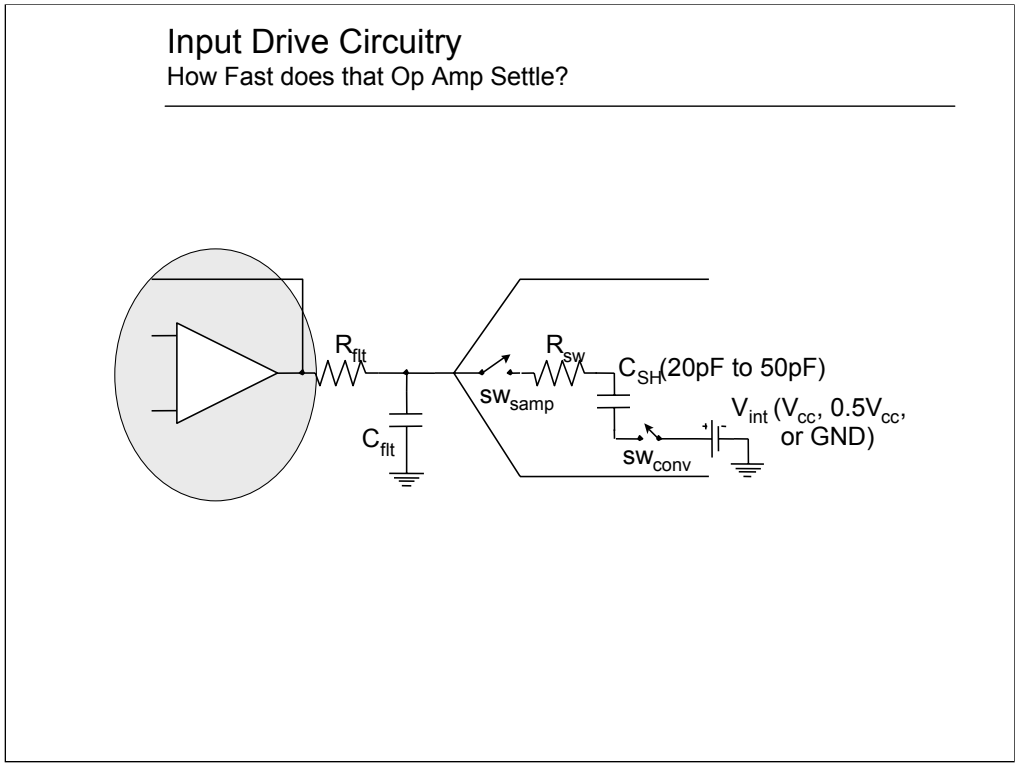


This chart is similar to the previous one, except now we are looking at distortion versus voltage applied at a fixed frequency. Again, the sliver mica capacitor approaches the measurement limit of the test system.

Input Drive Circuitry
Conclusions on “C” Type

- Best performance:
  - Silver Mica or C0G(NPO)
- Avoid all others
- Others may cost less and be smaller but can distort signal

From the previous data, we conclude that only silver mica or C0G ceramic capacitor types should be considered for use as the external capacitor. The other types may be less in cost but will hurt the overall system performance.



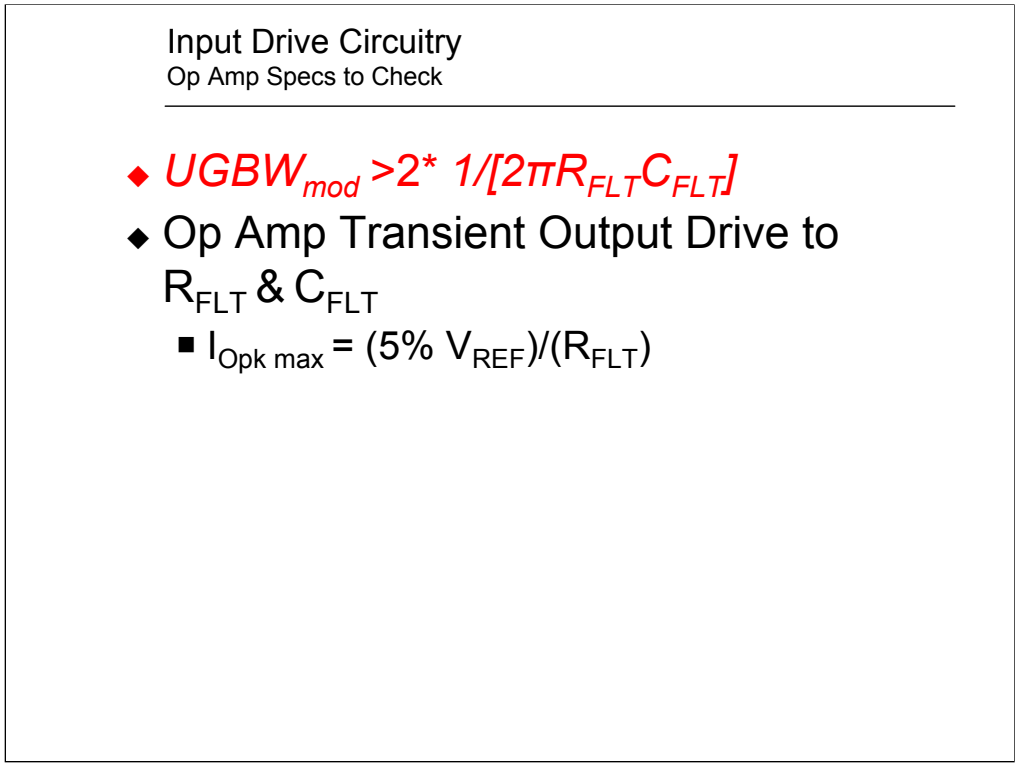
We now return to the op amp, and consider some further issues with it, now that we've chosen the RC values. Of prime importance, obviously, is how quickly can the op amp settle? This is key as it must settle within the acquisition time of the converter.

Input Drive Circuitry
What Settling Time?

- Think of a linear voltage regulator, there are **TWO** Settling Times.
  - Line Transient
  - Load Transient
- **Same** applies here.
- Data sheets report settling time to 0.01% at best.

As we consider the op amp settling behavior, we must understand that an op amp has a settling time which is specified only for a change in the input signal, and how long the output takes to settle to within 0.01% - 12 bits. Higher resolution systems will need to allow more time.

But this specified settling time is only for one behavior – we don't know anything about what happens to the op amp output as the load changes. Unlike a voltage regulator, where the response to both a line transient (input) and a load transient (output) is specified, we know only one of these for the op amp. Yet we have a circuit which we know clearly provides significant load transients to the op amp!



The Unity-Gain bandwidth (UGBW) of the op amp should be at least twice the bandwidth of the external RC filter. The op amp must have sufficient output drive current to charge the capacitor used.

Input Drive Circuitry
Modeling the SAR ADC Input Stage

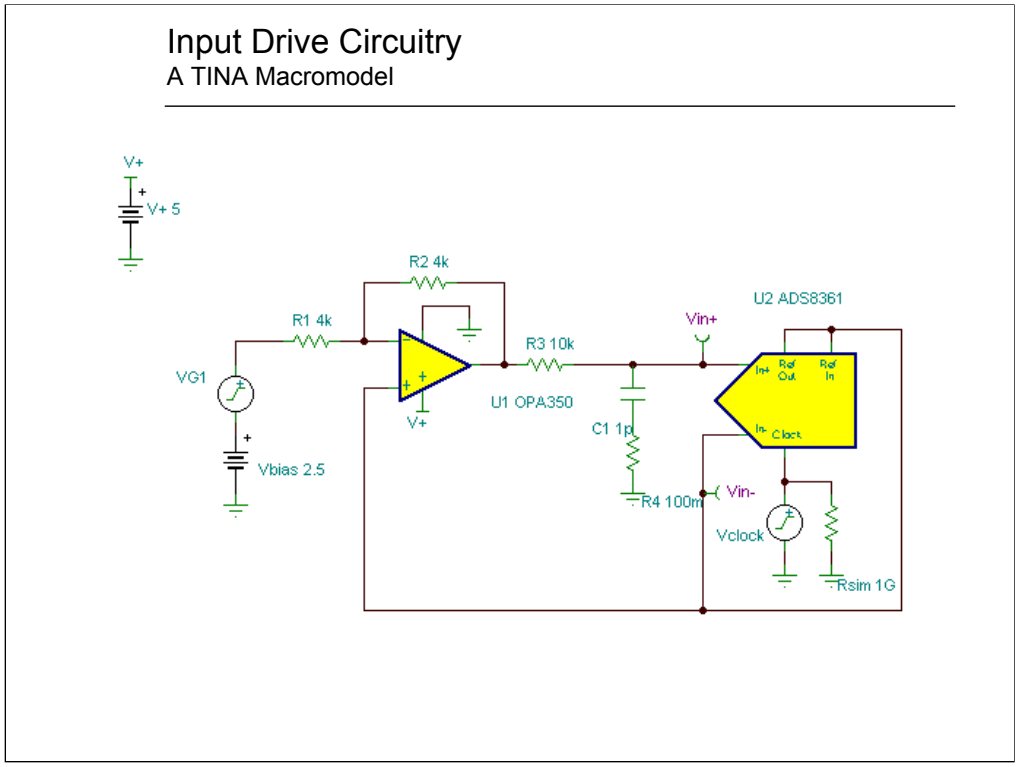
- Several steps to a complete model
- First step: model the input transient
  - Used data taken from ADS8361
- Next step: refine first step, then more:
  - Reference Input Load
  - Predict SNR/distortion?

One thing that would be very nice to be able to do is to model this SAR drive circuitry in SPICE. This would allow for quick evaluations of different op amps and RC values to help choose the optimal values.

Of course, SPICE is only as good as the models you give it. Constructing such a model can be laborious - but we've made an attempt at modeling a SAR ADC input stage and created a macromodel we can use in TI-TINA.

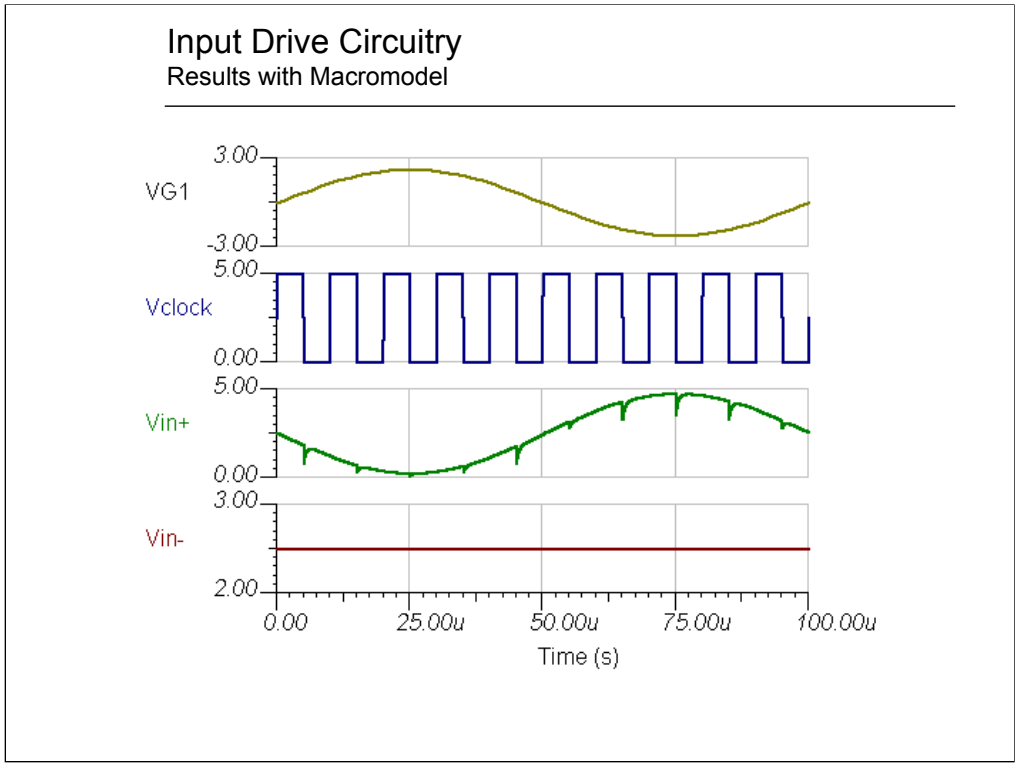
The macromodel we've created uses data taken from our evaluations of the ADS8361, which has been extensively tested over the past few years as we've done this study. The model we have today is a preliminary look – we need to set up many different scenarios in TI-TINA, then verify them on the bench and compare the results to give us confidence that the model we have accurately reflects the behavior of the device. Refinements to the model can then be made to have it more closely reflect actual device performance.

Following this, we'd like to be able to also model the reference input load as this can be even more demanding than the input load on a SAR ADC. From these, it would be interesting to see if one could predict SNR or distortion using these models. These are all on our list of things to investigate.



This is a look at a TINA circuit which uses this preliminary input stage model for the ADS8361. You'll notice that it is set up very much like the input stage design we showed earlier.

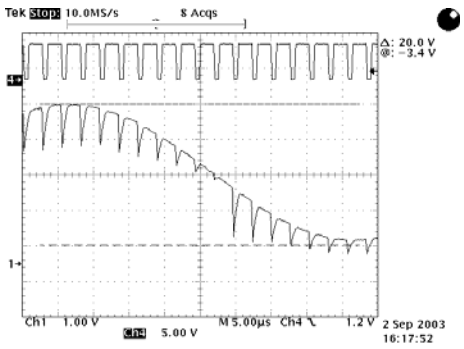
In this circuit, we've set the R to 10KΩ to mimic our first look at the charge transients, and set the C only to 1pF, in an attempt to model the scope probe capacitance used to take that data.



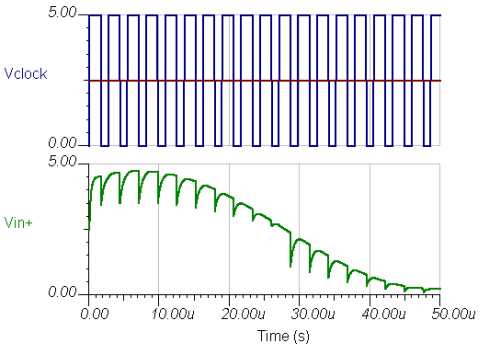
The results of a TINA simulation using this circuit clearly shows the load transients.

Input Drive Circuitry
Compare with Reality

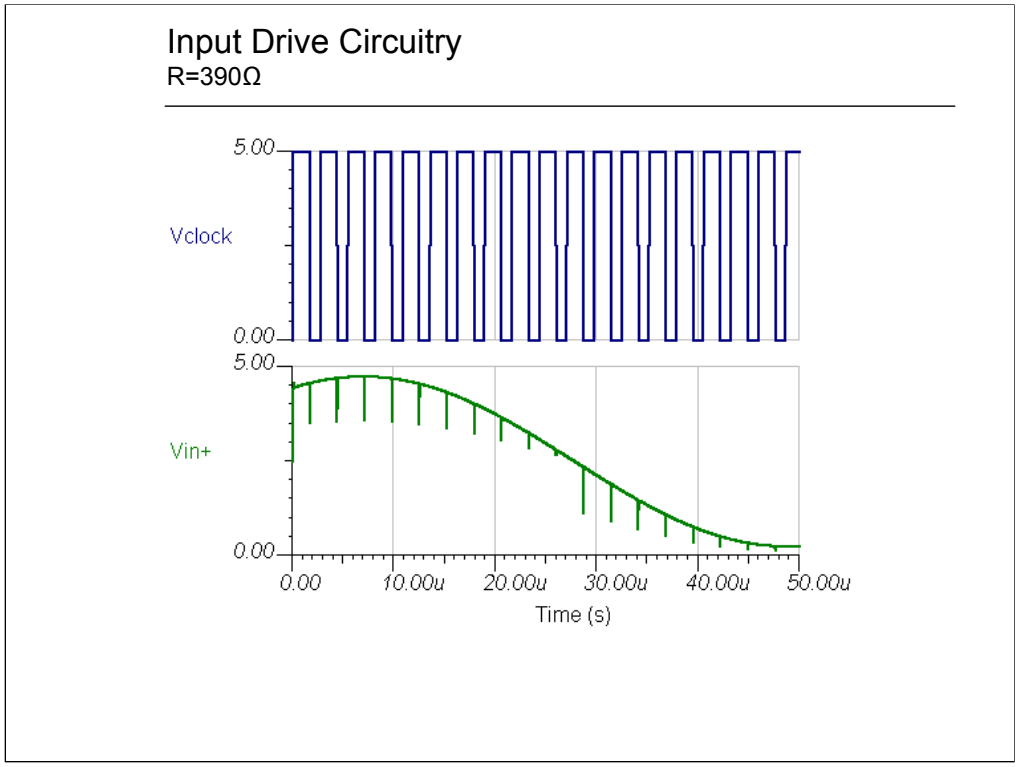
Actual ADS8361 Circuit



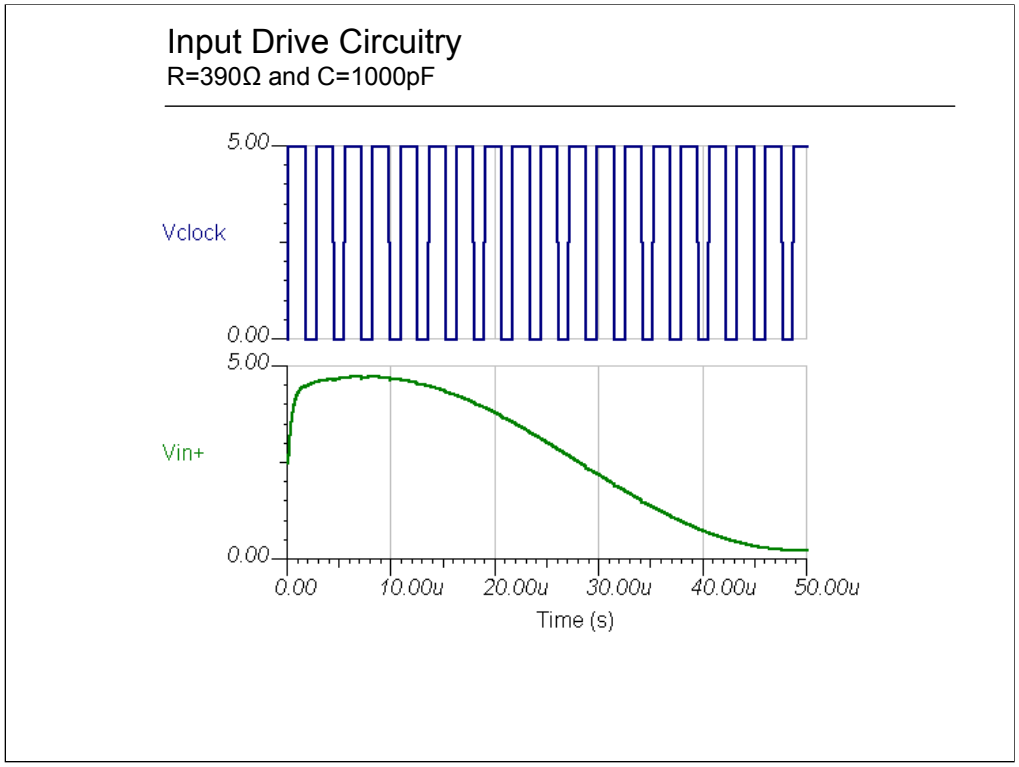
TINA Macromodel



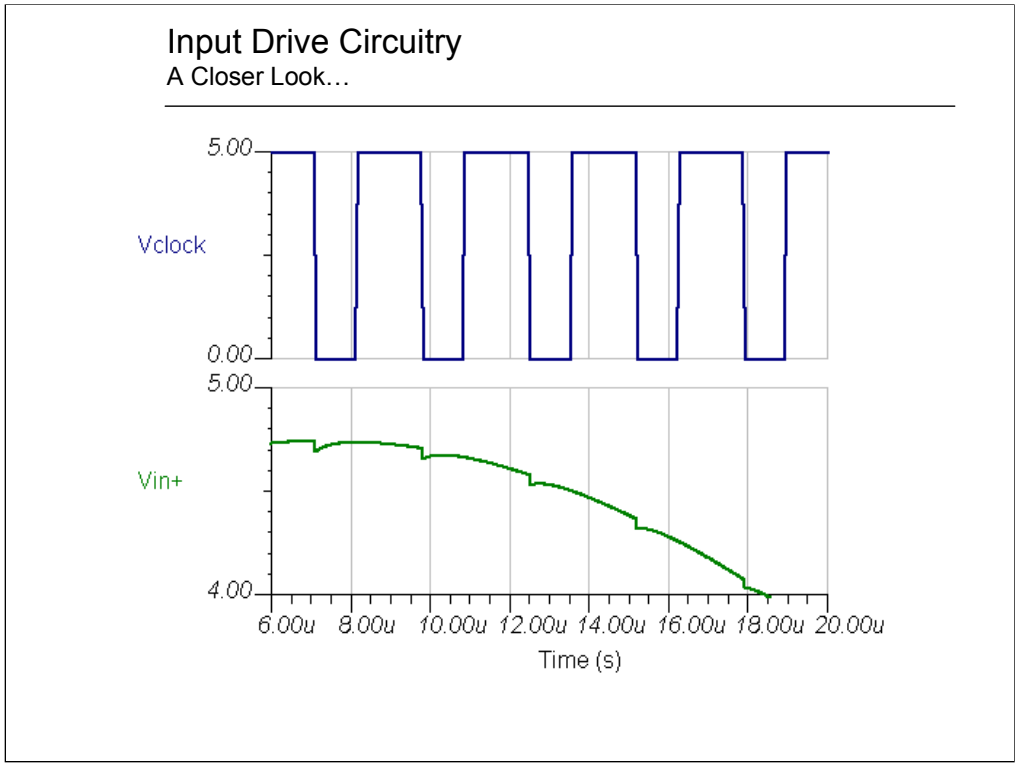
Comparing the actual circuit data with the simulation results from our TI-TINA model shows good agreement between what the model predicts and what we actually see in the lab.



One question you might ask is, what happens if you don't have the "flywheel" capacitor, but bring the resistor down to a reasonable level? Here's a simulation using only 390Ω as the resistor, rather than 10KΩ. Notice that the spikes are still quite large, but it appears that the width of the spike has diminished.

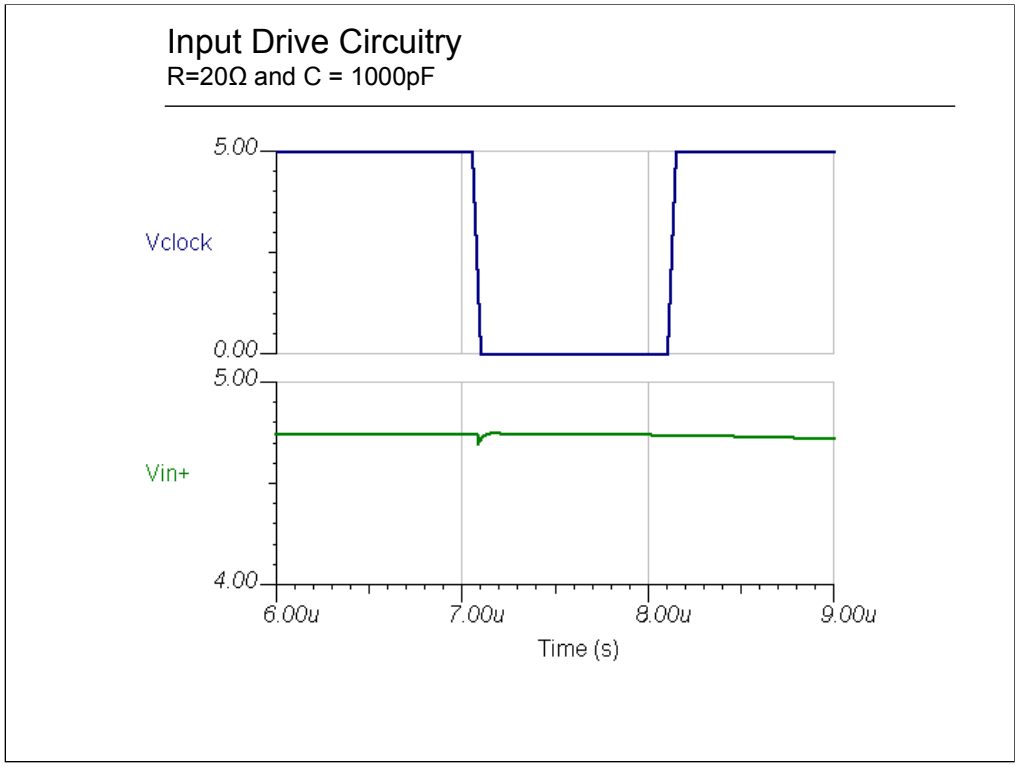


Now let's add the capacitor into the circuit – 1000pF with our 390Ω resistor. The input signal looks quite good now!



If we zoom in on a section of the TI-TINA simulation results, we can see that there is still some effect on the input signal, even with the flywheel circuit in place. But remember, it's not so much the transient we need to remove, it is that we must be assured that it is fully settled before the acquisition time of the converter has passed.

This looks like it may be settled, but much higher resolution on our output results would be required to know if it's settled to 16 bits by the time the clock signal goes high again.

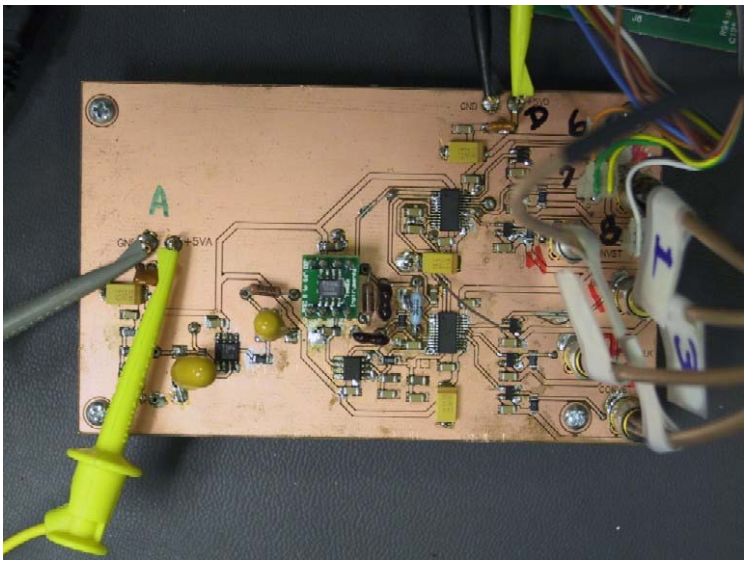


In some cases, very low values of resistance are used. Here's a look at the load transient with R dropped to 20 ohms. This looks like things have probably settled out well before the acquisition time is over.

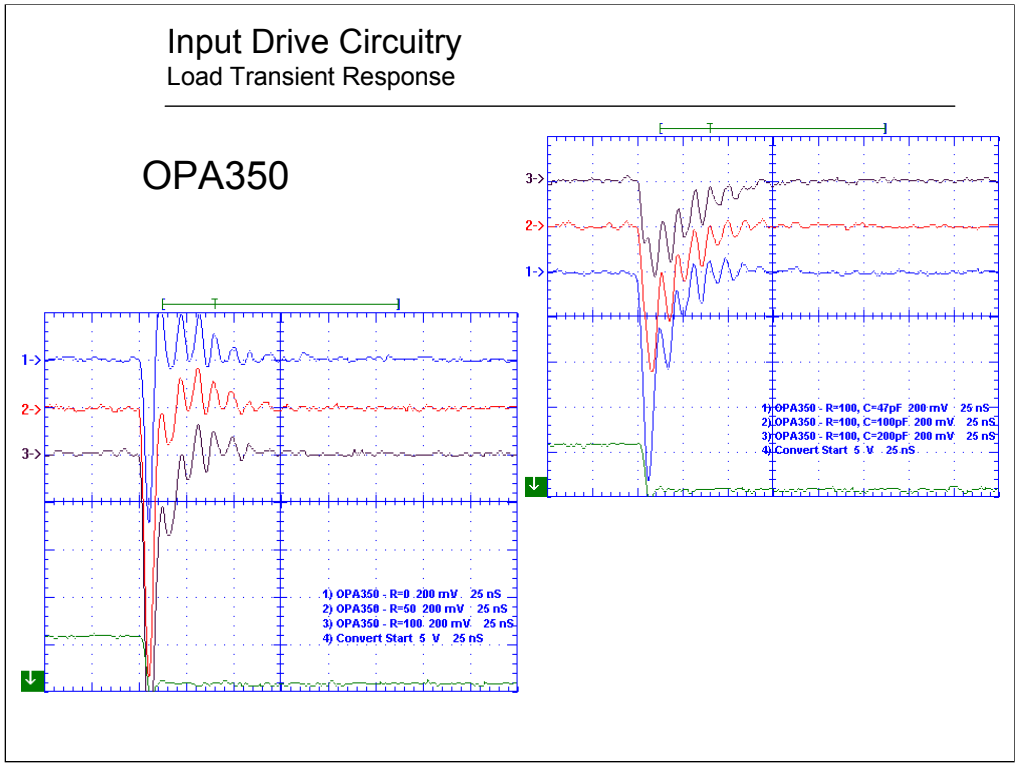
How can we verify this?

Input Drive Circuitry

Load Transient Test Bed



This is an experimental board that might allow us to actually measure the settling time of the input signal. It consists of two ADS8361s – one, the device used in the test, fed by an op amp and the RC filter. The second ADS8361 is looking at the same input. But the second ADS8361's timing is adjusted such that it converts slightly before or after the first converter. By stepping through conversion instants in 20ns steps, we can build a picture of the actual acquired values, and can see the settling time of the op amp while it is receiving the load transients from the main converter.

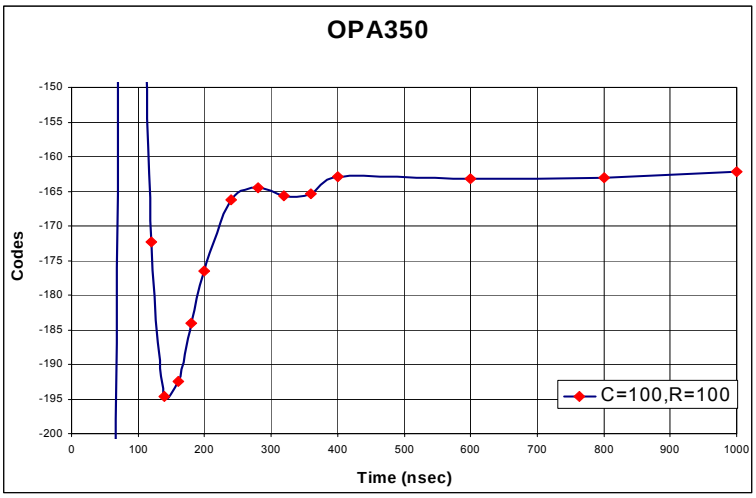


From looking at scope captures of the actual op amp under a transient load condition, we can see that there is significant ringing and settling. On the left, the settling with no external capacitor; on the right, different capacitors are used.

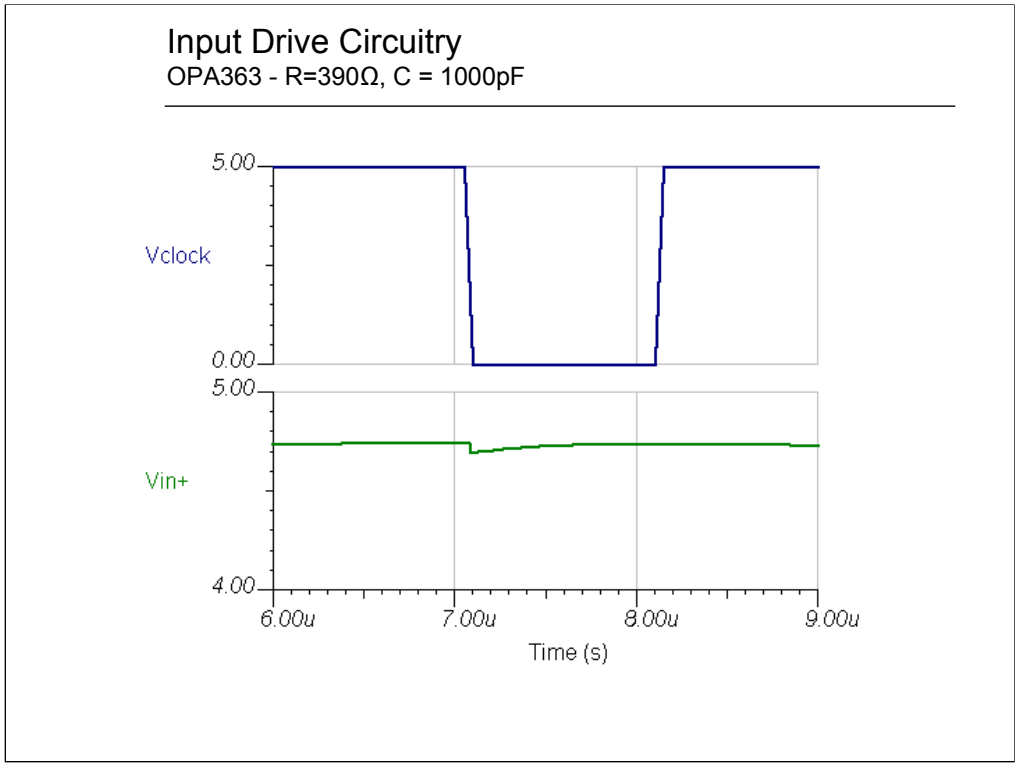
Input Drive Circuitry
OPA350 Data

StdDev=1.9

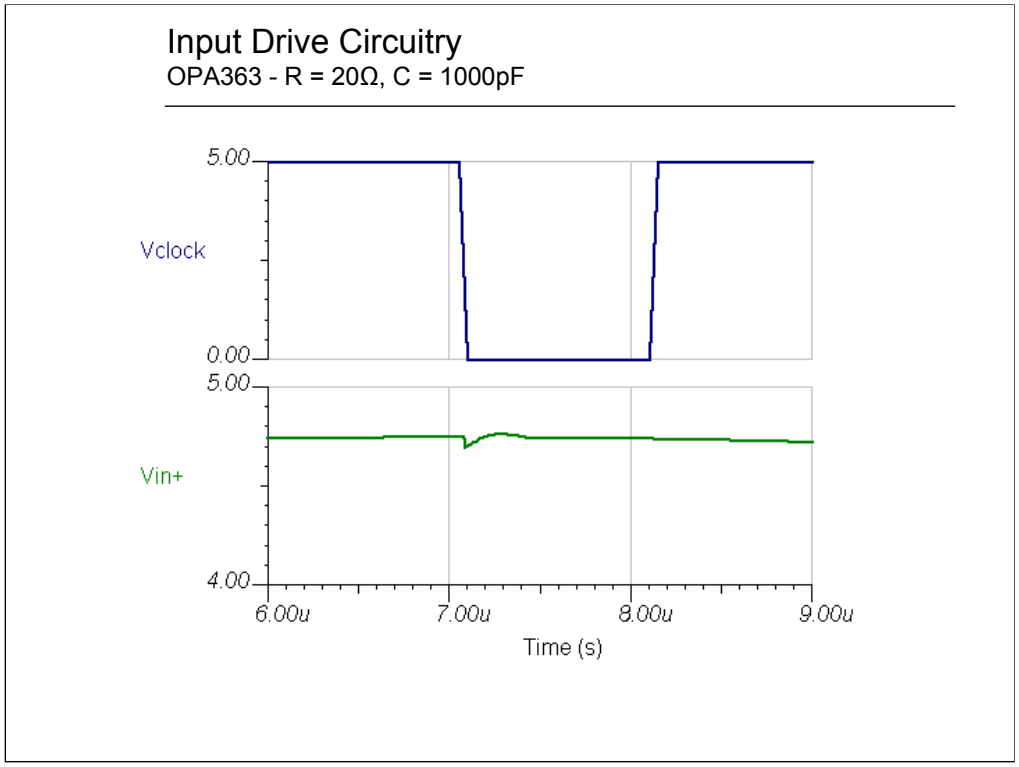
Delta=25



From our captured signals taken with the second ADC, we can “see” what the main ADC “sees” – a settling time of around 400ns to get within 2 codes of the final value, and longer to be truly “settled”. Note that the OPA350 macromodel used predicted much faster settling.



As with any modeling exercise, the results are only as good as the models used. The OPA350 macromodel does not model output characteristics very well; later models, such as the one for the OPA363, do a much better job of modeling output stage behavior. Here, we've used the OPA363 and can see the longer settling tail, although this is with a larger external R.



Dropping the R value to the same condition as the previous model with the OPA350, we can see some of the ringing behavior beginning to appear. This is as a result of the better model available for the OPA363.

Much more development is necessary on both the op amp models and the ADC input model before these can be used as true predictors of what actually happens in a system. This preliminary look at things points out some of the areas where more work needs to be done.

Input Drive Circuitry
Summary

- Choose the right input type for your system
  - Single-ended
  - Pseudo-differential
  - Differential
- Buffer Op Amp
  - Rail-to-Rail Considerations
  - Settling times and drive capability
- RC Circuit
  - Use the starting criteria established here
  - Experiment to optimize, or…
- Modeling the ADC Input Interface
  - A preliminary model exists
  - More work left to be done
  - Use simulation results with caution