A Baker's Dozen of High-Speed Differential Backplane Design Tips

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Abstract

LVDS (Low Voltage Differential Signaling) based technology is revolutionizing high-performance backplanes used for multi-point communication in Datacom, Telecom, ISP and Storage applications. It enables quadrupling the bandwidth in many cases while consuming less power and easing termination complexity. The use of a differential technology allows for a reduced voltage swing without compromising noise margins. This enables 100-400+ Mbps multi-point transmission, low bit error rates, live-insertion capability, and a general robustness not available from other single-ended small-swing technologies. This paper provides tips and practical design guidelines for Bus LVDS backplanes. Concepts are supported with design calculations, simulations, and actual hardware measurements.

Authors/Speakers

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John Goldie is a Member of the Technical Staff with National Semiconductor. He joined National in 1988 and has worked on a wide variety of Interface Products and applications. These span a wide array from RS-232 to Gigabit backplanes using LVDS technology. He is also the chairman of the TIA (Telecommunications Industry Association) Electrical Ad-hoc group TR30.2.1 that defined the TIA LVDS standard among many others. Current duties include: new product definition, system level product evaluation, participating on Industry Standard committees, and most importantly general customer support. John obtained his BSEE from San Francisco State University in 1988 along with a minor in Design & Industry. Outside of his work, John enjoys activities with his wife Rola and their three children: Sara, Jamie and Robert and also “Train Spotting”.

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Dr. Chen is a Signal Integrity and EMI engineer with NESA. As such he carries out simulation activities and confirmatory laboratory work for high performance busses, including semiconductor logic modeling, clocking and characterization test boards design. Presently, Dr. Chen is working on LVDS technology based interconnects. Dr. Chen is also re-writing the NESA Method of Moment field analysis and interconnect simulation codes to provide additional capabilities for layered media. Dr. Chen obtained his Doctorate in Physics from the University of Lowell. His concentration was medium energy neutron scattering and electromagnetic field theory as it applies to his research topic. Prior to attending the U. Lowell, Dr. Chen was a researcher in nuclear physics in the China Institute of Atomic Energy. Dr. Chen obtained his master's degree in Physics from the China Institute of Atomic Energy and his B. S. Physics from Shandong University in Solid State Physics

1.0 Bus LVDS Introduction

Bus LVDS (BLVDS) is a new family of bus interface circuits invented by National Semiconductor based on LVDS technology. This family of interface devices is optimized for multi-point cable and backplane applications. Bus LVDS differs from standard LVDS in providing increased drive current to handle double terminations that are required in multi-point applications. It is also enhanced in its contention protection, and balanced output impedance. Currently transceivers, repeaters, serializers, deserializers and clock buffers are available.

BLVDS features a low voltage differential signal of ~300 mV and fast transition times. This allows the drivers to support applications ranging from low speeds at a few Megahertz (or even DC) to high speeds in the 400+ Mbps range and even beyond. Additionally, the low voltage swing minimizes power dissipation and noise generation. The differential data transmission scheme provides a +/- 1Volt common mode range and live insertion (hot plug) of devices into an active bus.

In the past, the bus driving problem was solved by increasing the drive current of the standard logic single-ended drivers (244 type). With standard logic swings and increased drive current, application speeds were increased to the 10-20 MHz range, but not faster. Since increasing drive current alone was not enough, the next enhancement was made. As before, the drive current was once again raised; however, the signal swing was also reduced. Thus BTL (Backplane Transceiver Logic) was invented which supports 80mA-sink capability and a 1V signal swing. This approach easily drives heavily loaded backplanes up to the 50-66 MHz range. However, it is still single-ended (like generic TTL), and only provides about 400 mV of noise margin. To break the 100MHz barrier, a single-ended, reduced swing approach is not a feasible since noise margin is already at the minimum acceptable level.

Bus LVDS removes the needed for large amounts of current, by reducing the signal swing an order of magnitude from TTL levels, and also reducing drive current to 10 mA. To double the noise margin over that of the reduce-swing, single-ended technologies, BLVDS uses a differential data transmission scheme similar to LVDS but enhanced for multi-point applications. This enables the 300 mV swings to operate at 100s of Mbps, while doubling noise margin and reducing noise generation. It also supports live-insertion of devices into an active bus due to the receiver's common mode rejection capability.

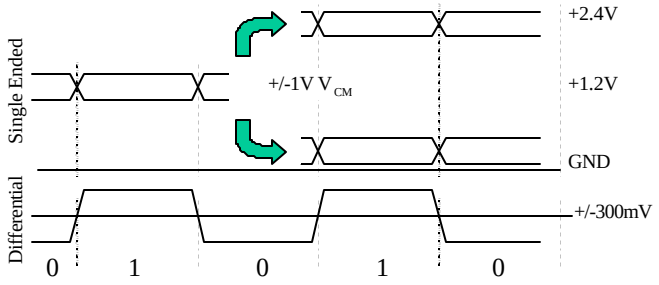

Figure 1 - Bus LVDS Signals

2.0 Bus Configurations

Bus LVDS devices may be used in Point-to-Point applications, Multi-drop data distribution applications, or in a classical multi-point shared bus application. It may be employed for data buses, control signals, or for clock distribution. Point-to-Point, Multi-drop, and Multi-point bus configurations are shown in figure 2. Multi-drop is a special case of multipoint. Multi-drop applications feature a single source driving multiple receivers. If the driver is located at the start of the bus, termination is only required at the far end. Multi-point allows the source to be located at any location on the bus, thus it requires termination at both ends of the bus. Multi-drop and multi-point are useful configurations when the same information needs to be delivered to many locations. This bus configuration is also very efficient in terms of interconnect density. Communication above 500 Mbps should consider the use of point-to-point links as it's interconnect offers superior signal quality.

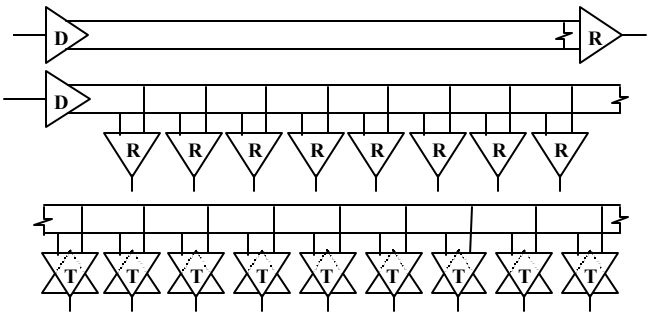

Figure 2 - Common Bus configurations: (A) Point-to-Point, (B) Multi-drop, and (C) Multi-point

3.0 A Baker's Dozen of Differential Backplane Design Tips

Thirteen topics are presented that provide tips, trends, tricks or design guidelines to achieve maximum performance out of a LVDS based differential backplane. Tips are shown in *italics*.

Tip Number 1 - Edge Rate

A multi-point backplane model was used to complete the TDR analysis that shows the effects of edge rate. This analysis utilized NESA's proprietary "Passive Signal Integrity" differential TDR/TDT simulation tool.

The differential TDR excitation was applied at slot 8 of the 11 slot backplane model simulation. The TDR simulations were made with 0.3, 0.5 and 1.0 ns of TDR rise time. The stub length was also varied from 0.5" to 1.0" and 1.5" providing a wide range of the most significant parameter variations. The loading and edge rate effects are shown in figure 3 below. Note that the curves approach 28 Ohm which is the parallel equalvence of the two 56 Ohm termination resistors. The faster the edge rate, the more the dynamic swing of the curve. The fast edge is needed for high-speed transmission, but it will also aggravate transmission line problems (but these can be dealt with).

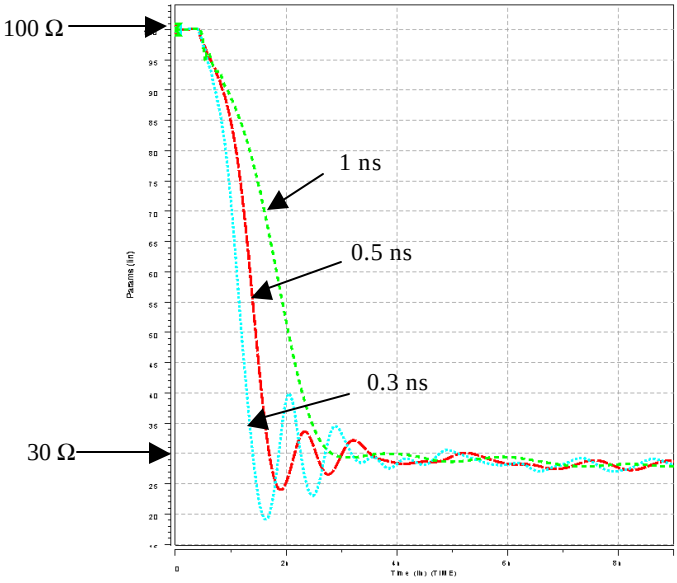

Figure 3 - Differential TDR simulation with 0.3, 0.5 and 1 ns TDR rise times with 0.5" stubs

The TDR shows the structure of the multi-port backplane discontinuities. The 100 Ω starting point is the differential impedance of the 0.5" stub at the launch point. The first dip is caused by the trace split and the connector loads. The bounced back point is the first backplane etch with a length ~ the slot pitch. The nearest pair of slots then causes the second dip due to the stub and connectors connected to the backplane etch at that point. The TDR stimulus slows down as it travels further down to the backplane due to reflective discontinuities, copper and dielectric losses. The observed impedance shows the net loading impedance effects of backplane etch, the connectors the stubs and devices. The final average value is about 28 Ω and is due to the parallel combination of the loaded backplane halves mentioned above.

Transition time (rise and or fall) is the most important parameter to understand for transmission line calculations, also edge rates faster than 300 ps should not be used for multi-drop or multi-point applications.

Tip Number 2 - Stub Lengths

The stub length effects have also been analyzed using NESA's TDR and TDT "Passive Signal Integrity" methodology. Figures 4 and 5 show the differential TDR and TDT simulations with 0.5", 1" and 1.5" of stubs variations respectively. The TDR stimulus has fixed 0.3 ns rise time.

Once again the impedance variations in the TDR simulation and the excessive ringing in the TDT simulation are demonstrated. The longer the stub length, the bigger the impedance discontinuity. The bigger the impedance discontinuity, the larger the ringing magnitude.

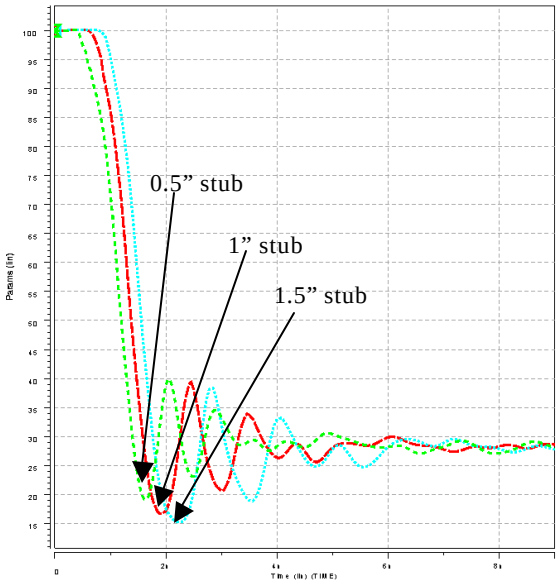

Figure 4 - Differential TDR simulations with 0.5", 1" and 1.5" stub length and 300ps rise time

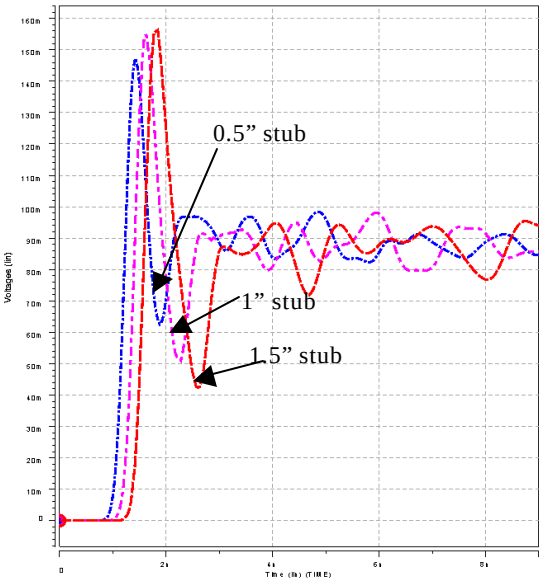

Figure 5 - Differential TDT simulations with 0.5”, 1” and 1.5” stub length and 300 ps rise time

The TDR/TDT simulations indicate that, the stub length in the daughter card should be kept as short as possible with the maximum recommended length of 1.5”. As in all backplane cases, the shorter the stubs, the better.

Minimize stub lengths to reduce transmission line effects.

Tip Number 3 – Interface Component Placement

To mitigate the transmission line effects as shown in the TDR simulations and also in the TDR/TDT simulation on stub lengths, priority should to placement of the interface devices to ensure the shortest possible stub lengths. This is a simple recommendation and if adhered to it can help to eliminate many Transmission Line problems.

Locate transceiver (multi-point) and receivers (multi-drop) closest to the connector as possible, and use both sides of the PCB to yield the shortest stub lengths.

Tip Number 4 - Differential Impedance

The NESA Method-of-Moments two dimensional field solver was used to determine the differential impedance geometry parameters. The geometry of choice is the broadside-coupled differential transmission lines as shown in figure 6.

The Bus LVDS requirement is for 100 Ω differential impedance pairs. This impedance can be realized using the suggested geometry shown below. The MoM calculations predict that for copper trace width W = 7 mils with a 1-oz thickness and dielectric thickness H1 = H2 = H3 = 12 mils utilizing FR4 material, the 100 Ω differential impedance is achieved. Keeping the spacing between trace pairs of at least 20 mils provides very low differential and common mode coupling between pairs. This trace structure has an advantage in that the traces can remain closely-coupled as the route through a connector field.

Using closely coupled traces ensures that noise picked up will appear as common-mode and rejected by the receivers and it also limits the amount of radiation.

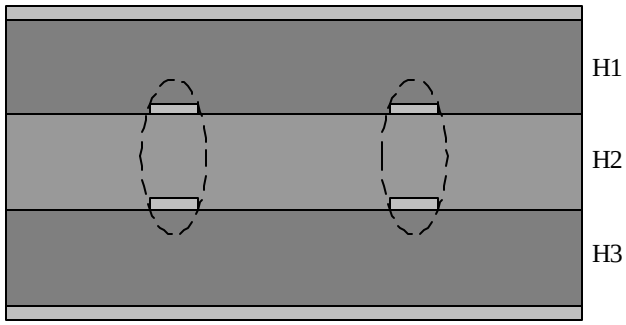

Figure 6 - Geometry of the broadside-coupled differential transmission lines

Tip Number 5 - Loaded Differential Impedance

The effective backplane impedance changes with the backplane loading. To determine the effective impedance, a 20-slot backplane was analyzed with NESA’s proprietary “Passive Signal Integrity” differential TDR simulation. A differential TDR stimulus was placed at one end of backplane with the TDR rise time set to 300 ps and the TDR differential internal impedance set to 100 Ω.

The backplane was then TDR analyzed under four different load conditions:

a) Raw 100 Ω differential impedance PCB backplane etch
b) The backplane is populated with the backplane half of the 2mm connector;
c) All the 20 slot logic cards were plugged in with 1” stubs (no devices);
d) The DS92LV090A transceivers were added on the end of each stub on each card.

The results shown in figure 7 correspond to these four (4) cases.

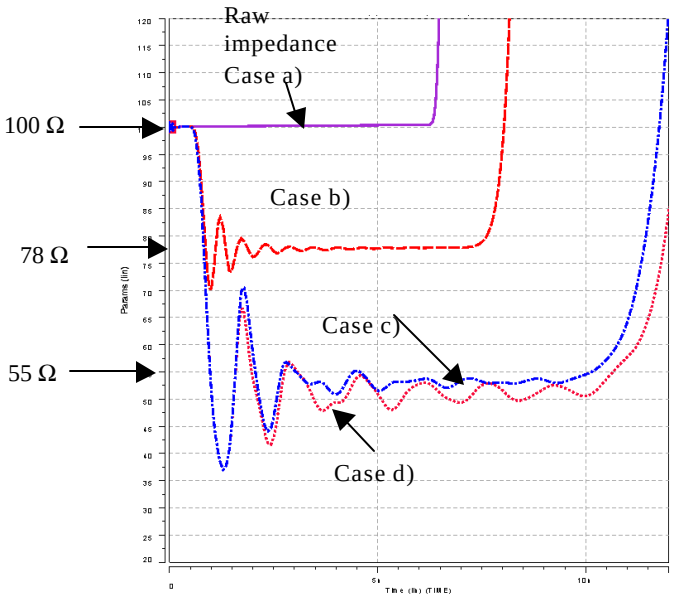

Figure 7 - Loading effect on the effective backplane impedance

Figure 7 shows that the loading reduces the backplane impedance as expected. With the backplane half of the 2mm connectors loaded (pins only), the effective backplane impedance is reduced to about 78 Ω. The fully loaded backplane with 1" stubs exhibits about a 55 Ω effective impedance. The addition of the device load (DS92LV090A) loading reduces this to about 53 Ω.

The ringing seen on the impedance traces is due to the impedance discontinuity reflections due to the connector and stub loads. The rise times near the TDR driving point are sharp enough to discriminate between the etch (higher impedance) and the connector-stubs (low Impedance). As the TDR step function travels down the backplane, it loses its risetime performance and the ability of the waveform to discriminate between loaded and unloaded portions is diminished and merges into the average impedance measured.

The effective backplane impedance (loaded impedance) is lower due to the distributed capacitive loading effects of the closely spaced cards. Also the signal transmission speed (per unit delay down the backplane) is also affected by backplane loading. The fully loaded backplane is nearly 50% slower due to the connector, stub and device capacitive loading.

Tip Number 6 - Bus Termination

For Bus LVDS, a single resistor is typically all that is required between the lines at both ends of the bus for multi-point applications. For multi-drop applications 1 or 2 resistors will be required depending upon the location of the driver. *The resistor value should be equal to the effective loaded differential impedance of the line. It is better to err on the high side and create a small positive reflection than to be too low in value thereby reducing received signal voltage.* The resistor value is determined by the application and depends upon line impedance (unloaded), distance between cards, and capacitive loading added by the cards. The value is typically in the 50 to 100 Ohm range. If doubly terminated, the driver sees both resistors in parallel; thus, the resulting load is 25 to 50 Ohms. This is also the reason that National's BLVDS parts provide about 3X the driver current of standard LVDS drivers. With a 10 mA drive level, impedances below 50 Ohms can be driven to levels similar to LVDS with its 100-Ohm load and 3 mA driver. Closely spaced loads in a backplane typically reduce the impedance of the backplane below 50 Ohms.

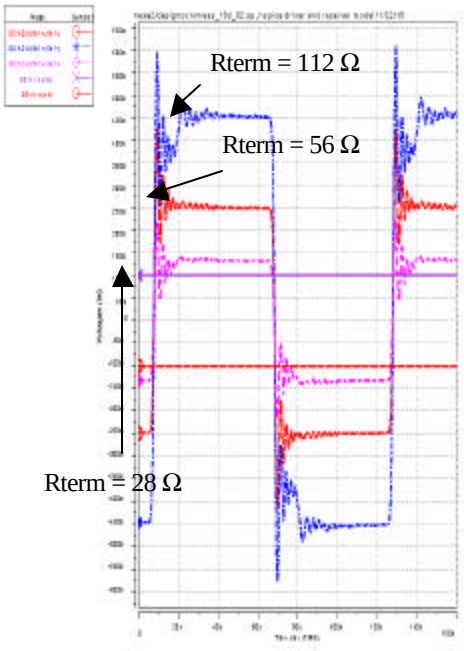

Figure 8 – Under, Matched, and Over Termination Waveforms

Figure 8 shows the differential waveform at a receiver input with three termination scenarios. The effective loaded backplane impedance is 56 Ω, and waveforms are show with a matched termination (56 Ω), an over 2X termination (112 Ω), and an under 0.5 termination (28 Ω). From a noise margin point of view matched and over termination cases provide the most margin. The simulation was made with full loaded 18-slot multi-point backplane. The driver was located at slot 18. The slot 1 receiver input was plotted.

Tip Number 7 -Stub Termination

The use of a series resistor (15-30 Ohm range) on each signal line, adjacent to the connector pins, provides a filtering effect to the edge rate. This slowing of the edge rate greatly reduces the magnitude of the differential ringing which can be caused by long stubs and fast edge rates.

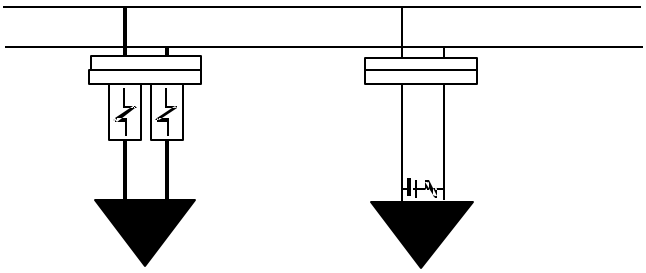

Figure 9 - Termination of stubs for Bus LVDS

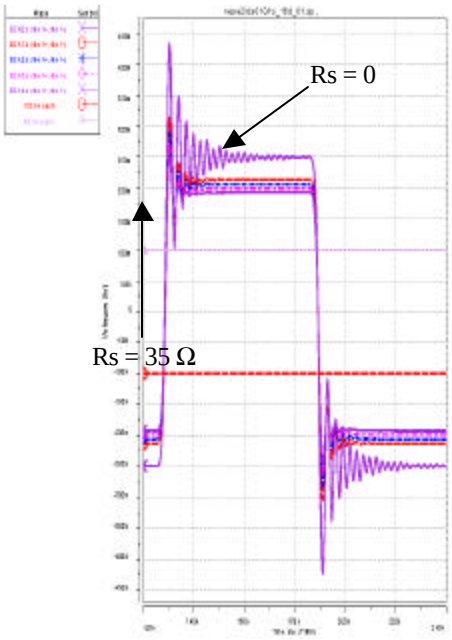

Figure 10 – Waveforms with series stub termination (Rs = 0, 20, 25, 30, 35 W)

This effect may also be accomplished by using an AC termination across in the inputs of the receivers. Transmission line problems are now greatly reduced on the stub. Figure 10 shows simulations of receiver input waveforms for different values of series resistor. These schemes are best for multi-drop applications only. *If you are dealing with fast edges and long stubs in a multi-drop application, consider the use of stub termination to eliminate transmission line effects.*

Tip Number 8 – Connectors and Sequencing

Connector selection is application dependent and depends upon factors such as: signal pin count required, mechanical specifications, electrical performance, and footprint issues. In general, the shortest rows are better than the long rows. Also, on most connectors, differential pairs should be routed within the same row, not between rows, to maintain equal path lengths. Route CMOS signal on non-adjacent pins from LVDS pins to isolate the dv/dt of the CMOS swing. These recommendations are shown in figure 11.

Special connectors or section should be used for power and ground. Staggered lengths on these pins will insure that the proper sequencing is achieved. The recommend order for insertion is ground, power, then I/Os. For removal the reverse is recommended.

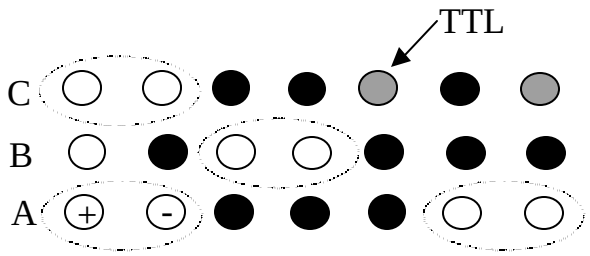

Figure 11 – Connectors Pins

Tip Number 9 - Failsafe Biasing

Failsafe is a common concern in multi-driver applications. If a known state is required when all drivers are off, a failsafe bias may be required. The devices (RXs) have a minimum amount of internal failsafe biasing, which may need to be boosted in the application (for example, if it has CMOS rail-to-rail signals swinging on adjacent pins in connectors). If this is the case, a pull-up and pull-down resistor should also be used at the site of the terminations as shown in figure 12. This will typically be in the 6-20K Ohm range. A slight positive bias conditions the line when all drivers are off. These resistors should not be reduced too much in value because this will load down the driver and reduce the signal swing.

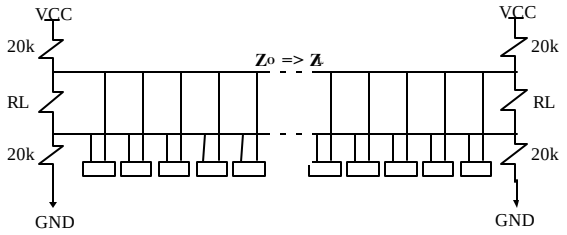

Figure 12 - Backplane Termination and Failsafe Biasing

In selecting failsafe resistor values note the following: magnitude of the resistors should be 1 to 2 orders higher than the termination resistor to prevent excessive loading to the driver and waveform distortion, the mid-point of the failsafe bias should be close to the offset voltage of the driver (+1.25V) to prevent a large common mode shift from occurring between active and TRI-STATE (passive) bus conditions, the pull-up and pull-down resistors should be used at both ends of the bus for quickest response, and finally note that signal quality is reduced as compared to active driving (on/on).

Tip Number 10 - Balanced vs. Unbalanced Pairs

Common mode noise can be generated when the differential traces are not balanced. In the simulation shown in figure 13, the transmission line pair is unbalanced. One line of the pair is 14.4" long, while the other is 16.2" long. The common mode noise created could cause EMI problems in the system.

To limit the unnecessary generation of common-mode noise, match the length of the two lines composing the differential pair. Maintain balance of both lines as much as possible.

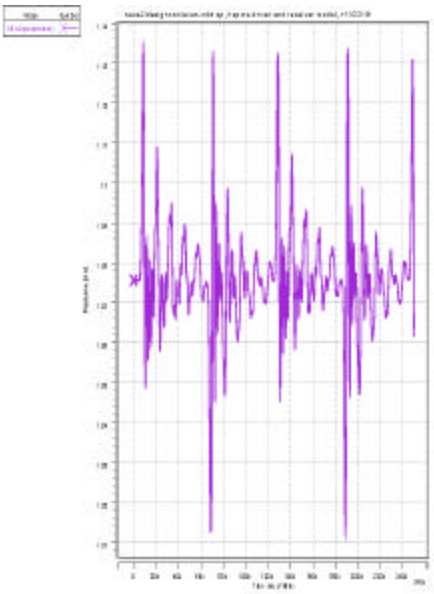

Figure 13 - Common mode noise of receiver input with an unbalanced pair

Tip Number 11 - Live Insertion Support

Inserting a card into a live bus may be required in applications where system down time must be minimized. This may be accomplished by the use of redundant logic cards and interconnect (systems), or with a system that is fault-tolerant. Bus LVDS provides a robust, fault-tolerant data transmission system that allows the insertion of a card into an active bus. In certain applications, this can eliminate the need for redundant paths altogether, thus reducing system cost.

Bus LVDS uses differential data transmission that provides protection of the information through its inherent common-mode rejection capabilities. When a card is plugged into the active bus, a capacitive load is added to the lines. The propagating signal must charge this load capacitance. As the capacitance charges, a dip in the signal level occurs. Since the data is carried differentially (A-B), the result is a modulation of common-mode voltage which does not affect the information. The common-mode voltage is rejected by the receivers. Common-mode voltage modulation is a great concern with low-swing, single-ended transmission, such as that used by GTL or BTL. In GTL or BTL, a dip in voltage can corrupt data if the dip enters the threshold region and is of sufficient duration for the receiver to respond.

The testing conducted included hot-plugging cards into the live backplane and monitoring for errors with the MB100 BERT system. Tests were run in the 18-slot backplane with the TX in slot #11, and the monitoring RX for the BERT tester in slot #12. Cards were plugged into

slots #1, 10, 13, and 18. During the hot-plug events, no errors were detected.

A static-channel, live-insertion event glitch was captured on the scope by using a single-trigger capture and a single-ended probe (trace #1 @ 100mV/div). A differential probe (trace #2 @ 200mV/div) monitored the static channel. Figure 14 shows that differential noise margin is maintained and the event is only a common mode modulation.

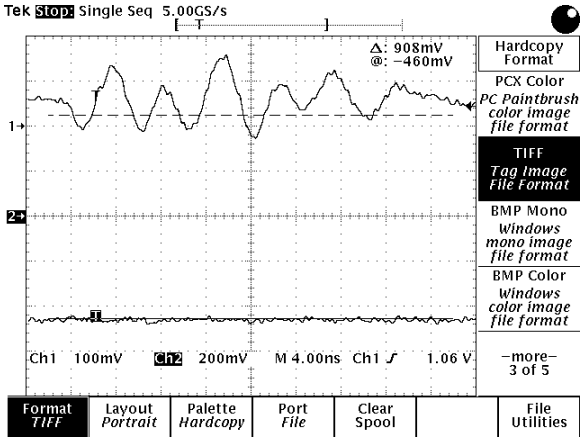

Figure 14 – Live Insertion Scope Waveshapes

To insure the best live insertion results, make sure that the stub loading is balanced and upon contact to the active bus both lines present the same capacitive loading.

Tip Number 12 - Signal Quality

The furthest receiver location from a driver should be checked for signal quality. An eye pattern measurement should be used with PRBS pattern to determine the ISI effects. This is the location that the edge rate from the driver has slowed the most and the eye pattern will be closed down. Different applications require different levels of signal quality, but the wider the eye opening the better. *Check the furthest Receiver location for determining that the signal quality meets the requirements of the specified data rate. Use Eye Patterns to check for ISI (Inter Symbol Interference) and resulting jitter magnitudes.* Figure 15 shows an eye pattern at the furthest receiver location.

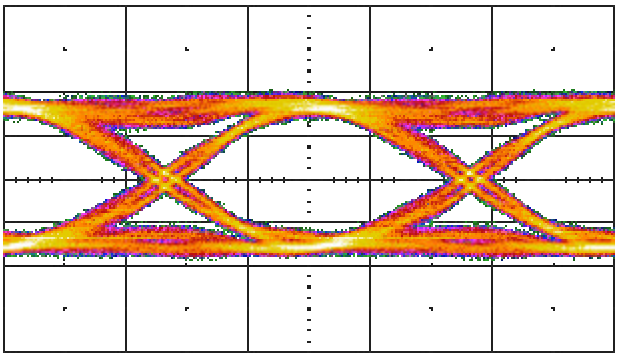

Figure 15. DS92LV090A, 18 slot, Full Load, TX@1, RX@18input pins, 200Mbps, PRBS15, Diff. Probe P6247, HP54720D Scope, 200mV/div, 1ns/div

Tip Number 13 - Signal Quality (again)

The nearest receiver location to the active driver should also be checked. At this location the edge rate is the fastest and transmission line effects will be the worse. Probing these signals is difficult due to location but the effort is well spent. To get an accurate measurement, remember to use a high bandwidth low capacitance differential probe.

Transmission line effects tend to be worse closer to the driver, as the signal's edge rate is the fastest there.

4.0 Summary

Bus LVDS ushers in a new era for high-performance multipoint backplanes. The multipoint configuration is a very efficient bus, as it enables communication between all cards with the minimum amount of interconnect. This advantage is also its limitation. The resulting stubs from the main line create a challenge to transmission line signal quality. Also, communication is bi-directional but only half duplex.

The merits of Bus LVDS (BLVDS) are great compared to prior generation technology solutions for multipoint backplanes. Data rates in the 100-400+ Mbps range are now possible. This is a 4X improvement over BTL or GTL+ based applications and an astounding 10X improvement over TTL driver applications. Power dissipation is greatly reduced by the use of low current steering drivers, the use of CMOS technology, and the common low voltage supply rail. Termination is required to prevent reflections (this provides the incident wave switching and boosts data rate) and complete the output current path. Unusual termination voltage rails are not required (2.1V for BTL, and 1.5V for GTL+). This greatly reduces the complexity of termination to just a single passive surface-mount resistor at each end of the bus. In some application these may even free up two card slots that had been devoted to active termination of the single-ended bus. Live insertion is also supported, as the "hot-plug" event creates a common-mode modulation on the bus that is rejected by the receivers.

In summary, BLVDS provides a quantum jump in performance for mainstream multipoint backplane applications in datacom, telecom, ISP and storage applications.

5.0 References

AN-1115, *DS92LV010A Bus LVDS Transceiver Ushers in a New era of High - Performance Backplane Design*, National Semiconductor, July 1998, www.national.com/an/AN/AN-1115.pdf

Bus LVDS White Paper, *Signal integrity and Validation of National's Bus LVDS (BLVDS) Technology in Heavily Loaded Backplanes*, North East Systems Associates, May 1998, www.national.com/appinfo/lvds/blvds_wp.pdf